technische universität
dortmund

fakultät für informatik
informatik 12

2nd Workshop on Mapping of Applications to MPSoCs

Schloss Rheinfels
St. Goar, Germany

June 29/30th, 2009

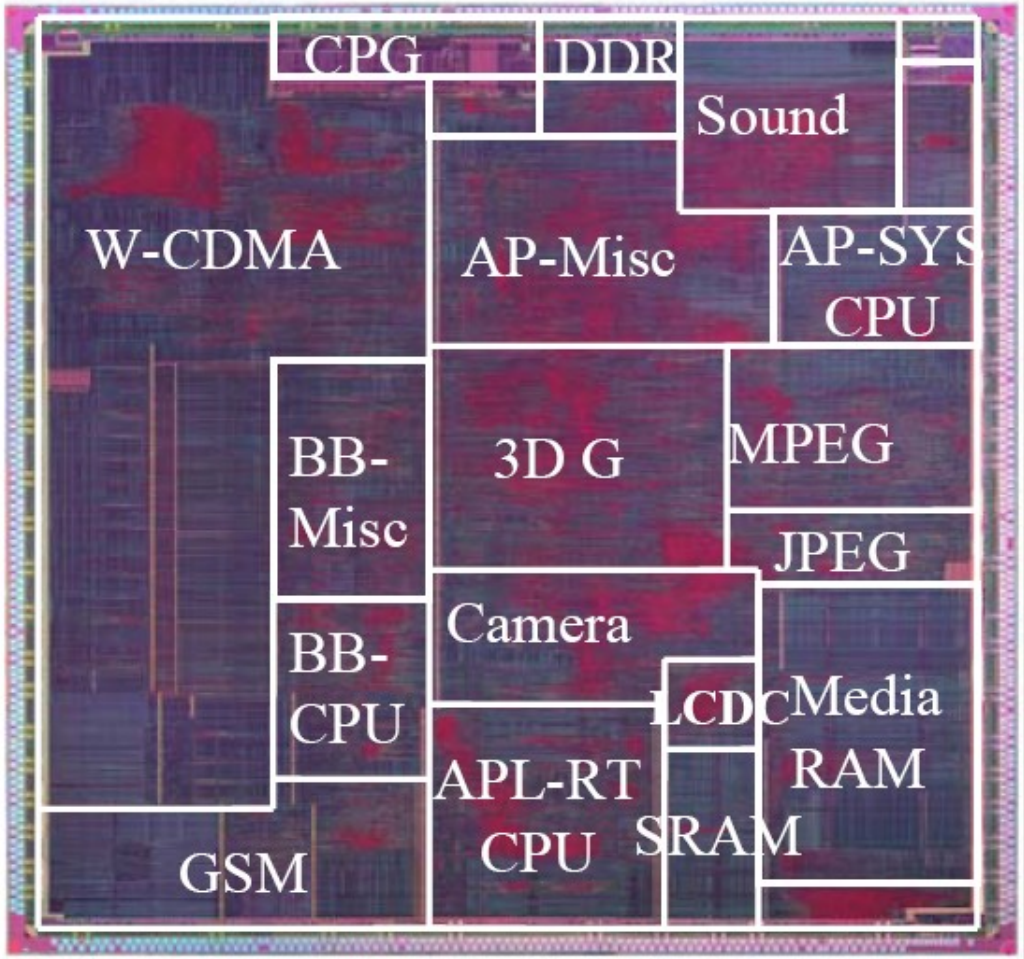
http://www.schloss-rheinfels.de/content/view/113/218/

Trend

Obvious trend toward using many processors in one system: multi-cores, many-cores, MPSoCs

Example

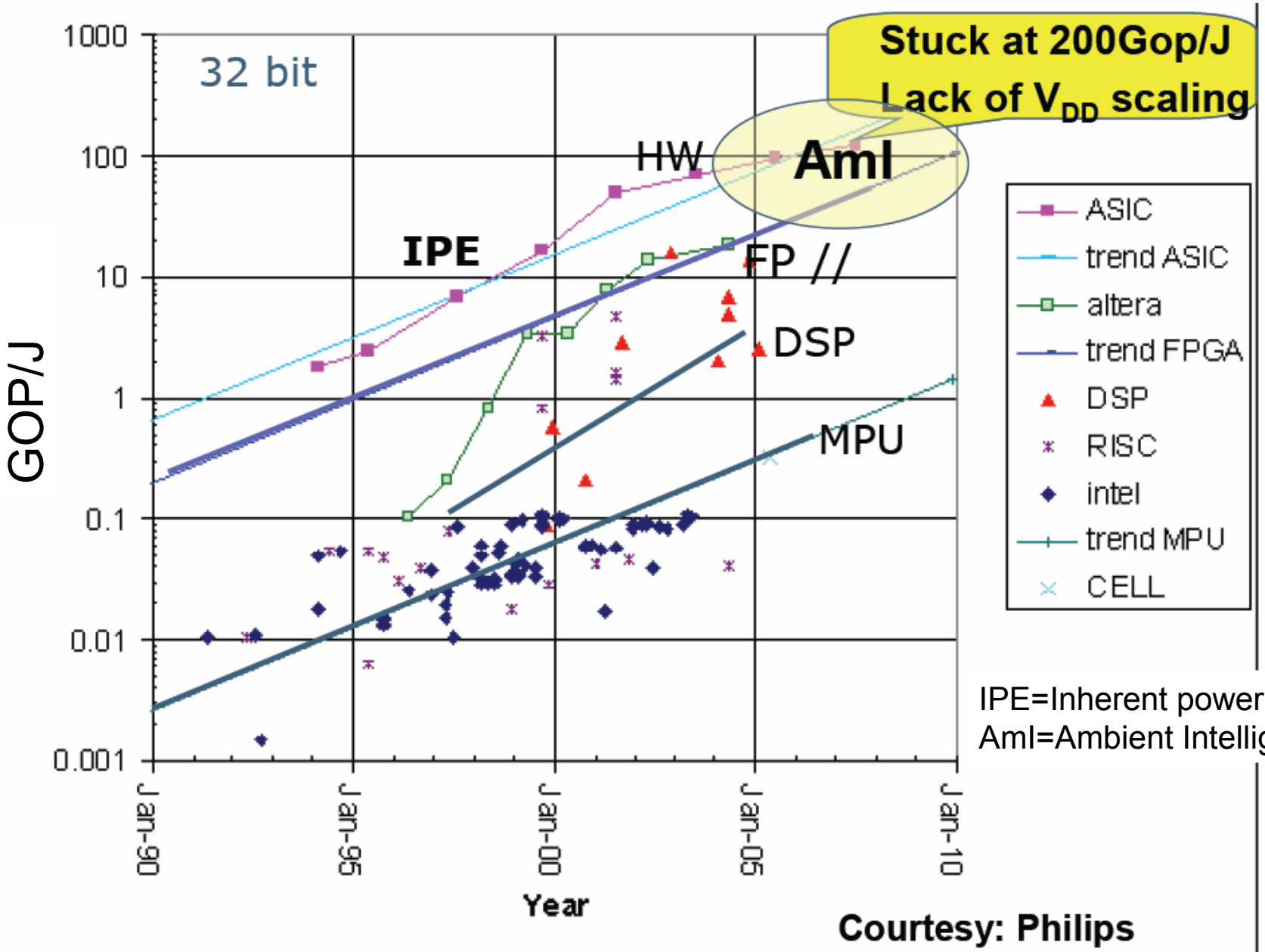
SH-MobileG1: Chip Overview



Die size	11.15mm x 11.15mm
Process	90nm LP 8M(7Cu+1Al) CMOS dual-Vth
Supply voltage	1.2V(internal), 1.8/2.5/3.3V(I/O)
# of TRs, gate, memory	181M TRs, 13.5M Gate 20.2 Mbit mem

http://www.mpsoc-forum.org/2007/slides/Hattori.pdf

Reason for heterogeneity: Energy Efficiency



IPE=Inherent power efficiency
AmI=Ambient Intelligence

Courtesy: Philips

What happened last year?

- 1st Rheinfels Workshop, June 16/17th, 2008
- Report at CASA workshop (Atlanta), Oct. 19th, 2008
- Working meeting at Düsseldorf, Nov. 27th, 2008
- Visits between ArtistDesign partners.

Schedule (June 29th)

11:45	**Lunch**
12:20	Opening (*Peter Marwedel)*
12:30	Soonhoi Ha (Seoul National U): Programming-platform based Design of MPSoCs: The HOPES Approach
13:15	Jürgen Teich (U. Erlangen): SystemCoDesigner - Automatic Design Space Exploration and Prototyping from Behavioral Models
14:00	Qiang Xu (Chinese University, Hong Kong, CN): Minimizing Energy Consumption of MPSoCs under Lifetime Reliability Constraints
14:45	Tajana Simunic (UCSD, US): Energy and thermal management in MPSOCs
15:30	**Break**
16:00	E. Deprettere (U Leiden, NL) with contributions by Todor Stefanov (U. Leiden, NL), Iuliana Bacivarov (ETHZ, CH) and Bastian Ristau (TU Dresden, D): Benchmarking
16:55	Björn Franke (U. Edinburgh, UK): Towards a Holistic Approach to Auto-Parallelization: Integrating Profile-Driven Parallelism Detection and Machine-Learning Based Mapping
17:20	Marco Bekooij (NXP, NL): Automatic Parallelization for Embedded Multiprocessor Systems with Non-Uniform Memory Access Latencies
17:45	Fabrizio Ferrandi (Polyt. di Milano): Mapping and Scheduling of Parallel C Applications with Ant Colony Optimization onto Heterogeneous Reconfigurable MPSoCs
18:10	Session ends
18:45	**Departure for social event**
19:15	**Social event: cruise on the river aboard MS “Rheinkrone” (Hebel Line)**

Schedule (June 30th)

9:00	Per Larsen (TU Lyngby, DK): Data-dependencies and Thread Interaction in Parallel Loops
9:25	Michael Claßen (U. Passau): Introducing the GCC to the Polyhedron Model
9:50	Gerard Smit (TU Twente, NL): Run-time Spatial Mapping on MPSoCs
10:15	**Break**
10:45	Iuliana Bacivarov (ETHZ, CH): An Integrated Software Design Flow for Mapping Stream-Oriented Applications to Tile-Based MPSoCs
11:10	Anastasia Stulova (RWTH Aachen, D): MAPS and a high-level virtual platform (MVP)
11:35	Alessio Bonfietti (U. Bologna, I): Throughput constraint for Synchronous Data Flow
12:00	**Lunch**
13:15	Henrik Theiling (AbsInt, D): How Unthoughtful Resource Sharing Counteracts WCETAnalysis
13:40	Mircean Negrean (TU Braunschweig, D): Timing Analysis on Complex Real-Time Automotive Multicore Architectures
14:05	Discussion
14:45	**Tea break**
15:15	**End of the workshop; Start of Mnemee project demo**

Logistics

- 100 € payable to the hotel, covers
  - Food
  - Drinks in the meeting room (but not on the boat)

No liability for personal injuries

Don’t forget: we want an interactive atmosphere!