



IST-214373 ArtistDesign  
Network of Excellence  
on Design for Embedded Systems

Activity Progress Report for Year 2

## Platform and MPSoC Design

Cluster:

**Hardware Platforms and MPSoC**

Activity Leader:

**Prof. Luca Benini (UNIBO)**

<http://www-micrel.deis.unibo.it/>

*Policy Objective (abstract)*

The main objective of the activity is to build a common research environment and a wide basis of technical and scientific competences on embedded platforms, with special emphasis on Multi-processor Systems-on-Chip (MPSoCs). The main challenges are the significant fragmentation and lack of integration in this area. The consensus on the fact that hardware platforms for embedded applications will be multi-core, with increasing degrees of parallelism, is not matched at the software and system design level. The teams involved in the activity aim at building stronger common techniques for modeling, analysis and run-time management of embedded hardware platforms. The expected impact will be a faster and more consistently focused development of methods and tools in support of application development and mapping.

## Versions

number	comment	date
1.0	First version delivered to the reviewers	December 18 <sup>th</sup> 2009

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# 1. Overview of the Activity

## 1.1 ArtistDesign participants and their role within the Activity

Team leader: Prof. Lothar Thiele – TIK, ETH Zürich (Switzerland).

*Role: design methods for MPSoC that combine performance analysis with multi-objective application mapping strategies. To this end, an available programming environment DOL (distributed operation layer) will be enhanced and combined with tools from other partners.*

Team leader: Prof. Petru Eles – Linköping University (Sweden).

*Roles: (i) Analysis and Optimization of real-time and fault-tolerant applications implemented on distributed Platforms and MPSoC. (ii) Analysis and Optimization of energy efficient, time constrained embedded systems.*

Team Leader: Prof. Luca Benini – University of Bologna (Italy).

*Roles: (i) Development of power modeling and estimation framework for systems-on-chip. (ii) Development of optimal allocation and scheduling techniques for energy-efficient mapping of multi-task applications onto multi-processor systems-on-chips. (iii) Development of energy-scavenging techniques for ultra-low power sensor network platforms.*

Team Leader: Prof. Jan Madsen – IMM, Technical University of Denmark (Denmark).

*Role: Work on: abstract RTOS and NoC models for multiprocessor system simulation and verification. Modeling and analysis of fault-tolerant embedded systems.*

Team Leader: Prof. Rolf Ernst – TU Braunschweig (Germany)

*Roles: TU Braunschweig contributes methods to deal with variability and reliability issues for systems built from unreliable components.*

Team Leader: Dr. Stylianos Mamagkakis –IMEC vzw. (Belgium)

*Role: 'Develop novel design-time and run-time resource management optimizations for MPSoC platforms*

Team Leader: Dr. Raphaël David – CEA LIST (France)

*(i) Development of exploration framework for multi- and many-core architectures  
(ii) Development of advance strategies for the deployment and the management of multi-tasks applications onto multi- and many-core devices  
(iii) Design of multi-core architectures for dynamic multi-task applications*

Team Leader: Prof. Giovanni De Micheli – EPF Lausanne (Switzerland).

*Role: Develop novel models and policies for run-time control of MPSoC platforms. Areas of expertise include hardware design methods and tools, algorithms, real-time systems and 3D integration.*

### -- Changes wrt Y1 deliverable --

*Dr. Raphaël David (CEA LIST) and Prof. Giovanni De Micheli (EPFL) joined to this Cluster activity in Y2.*

## 1.2 Affiliated participants and their role within the Activity

Bjørn Sand Jensen – Bang & Olufsen ICEpower (Denmark)

*Areas of his team's expertise: chip design for audio signal processing*

Rune Domsteen – CTO Prevas (Denmark)

*Areas of his team's expertise: platform design for embedded systems*

Prof. Krish Chakrabarty - Duke University (USA).

*Role: to develop droplet-based biochips that use electrowetting on dielectric for droplet transport. Design methods and tools for droplet-based biochips*

Prof. Dimitrios Soudris – Democritus Uni. of Thrace, DUTH (Greece)

*Role: develop novel dynamic data type and data allocation optimizations for MPSoC platforms.*

Prof. Per Gunnar Kjeldsberg - Norges Teknisk-Naturvitenskapelige Uni., NTNU (Norway)

*Role: Develop novel task migration methodologies for MPSoC platforms utilizing hardware accelerators.*

Prof. David Atienza – EPFL (Switzerland)

*Role: Develop novel run-time memory management optimizations for MPSoC platforms.*

Dr. Valter Bella, Telecom Italia Lab

*Role: Consider Architecture and Design of Wireless Sensor Networks and Embedded Systems for Ambient Intelligence.*

Dr. Daniel Karlsson, Volvo Technology Corporation

*Role: Consider Architecture and Design of Automotive Embedded Systems.*

**-- Changes wrt Y1 deliverable --**

*No changes with respect to Year 1.*

## 1.3 Starting Date, and Expected Ending Date

**Starting date:** January 2008.

**Ending date:** the activity will span the duration of the project, and continue beyond the end of the project. This is because all current trends indicate that MPSoC and platform design will increasingly become a primary concern and focus of action for researchers, designers and developers working on embedded systems.

Moreover, the integration achieved by this activity is creating the know-how and the skills required for the definition of new research and development initiatives. As a result, all partners are already actively involved in long term funded research programs in MPSoC and embedded design, whose end-date is beyond the duration of ArtistDesign.

**-- Changes wrt Y1 deliverable --**

*No changes with respect to Year 1.*

## 1.4 Policy Objective

While there is wide consensus on the fact that hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application mapping and management environments is much less clear. The consequence is fragmentation: while many research teams are working on one or more of these domains, there is little communication and integration, this leads to duplication of research efforts and overall slow progress.

The teams involved in this activity have a wide-ranging research experience which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ARTIST-DESIGN will help the participants in the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion. In particular, there will be an initial effort in reaching a common consensus on the most critical issues to be addressed, define common terminology and decide about the operational strategy to address them in a collaborative fashion. The expected impact will be a faster and more consistently focused development of methods and tools in support of application development and mapping.

*-- Changes wrt Y1 deliverable -- No changes with respect to Year 1.*

## 1.5 Background

The partners involved in this activity have very active ongoing cooperations on a number of topics. A non-exhaustive set of examples of background cooperation activities is given here.

IMEC, UNIBO, University of Madrid and DUTH have ongoing collaboration on dynamic memory management optimizations at the system level for single processor systems, which they plan to extend in the domain of multiprocessor systems.

ETHZ and UNIBO have ongoing collaborations on optimal management of smart sensors with energy harvesting capabilities. Wireless sensor networks are very relevant example hardware platforms with very tight energy constraints. The limited battery lifetime can be extended indefinitely if the node is equipped with energy harvester that collect and store energy from the environment. However, given the erratic nature of environmental energy sources, the rate at which sensing, computation and storage operations can be performed should be dynamically adjusted to the energy availability using a closed-loop optimal control policy

KTH and UNIBO have cooperated on the development of optimal static mapping strategies for real-time biomedical applications onto multi-core platforms. This work has demonstrated that workload allocation is not sufficient to obtain energy-optimal mappings, as a very significant contribution to the power budget is spent in memory transfers. Hence synergistic memory and computation allocation approach is required.

Linköping and UNIBO have cooperated on allocation and scheduling policies for low power systems, where clock frequency and voltage setting are also degrees of freedom for optimization.

DTU and Linköping have cooperated on optimisation of distributed embedded systems.

EPFL and UNIBO have ongoing activities in the areas on Networks on Chip. Interactions between De Micheli and Madsen are planned through site visits and discussions of research ideas.

*-- Changes wrt Y1 deliverable -- No changes with respect to Year 1.*

## 1.6 Technical Description: Joint Research

The main scientific challenges addressed in this activity are focused on how to map complex applications onto multi-core hardware platforms. This includes addressing allocation and scheduling issues like scalability, flexibility, composability, predictability, design-time reduction and increased dynamism. The problem is complex and multi-faceted. On one hand, we have static (design/compile time) approaches, where applications are analyzed and optimal mapping decisions are taken before the platform is deployed in the field. On the other hand, we have dynamic, run-time approaches where mapping decisions are taken online, and they are triggered by environmental and workload variations. While these approaches start from different premises, they should not be regarded as alternative, rather they are synergistic.

Design time analysis and decisions can help in providing a good starting point for run-time adaptation, moreover off-line pre-computation can reduce the overhead of online policies making them more reactive and less resource-hungry. One important requisite for any mapping strategy is to ensure predictability AND efficiency. Note that online adaptation is not adverse to predictability: if online adaptation is based on feedback control (e.g. finite horizon), it can be used to “stabilize” the system, and make it more robust (predictable) in response to environmental variations (e.g. temperature).

Another scientific challenge addressed in this activity is the development of innovative reliable multicore programming models and architecture platforms able to address computation and control-oriented applications. One key building block is the development of efficient synchronization & communication abstractions that are required for successfully deploying MPSoCs in embedded application domains. Efficiency is inherently related to both power and performance, hence it is an energy metric. In embedded systems, productivity-enhancing abstractions are acceptable only if they do not compromise efficiency, so the focus is on how to enable fast development (debugging, tuning) without losing efficiency. It is also extremely important to take into account variability of both hardware fabrics and application workloads, which is deemed to rapidly increase. Hence, the concurrency management layer should provide means for dynamically managing workload variations, as well as hardware unpredictability sources.

**-- Changes wrt Y1 deliverable --**

*No changes with respect to Year 1.*

## 1.7 Work achieved in Year 1

A number of problems were tackled in Year 1, through several cooperations involving two or more partners. In the following paragraphs, we briefly summarize the problems tackled and the partners involved.

**ETHZ** has been mainly involved in cooperations with **UNIBO** and **TU Dortmund** on new approaches to map algorithms onto highly parallel MPSoC platforms. To this end, the specification and mapping environment DOL (distributed operation layer) was linked to the MPARM simulation platform from UNIBO.

The **Linköping** group has addressed two major issues: *Design optimisation of fault tolerant distributed real-time systems* and *energy efficient design of embedded real-time systems*. Linköping has addressed the problem of energy-efficient design for time constrained

multiprocessor systems. In particular, the problem of thermal-aware energy optimisation has been tackled. The major challenge was to integrate temperature modelling into the framework of energy efficient system level scheduling and voltage selection.

**DTU** has addressed issues related to the following macro-topics: (i) *MPSoC design and architectures*. In this context, the emphasis has been on methods to develop MPSoC platforms, covering application-specific platforms as well as platforms for dynamic reconfiguration. (ii) *MPSoC programming*. In this context, the emphasis has been on exploring high-level programming models for multi-core architectures and on understanding the dynamic behavior of run-time reconfigurable systems with the aim of developing efficient run-time management algorithms. (iii) *Synthesis for Biochips*. This is a new activity which aims at using principles from MPSoC design to design biochips based on digital microfluidics. Emphasis has been on understanding the biochip platform and identifying the design problems related to it.

**UNIBO** has addressed, in cooperation with **ETHZ**, the modelling of miniaturized energy harvesting devices for perpetually powered systems. In particular design of photovoltaic energy harvester for distributed embedded systems was optimized with a methodology, which can be easily applied to embedded systems in order to extend battery lifetime. Furthermore it can be used to optimize the design of harvesting ICs. To this end we proposed an inductor-less architecture, suitable for on-chip integration, which permits to increment the conversion process efficiency at the minimum power consumption.

**IMEC** and its affiliated partners (ie, **DUTH**, **UCM** and **NTNU**) have tackled the establishment of a common profiling and run-time MPSoC resource management exploration framework. More specifically, the existing **MATISSE** and **MATADOR** frameworks were used as foundation and extended using the software metadata and system scenario approaches. Additionally, in collaboration with **DUTH**, **KTH**, **TU/e** and **TU Dortmund** a common design flow and tool flow was investigated in order to link the run-time memory optimization methodologies and tools with the design-time memory optimization and source code parallelization methodologies and tools. This work was performed in cooperation with the Software, Synthesis, Code Generation and Timing Analysis cluster and involved additional teams outside the ArtistDesign network.

Some significant achievements obtained by the partners involved in this activity are summarized below.

### **Temperature Aware System-level Power Optimization (Linköping, UNIBO)**

Linköping and UNIBO have cooperated on system-level design issues, focusing on energy optimization, and more specifically on the optimization of energy-efficient time-constrained multiprocessor systems. In particular, the problem of thermal-aware energy optimisation has been tackled.

The major challenge was to integrate temperature modelling into the framework of energy-efficient system level scheduling and voltage selection.

High power densities in current SoCs result in both huge energy consumption and increased chip temperature. We have elaborated a temperature-aware dynamic voltage-selection technique for energy minimization and performed a thorough analysis of the parameters that influence the potential gains that can be expected from such a technique, compared to a voltage selection approach that ignores temperature. We have also made a study regarding the relevance of taking into consideration transient temperature effects at optimization, the impact of the percentage of leakage power relative to the total power consumed and of the degree to which leakage depends on temperature. Moreover, we have also proposed a temperature-aware task mapping technique for energy optimization in systems with dynamic voltage selection capability.

### Run-time resource management (DTU, IMEC)

Understanding the dynamic behavior of run-time reconfigurable systems is a very complicated task, due to the often very complicated interplay between the application, the application mapping, and the underlying hardware architecture. However, it is a key issue to determine the right reconfigurable architecture and a matching optimal on-line resource management policy. Although architecture selection, application mapping and run-time system have been studied intensively in the past, they have not been thoroughly studied and modelled in the context of run-time reconfigurable systems. DTU has extended its simulation framework COSMOS to study the dynamic behavior of run-time reconfigurable systems. COSMOS is an extension of the ARTS multiprocessor simulation framework which was developed during ARTIST2.

Through a number of design-space exploration experiments, they have pinpointed the critical design issues in the reconfigurable architecture study and analyze their impact on the architecture performance. Experiments with various run-time resource management policies have shown that it is possible to gain performance from such architectures and have suggested some general guidelines for obtaining efficient run-time resource management.

**-- No changes wrt Y1 deliverable --**

*This section was already presented in the Y1 deliverable, in sections 1.7 and 3.1.*

### 1.8 Problem Tackled in Year 2

**UNIBO and ETH Zurich** have contributed in **Optimization-centric MPSoC Design** and have successfully coupled the DOL with MPARM. A runtime environment and a software synthesis tool have been developed by which an application mapping to a multicore system modeled by MPARM can be automatically generated in a correct-by-construction manner from the DOL system-level specification.

**TU Braunschweig** has continued the work on the **reliability analysis for unreliable components** with its industrial partners (in particular Symtavision and Toyota-ITC). Special focus has been put on reliability analysis for the CAN protocol, but the insights can generally be applied to on-chip buses. The interesting emphasis is on the design of mixed-criticality bus configurations. In this context several extensions of the previous analysis methodologies have been developed. While the original approach addresses the occurrence of single bit errors only without any consideration of error correlations, in 2009 models have been proposed to describe interdependencies between errors, especially the occurrence of burst errors. Additionally analysis algorithms have been developed to integrate the burst error models into the original analysis approach.

The **Linköping** group has continued its work on the following two major issues: **Design optimisation of fault tolerant distributed real-time systems** and **Energy efficient design of embedded real-time systems**. Linköping has addressed the problem of energy-efficient design for time constrained multiprocessor systems. In particular, the problem of thermal aware energy optimisation has been tackled. The main goal for the second year was to develop an *on-line* temperature aware dynamic voltage and frequency scaling (DVFS) technique which is able to exploit both static and dynamic slack. An important aspect to be taken into consideration was the fact that temperature has an important impact on frequency and, thus, the frequency does not only depend on the voltage but also on the temperature.

**DTU and Linköping** have continued their cooperation related to the **design and optimisation of fault tolerant mixed hard/soft real-time systems**. During the second year the emphasis of

the work has been on the analysis and optimisation of fault-tolerant hard real-time embedded systems, based on an approach in which hardware and software fault tolerance techniques are combined. The basic trade-off is between processor hardening in hardware and process re-execution in software which, together, have to provide the required levels of fault tolerance against transient faults with the lowest-possible system costs.

**DTU** has studied language constructs that allows the programmer to express communication among tasks in shared memory programming models. **MPSoC design and programming** has also been performed on hardware structures which makes it possible to expose the memory hierarchy to software and allows multiple programming models to co-exist on the same platform. In addition **DTU** is collaborating with Duke University (**DUKE**) on **Synthesis for Biochips**. **DUKE** has proposed a checkpointing-based method, where the droplets that have the right volume are stored on-chip for later use if subsequent operations are faulty. The droplet volumes are determined using capacitance sensing. To capture the fault occurrences in the split operations, **DTU** has proposed a new biochemical application model based on a fault-tolerant sequencing graph, and has shown how scheduling can be performed in this case. **DTU** has proposed a new placement method that considers dynamically moving the operations during their execution. **DTU** has shown that such an approach can lead to significant reductions in biochemical application completion times. **DTU** has also started investigating continuous-flow microfluidic biochips (**CMBs**), which are especially suited for cell culturing.

**UNIBO** has contributed to defining **Design Methodologies for Energy Harvesters**. While in **Y1** a photovoltaic harvester design was optimized, during the second year the focus has been the optimization of power conversion from microwind turbines. In the area of energy harvesting systems, **ETHZ** has worked on **Performance Optimization of Energy Harvesting Embedded Systems**. The work on design of energy harvesting systems has been extended. In particular, we studied systems which switch between a discrete set of modes of operation. To optimize the reward, dedicated algorithms were developed which are highly runtime efficient.

**CEA LIST** has explored various **Architectural Approaches to Design Multi-core Components** able to support dynamically deployment and execution of multi-task applications. In particular, **CEA LIST** has started collaboration with **UNIBO** to analyze pros and cons of asymmetric and symmetric approaches, i.e. architecture with dedicated hardware support for the control w.r.t. architecture built on a set of fully homogeneous resources on top of which control is distributed. For that several architecture are being designed by **CEA LIST**. **CEA LIST** has a dual approach with both timed transaction level simulation and hardware prototyping experiments.

**EPFL** and **UNIBO** have ongoing activities in the areas on **Networks on Chips**. Profs. Demicheli and Benini have been co-advising Ciprian Seiculescu in his doctoral work. Specific joint research topics include design methods and tools for **3D networks on chip**, with particular interest on wire-planning three-dimensional routes. Another common research interest is the design of NoCs with Quality of Service (QoS) guarantees.

-- The above is new material, not present in the Y1 deliverable --

## 2. Summary of Activity Progress in Year 2

### 2.1 Technical Achievements

#### **Design optimisation of fault tolerant distributed embedded systems (Linköping, DTU)**

Linköping University and DTU have an ongoing collaboration concerning the design of fault tolerant embedded systems. During the second year the emphasis of the work has been on the analysis and optimisation of fault-tolerant hard real-time embedded systems, based on an approach in which hardware and software fault tolerance techniques are combined (for the analysis aspects see “Platform and MPSoC Analysis” activity report). The basic trade-off is between processor hardening in hardware and process re-execution in software which, together, have to provide the required levels of fault tolerance against transient faults with the lowest-possible system costs. We have developed design optimization heuristics, to select the fault-tolerant architecture and decide process mapping such that the system cost is minimized, deadlines are satisfied, and the reliability requirements are fulfilled. Our experimental results have shown that, by selecting the appropriate level of hardware hardening and software re-executions, we can satisfy the reliability and time constraints of the applications with considerable reduction of the total hardware cost.

#### **Temperature Aware System-level Power Optimization (Linköping, UNIBO)**

Linköping and UNIBO have cooperated on system-level design issues, focusing on energy optimization, and more specifically on the optimization of energy-efficient time constrained multiprocessor systems. In particular, the problem of thermal-aware energy optimisation has been tackled.

One of the main goals for the second year was to develop an *on-line* temperature-aware dynamic voltage and frequency scaling (DVFS) technique that is able to exploit both static and dynamic slack. The approach implies an offline temperature-aware optimization step and on-line voltage/frequency settings based on temperature sensor readings. An important aspect that we have taken into consideration is the fact that temperature has an important impact on circuit delay and, implicitly, on frequency, mainly through its influence on carrier mobility and threshold voltage. Thus, the frequency does not only depend on the voltage but also on the temperature. In this context, the proposed approach is aware of the frequency/temperature dependency, by which important additional energy savings are obtained.

#### **Synthesis for Biochips (DTU together with DUKE)**

All the current research on the synthesis of digital microfluidic biochips (DMBs) considers that on-chip operations, such as splitting a droplet of liquid, are perfect. However, the reality is that these operations have variability margins, which can impact the correctness of the biochemical application. We consider that an operation which goes beyond specified variability bounds is faulty.

Duke University (DUKE) and the Technical University of Denmark (DTU) are collaborating on this topic. DUKE has proposed a checkpointing-based method, where the droplets that have the right volume are stored on-chip for later use if subsequent operations are faulty. The droplet volumes are determined using capacitance sensing. To capture the fault occurrences in the split operations, DTU has proposed a new biochemical application model based on a fault-tolerant sequencing graph, and has shown how scheduling can be performed in this case.

DTU has proposed a new placement method that considers dynamically moving the operations during their execution. DTU has shown that such an approach can lead to significant reductions in biochemical application completion times. This work was presented at CASES'09 [MPM09] during ESWeek, where it received a best paper award.

DTU has also started investigating continuous-flow microfluidic biochips (CMBs), which are especially suited for cell culturing.

### **MPSoC design and programming (DTU, KTH)**

DTU has studied language constructs that allows the programmer to express communication among tasks in shared memory programming models. Work has also been performed on hardware structures which make it possible to expose the memory hierarchy to software and allows multiple programming models to co-exist on the the same platform [LKM09a, LKM09b, RKS09].

Furthermore, in year 2 DTU and KTH have started a joint research effort aimed at providing SMEs with system-level modeling tools for the design and implementation of time and power critical, heterogeneous systems. The joint research is carried out within a new research project funded by the ARTEMIS JU. The vision is to allow SMEs to build cost-efficient ambient intelligence systems with optimal performance, high confidence, reduced time to market and faster deployment. The focus is on the development of modeling concepts, methods and tools that master system's complexity by allowing cost-efficient mapping of applications and product variants onto an embedded platform; while respecting constraints in terms of resources (time, energy, memory, etc.), safety, security and quality of service. The focus has been on defining a model-of-computation (MoC) which allows to capture continuous time, synchronous time, discrete time and untimed models and their interaction. The MoCs are formally defined using ForSyDe (developed at KTH) and then translated into SystemC modeling templates, which will allow designers to capture and simulate their systems.

### **Runtime resource management (DTU)**

DTU has developed a new reconfigurable hardware platform with self-organizing and self-healing capabilities. The approach has been validated through simulation and a prototype implementation is currently being developed.

Due to the increased need for fault-tolerant systems, several reconfigurable self-healing hardware platforms have emerged in the last decade. This contribution distinguishes itself by being on a higher level of logical granularity and consequently, lowering the cost of implementing large scale systems.

The eDNA platform consists of multiple processors (called cells) interconnected through a NoC. The key to the eDNA platform is the "eDNA" (electronic DNA) which is the medium with which the user programs the platform. The eDNA is simply a behavioural specification of the algorithm the user wants to implement encoded in a binary format such that the cells can read it. The cells self-organise by translating the behavioural specification into a task-graph using a software-to-hardware translational model. Finally, the cells map the task using a mapping strategy called a "growing pattern". The self-healing is implemented by rerunning the self-organisation algorithm. This migrates tasks to healthy cells. eDNA is aimed at becoming a new type of fault-tolerant coarse-grained FPGA. [BoMa09]

*The work on runtime resource management has also been reported in the transversal activity on design for adaptivity.*

### **Component-based service model (DTU together with B&O ICEpower)**

The focus of year 2 has mainly centred on an elaborate case study in which an audio processing platform from ICEpower was explored using the proposed framework. The objective of the exploration was to optimize the platform in terms of silicon area and power consumption, both of which need to be minimized. Due to the very high production volumes of the platform, both cost and performance are critical elements in order to obtain commercial success, making the flexibility of the implementation a secondary objective only. In addition to these objectives, the time-to-market constraints of the system is added, complicating the design process even further by limiting the possibility of exploring the design space severely due to the absence of the possibility of getting feedback on design choices until the system has been realized at a

very low level of abstraction with the current tools available. The increasing time-to-market constraints, however, is making a flexible implementation more attractive both in terms of design time for the current design but also increases the possibility of reusing the platform in future systems. The results of the case-study showed that a platform consisting of application specific processors were actually directly comparable to versions based on a dedicated hardware implementation in terms of silicon area and computational power offered – this is not the case if a standard DSP processor is used. A system level simulations performed using the proposed framework allows the simulation of approximately 20 million cycles per second where as the simulations performed on the traditional RTL descriptions employed at ICEpower only allow the simulation of approximately 15 thousand cycles per second. This work has resulted in two publications [THM09a, THM09b].

### **Slot assignment for TDMA arbiter of system bus through PISA (UNIBO, ETHZ)**

PISA is a framework developed by ETHZ Zurich to represent and solve optimization problems via genetic algorithms. PISA is mainly dedicated to multi-objective search. It splits any problem in two modules: one containing all parts specific to the optimization problem itself (*variator*) and one containing the problem independent part (*selector*). These modules communicate and iterate continuously to reach the solution in a finite time.

UNIBO has interfaced the PISA framework to the MPARM environment. The PISA framework is being used to model and solve the Slot assignment for TDMA arbiters of the system bus. This project has just started and it is still ongoing. The main results will be validated on the MPARM virtual platform developed by UNIBO.

### **Reliability Analysis with mixed-criticality workloads (TU Braunschweig, Toyota-ITC, Symtavision) (see also report section *Integration Driven by Industrial Applications*)**

In 2008 a research trilateral cooperation between TU Braunschweig, Toyota Information Technology Center (T-ITC), and Symtavision GmbH has been initiated, investigating the effects of errors on reliability and safety of real-time networks. Some of the results have been published in 2009 [SE09a], [SE09b]. A follow-up project has been started in 2009. In this context special focus has been put on reliability analysis for the CAN protocol, with special emphasis on the design of mixed criticality bus configurations. In this context several extensions of the analysis methodology have been developed. While the original approach addresses the occurrence of single bit errors only without any consideration of error correlations, in 2009 models have been proposed to describe interdependencies between errors, especially the occurrence of burst errors. Additionally analysis algorithms have been developed to integrate the burst error models into the original analysis approach.

Another subject of interest is the extension of the message release model, which has been restricted to strictly periodic activations in previous approaches. The inclusion of release jitter enables the approach to be applicable to a wider variety of systems. For that purpose the analysis has been extended such that activation patterns with jitter can be incorporated.

### **Architectures for on-chip communication in future multi- and many-core processors (TU Braunschweig, Intel Labs)**

In the COMPOSE Project, the IDA cooperates with Intel Braunschweig on new architectures for on-chip communication in future multi- and many-core processors. The goal is to develop predictable communication mechanisms and service guarantees for real-time and streaming applications. In existing embedded MPSoC, predictable communication comes at the cost of increased latencies for regular best-effort traffic, because this traffic class is treated as a "second class citizen". At the same time, a prioritization of traffic with guaranteed throughput requirements is not beneficial, because streaming applications are usually very latency-tolerant due to their predictable access patterns. IDA has proposed and developed an architecture that is based on distributed traffic shaping and dynamic scheduling to achieve this goal. In contrast to existing schemes, best-effort traffic is prioritized over traffic with throughput guarantees,

which results in improved latency. Traffic shapers in the network routers make sure that best-effort traffic leaves enough free bandwidth to meet the guarantees. An initial version has been presented at the DATE conference 2009 [DE09] and further publications are pending.

### **Optimization-centric MPSoC Design (UNIBO together with ETHZ)**

Multi-Processor System-on-Chip (MPSoC) becomes prevalent for modern embedded system design. Nevertheless, how to program an MPSoC is still an open question. The Distributed Operation Layer (DOL) framework proposes a specific way to answer this question, i.e., adopting the Kahn process network as the model of computation and C/C++ plus XML as the programming language. Within the DOL framework, an MPSoC is specified separately into application, architecture, and mapping, following the orthogonalization of concerns methodology. The DOL application is specified in an architecture-independent manner for the potential design-space exploration of heterogeneous architectures. Therefore, to execute a DOL application on top of a given architecture, a run-time environment is requested to provide architecture-dependent services, such as multi-processing of each processor core and the inter-process communication.

We have successfully coupled the DOL framework (developed at ETHZ) with the MPARM cycle-accurate simulator (developed at UNIBO) such that an application specified within the DOL can efficiently execute on top of the MPARM platform in a correct-by-construction manner. The MPARM is a cycle-accurate simulator which consists of a variable number of ARM cores connected via a shared AMBA bus. We focused on the run-time environment built on top of the MPARM simulator. We developed a multi-processing implementation based on the RTEMS operating system. For the inter-process communication, four mechanisms are introduced to exploit the potential of the MPARM architecture.

### **Performance Optimization in Energy Harvesting Systems (ETHZ)**

We have continued to work on the design of embedded systems which are powered by environmental sources, such as solar energy. For such systems, power management is still a critical issue, since the quality of service has to be adapted dynamically. As the available energy of an electronic device changes over time and is limited by many environmental factors, the system has to decide when to change to which service level to optimize the system performance.

In contrast to our recent work, where the adaptation of *continuous* parameters (e.g. the duty cycle, data sensing or transmission rates) has been studied, we now turned to systems with *discrete* parameters. Specifically, we take a first step to obtain a more realistic application model using a *finite set of discrete levels* of service. We explore how to allocate service levels when the number of the available service levels is fixed and the reward function is an arbitrary function. Our main results are algorithms which are based on the principle of dynamic programming to compute optimal as well as approximated service levels. In addition, we propose methods to dimension important platform parameters, like e.g. the battery size, the size of the solar panels (for solar harvesting systems) as well as a suitable prediction horizon.

### **Design and optimization of Energy Harvesting Systems (UNIBO)**

Energy harvesting has confirmed as an innovative way to keep small stationary hardware platforms running unattended for years or even decades relaxing hard constraints of battery autonomy. UNIBO, after having addressed photovoltaic solutions in Y1 analysed wind flow as feasible energy source to meet the energy needs of a standalone embedded systems. UNIBO provided a detailed model and characterization of the micro wind turbine and an effective power-saving architecture to control the circuit through ultra low-power components. The optimized design a wind flow harvester has been addressed and highly efficient buck-boost converters which perform automatic power point tracking circuit have been developed.

**Erika RTOS porting on MPARM (UNIBO, SSSA)**

Erika (Embedded Real time Kernel Architecture) is a fully functional RTOS developed by Scuola Superiore Sant'Anna of PISA (SSSA) With Erika it is possible to create periodic Real Time task sets and to schedule them under different policies. The kernel provides all functionalities to specify and run such tasks.

The cooperation between UNIBO and SSSA mainly regards the porting of Erika on MPARM. The main goal of the collaboration between SSSA and UNIBO was to couple the Erika framework with the MPARM simulator, such that on one hand, Erika applications can execute on a cycle-accurate MPSoC simulator, and on the other hand, MPARM can benefit from the Erika RTOS features.

**MPSoC mapping tools for multimedia and wireless applications (IMEC vzw.)**

The MPSoC mapping tools help with two common tasks when developing software for MPSoC systems. The memory hierarchy (MH) tool deals with exploiting the memory hierarchy of embedded systems by transforming code and mapping data on particular memory regions to minimize the application's overall power consumption. The second tool, MPSoC Parallelizing Assistant (MPA), helps with parallelizing applications. In the second year of the MPSoC design activity, the MPSoC mapping tools were used to explore optimization options for the MPSoC mapping of multimedia (e.g., MPEG4 encoder) and wireless network applications (e.g., Software Defined Radio applications).

**Multi-granularity NoC simulation framework (IMEC vzw. and National Technical Univ. Athens (NTUA)/ DUTH).**

This collaboration focuses on a modeling framework that enables the simulation of complex, dynamic hardware/software Software Design Radio designs. It enables an exploration, which can pinpoint the platform component requirements for future SDR applications in a very early design phase based on functional and cycle accurate simulation of software components on the explored multicore virtual platforms.

**MPSoC Architecture exploration (CEA LIST)**

The CEA LIST has worked on a prototype of an FPGA board, realising an asymmetric architecture (SCMP), based on a hardwired control unit dealing with task selection, scheduling and allocation. Some special low power features was also implemented. On this prototype, for a connected-component labeling application, and despite the dynamic behavior of the application, the dedicated control structure allows to take full advantage of the application parallelism. The average processor usage rates have been increased by 35% regarding a solution with static allocation of the tasks onto processors. In the same time, low power features allow to save 30% of the energy. In conjunction to these prototyping experiments, CEA LIST has studied flexible approaches replacing the hardwired controllers by programmable ones to deploy application-specific control schemes. Objective is to compare performance degradation due to the lower performance of the controller, to the control complexity reduction, and due to the specialization of the runtime services.

In parallel to the design of the asymmetric MPSOC,, CEA LIST has started, in cooperation with UNIBO, to explore symmetric solutions. In that context, objective is to provide dedicated hardware support to accelerate the runtime services that are running in a distributed fashion accross all of the processors. This solution saves the silicon of a centralized controller but reduces occupation rates of computing resources. Objective is thus to reduce time needed to execute runtime services by using a shared accelerator helping to deal with synchronization of shared memory structures.

**Quality of Service guarantees for Networks on Chips (EPFL with UNIBO)**

The activities of the group LSI of EPFL (De Micheli) started in the late summer 2009. Thus, the

activities have been limited. Nevertheless, there has been an important collaboration with UNIBO (Benini) on Quality of Service (QoS) guarantees for NoCs. This work has led to a paper presented at the ICCAD conference [Rahm09] in November 2009.

The research contribution can be summarized as follows. Many Networks-on-Chip (NoC) applications exhibit one or more critical traffic flows that require hard Quality of Service. Guaranteeing bandwidth and latency for such real time flows is crucial. In this research, we investigated novel methods to efficiently calculate worst-case bandwidth and latency bounds and thereby provide hard QoS guarantees. It is important to stress that the proposed methods apply even to best-effort NoC architectures, with no extra hardware dedicated to QoS support. By applying our methods to several realistic NoC designs, we show substantial improvements (on average, more than 30% in bandwidth and 50% in latency) in bound tightness with respect to existing approaches.

**-- The above is new material, not present in the Y1 deliverable --**

## 2.2 Individual Publications Resulting from these Achievements

### DTU

[MPM09] Elena Maftai, Paul Pop, Jan Madsen, "Tabu search-based synthesis of dynamically reconfigurable digital microfluidic biochips", in Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, 2009, pp. 195-204.

[LKM09a] P. Larsen and S. Karlsson and J. Madsen, Identifying Inter-Task Communication in Shared Memory Programming Models, Proceedings of IWOMP '09

[LKM09b] P. Larsen and S. Karlsson and J. Madsen, Data-dependencies and Thread Interaction in Parallel Loops, Proceedings of Artist Workshop on Mapping Applications to MPSoC, 2009

[RKS09] M. S. Rasmussen, S. Karlsson and J. Sparsø, Performance Analysis of a Hardware/Software-based Cache Coherence Protocol in Shared Memory MPSoCs, Workshop on Programming Models for Emerging Architectures (PMEA), 2009.

[BoMa09] Michael Reibel Boesen, Jan Madsen, eDNA: A Bio-Inspired Reconfigurable Hardware Cell Architecture Supporting Self-organisation and Self-healing, in the proceedings of the 2009 NASA/ESA Conference on Adaptive Hardware System (AHS-2009), July-August 2009.

[THM09a] A. Tranberg-Hansen, J. Madsen, Exploration of a Digital Audio Processing Platform Using a Compositional System Level Performance Estimation Framework, In proceedings of the IEEE Symposium on Industrial Embedded Systems (SIES), 2009

[THM09b] Anders Tranberg-Hansen, Jan Madsen, Framework for Exploring MPSoC Systems, in Proceedings of the International Conference on Hardware-Software Codesign and System Synthesis (CODES-ISSS), 2009

### ETHZ

[HKH09] Wolfgang Haid, Matthias Keller, Kai Huang, Iuliana Bacivarov, and Lothar Thiele. Generation and Calibration of Compositional Performance Analysis Models for Multi-Processor Systems. In Proc. Int'l Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), pages 92—99, Samos, Greece, July 2009.

[HHB09] Kai Huang, Wolfgang Haid, Iuliana Bacivarov and Lothar Thiele: Coupling MPARM with DOL, TIK-report number 314, Computer Engineering and Networks Laboratory, ETH Zurich, November 2009.

[MCT09a] Clemens Moser, Jian-Jia Chen and Lothar Thiele, Power Management in Energy Harvesting Embedded Systems with Discrete Service Levels In The International Symposium on Low Power Electronics and Design (ISLPED 09), San Francisco, California, August 19-21, 2009.

[MCT09b] Clemens Moser, Jian-Jia Chen and Lothar Thiele, Optimal Service Level Allocation in Environmentally Powered Embedded Systems In *The 24th ACM Symposium on Applied Computing (SAC 09)* Honolulu, Hawaii, March 8-12, 2009.

### **TU Braunschweig**

[DE09] Jonas Diemer and Rolf Ernst. A Link Arbitration Scheme for Quality of Service in a Latency-Optimized Network-on-Chip, in Proceedings of the conference on Design, Automation and Test in Europe (DATE), April 2009

[SE09a] Maurice Sebastian and Rolf Ernst. Reliability and Safety Guarantees in Modern MPSoCs with Real-Time Requirements. edaWorkshop 2009. Dresden. (see also report section Integration Driven by Industrial Applications)

[SE09b] Maurice Sebastian and Rolf Ernst. Reliability Analysis of Single Bus Communication with Real-Time Requirements. 15th Pacific Rim International Symposium on Dependable Computing. Shanghai, November 2009. (see also report section Integration Driven by Industrial Applications)

### **UNIBO**

[BB09] Davide Brunelli and Luca Benini. Designing and Managing Sub-milliwatt Energy Harvesting Nodes: Opportunities and Challenges. in Proceedings of the First International Conference on Wireless Communications, Vehicular Technology, Information Theory and Aerospace & Electronic Systems Technology. Wireless VITAE 2009, pp.11-15, 17-20 May 2009, Aalborg, doi: 10.1109/WIRELESSVITAE.2009.5172413

[BRB09] Andrea Bartolini, Martino Ruggiero, Luca Benini. HVS-DBS: human visual system-aware dynamic luminance backlight scaling for video streaming applications. EMSOFT 2009: 21-28

[BBB09] Carlo Bergonzini, Davide Brunelli and Luca Benini. Algorithms for Harvested Energy Prediction in Batteryless Wireless Sensor Networks. in Proceedings of the 3rd IEEE International Workshop on Advances in Sensors and Interfaces, IWASI 2009, pp.144-149, 25-26 June 2009, doi: 10.1109/IWASI.2009.5184785

### **Linköping**

[BAEP09] M.Bao, A. Andrei, P. Eles, Z. Peng, "On-line Thermal Aware Dynamic Voltage Scaling for Energy Optimization with Frequency/Temperature Dependency Consideration," Design Automation Conference (DAC 2009), San Francisco, USA, July 26-31, 2009, pp. 490-495.

**IMEC vzw**

[PRAF09] Palkovic, M.; Raghavan, P.; Ashby, T.; Folens, A.; Cappelle, H.; Glassee, M.; Van der Perre, L. and Catthoor, F.: Parallelization exploration of wireless applications using MPA. In International Conference on Parallel Computing. Mini-Symposium: Programming Heterogeneous Architectures, Lyon, France, (2009)

[PRLD09] Palkovic, M.; Raghavan, P.; Li, M.; Dejonghe, A.; Van der Perre, L. and Catthoor, F.: Architecture and Mapping Flow for Multi-Core SDR Platforms. In IEEE Signal Processing Magazine, (to appear in 2009)

[MW09] Jean-Yves Mignolet, Roel Wuyts: Embedded Multiprocessor Systems-on-Chip Programming. In IEEE Software journal p.34-41, Vol.26, Issue 3, (2009)

**EPFL**

[Rahm09] Dara Rahmati, Srinivasan Murali, Luca Benini, Federico Angiolini, Giovanni De Micheli and Hamid Sarbazi-Azad, "A Method for Calculating Hard QoS Guarantees for Networks-on-Chip," ICCAD, San Jose, November 2009.

[Mula09] F. Mulas, D. Atienza, A. Acquaviva, S. Carta, L. Benini, and G. De Micheli, "Thermal Balancing Policy for Multiprocessor Stream Computing Platforms," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 28, no. 12, pp. 110-123, 2009.

**-- The above are new references, not present in the Y1 deliverable --**

**2.3 Interaction and Building Excellence between Partners****Energy efficient embedded system design (Linköping, UNIBO)**

The interaction in this activity has been between Linköping and UNIBO.

- Meeting/discussion at the conference "Design, Automation and Test in Europe (DATE09)", Nice, France, April 20-24, 2009.
- The MPARM platform from UNIBO has been extensively used for the thermal-aware energy minimisation experiments at Linköping. This has led to frequent interactions between the groups.

**DOL-MPARM (ETHZ)**

Joint meeting with Joseph Sifakis' group; location: Grenoble, France; date: 13th of October 2009: Kai Huang presented the currently available execution platforms for the DOL framework, in particular the DOL runtime environment for the MPARM platform.

**Design of fault tolerant distributed embedded systems systems (Linköping, DTU)**

The interaction in this activity has been between Linköping and DTU.

- Meeting/discussion at the conference "Design, Automation and Test in Europe (DATE09)", Nice, France, April 20-24, 2009.
- Paul Pop from DTU has visited Linköping several times during 2009.

**Slot assignment for TDMA arbiter of system bus through PISA (UNIBO, ETHZ)**

The interaction in this activity has been between ETHZ and UNIBO.

- Several phone meetings/discussions between UNIBO and ETHZ during 2009.
- The MPARM platform from UNIBO has been extensively used by ETHZ. This has led to frequent interactions between the groups.
- The PISA environment from ETHZ has been used by UNIBO. This has led to frequent interactions between the groups.

### **Erika RTOS porting on MPARM (UNIBO, SSSA)**

The interaction in this activity has been between SSSA and UNIBO.

- Several phone meetings/discussions between UNIBO and SSSA during 2009.
- The MPARM platform from UNIBO has been extensively used by SSSA. This has led to frequent interactions between the groups.

### **Multi-granularity NoC simulation framework (IMEC vzw. and National Technical Univ. Athens (NTUA)/ DUTH).**

- Several phone meetings/discussions between IMEC and **DUTH** during 2009.

### **MPSoC Architecture exploration**

Interaction between CEA LIST and UNIBO in this activity is based on face-to-face meetings in Saclay and Genoble and numerous phone meetings to clarify technical aspects regarding symmetric architecture design or runtime software.

#### **-- Changes wrt Y1 deliverable --**

*Extensive used of MPARM platform (UNIBO) and PISA environment (ETHZ) by the partners.*

## **2.4 Joint Publications Resulting from these Achievements**

### **Linköping and DTU:**

[PIE09] P. Pop, V. Izosimov, P. Eles, and Z. Peng, "Design Optimization of Time- and Cost-Constrained Fault-Tolerant Embedded Systems with Checkpointing and Replication," IEEE Trans. on Very Large Scale Integrated (VLSI) Systems, V17, N3, 2009, pp. 389-402.

[IPP09] V. Izosimov, I. Polian, P. Pop, P. Eles, and Z. Peng, "Analysis and Optimization of Fault-Tolerant Embedded Systems with Hardened Processors," Design Automation and Test in Europe (DATE) Conference, Nice, 2009, pp. 682 – 687.

### **UNIBO and ETHZ**

[MBT09] M. Magno, D. Brunelli, L. Thiele and L. Benini, "Adaptive Power Control for Solar Harvesting Multimodal Wireless Smart Camera", in proceedings of the 3rd ACM/IEEE International Conference on Distributed Smart Cameras ICDSC, 2009

[BMT09] Brunelli, D., Moser, C. Thiele, L. and Benini, L., Design of a Solar Harvesting Circuit for Battery-less Embedded Systems (2009), in: IEEE Transactions on Circuits and Systems I: Regular Papers,, 56:11(2519-2528)

## IMEC vzw. and National Technical Univ. Athens (NTUA)/ DUTH

[ZTB09] Zompakis, N.; Trautmann, M.; Bartzas, A.; Mamagkakis, S.; Soudris, D.; Van der Perre, L. and Catthoor, F.: Multi-granularity NoC simulation framework for early phase exploration of SDR hardware platforms . In 19th International Workshop on Power and Timing Modeling, Optimization and Simulation – PATMOS, Delft, Netherlands, (2009)

## UNIBO and EPFL

[ZAB09] Zanini, F.; Atienza, D.; Benini, L.; De Micheli, G.; Multicore thermal management with model predictive control. Circuit Theory and Design, 2009. ECCTD 2009. 23-27 Aug. 2009 Page(s):711 - 714

[SMBD09] Seiculescu, C.; Murali, S.; Benini, L.; De Micheli, G.; NoC topology synthesis for supporting shutdown of voltage islands in SoCs. Design Automation Conference, 2009. DAC '09. 46th ACM/IEEE; 26-31 July. 2009 Page(s):822 - 825

[SPBD09] Sathanur, A.; Pullini, A.; Benini, L.; De Micheli, G.; Macii, E.; Physically clustered forward body biasing for variability compensation in nanometer CMOS design. Design, Automation & Test in Europe Conference & Exhibition, 2009. DATE '09. 20-24 April 2009 Page(s):154 - 159

[SMB09] Seiculescu, C.; Murali, S.; Benini, L.; De Micheli, G.; SunFloor 3D: A tool for Networks On Chip topology synthesis for 3D systems on chips. Design, Automation & Test in Europe Conference & Exhibition, 2009. DATE '09. 20-24 April 2009 Page(s):9 - 14

**-- The above are new references, not present in the Y1 deliverable --**

## 2.5 Keynotes, Workshops, Tutorials

### Seminar: Integrated Control-Path Design and Error Recovery in the Synthesis of Digital Microfluidic Biochips

*Lyngby, Denmark – October 27<sup>th</sup>, 2009*

Krishnendu Chakrabarty (Duke University) visited DTU on October 27 for a full day workshop with the aim to discuss and plan joint research within the area of biochips. During the event, Krishnendu gave a seminar on "Integrated Control-Path Design and Error Recovery in the Synthesis of Digital Microfluidic Biochips".

### Tutorial: Mapping applications onto Multi-Core Platforms

#### ARTIST Summer School in China

*Beijing, China – July 19-24, 2009*

Jan Madsen gave a tutorial/course on the challenges of mapping applications onto a multi-core platform. The course covered basic and advanced scheduling algorithms for task scheduling on parallel systems.

<http://www.artist-embedded.org/artist/Overview,1630.html>

### Mini Keynote : Mapping bio-chemical applications onto microfluidic-based biochips

#### 9th International Forum on Embedded MPSoC and Multicore

*Savannah, Georgia, USA – August 2-7, 2009*

Jan Madsen gave an in-depth technical presentation on the challenges of mapping bio-chemical applications onto microfluidic-based biochips. The presentation discussed similarities and new challenges as compared to online dynamic reconfigurability of digital reconfigurable

multicore architectures.

<http://www.mpsoc-forum.org/2009/index.html>

**Presentation: Identifying Inter-Task Communication in Shared Memory Programming Models**

**ArtistDesign/HiPEAC2 workshop (IWOMP'09)**

*Dresden, Germany– June 3-5, 2009*

Per Larsen from DTU presented work on extending OpenMP for multicore programming, by having constructs to help identifying the actual inter-task communication.

<https://iwomp.zih.tu-dresden.de/>

**Presentation: Data-dependencies and Thread Interaction in Parallel Loops ArtistDesign workshop on Mapping Applications to MPSoC**

*Schloss Rheinfels, St. Goar, Germany– June 29-30, 2009*

Per Larsen from DTU presented the initial work on extending OpenMP for multicore programming.

<http://www.artist-embedded.org/artist/Overview,1614.html>

**Workshop: ESTIMedia 2009: Workshop on Embedded Systems for Real-Time Multimedia, October 15-16, 2009, Grenoble, France**

The aim of this workshop was to bring together people from different multimedia-related research communities (e.g, software, architectures, real-time systems, DSP, compilers, multimedia applications) who have worked separately, but did not interact sufficiently to address the challenges facing the design of hardware and software for multimedia systems.

<http://www.science.uva.nl/events/ESTIMedia09/>

**Workshop: Smart and Efficient Energy Council (SEEC'2009)**

Invited talk: "Energy-neutral distributed sensing for proactive energy management in buildings and plants"

October 8-9, 2009, Trento, Italy

Speaker: Luca Benini

Luca Benini gave a talk on the system challenges of designing wireless sensor networks, particular emphasizing the challenges of making these systems self-powered using energy harvesting techniques. The focus of the workshop was on energy efficiency as a major contributor to the green economy

<http://www.artist-embedded.org/artist/-SEEC-09-.html>

**Tutorial: S. Mamagkakis and P. R. Panda 'Memory Architectures and Software Transformations for System Level Design', ASP-DAC 2009**

*Yokohama, Japan, – January, 2009*

In this tutorial a memory-aware system level design flow was presented that can address strict power and performance budgeting problems by customizing both the underlying memory architectures/organizations, as well as by transforming the system-level source code to generate an input for system-level design that is better tuned to the memory architectures and organizations. Such a "memory-aware" system level design flow can result in LSI designs exhibiting superior performance, power and memory footprint characteristics.

<http://www.aspdac.com/aspdac2009/tutorial/>

**Keynote: D. Verkest 'Multimedia systems in a changing technology landscape', ESTIMedia 2009**

*Grenoble, France, – October, 2009*

Silicon IC technology scaling delivers the required transistor densities to meet the computational needs of multimedia systems, however, at an ever increasing cost. Changes in the technology landscape influence multimedia systems architectures, resulting in design challenges and opportunities. In this presentation, we provided a glimpse of this technology-design interaction in the context of multimedia systems, touching upon multi-core architectures, 3D chip-stacking, and embedded MEMS technology.

<http://www.science.uva.nl/events/ESTIMedia09/keynotes.html>

**Keynote: S. Mamagkakis 'Emerging multicore hardware platforms and their software support challenges', ECRTS 2009**

*Dublin, Ireland, – July, 2009*

In this keynote talk, the latest developments and future directions of hardware MPSoC platforms for nomadic embedded applications were presented. Next to the hardware perspective, the software related challenges of these emerging MPSoC platforms were discussed and some of the proposed parallelization and memory hierarchy management solutions were evaluated. This keynote is also relevant for the Scheduling and Resource Management activity.

<http://ecrts09.dsg.cs.tcd.ie/keynote-speaker.php>

**Keynote: Giovanni De Micheli: 'System-Level Design Technologies for Heterogeneous Distributed Systems', CATRENE, Dresden 2009 and SIES, Lausanne, 2009**

Smart micro/nano systems will foster a revolution in health and environmental management, with the final objective of improving security and quality of life. At the same time, they will create a large market of components and systems, and a renewed perspective for electronic design and manufacturing companies. Such systems will be the fundamental building blocks of wearable and ambient systems, to gather and integrate heterogeneous data in real time and to operate and communicate in a wireless and ultra low power mode. The design of these systems will be enabled by the hybridization of manufacturing technologies which enables us to attain unprecedented levels performance as well as to integrate electronic and fluidic circuits with sensors and actuators. To accomplish this ambitious goal, new technologies and architectures must be matched and tailored to the operational environment by solving novel and challenging design and optimization problems, through the creation of novel design methodologies and tools.

**Keynote: Giovanni De Micheli: 'Design of Micro/Nano Systems for a healthier and safer tomorrow', FETCH, Chexbres 2009.**

Intelligent microsystems will revolutionize health and environmental management systems and will be the core of large-scale distributed systems capable of collecting, integrating and analyzing large-scale data. Such systems will be realized through an hybridization of technologies that will merge sensors, electronic, processing and communication components. We expect this area to do a driving force in the semiconductor and system sectors of the European economy.

**-- The above is new material, not present in the Y1 deliverable --**

### 3. Milestones, and Future Evolution

#### 3.1 *Problems to be tackled over the next 12 months (Jan 2010 – Dec 2010)*

##### **Design of fault tolerant distributed embedded systems (DTU, Linköping)**

During the third year Linköping and DTU will continue their work on fault tolerant distributed and multiprocessor embedded systems. The emphasis during the third year will be on the optimised implementation of error detection techniques.

##### **Energy efficient embedded system design (Linköping)**

Linköping will continue the research concerning temperature aware and energy efficient design of real-time embedded systems. During the third year we will continue our work on elaboration of fast and sufficiently accurate analytical temperature models for the system level. We will also elaborate, in addition to our temperature aware dynamic voltage scaling techniques, new techniques for temperature aware power management.

##### **Design and optimization of Energy Harvesting Systems (UNIBO)**

University of UNIBO will continue the research concerning on energy-harvesting system design and their optimization techniques through maximum power point techniques. Innovative and different energy conversion methods will be explored and assessed.

##### **Slot assignment for TDMA arbiter of system bus through PISA (UNIBO, ETHZ)**

The PISA framework is being used to model and solve the Slot assignment for TDMA arbiter of system bus. The PISA framework will provide a feasible TDMA slot assignment and the MPARM simulator will be used to validate the PISA solution. Each slot assignment can be modeled as an Individual, and the Fitness function can be set to the number of deadline misses obtained with the system validation through a simulation. The final goal is to minimize the fitness function. The key for improving performance is the choice of a good selection function (PISA selector module) which should provide a fast and optimal search over the design space to produce good new candidates for Recombination and Mutation. Since mutation and recombination are done randomly, a good heuristic should be designed to ensure an algorithm quick convergence.

##### **Erika RTOS porting on MPARM (UNIBO, SSSA)**

Erika RTOS will be used to analyze different bus scheduling policies for enhancing system predictability. How overall task predictability is affected by non-uniform traffic on the bus will be analyzed for different bus arbitration policies.

##### **Synthesis for Biochips (DTU)**

Regarding Digital Microfluidic Biochips (DMBs), we will continue the investigation on the issue of operation variability. First, DTU and DUKE will propose a fault model for DMBs to capture the probability of faulty operations. DTU will focus on providing synthesis methods that can take as input a fault-tolerant sequencing graph that describes the different fault scenarios. These methods will be compared with the checkpointing techniques proposed by DUKE.

Another avenue to be explored is related to the modeling of on-chip devices. Currently the devices are considered of fixed rectangular size. However, the devices are virtual in their nature (grouping together identical electrodes), and thus any electrodes can be used, constructing any shapes, not only rectangles. We will investigate if improvements can be obtained by considering devices of any shape.

Regarding Continuous Fluidic Biochips (CFBs), we are interested to propose models for the biochemical application and for the biochip architecture. Once the right modeling approach has been identified, we will implement a simulator in SystemC to simulate a prototype of a cell culture chamber with 256 parallel virtual experiments.

### **MPSoC architectures and programming models (DTU)**

DTU will continue to work on programming models for multi-core architectures. In particular,

- developing a task-based shared-memory programming model where inter-task communication is made explicit.
- studying how a programmable interconnect interface can be used to implement multiple programming models and facilitate performance debugging.
- initiating research into scalable operation systems with emphasis both on homogeneous and heterogeneous architectures.

We will aim to initiate the cooperation between DTU and IMEC in year 3. The cooperation between DTU and KTH will be continued with emphasis on the MoCs and their interaction, captured in ForSyDe as well as in SystemC. Work towards design space exploration will also be initiated, in particular towards capturing cost models and risk analysis.

### **Runtime resource management (DTU)**

DTU will continue to develop on the new reconfigurable hardware platform with self-organizing and self-healing capabilities. Two directions will be taken,

- development of a prototype of the platform
- investigation of self-healing strategies which will ensure high performance after fault recovery.

### **Component-based service model (DTU)**

DTU will continue the refinement of the modelling framework and development of tools for design space exploration. The modeling framework will be used to initiate the specification of a new generation of mobile audio processing platforms at B&O ICEpower.

### **Quality of Service on Network on Chip (EPFL, UNIBO, ETHZ)**

EPFL plans include several activities. On the research side, we plan to extend research on Networks on Chip enhancing quality of service measures, with specific attention to switch design. Furthermore EPFL plans an interaction with Profs. Benini and Thiele to study hardware abstractions for 3D systems, also in conjunction with an approved FP7 project.

### **MPSoC Architecture exploration (CEA LIST, UNIBO)**

The CEA LIST and UNIBO will focus during year 2010 on the optimization of hardware support for runtime services in symmetric architectures. The runtime services explored in the "Platform and MPSOC Analysis" group will be considered to run on this platform, and efficient implementation of these services, taking benefits from the hardware support, will be proposed. The asymmetric and symmetric approaches will finally be compared in their ability to deal with dynamicity of multi-task applications.

**-- Changes wrt Y1 deliverable --**

*Milestones and problems to be tackled over the next 12 months are expected to be the evolution of Y1 deliverable.*

### **3.2 Current and Future Milestones**

#### **Design of fault tolerant distributed embedded systems**

During the second year we will address the issue of design and optimisation of fault tolerant distributed and MPSoC systems considering various hardening degrees of the underlying hardware platform. This will be based on the analysis techniques developed as part of the "Platform and MPSoC Analysis" activity.

*The above milestone has been fulfilled.*

#### **Milestone for the third year:**

**Development of new optimisation approaches for implementation of error detection techniques.**

#### **Energy efficient embedded system design**

During the second year the research concerning temperature aware and energy efficient design of real-time embedded systems will be continued with the following two milestones:

1. Exploiting the relation between temperature and frequency in order to further improve the efficiency of dynamic voltage/frequency selection.

*The above milestone has been fulfilled.*

2. Application of fast and sufficiently accurate analytical temperature models for the system level, which allow for a more efficient design space exploration.

*The above milestone has been fulfilled with work in the same direction also continuing during the third year.*

#### **Milestone for the third year:**

- **Development of new techniques for energy efficient, temperature aware power management, in addition to the existing DVS techniques.**

#### **Modelling of and evaluation of fault-tolerance mechanisms with respect to real-time Y1:**

TU Braunschweig will investigate the performance implications of fault-tolerance mechanisms in real-time systems. For this, event and error models will be introduced to model the occurrence of transient errors. We will propose and evaluate different methods to capture the run-time behaviour of unreliable components.

*This milestone has been fully achieved. Initial timing models have been developed to reflect the performance of such systems in the error-free case as well as in case of errors. These models enable an exact specification of the timing effects different fault-tolerance mechanisms may have. We have proposed two methods for reliability evaluation: One is Monte-Carlo simulation, in which errors are randomly introduced into a simulation, another one is formal analysis, which delivers faster results.*

- **Y2: Extension of reliability analysis to more general systems with extended event and error models**

To improve the applicability and precision of the initial reliability analysis, TU Braunschweig will work on extending this concept to more complex models, such as release jitter and burst errors. This will remove the current constraints of reliability analysis methods, which are restricted to simplified system and component models. Constraints to be addressed are the exclusive consideration of strictly period activations as well as the analysis of single bit errors without any correlation amongst each.

*This milestone has been partially achieved until now. First internal analysis prototypes are available to explore the effects of release jitter and burst error occurrences on reliability.*

**Y3: In 2010 these prototypes will be refined. Further on the consideration of other protocols will be taken into account, especially FlexRay as an up-to-date automotive bus system.**

### **Synthesis of digital microfluidic biochips**

In year 1 DTU and Duke will work on digital microfluidic biochips. The goal is to model a biochemical application executing on a two-dimensional array of cells, where each cell can hold a droplet. A synthesis methodology that, starting from a biochemical application and a given biochip, determines the allocation, placement, resource binding, and scheduling of the operations in the application will be developed. The placement step should take into account potentially faulty cells, reconfiguring the biochip to provide fault-tolerance.

*The above milestone has been fulfilled*

In year 2 DTU and Duke will propose a more realistic biochip and biochemical application model, which can take into account the variability in the current biochip implementations, and the potential for contamination during operations. The addressed design tasks will be revisited considering the new stochastic model and contamination constraints.

*The above milestone has been fulfilled, except for the contamination model which has turned out to be a more challenging task*

**During the third year, DTU and DUKE will propose a fault model for DMBs to capture the probability of faulty operations. DTU will focus on providing synthesis methods that can take as input a fault-tolerant sequencing graph that describes the different fault scenarios. DTU will work on developing a model for continuous fluidic-based biochips.**

### **MPSoC architectures and programming models**

In year 1, DTU worked on architectures and programming models for MPSoC platforms. The goal was to focus on two areas i) exploring high-level programming models focusing on programmer-productivity and ii) investigating the hardware/software interface between the processing elements and the interconnect network.

*The above milestone has been fulfilled*

In year 2, DTU will continue this work and start a collaboration with IMEC. No concrete collaboration action points have been defined. The primary purpose is to discuss memory performance models. However, IMEC's work on nomadic embedded systems will also be discussed and possible collaboration areas will be identified.

*The above work planned for DTU has been fulfilled. The collaboration with IMEC has not been initiated.*

During the third year, DTU will continue to work on programming models for multi-core architectures. In particular, developing a task-based shared-memory programming model where inter-task communication is made explicit. Potential programming models for dynamically reconfigurable architectures will also be studied. DTU will continue studying how a programmable interconnect interface can be used to implement multiple programming models and facilitate performance debugging. DTU is also initiating research into scalable operation systems with emphasis both on homogeneous and heterogeneous architectures. DTU and KTH will continue their work on defining a set of MoCs and their interactions, captured in ForSyDe as well as in SystemC. Initial experiments with industry cases are planned. Design space exploration able to incorporate risk analysis and development cost models will also be considered.

### Run-time resource management

In year 1 DTU extended work on run-time reconfigurable systems started in ARTIST2. The goal is to extend the COSMOS model to be able to experiment with different run-time resource management policies.

*The above milestone has been fulfilled*

In year 2 DTU will continue the work on run-time reconfigurable systems and extend the focus on the hardware architecture to support run-time reconfiguration and selfmaintenance.

*The above milestone has been fulfilled*

During the third year, DTU will continue to develop on the new reconfigurable hardware platform with self-organizing and self-healing capabilities. A prototype of the platform will be implemented as a multicore architecture on a FPGA. One of the aims of the platform is to have a very robust and fault-tolerant platform. A key issue to be studied is how to make sure that the platform performs well after faultrecovery, this topic will be explored.

### Component-based service model

In year 1 DTU extended its service-based model initiated during ARTIST2, to be applied in an industrial setting together with B&O ICEpower. The goal is to extend the model to capture MPSoC systems and to show the feasibility of the model by applying it to a simple industrial case.

*The above milestone has been fulfilled*

During the second year, DTU and B&O ICEpower will extend the work on the service-based model with focus on performance evaluation of MPSoC platforms. Focus will be on modeling the software executing on the platform and on experimenting with a larger case study.

*The above milestone has been fulfilled*

During the third year, DTU will focus on a further refinement of the framework and development of tools that will allow a higher degree of automation supporting the individual steps in the framework. Furthermore, the framework will be used in parallel with the traditional design flow at the B&O ICEpower to initiate the specification of a new generation of mobile audio processing platforms, continuing the assessment and improvement of the framework based on real use.

### Optimization-centric MPSoC Design (UNIBO, ETHZ)

The DOL and MPARM tools of ETHZ and UNIBO have been coupled in the first year.

*The above milestone has been fulfilled*

**During the third year, UNIBO and ETHZ will use the integrated mapping/simulation framework in their research activities assessing its performance, and they will improve it to have a full-featured prototype within the time frame of the ARTISTDesign NoE.**

### Designing Best Effort Networks-on-Chip to Meet Hard Latency Constraints (EPFL and UniBO)

Many classes of applications require Quality of Service (QoS) guarantees from the system interconnect. In Networks-on-Chip (NoC) QoS guarantees usually translate into bandwidth and latency constraints for the traffic flows and require hardware support in the NoC fabric and its interfaces. We will investigate NoC synthesis techniques to automatically build networks that meet hard latency constraints of end-to-end traffic streams without requiring specialized hardware for the network components. The hard latency constraints will be met by carefully designing the NoC topology and selecting the appropriate routes for flow using lean best-effort network components

## 3.3 Main Funding

### Linköping University:

- Swedish Foundation for Strategic Research (SSF)  
Project name: "Fault-Tolerant and Secure Automotive Embedded Systems."
- Swedish research Council  
Project name: "Predictability and Timeliness of Multiprocessor Applications in the Presence of Faults."

### TU Braunschweig

- **COMPOSE Project**  
Future computer architectures are likely to have tens to hundreds of processor cores, running different application classes in parallel. This project investigates techniques to combine their heterogeneous requirements and make such architectures predictable. Examples are partitioning of on-chip memories, quality of service for the network-on-chip, and mechanisms for flexible yet efficient data transfers.  
<http://www.ida.ing.tu-bs.de/en/research/projects/compose/>
- **Autonomous Integrated Systems (AIS) Project**  
Within the German research project "Autonomous Integrated Systems" (AIS) new design methodologies are explored to tackle the challenges resulting from unreliable components. The project is funded half by the German "Federal Ministry of Education and Research" and half by an industry consortium arranged within the "edaCentrum".  
<http://www.edacentrum.de/ais>
- **Toyota-ITC**  
In 2008 a research cooperation between TU Braunschweig, Toyota Information Technology Center (T-ITC), and Symtvision GmbH has been initiated, investigating the effects of errors on reliability and safety of real-time networks. A follow-up project has been started in 2009.

**UNIBO**

- **ICT-Project PREDATOR**
- **ICT-Project Scalopes** (funded by ARTEMIS JU. Period 2009-2011)
- **Industrial funding on Sensor Networks from Telecom Italia spa**

**DTU**

- **DaNES** (Danish Network for Embedded Systems, funded by the Danish Advanced Technology Foundation), Denmark. Period 2007-2010.
- **MoDES** (project on Model Driven Development of Intelligent Embedded Systems funded by the Danish Strategic Research Council), Denmark. Period 2006-2009.
- **ProCell** (project on programmable cell chip: culturing and manipulation of living cells with real-time reaction monitoring funded by the Danish Strategic Research Council),
- **SYSMODEL** ( System-Level Modeling for SMEs) funded by ARTEMIS JU. Period 2009-2011.

**CEA LIST**

- **MC2H (ManyCore for Computing and Healing).** French R&D cooperation program (Nano 2012)
- **SCALOPES (SCAlable LOw Power Embedded platformS).** ARTEMIS project

**EPFL**

- **PROD3D Programming for Future 3D Architecture with Many Cores**

*-- Changes wrt Y1 deliverable --*

*SCALOPES and SYSMODEL are ARTEMIS JU projects and new outside funding sources.*

## **4. Internal Reviewers for this Deliverable**

- **Prof. Giovanni De Micheli** (EPFL)
- **Reinhard Wilhelm** (Saarland University)