IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Activity Progress Report for Year 2

Platform and MPSoC Analysis

Cluster:

Hardware Platforms and MPSoC

Activity Leader:

Prof. Jan Madsen (DTU)

http://www.imm.dtu.dk/

Policy Objective (abstract)

The main objective of the activity is to build a common research environment, which integrates performance analysis algorithms and tools for hardware platforms and Multi-Processor System-on-Chip (MPSoC). The main challenge is the introduction of new aspects such as robustness, adaptivity and power consumption, which need to be addressed at run-time. The teams involved in the activity aim at developing and integrating modeling and analysis techniques for scalable performance analysis of applications executing on embedded hardware platforms.

Versions

number	comment	date
1.0	First version delivered to the reviewers	December 18th 2009

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1. Overview of the Activity

1.1 ArtistDesign participants and their role within the Activity

Activity leader: Prof. Jan Madsen – Technical University of Denmark, DTU (Denmark)

System-level modeling and analysis of MPSoC and networked embedded systems. Architectures and programming models for multi-core embedded systems. Analysis and Optimization of real-time and fault-tolerant applications implemented on distributed Platforms and MPSoC. Reconfigurable platforms and run-time resource management.

Team leader: Prof. Petru Eles – Linköping University, LiU (Sweden)

(i) Timing Analysis.
(ii) Analysis and Optimization of real-time and fault-tolerant applications implemented on distributed Platforms and MPSoC.
(iii) Analysis and Optimization of energy efficient, time constrained embedded systems.

Team leader: Prof. Lothar Thiele – TIK, ETH Zürich, ETHZ (Switzerland)

Developing a calculus to describe the performance of communication-centric systems, unifying the models for computation, combining tools for component-based performance analysis of MPSoC. Our role in this activity will be on component-based analytic methods to analyze the performance properties and memory requirements of distributed embedded systems.

Team leader: Prof. Rolf Ernst – TU Braunschweig, TUBS (Germany)

TU Braunsciweg contributes formal performance analysis methods for MpSoCs, with a focus on the timing implications of inter-task synchronization.

Team leader: Dr. Stylianos Mamagkakis – IMEC vzw. (Belgium)

This team will introduce novel design-time and run-time resource management optimizations for MPSoC platforms.

Team leader: Prof. Luca Benini – University of Bologna, UNIBO (Italy)

(i) Development of power modeling and estimation framework for systems-on-chip.
(ii) Development of optimal allocation and scheduling techniques for energy-efficient mapping of multi-task applications onto multi-processor systems-on-chips.
(iii) Development of energy-scavenging techniques for ultra-low power sensor network platforms.

Professor, Prof. Axel Jantsch and Hannu Tenhunen, Royal Institute of Technolgy, KTH (Sweden)

The contribution form KTH focuses on various design aspects, architectures, run-time reconfigurability and adaptivity.

Team Leader : Dr. Raphaël David – CEA LIST (France)

(i) Development of exploration framework for multi- and many-core architectures
(ii) Development of advance strategies for the deployment and the management of multi-task applications onto multi- and many-core devices
(iii) Design of multi-core architectures for dynamic multi-task applications

-- Changes wrt Y1 deliverable --

Professor Axel Jantch (KTH) and Dr. Raphaël David (CEA LIST) have been added.

1.2 Affiliated participants and their role within the Activity

Dr. Daniel Karlsson, Volvo Technology Corporation
Architecture and Design of Automotive Embedded Systems

Dr. Kai Richter – Symtavision (Germany)
Symtavision contributes industrial methodologies.

Dr. Arne Hamann – Robert Bosch GmbH (Germany)
Contributes on important embedded systems related research problems in the automotive industry.

Prof. Dimitrios Soudris – Democritus Uni. of Thrace, DUTH (Greece)
This team will introduce novel dynamic data type and data allocation optimizations for MPSoC platforms.

Prof. David Atienza – Uni. Complutense de Madrid, UCM (Spain)
This team will introduce novel run-time memory management optimizations for MPSoC platforms.

Prof. Per Gunnar Kjeldsberg - Norges Teknisk-Naturvitenskapelige Uni., NTNU (Norway)
This team will introduce novel task migration methodologies for MPSoC platforms utilizing hardware accelerators.

Bjørn Sand Jensen – Bang & Olufsen ICEpower (Denmark)
Areas of his team's expertise: chip design for audio signal processing

CTO Rune Domsteen – Prevas (Denmark)
Areas of his team's expertise: platform design for embedded systems

Dr. Patrick Schaumont – Virginia Tech (USA)
Design methods and architectures for secure embedded systems. Hardware/software codesign tool.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.3 Starting Date, and Expected Ending Date

Starting date: January 2008.

Ending date: Modeling and analysis is a long term effort and is expected to continue after the end of the project due to the lasting integration achieved by the NoE.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.4 Policy Objective

With growing maturity of scalable performance analysis algorithms and tools, new aspects such as the platform robustness can be included in analysis. Robustness to changes is particularly important for systems on chip since the cost of a redesign is high. At the same time robustness to faults is becoming a concern with shrinking feature sizes. In most practical cases, power consumption must be considered. There is currently no team in Europe that addresses all aspects. So integration of methods and tools will be needed to be able to (1) define meaningful robustness metrics that reflect design tradeoffs (2) assess the robustness of a design based on such metrics. This integration will extend the world leading position of Europe in the field of scalable formal performance analysis to hardware platform and MPSoC design.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.5 Background

The activity will be based on the complementary expertise of the participating partners in terms of Hardware Platform and MPSoC Analysis. In particular, the following areas are covered: Power modeling and analysis, power robustness assessment (University Bologna), platform performance modeling (University Braunschweig), analytical methods for reliability, performance and adaptability analysis of execution platforms (University of Denmark), reliability modeling, analysis and optimization (University Linköping), interfaces that communicate at run-time, aspects that are relevant for the efficiency of the run-time mapping components (IMEC, Belgium), simulation techniques and tools for NoC performance estimation and validation, interconnect and communication centric performance estimation techniques (KTH Sweden).

In addition, there have been already joint work and publications by some of the members of this activity, which will be used as a valuable starting point.

In more details, the above mentioned group has been working intensively on Power Modeling for SoC Platforms. In particular, they developed a virtual platform for power modeling of complex multi-core systems on chip. This platform can facilitate further integration among partners and associates, thanks to is flexibility and generality. In terms of “scheduling based energy optimization for energy-scavenging wireless sensor networks”, a novel scheduling strategy (called lazy scheduling) that is well suited to energy-harvesting systems operating under real-time constraints has been developed by ETHZ and University Bologna. It is the first result of this kind in this quickly growing research area and received a lot of attention in the scientific community.

At ETHZ, an open tool set is available that allows the performance analysis of distributed embedded systems and MPSoC. It is based on the concept of Modular Performance Analysis (MPA). In addition, there are first results available that connect this system to the MPARM simulation framework from University Bologna and the Symta/S analysis system from University Braunschweig/Symtavision.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.6 Technical Description: Joint Research

The major focus of the activity on Platform Analysis is to establish a set of models and analysis methods that (a) scales to massively parallel and heterogeneous multiprocessor architectures, (b) is applicable to distributed embedded systems as well, (b) allows for the analysis of global predictability and efficiency system properties and (c) takes the available hardware resources and the corresponding sharing strategies into account. Promising approaches are based on composable frameworks and treating resources as first class citizens in the analysis. Both, simulation-based and analytic methods will be combined. In addition, methods that focus on worst-case/best-case results as well as those based on stochastic models will be combined.

As a central ingredient of any analysis model, synchronization & communication abstractions are required for successfully deploying MPSoC hardware in embedded application domains. Efficiency is inherently related to both power and performance; hence it is an energy metric. In embedded systems, abstractions are acceptable only if they do not compromise efficiency. It also extremely important to take into account variabilities of both hardware fabrics and application workloads, which are deemed to rapidly increase. In particular, the above abstractions need to be embedded into a framework that allows to analyze the performance properties and memory requirements of distributed systems. In particular, we will focus on methods that satisfy composability properties and to lift the component-based methods as known from software design to interfaces that talk about resource interaction. In addition, we are interested in adding run-time adaptivity to systems while using efficient run-time estimation methods combined with distributed finite horizon control methods. Again, the focus is on predictability AND efficiency. Here, we will use the expertise that is available at ETH Zurich (Lothar Thiele) and University Bologna (Luca Benini), Hannu Tenhunen (KTH), Stylianos Mamagkakis (IMEC), Jan Madsen (DTU), TU Braunschweig (Rolf Ernst) are involved in this activity.

Another major challenge is to provide analysis tools and techniques to support the transitions between different abstraction levels in the design flow. Constraints should be communicated at design-time from one step to the next, taking into account the global effect that they will introduce in the system. Also, in order to ensure adaptivity of the system an interface should communicate at run-time the changes in the resource requests and the changes in the actual resource availability.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.7 Work achieved in Year 1

A number of problems were tackled in Year 1, through several cooperations involving two or more partners. In the following paragraphs, we briefly summarize the problems tackled and the partners involved.

The Linköping group has addressed two major issues: *Timing analysis of distributed real-time systems*. In this context, the emphasis was on heterogeneous systems using various task scheduling policies and heterogeneous communication protocols with static and dynamic phases. Both formal and simulation based approaches were developed. *Analysis of fault tolerant real time systems considering various reliability requirements and fault tolerance mechanisms has been done*. In particular, the issue of transient faults has been considered.

The basic effort was toward development of adequate scheduling algorithms. This work has been performed in cooperation with the DTU group.

As a central ingredient of any analysis model, synchronization & communication abstractions are required for successfully deploying MPSoC hardware in embedded application domains. Efficiency is inherently related to both power and performance; hence it is an energy metric. In embedded systems, abstractions are acceptable only if they do not compromise efficiency. It is also extremely important to take into account variability of both hardware fabrics and application workloads, which are deemed to rapidly increase. In particular, the above abstractions need to be embedded into a framework that allows to analyze the performance properties and memory requirements of distributed systems. In particular, ETHZ had its focus on methods that satisfy composability properties and to lift the component-based methods as known from software design to interfaces that talk about resource interaction. In the past year, ETHZ followed the following research directions: Together with University Bologna, ETHZ worked on combining the MPARM simulation framework with the performance analysis framework MPA (modular performance analysis). In particular, we attempted to set up the simulation environment in a way, that it follows the semantics of the analytic models and a comparison is possible. Together with University Braunschweig, ETHZ worked on the combination of the Symta/S symbolic analysis tool with the MPA (modular performance analysis framework). In particular, a tool coupling has been established that allows a seamless integration of both analysis methodologies. In addition, both research groups worked on a proper modeling of hierarchical event stream concepts.

To provide a formal performance analysis that captures the timing implications of multiprocessor systems on chip, the applicability of concepts from the analysis distributed systems is limited. A major difference lies in the use of common resources, either physically, such as a shared coprocessor or memory, or logically, such as a semaphore or a shared data structure in the memory. In ARTIST2 already first steps were taken towards addressing implications of a shared memory, which need to be extended in order to achieve the goals of this activity. We have taken steps towards generalization of the concepts from shared memory modeling to cover arbitrary shared resources. The approach chosen promises a higher accuracy than traditional approaches, due to more sophisticated modeling of shared resource load, and a better composability of designs, as the analysis of the shared resource delay is decoupled from the response time analysis of the requesting tasks.

The main problem tackled by IMEC and its affiliated partners (ie, DUTH, NTNU and UCM) was the definition of a specific software metadata format, which can be linked to each embedded software application or downloadable software service. This software metadata information can be used to configure and self-adapt the run time resource management software for dynamic data transfer and storage on MPSoC platforms. Additionally, IMEC has developed profiling and analysis tools that extract and post-process these software metadata, in order to be used for both memory hierarcy assignment (ie, MH tool) and source code parallelization tools (ie, MPA tool).

University of Bologna has addressed, in cooperation with DTU, the issue of prolonging the system life-time. Even though systems that harvest energy from the environment are adopted, such an environmental energy is not distributed uniformly and there is a lot of parameters that influence the efficiency and the schedulability of tasks. In particular we tackled the problem of routing messages in a sensor network with energy awareness and real-time responsiveness together with scheduling policies, which guarantee to execute tasks under unpredictable profile of the harvested energy.

-- No changes wrt Y1 deliverable --

This section was already presented in the Y1 deliverable, in sections 1.7 and 3.1.

1.8 Problem Tackled in Year 2

Many of the problems tackled in Year 2 are continuations of the problems and cooperations initiated in Year 1.

Linköping and DTU have continued their work regarding analysis and optimization of distributed embedded real-time systems, with application in automotive electronics. The issue of average response time (as a complement to the previous work, regarding worst case response times) of FlexRay-based distributed systems has been addressed.

At Linköping, in cooperation with Lund, analysis and optimisation techniques for control–scheduling co-design have been developed. It integrates a controller design with both static and priority-based scheduling of the tasks and messages, and in which the overall control performance is optimized. The technique has also been extended to cover the case of multimode control systems.

As a main result during the second year, the groups at Linköping and DTU have developed an analysis approach that determines the system failure probability, based on the number of re-executions introduced in software and the process failure probability of the computation node with a given hardening level. Based on this analysis, an optimisation technique has been proposed in which hardware and software fault tolerance techniques are combined.

TU Braunschweig and GM Labs have collaborated in the COMBEST project on the definition of methods and tools for the timing analysis of automotive systems based on a mix of complex communication protocols/software scheduling techniques. Within this area, ETHERNET (and its different implementations, e.g., AFDX and TT-ETHERNET) was of special interest, because increasing bandwidth, low latency/jitter, and time determinism requirements make an Ethernet based solution for in-vehicle networking attractive. In this scope, the partners examined the application of methods and tools to possible future use cases from the automotive domain. To examine the accuracy of the conservative performance bounds obtained by the formal worst case analysis, a comparison between results of formal analysis and results obtained by simulation was performed. A joint publication containing the results of the comparison has been submitted for publication.

UNIBO and Linköping have tested Basic Scheduling Alternative (BSA) in a Multi-Processor System-on-Chip shared bus. A RTL-level cycle accurate TDMA bus arbiter model has been developed and plugged in MPARM simulator. Many exhaustive sets of experiments have been done in order to validate the BSA framework and during each step of the exploration, a hardware synthesis has been performed to keep under control the underlying logic complexity.

DTU has continued the work on analytical performance models. In particular, the formalisation of the ARTS model has been extended to capture more aspects of both the application and the platform. Another important issue to be addressed is the scalability of the model such that larger and more complex systems can be modelled.

During the annual Meeting of the ArtistDesign Cluster on Hardware Platforms and MpSoC in Braunschweig, the partners of this activity have identified common goals and similarities in their approaches to address shared resources in multiprocessor systems. Shared resources generally complicate the timing verification, because they introduce timing inter-dependencies between the tasks on different cores. To address this challenge, Linköping University, ETH Zürich, TU Braunschweig are working on formal approaches to increase the predictability of

such systems: Linköping Universitys focus is finding static bus schedules that minimize the overhead from a worst-case perspective. At the ETH Zürich, work is being done on finding the worst-case timing interference within assigned time-slots. The TU Braunschweig is working on an approach that allows to bound the interference in the absence of static schedules.

In the collaboration between ETHZ and University of Bologna, further investigation of energy harvesting systems was performed. In particular, this concerned both hardware and software asptects of sensor nodes which are powered solar energy. The main goal was to merge the different approaches and illuminate several application scenarios that are of practical relevance.

Concerning the integration of SymTA/S and MPA as well as unifying approaches for hierarchical scheduling, hierarchical event streams have been in the focus of research in the second year. The major issue here is to also allow an extraction of single event streams from previously merged and transformed event streams. The transformation is hereby due to the fact that incoming streams can be combined via OR-operation and may pass different system components, which may buffer these streams due to scheduling policies.

CEA LIST has been involved in a new cooperation with university of Bologna for the definition of a Software Runtime Architecture for the management of many-cores components. CEA LIST has proposed with University of Bologna a framework supporting the development of various services, ranging from dynamic application deployment, task scheduling, resources allocation to fault and power management.

IMEC focused its research closer to the hardware platform and more specifically regarding variability and reliability issues arising from the usage of sub 45nm technology nodes. To this end Variability Aware Modeling focused on analysis of SRAM designs and the Knobs and Monitors framework extensions focused on RTL2RTL transformations for latency monitors.

Finally, KTH and DTU have started an collaboration within the SYSMODEL project on the development of a multi-MoC modeling framework for heterogeneous systems integrated with performance analysis and design space exploration tools.

-- The above is new material, not present in the Y1 deliverable --

2. Summary of Activity Progress in Year 2

2.1 Technical Achievements

Simulation-based and analytical methods for performance estimation of distributed real-time systems for control applications (Linköping, DTU, Lund)

University of Linköping and DTU have continued their work regarding analysis and optimization of distributed embedded real-time systems, with application in automotive electronics. During the second year we have concentrated on two issues: (1) analysis and optimisation of FlexRay based distributed embedded systems and (2) quality of control issues in distributed control systems (in cooperation also with Lund).

In the most recent research regarding FlexRay based distributed embedded systems we have studied the issue of average response time (as a complement to our previous work, regarding worst case response times). We have also proposed an approach to optimization of average response times by assigning priorities and frame identifiers to tasks and messages.

Many embedded control systems comprise several control loops that are closed over a network of computation nodes. In such systems, complex timing behaviour and communication lead to delay and jitter, which both degrade the performance of each control loop and must be considered during the controller synthesis. Also, the control performance should be taken into account during system scheduling. We have developed analysis and optimisation techniques for control–scheduling co-design, that integrate controller design with both static and priority-based scheduling of the tasks and messages, and in which the overall control performance is optimized. Moreover, at runtime, an embedded control system can switch between alternative functional modes. In each mode, the system operates by using a schedule and controllers that exploit the available computation and communication resources to optimize the control performance in the running mode. The number of modes is usually exponential in the number of control loops, which means that all controllers and schedules cannot be produced in affordable design-time and stored in memory. We have developed techniques for trading control quality with optimization time, and for efficiently selecting the schedules and controllers to be synthesized and stored in memory. This work has been done in cooperation with Lund.

Modeling and analysis of fault tolerant distributed embedded systems (Linköping, DTU)

As part of the collaboration between Linköping University and DTU and as a continuation of the work in the previous years, an approach to the analysis and scheduling of safety critical, fault tolerant embedded applications has been developed.

As a main result during the second year, we have developed an analysis approach that determines the system failure probability, based on the number of re-executions introduced in software and the process failure probability of the computation node with a given hardening level. This allows us to evaluate if the system meets its reliability goals with a given reliability of hardware components and a given number of re-executions in software.

Based on the above analysis, an optimisation technique has been proposed in which hardware and software fault tolerance techniques are combined (for the optimisation aspects see “Platform and MPSoC Design” activity report). The basic trade-off is between processor hardening in hardware and process re-execution in software which, together, have to provide the required levels of fault tolerance against transient faults with the lowest-possible system costs.

DTU has also addressed the issue of permanent faults in a distributed architecture. Thus, when a processor fails permanently, the tasks executing on that processor are migrated to the

remaining healthy processors. They have proposed a greedy heuristic that runs online and can determine at runtime what a mapping and processor bandwidth allocation such that the performance degrades gracefully.

Integration of SymTA/S – MPA and unifying approaches for hierarchical scheduling (ETHZ, TUBS)

The existing methods for analyzing heterogeneous distributed embedded systems have been extended such that different types of data streams can be composed to a higher level event stream with multiple hierarchies. The method is based on a novel characterization of structured event streams, i.e., event streams for which the individual events belong to a finite number of classes. The new methods can be embedded into well known compositional frameworks for performance analysis such as Symta/S and MPA (Modular Performance Analysis). Two different approaches which take advantage of event stream structures are proposed and compared. Realistic examples are given that are used to apply these new models and methods to performance analysis. The new methods have been implemented in the respective tools and applied to realistic case studies. To this end, an improved tool coupling between MPA and Symta/S has been developed jointly.

Hardware and Software Optimization of Energy Harvesting Sensor Nodes (ETHZ, UNIBO)

In the ongoing collaboration between ETHZ and University of Bologna, significant progress has been achieved, both on the hardware and the software of sensor nodes which are powered by environmental energy sources.

Concerning the hardware side, we have carefully analysed and improved our previous prototype. Particular care has been taken to analyse the efficiency of the used storage devices (supercapacitors). Furthermore, the performance of the circuit has been analysed by means of simulation and extensive testing under various charging and discharging conditions. Much attention has been given to identify the power losses of the different circuit components. Results show that the system can achieve low power consumption with an increased efficiency and cheap implementation. The respective work has been accepted for publication in IEEE Transactions on Circuits and Systems I: Design of a Solar Harvesting Circuit for Battery-less Embedded Systems.

Concerning the software, we extended our previous work to a general power management framework for energy harvesting systems. The respective work has been accepted for publication in IEEE Transactions on Computers: Adaptive Power Management for Environmentally Powered Systems. In the latter work, a set of tools and methods for power management in energy harvesting embedded systems is presented. The basic idea is to use simple model predictive controllers to adapt the application rate on sensor nodes. Concretely, results of the well-established field of multiparametric programming are applied to the emerging area of energy harvesting systems. The relevance of the work is highlighted by showing implementations and measurements of the proposed methods on real sensor nodes

Modeling of Shared Resources in Multiprocessor Systems (TUBS, Symtavision)

Based on the results of year 1, which has produced a basic analysis methodology to capture the timing implications of multiprocessor systems with shared resources that are arbitrated with the M-PCP (multiprocessor prioriyy ceiling protocol), the work was extended and applied in several new directions: In [SNE09] the work by TU Braunschweig has been complemented by embedding the analysis into larger scale embedded systems, in which a multicore component may only be a subsystem. In [SRN+09] the ideas by TU Braunschweig, and the industrial expertise by Symtavision were applied to the particular problems in the automotive domain, highlighting challenges considering the formal analysis and model building with respect to the

AUTOSAR standard. Furthermore, we have continued the effort to model both kinds of shared resource conflicts with the same methods. A common approach to derive the shared resource load (triggered either through semaphore locks or by memory accesses) in multicore systems will be presented in [SNE10].

TDMA arbitration policy on AMBA AHB protocol for MPSoC's system bus (UNIBO, Linköping)

Basic Scheduling Alternative (BSA) is a scheduling algorithm for TDMA Slot assignment in a Multi-Processor System-on-Chip shared bus. This algorithm had never been tested on a real MPSoC simulator. The main task was to develop a RTL-level cycle accurate TDMA bus arbiter model and plug it in MPARM simulator. The bus protocol chosen was AMBA AHB by ARM, which represent a modern high-performance bus and it is commonly used by embedded system suppliers. After developing the TDMA arbiter module, many exhaustive sets of experiments have been done in order to validate the BSA framework. A first set of experiments has demonstrated that the TDMA tables were too big and complicated to be efficiently handled by a real hardware module. New and improved algorithms were designed in order to shrink and simplify the table size and structure. During each step of the exploration, a hardware synthesis has been performed to keep under control the underlying logics complexity.

Energy Harvesting Aware Routing with Scheduling optimization (DTU, UNIBO)

DTU and UNIBO has continued their collaboration on a simulation framework for wireless sensor networks with focus on energy efficient execution of tasks and datatransfer when powered by energy harvesters. The energy harvesting aware routing protol developed at DTU and the energy harvesting aware task scheduler developed by UNIBO and ETHZ, have been integrated into the simulation framework. A large set of simulations have been conducted, showing the feasibility of the combined approach, i.e. being able to prolong the life-time of sensor nodes. UNIBO and DTU are currently writing a joint paper on the results.

Modeling and Verification of Embedded Systems (DTU, AAU)

DTU has continued the work on analytical performance models. In particular, the formalisation of the ARTS model has be extended to capture more aspects of both the application and the platform. Another important issue to be addressed is the scalability of the model such that larger and more complex systems can be modelled.

The MoVES framework for analysis of embedded systems, developed by DTU, is now available online. The framework includes a specification language, a model generator and a trace interpreter. The framework provides schedulability analysis of embedded systems and can guide in systems design through traces that lead to missed deadlines.

Formal verification of design properties of hardware architectures (DTU, Virginia Tech)

DTU has extended its collaboration with Virginia Tech to support model based design and analysis of hardware platforms and MPSoC. Studies and experiments on quantitative properties of hardware specifications based on the Gezel language. These experiments serve as an inspiration and guidance for establishment of a refinement framework for hardware models. DTU has started to investigate how this platform level modeling can be linked with the system-level models. Further, initial studies towards using the model for education in Embedded Systems Design has be conducted.

Analysis tools for embedded systems (DTU, Oldenburg)

The goal is to establish efficient methods for verification of resource constraints, where one activity will focus on the real-time logic durations calculus. The aim of DTU is to develop a prototype model-checking tool and experiment with verifying strong timing constraints. A fist prototype model checker has developed during the second year. The theory for model checking Duration Calculus formulas abased on approximations has been strengthened.

Contract Based Architecture Dimensioning (KTH, NUDT (Changsha, China))

KTH, together with partners from NXP, ARM and ST, has developed extensions to (the use of) IP communication interfaces that enable the correct integration of IP modules so that performance requirements are met and the required Quality of Service (QoS) is obtained. The extensions to the interfaces enable a SoC integrator to explicitly define the services that need to be provided by a communication infrastructure to an IP module so that it can provide the desired QoS. Specifically we have introduced the notion of QoS contract to specify the services required for correct operation of an IP. We have defined different types of QoS contracts for Device-Level Interfaces (like AMBA-AXI) and we have studied how they can be configured and how monitoring and traffic regulation can be included [LMJ2009]. We have implemented a traffic regulator and studied its cost and performance [LBJ2009].

Based on Network Calculus we have developed an analysis method for worst case delay bounds in NoC based MPSoCs [QLD2009b], [QLD2009c], [QLD2009d], [QLD2009e] and for 3D topologies [QLD2009a], [QLD2009f].

Based on the theory of a regulation spectrum [LMJ2009] we have developed an optimization methodology to determine traffic contract parameters for minimizing buffers while meeting delay and bandwidth constraints [under submission].

Integration of the communication architecture with the memory architecture (KTH, IMEC, NTUA, NUDT (Changsha, China))

Efficient MPSoC platforms have to efficiently integrate the communication infrastructure with the memory architecture [LJ2009] and they have to provide proper memory abstractions to application designers and programmers. The required memory abstractions should offer an intuitive memory consistency model and it has to be efficiently implemented. Moreover, it should offer an intuition of the delay of different memory accesses since that will differ significantly depending on the physical location of the addressed memory.

KTH, together with partners from NTUA in Greece, Thales Communciation, IMEC, VTT in Finland, Inracom in Greece and NUDT in Changsha, China, started developing a MPSoC platform in the context of the MOSART project, which integrates memory services into the communication infrastructure [CLJC2009] with the aim of providing an appropriate memory abstraction to programmers. Furthermore, the MPSoC platform shall support cache coherency [ZLJ+2009], a release consistency memory model and basic support for dynamically allocated abstract data types such as lists, arrays and container classes.

Analytic Real-Time Analysis and Timed Automata (ETHZ, UPPSALA)

In this activity, a strict compositional and hybrid approach for obtaining key (performance) metrics of embedded systems has been developed. At its core the developed methodology abstracts system components by either flow-oriented and purely analytic descriptions or by state-based models in the form of timed automata. The interactions among the heterogeneous components are modeled by streams of discrete activity- triggers. In total this yields a hybrid framework for the compositional analysis of embedded systems. It supplements contemporary techniques for the following reasons: (a) state space explosion as intrinsic to formal verification

is limited to the level of isolated components; (b) computed performance metrics such as buffer sizes, delays and utilization rates are not overly pessimistic, because coarse-grained purely analytic models are used for components only which conform to the stateless model of computation. For demonstrating the usefulness of the presented ideas, we implemented a corresponding tool-chain and investigated the performance of a two-staged computing system, where one stage exhibits state-dependent behavior only coarsely coverable by a purely analytic and stateless component abstraction. The work has been based on discussions with the university of UPPSALA, in particular with respect to the symbolic model checker UPPAAL that has been used. As a result, a close coupling of UPPAAL (timed automata) and the MPA toolbox (analytic real-time analysis) has been achieved.

Runtime layer design for many-cores architectures (CEA LIST, Bologna)

CEA LIST has worked with the university of Bologna on the definition of a scalable framework for the integration of various runtime services. The objective is to propose efficient support for dynamic applications whose behaviour cannot be fully analyzed at compile-time. This Runtime software will include a wide range of services, ranging from low-level hardware drivers to high level strategies to optimize the usage of the fabric resources. These features fall in three categories: deployment, execution, and quality of service.

- The deployment category gathers all software needed prior to application execution. It includes software to load application code (statically or dynamically), to reserve computing and storage resources …
- The execution category is related to application support during execution. It includes a set of low level API to control the different part of the fabric as well as an additional level of programming models support (scheduling, memory and communication allocation).
- The QoS category relates to software runtime that may monitor the platform and performance sensors to provide the software runtime with needed information to drive fault-tolerance and power management strategies.

More specifically, CEA LIST has implemented flexible, i.e. usable independently from the programming model, runtime services for task, memory and synchronization management of a symmetric multi-core devices.

New bus model for MPSoC's system bus analysis and optimization (UNIBO)

We carried out extensive design space explorations analyzing how different architectural parameters can influence overall system behavior in terms of performance, modularity and predictability. More in detail, we compared several communication bus protocol arbitration algorithms and memory configurations, under different traffic patterns generated by real-time applications. Our analysis shows how bus arbitration policy has a great impact non only on performance but also on predictability and modularity. Adopting TDMA-based policies we implicitly give guarantees of predictability and modularity. On the contrary, traditional protocols such as Round Robin cannot give these guarantees and that is why their performance deteriorated with high traffic loads. In a bus system where concurrency is handled via a pure TDMA policy:

1. Predictability is guaranteed because no other master will be allowed to access the bus at the same time of the allowed one. Moreover, we can bind the maximum bus access time as a function of slot dimension and configuration and number of masters in the entire system.
2. Modularity property is guaranteed since adding a new master in the system has the only impact on performance due to the insertion of a new Time Slot in the TDMA wheel.

3. Performance and scalability are however still unbounded, since they are function of time slot dimensioning.

Variability Aware Modeling - VAM (IMEC)

Imec worked in the Variability Aware Modeing framework, which is a general modeling framework to propagate variability information from the technology to the SoC level including a holistic treatment of energy and timing. This enables designers to predict the parametric yield of their chip early in the design cycle.
http://www.imec.be/tad/

Knobs and monitors for energy efficiency and reliability (IMEC)

Imec continued research in knobs and monitors, and the complementary control algorithms framework. They consist of a large, generic class of run-time countermeasures that tackle both variability and reliability (degradation) mechanisms. The general concept is to `monitor' at fine granularity sub circuit performance, and tune the system by `knobs' at run-time to fully exploit actual/typical case. Our 'knobs and monitors' approach aims to develop performance-configurable components; run-time performance monitoring (such as delay/energy) measurement incl. test pattern generation infrastructure; and generic, holistic, system-level control algorithms.

http://www.imec.be/tad/

Modeling and Analysis of Adaptive Systems (KTH, Offis)

Adaptivity is a common concept used in embedded system and custom hardware design for many years. Reconfigurable FPGAs, embedded software, configurable datapaths and parameterisable analog components are all familiar examples of adaptivity. We use the term to denote the general, abstract concept of changing the behaviour of a system at run-time which encompasses software, configurable or parameterisable digital and analog hardware.

KTH, together with partners from OFFIS, TU Vienna, University of Cantabria, THALES and DS2, has developed concepts for modeling adaptivity in an abstract way to make relevant and interesting properties of adaptive systems explicit. The type and level of adaptivity is an important design consideration in many systems. It should be possible for the designer to systematically explore the design space with adaptivity being one more design parameter just like performance, cost and power consumption. In order to provide a sound basis that captures adaptivity in a broad and general sense we have introduced adaptivity as an extension to a formal modeling framework. This allows us to formally and systematically study adaptivity and its interesting properties. It establishes a clean and consistent conceptual basis for development of design analysis and exploration methods and tools.

Together with its partners, KTH has developed general concepts for formally modeling adaptive objects and applied them to dynamically reconfigurable systems. Based on these concepts, a performance analysis method and accompanying tools for reconfigurable systems [SZJ+2009] has been developed. Moreover, we have developed a method to minimize buffer space for streaming applications on MPSoC platforms while meeting all real-time constraints [ZSJ2009].

-- The above is new material, not present in the Y1 deliverable --

2.2 Individual Publications Resulting from these Achievements

Linköping

1. [SYPE+09] S. Samii, Y. Yin, Z. Peng, P. Eles, Y. Zhang, ”Immune Genetic Algorithms for Optimization of Task Priorities and FlexRay Frame Identifiers,” International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA), Beijing, China, August 2009, pp. 486 - 493

TU Braunschweig

2. [NSE09] Mircea Negrean and Simon Schliecker and Rolf Ernst. " Response-Time Analysis of Arbitrary Task Activations in Multiprocessor Systems with Shared Resources" In *Proc. of the Design Automation and Test in Europe (DATE)*, Nice, France, April 2009.

3. [SE09] Simon Schliecker and Rolf Ernst, **"A Recursive Approach to End-To-End Path Latency Computation in Heterogeneous Multiprocessor Systems,"** in *Proc. 7th International Conference on Hardware Software Codesign and System Synthesis (CODES-ISSS)*, Grenoble, France, ACM, October 2009

4. [SNE09] Schliecker, Simon; Negrean, Mircea; Ernst, Rolf, **"Response Time Analysis in Multicore ECUs with Shared Resources,"** *IEEE Transactions on Industrial Informatics*, vol. 5, No. 4, November 2009. (to appear).

5. [SRH+09] Simon Schliecker, Jonas Rox, Rafik Henia, Razvan Racu, Arne Hamann and Rolf Ernst, **"Formal Performance Analysis for Real-Time Heterogeneous Embedded Systems,"** in *Model-Based Design of Heterogeneous Embedded Systems*, pp. (to appear), CRC Press, November 2009

6. [SNE10] Simon Schliecker, Mircea Negrean and Rolf Ernst, **"Bounding the Shared Resource Load for the Performance Analysis of Multiprocessor Systems,"** in *Proc. of Design, Automation, and Test in Europe (DATE)*, (Dresden, Germany), March 2010 (to appear)

ETHZ

7. [LPT09] Kai Lampka, Simon Perathoner, Lothar Thiele: Analytic Real-Time Analysis and Timed Automata: A Hybrid Method for Analyzing Embedded Real-Time Systems In the 8th ACM & IEEE International conference on Embedded software, EMSOFT 2009, CD edition, ACM, Grenoble, France, pages 107-116, October, 2009.

DTU

8. Aske Brekling, Michael R. Hansen, Jan Madsen, MoVES - A Framework for Modelling and Verifying Embedded Systems, The 21st International Conference on Microelectronics, Marrakech, Morocco, 2009

9. Jan Madsen, Michael R. Hansen, Aske W. Brekling, A Modelling and Analysis Framework for Embedded Systems, Model-Based Design of Heterogeneous Embedded Systems, CRC Press, 2009

10. Aske Brekling, Michael R. Hansen, Jan Madsen, Analysis of Quantitative Properties of Hardware Specifications, The 21st Nordic Workshop on Programming Theory, Technical University of Denmark, 2009

IMEC

11. Trautmann, M.; Mamagkakis, S.; Bougard, B.; Declerck, J.; Umans, E.; Dejonghe, A.; Van der Perre, L. and Catthoor, F.: Simulation framework for early phase exploration of SDR platforms: a case study of platform dimensioning. In Design, Automation and Test in Europe, DATE 2009, Nice, France, April 20-24, (2009).
12. AbdelHamid, A.; Anchlia, A.; Mamagkakis S.; Miranda Corbalan, M.; Dierickx, B.: A Standardized Knobs and Monitors RTL2RTL Insertion methodology for Fine Grain SoC Tuning. In DSD2009 12th EUROMICRO Conference on Digital System Design, Patras, Greece, (2009)
13. Miranda Corbalan, M.; Zuber, P.; Dobrovolny, P. and van der Zanden, K.: Statistical analysis for robust SRAM design. In IEEE Design for Variability and Reliability Workshop – Austin, USA, (2009)
14. Zuber, P.; Matvejev, V.; Dobrovolny, P.; Roussel, P. and Miranda Corbalan, M.: Using exponent Monte Carlo for quick statistical circuit simulation. In International Workshop on Power And Timing Modeling, Optimization and Simulation- PATMOS, Delft, Netherlands, (2009)

UNIBO

15. Luca Benini, Predictability vs. Efficiency in the Multicore Era: Fight of Titans or Happy Ever after? Lecture Notes in Computer Science p. 50, vol. 5643, 2009.
16. Bartolini, A.; Ruggiero, M.; Benini, L.;Visual quality analysis for dynamic backlight scaling in LCD systems Design, Automation & Test in Europe Conference & Exhibition, 2009. DATE '09. 20-24 April 2009 Page(s):1428 – 1433

KTH

17. [LMJ2009] Zhonghai Lu, Mikael Millberg, Axel Jantsch, Alistair Bruce, Pieter van der Wolf, and Tomas Henriksson. Flow regulation for on-chip communication. In *Proceedings of the Design Automation and Test Europe Conference (DATE)*, April 2009.
18. [LBJ2009] Zhonghai Lu, Dimitris Brachos, and Axel Jantsch. A flow regulator for on-chip communication. In *Proceedings of the System on Chip Conference*, Belfas, Northern Ireland, 2009.
19. [JL2009] Axel Jantsch and Zhonghai Lu. Resource allocation for quality of service in on-chip communication. In Fayez Gebali and Haytham Elmiligi, editors, *Networks on Chip: Theory and Practice*. Taylor & Francis Group LLC - CRC Press, 2009.
20. [ZSJ2009] Jun Zhu, Ingo Sander, and Axel Jantsch. Buffer minimization of real-time streaming applications scheduling on hybrid CPU/FPGA architectures. In *Proceedings of the Design and Test Europe Conference (DATE)*, April 2009.
21. [LJ2009] Zhonghai Lu and Axel Jantsch. Trends of terascale computing chips in the next ten years. In *Proceedings of IEEE ASICON 2009*, ChangSha, China, October 2009.
22. [ZLJ+2009] Yuang Zhang, Zhonghai Lu, Axel Jantsch, Li Li, and Minglun Gao. Towards hierarchical cluster based cache coherence for large-scale network-on-chip. In *Proceedings of the 4th IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era*, Cairo, Egypt, April 2009.
23. [QLD2009a] Yue Qian, Zhonghai Lu and Wenhua Dou. Comparative Analysis of Worst-Case Communication Delay Bounds for 2D and 3D NoCs. In ``Workshop on 3D

Integration and Interconnect-Centric Architectures" held in conjunction with ``International Symposium on High-Performance Computer Architecture 2009 (HPCA-15)", Raleigh, North Carolina, USA, Feb., 2009.

24. [QLD2009b] Yue Qian, Zhonghai Lu and Wenhua Dou. Analysis of Communication Delay Bounds for Network on Chips. Proceedings of 14th Asia and South Pacific Design Automation Conference (ASPDAC'09). Yokohama Japan, Jan. 2009.
25. [QLD2009c] Yue Qian, Zhonghai Lu and Wenhua Dou. Applying Network Calculus for Worst-case Delay Bound Analysis in On-chip Networks. Proceedings of the 4th IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS'09). Cairo, Egypt, April 2009.
26. [QLD2009d] Yue Qian, Zhonghai Lu, Wenhua Dou. Analysis of Worst-case Delay Bounds for Best-effort Communication in Wormhole Networks on Chip. Proceedings of the 3rd ACM/IEEE International Symposium on Networks-on-Chip (NOCS'09), San Diego, CA, May 2009.
27. [QLD2009e] Yue Qian, Zhonghai Lu and Wenhua Dou, "Applying Network Calculus for Performance Analysis of Self-Similar Traffic in On-Chip Networks", IEEE/ACM/IFIP 2009 International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS'09), Grenoble, France, Oct. 11-16, 2009.
28. [QLD2009f] Yue Qian, Zhonghai Lu and Wenhua Dou, "From 2D to 3D NoCs: A Case Study on Worst-Case Communication Performance", IEEE/ACM 2009 International Conference on Computer-Aided Design (ICCAD'09), San Jose, CA, Nov. 2-5, 2009.
29. [CLJC2009] Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen. Speedup analysis of data-parallel applications on multi-core NoCs. In *Proceedings of the IEEE International Conference on ASIC (ASICON)*, Changsha, China, October 2009

-- The above are new references, not present in the Y1 deliverable --

2.3 Interaction and Building Excellence between Partners

Simulation-based and analytical methods for performance estimation of distributed real-time systems for control applications (Linköping, DTU, Lund)

The interaction in this activity has been between Linköping, DTU and Lund.

- -Meeting/discussion at the conference “Design, Automation and Test in Europe (DATE09)”, Nice, France, April 20-24, 2009.
- Prof. Paul Pop from from DTU has visited Linköping several times during 2009.
- Prof. Anton Cervin from Lund has visited Linköping.
- Soheil Samii from Linköping has visited Lund several times during 2009.

Modeling and analysis of fault tolerant distributed embedded systems (Linköping, DTU)

The interaction in this activity has been between Linköping and DTU.

- -Meeting/discussion at the conference “Design, Automation and Test in Europe (DATE09)”, Nice, France, April 20-24, 2009.
- Paul Pop from DTU has visited Linköping several times during 2009.

TDMA arbitration policy on AMBA AHB protocol for MPSoC's system bus (UNIBO, Linköping)
The interaction in this activity has been between Linköping and UNIBO.

- Several phone meetings/discussions between UNIBO and Linköping during 2009.
- The MPARM platform from Bologna has been extensively used by Linköping. This has led to frequent interactions between the groups.

Analysis tools for embedded systems (DTU, Oldenburg)
The interaction in this activity has been between DTU and Oldenburg.

- There is ongoing joint work between Prof. Martin Fränzle, Oldenburg University, and Michael R. Hansen, from DTU, which this year has resulted in a joint journal article and two workshop contributions. Several mutual visits are expected next year.

Modeling and Verification of Embedded Systems (DTU, AAU)
The interaction in this activity has been between DTU and AAU.

- Joint work on modeling the ARTS framework using the timed automata semantics of UPPAAL and extension to handle detailed hardware aspects.
- Several visits between DTU and AAU have taken place.
- Aske Brekling from DTU has visited AAU

Formal verification of design properties of hardware architectures (DTU, Virginia Tech)
The interaction in this activity has been between DTU and Virginia Tech.

- Several phone meeting on Embedded Systems education based on the Gezel hardware description language from Virginia Tech has been conducted.

Mircea Negrean gave a presentation at the ArtistDesign Workshop Mapping Applications to MPSoCs in St. Goar, 29-30.June 2009, on the timing analysis on complex real-time automotive multicore architectures.

Runtime layer design for many-cores architectures
Interaction between CEA LIST and University of Bologna in this activity is based on face-to-face meetings in Saclay and Genoble and numerous phone meetings to clarify technical aspects regarding runtime organization and development.

KTH has been closely collaborating with Turku University in Finland with regular visits and joint workshops (Nov. 23, 2009).

KTH, NTUA and IMEC cooperate closely in developing a memory architecture for MPSoC platforms.

KTH cooperates with OFFIS and TU Vienna in developing methods for modeling, design and analysis of adaptive systems.

KTH and DTU jointly develop a multi-MoC modeling framework for heterogeneous systems integrated with performance analysis and design space exploration tools as part of the SYSMODEL project < http://www.sysmodel.eu>. Mikkel Koefoed Jacobsen, a PhD student from DTU, has visited KTH for one month in May-June 2009.

KTH and ETH start cooperation on performance analysis. Zhonghai Lu from KTH is visiting ETH from November 16, 2009, to January 20, 2010.

KTH and NUDT from Changsha, China, have a very tight cooperation on performance analysis and memory architectures.

KTH and Fudan Univerisity in Shanghai, China, have initiated a cooperation on developing MPSoC platforms for security applications.

Hardware and Software Optimization of Energy Harvesting Sensor Nodes (ETHZ, UNIBO)
The interaction in this activity has been between ETHZ and UNIBO.

- Joint work in developing new algorithms to perform application control in energy harvesting sensor networks.
- Michele Magno from UNIBO visited ETH Zurich for half a year in order to investigate possibilities of distributed application control.
- As a result, a joint paper has been published.

Integration of SymTA/S – MPA and unifying approaches for hierarchical scheduling (ETHZ, TUBS)
The interaction in this activity has been between ETHZ and TUBS.

- Joint work in developing new schemes to analyse hierarchical event streams.
- Several visits and meetings between TUBS and ETHZ have been taken place, laso in the context of the FP7 COMBEST project.
- The MPA and Symta/S tool coupling has been improved in order to include the new class of hierarchical event streams.

-- Changes wrt Y1 deliverable --

DTU and KTH have increased the level of cooperation for developing a system modeling framework, analysis and design tools as part of the SYSMODEL project.

KTH and NUDT have intensified their cooperation.

KTH has initiated cooperation with ETH and with Fudan University.

2.4 Joint Publications Resulting from these Achievements

1. V. Izosimov, I. Polian, P. Pop, P. Eles, and Z. Peng, “Analysis and Optimization of Fault-Tolerant Embedded Systems with Hardened Processors,” Design Automation and Test in Europe (DATE) Conference, Nice, 2009, pp. 682 – 687.

2. S. Samii, P. Eles, Z. Peng, A. Cervin, “Quality-Driven Synthesis of Embedded Multi-Mode Control Systems,” Design Automation Conference (DAC), San Francisco, California, USA, July 2009, pp. 864 - 869.

3. S. Samii, A. Cervin, P. Eles, Z. Peng, “Integrated Scheduling and Synthesis of Control Applications on Distributed Embedded Systems,” Design Automation and Test in Europe (DATE) Conference, Nice, 2009, pp. 57 - 62.

4. [SRN+09] Simon Schliecker, Jonas Rox, Mircea Negrean, Kai Richter, Marek Jersak and Rolf Ernst, **"System Level Performance Analysis for Real-Time Automotive Multi-Core and Network Architectures**,"*Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 28, No. 7, pp. 979-992, July 2009

5. [PWT+09] Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst and Michael González

Harbour, **"Influence of different abstractions on the performance analysis of distributed hard real-time systems,"** *Journal Design Automation for Embedded Systems (available as "online first", April 2008)*, vol. 13, No. 1, pp. 27-49, June 2009

6. Clemens Moser, Lothar Thiele, Davide Brunelli and Luca Benini: Adaptive Power Management for Environmentally Powered Systems, Accepted for publication in *IEEE Transactions on Computers*, 2009, regular papers.

7. Davide Brunelli, Clemens Moser, Lothar Thiele and Luca Benini: Design of a Solar Harvesting Circuit for Battery-less Embedded Systems Accepted for publication in *IEEE Transactions on Circuits and Systems I*, 2009, regular papers.

8. Simon Perathoner, Tobias Rein, Lothar Thiele, Kai Lampka: FIFO Scheduling and Event Count Curves for Modeling Structured Event Streams in Modular Performance Analysis TIK Report Nr. 312, ETH Zurich, October, 2009.

9. Simon Perathoner, Tobias Rein, Lothar Thiele, Kai Lampka and Jonas Rox: Modeling Structured Event Streams in System Level Performance Analysis, submitted to Conference on Languages, Compilers, and Tools for Embedded Systems LCTES, Stockholm, Sweden, April 2010.

10. Facchini, M.; Carlson, T.; Vignon, A.; Palkovic, M.; Catthoor, F.; Dehaene, W.; Benini, L. and Marchal, P.: System-level power/performance evaluation of 3D stacked DRAMs for mobile applications In Design, Automation and Test in Europe, DATE 2009, Nice, France, April 20-24, (2009).

11. Christos Baloukas, José Luis Risco-Martín, David Atienza, Christophe Poucet, Lazaros Papadopoulos, Stylianos Mamagkakis, Dimitrios Soudris, José Ignacio Hidalgo, Francky Catthoor, Juan Lanchares: Optimization methodology of dynamic data structures based on genetic algorithms for multimedia embedded systems. Journal of Systems and Software 82(4): 590-602 (2009)

12. [SZJ+2009] Ingo Sander, Jun Zhu, Axel Jantsch, Andreas Herrholzy, Philipp A. Hartmanny, and Wolfgang Nebel. High-level estimation and trade-off analysis for adaptive real-time systems. In *Proceedings of the 16th Reconfigurable Architectures Workshop*, Rome, May 2009.

13. Martin Frãnzle and Michael R. Hansen. Efficient model checking for duration calculus. International Journal of Software and Informatics, Vol.3, no.2-3, pp. 171-196, 2009

14. William~P. Heise, Martin Fränzle and Michael R. Hansen. A prototype model checker for Duration Calculus. In proceedings of the 21st Nordic Workshop on Programming Theory (NWPT'09). DTU Informatics, 2009, pages 26-29.

15. Gerald Sauter, Henning Dierks, Martin Fränzle and Michael R. Hansen. Leight-weight hybrid model checking facilitating online prediction of temporal properties. In proceedings of the 21st Nordic Workshop on Programming Theory (NWPT'09). DTU Informatics, 2009, pages 20-23.

-- The above are new references, not present in the Y1 deliverable --

2.5 Keynotes, Workshops, Tutorials

Invited talk: Predictable Implementation of Real-Time Applications on Multiprocessor Systems on Chip,

Ninth International Workshop on Worst-Case Execution Time Analysis

Dublin, Ireland - June 30, 2009.

Speaker: Petru Eles

With this occasion several results obtained in the ARTIST context have been made accessible to an international audience. They are related, in particular, to the predictability of applications running on multiprocessor systems with shared communication infrastructure. http://www.artist-embedded.org/artist/Overview,1611.html

Invited Talk : On-line Timing Analysis in Organic Computing and Self-healing Systems (Rolf Ernst)
Symtavision NewsConference 2009
Braunschweig, Germany - Oct 01, 2009

The SymTA/S NewsConference is an annual event organized by the Symtavision GmbH that brings together engineers, managers, technology experts and researchers in the field of embedded real-time systems. Rolf Ernst was invited to present current research results to this audience.
http://www.symtavision.com/newsconference2009.html

Keynote : Adaptive solutions for the emerging reliability and multicore resource management challenges (S. Mamagkakis)
2nd Workshop on Adaptive and Reconfigurable Embedded Systems - APRES 2009
Grenoble, France, October 11th, 2009 within ESWEEK 2009

In this talk, the reliability and resource management challenges of the emerging multicore platforms were discussed and the proposed adaptive solutions were evaluated. As technology scaling approaches nanoscale dimensions, we expect integration to move even further, thus increasing dramatically the number of cores on a chip and enabling the mapping of a higher number of software applications. The main challenges that arise are related with run-time resource management of shared multicore platform resources and variability and reliability issues that are linked with nanoscale technology.

http://www.artist-embedded.org/artist/Keynote.html

Invited Talk : Mapping Applications onto Multicore Platforms (Jan Madsen)
ARTIST Summer School in China
Tsinghua University, Beijing, China – July 20 - 24, 2009

The course gave an introduction to the problem of mapping applications onto multi-core platforms. The process of mapping covers the allocation of tasks to processors of the platform and the definition of their execution order, i.e. the task scheduling. The course focused on task scheduling for parallel systems. It covered basic architectures for multi-core platforms (homogeneous and heterogeneous architectures) and how to model these, as well as how to model the application as a parallel program. The course covered both basic scheduling algorithms (handling static scheduling) and more advanced algorithms, which are able to handle consequences of the, often complex, communication structures of the platform. The course covered issues of real-time systems, including real-time operating systems (handling dynamic scheduling), as well as other quantitative aspects such as power consumption and

memory usage. Finally, the course gave an introduction to how quantitative aspects of such systems may be formally modeled and analyzed.

http://www.artist-embedded.org/artist/Overview,1630.html

Keynote: Predictability vs. Efficiency in the Multicore Era: Fight of Titans or Happy Ever after?
CAV (Computer Aided Verification), Grenoble, France – July 2009
Luca Benini, DEIS Università di Bologna,

The talk gave an overview of recent trends in multi-core platforms for embedded computing. The shift toward multicore architectures has been imposed by technology reasons (power consumption and design closure issues in nanometer technology) and not by the ”coming of age” of parallel programming models, compilation, analysis and verification environments. Thus, we may be building terascale many-cores architectures that we cannot program efficiently. Even worse, we may not be able to give any guarantees on execution timing, constraints and real time properties of applications. This is a challenge AND an opportunity for the software design and verification community: The talk gave some views on what is being done, what could be done to build efficient and predictable multi-core platforms.

Keynote: Trends of terascale computing chips in the next ten years
IEEE ASICON
ChangSha, China - October 2009.

Invited talk by Zhonghai Lu, Axel Jantsch, KTH

Invited talk: MoVES - A Framework for Modeling and Verifying Embedded Systems
The 21st International Conference on Microelectronics
Marrakech, Morocco – December, 2009

The talk gave an overview of the MoVES framework. MoVES is being developed to assist in the early phases of embedded systems design. A system is modelled as an application running on an execution platform. The MoVES framework can be used to conduct schedulability analysis and has the potential to reason about different types of resource usage such as memory usage and power consumption. Through the use of a number of small examples, the capabilities of MoVES to model and analyze embedded systems were demonstrated.

Keynote Lothar Thiele (ETHZ): ` Scalable software for MPSoC platforms',

FETCH, Chexbres 2009.
The keynote presentation summarized the work done in ARTISTDesign together with partners from RWTH Aachen and TIMA Grenobles in mapping applications onto MPSoC platforms. It focussed on the integration of various tools and future challenges:
http://sites.google.com/site/fetch2009/programme.

Keynote Lothar Thiele (ETHZ): `Component-based schedulability analysis', 4th International School on Model Driven Development for Distributed Realtime Embedded Systems
Aussois, France – April 20-24, 2009.

The talk describes an environment to map applications to Multiprocessor Platforms which is based on ARTISTDesign cooperations. The corresponding platform enables the specification, simulation, performance evaluation and mapping of distributed algorithms. Major

characteristics are scalability and multi-resolution methods for validation and estimation that combine simulation-based and analytic approaches: http://www.mdd4dres.info/lectures/thiele.

Invited Talk Lothar Thiele (ETHZ): `Distributed Embedded Systems: Reconciling Computation, Communication and Resource Interaction`, Seventh International Andrei Ershov Memorial Conference «PERSPECTIVES OF SYSTEM INFORMATICS»
Akademgorodok, Russia - June 15 - 19, 2009.

Embedded systems are characterized by a close interaction between computation, communication, the associated resources and the physical environment. The solution of the above complex analysis and design problems relies on our abilities to properly deal with some of the following challenges:

Challenge 1: Designing component models whose interfaces talk about extra-functional properties like time, energy and resource interaction.

Challenge 2: Designing models of computation that talk about functional component properties and resource interaction.

Challenge 3: Developing system design methods that lead to timing-predictable and efficient embedded systems.

It will be necessary to (re)think the classical separation of concerns which removed very successfully physical aspects from the concept of computation. It will be necessary to (re)combine the computational and physical view of embedded software. The presentation covered the following aspects: Component-based performance analysis of distributed embedded systems (Modular Performance Analysis): basic principles, methods and tool support. Real-time Interfaces: from real-time components to real-time interfaces, adaptivity and constraints propagation. Application examples that show the applicability of the concepts and their use in embedded system design http://psi.nsc.ru/psi09/.

Keynote Lothar Thiele (ETHZ): `Predictability and Efficiency in Wireless Sensor Networks`, First Annual Conference, Center for Informatics and Information Technology
Braunschweig Germany - 2009

Recently, there has been lots of interest in various aspects of wireless sensor networks. They can be characterized by a potentially large number of individual nodes that perform sensor, computation and communication tasks. These small embedded systems are interconnected via wireless links. Application domains can be found in environmental monitoring, logistics, security, safety, health and building automation. Much of the research and development effort in this area has been devoted to increase the efficiency of these massively distributed embedded systems in terms of computing power, memory space, communication bandwidth and energy. On the other hand, predictability of the system functionality in terms of functionality, timing and battery lifetime has only been of secondary interest. The talk covers several novel techniques that can be used to design predictable and efficient large scale distributed embedded systems. Two application scenarios will be described where these methods have been successfully applied. Results of the ETHZ-UNIBO cooperation in ARTISTDesign have been presented. http://city.tu-bs.de/index.php/en/events/symposium-2009.

Keynote Lothar Thiele (ETHZ): 'Distributed Embedded Systems - Reconciling Computation, Communication and Resource Interaction'. 5th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2009)

August 24-26 2009.

The keynote presentation related to results obtained in ARTISTDesign in terms of designing MPSoCs with predictable timining behaviour. It relates to the cooperation with Bologna in terms of predictable communication fabrics, TDMA scheduling optimization and associated analysis methods. http://www.cs.cityu.edu.hk/rtcsa2009/

Invited Talk Lothar Thiele (ETHZ): 'Scalable Software for MPSoC Platforms' . ARTISTDesign Summer School

Autrans (near Grenoble), France - September 7-11, 2009

The presentation describes an environment to map applications onto MPSoC platforms. The corresponding platform enables the specification, simulation, performance evaluation and mapping of distributed algorithms. Major characteristics are scalability and multi-resolution methods for validation and estimation that combine simulation-based and analytic approaches. http://www.artist-embedded.org/artist/Programme,1636.html#Thiele

Invited Talk Jan Beutel (ETHZ): 'Tools for Distributed Embedded Systems'. ARTISTDesign Summer School

Autrans (near Grenoble), France - September 7-11, 2009

Although a decade has passed since prominent visions of wireless sensor networks were put forth by Estrin, Pister and others designing such systems today is more an art dominated by experience than a coordinated process yielding predictive results. In this lecture, we will review the current state-of-the-art and define what is actually hard (and new) about this (new?) class of systems. For this purpose we will learn about the PermaSense project, a sensor network deployed in an extremely hazardous environment on glaciated peaks in the Swiss Alps. The main characteristics of the design and testing strategies used in the development of the PermaSense application will be presented and discussed in the light of a holistic system design goal. We will continue to discuss recent achievements in the area of multi-contextual and automated test and validation tools developed at ETH Zurich. The talk will end with a look ahead at a proposed future system design methodology that should allow a tighter integration of virtual and real-world design spaced, which we feel is a necessity for a successful adoption of larger and more complex networked embedded systems. http://www.artist-embedded.org/artist/Programme,1636.html#Beutel

Tutorial Lothar Thiele: 'Complex Distributed Systems: Managing very complex distributed systems with real-time constraints' .COMES Autumn School on Complexity Management in Embedded Systems

Lugano, Switzerland - November 16 - 20, 2009

It becomes one of the major challenges in the design process to analyze specific characteristics of a system design, such as end-to-end delays, buffer requirements, or throughput in an early design stage, to support making important design decisions before much time is invested in detailed implementations. Because of the import role of resource interaction, these components not only need to talk about functional properties but also about resource interaction. In the presentation, we covered the following aspects of system level performance analysis of distributed embedded systems: a. Approaches to system-level performance analysis (simulation-based vs. analytic methods, review of existing methods and tools).Requirements in terms of accuracy, scalability, composability and modularity. b. Modular Performance Analysis (MPA): basic principles, methods and tool support. c. Examples that show the applicability, the embedding into design space exploration, and a comparison to simulation-based approaches. The tutorial covered joined results with TU Braunschweig on Performance Analysis and University Bologna on MPSOC Design. http://www.alari.ch/comes/

Workshop : ESTIMedia 2009

Workshop on Embedded Systems for Real-Time Multimedia,

Grenoble, France - October 15-16, 2009

The aim of this workshop was to bring together people from different multimedia-related research communities (e.g, software, architectures, real-time systems, DSP, compilers, multimedia applications) who have worked separately, but did not interact sufficiently to address the challenges facing the design of hardware and software for multimedia systems. http://www.science.uva.nl/events/ESTIMedia09/

Workshop : ArtistDesign WP6 Cluster Meeting on Hardware Platforms and MpSoC
Braunschweig, Germany – June 25/26 2009

The main objective of this meeting was a mutual update on the joint research progress of the WP6 cluster participants, but speakers from the relevant industrial domains traditionally join (in tradition to previous years). The meeting was organized by Rolf Ernst (TU Braunschweig). All cluster members were present with several people. Other participants included Matthias Gries, Gregor Stellpflug (Intel Labs), Nico Feiertag, Kai Richter (Symtavision), Fabian Wolf (Volkswagen). The meeting has highlighted key problems in the design and analysis of upcoming embedded systems and suggested solutions in different stages of maturity. Topics included performance analysis, reliability, adaptivity, and early design space exploration. The industrial speakers have contributed talks about timing analysis in automotive applications. The meeting has shown that formal methods as developed in this project are increasingly adopted in the industrial design practice.

https://webmail.ida.ing.tu-bs.de/twiki/bin/view/Main/ArtistDesignClusterMeeting

Workshop : Embedded Communication
TUBS.city Symposium
Braunschweig, Germany – July 1-3, 2009

Tubs.CITY, the TU Braunschweig Center for Informatics and Information Technology, was founded by 28 faculty members of computer science, electrical engineering, information technology, and economics to support and coordinate the research activities in the field. At the end of its first year, tubs.CITY organized a symposium inviting leading scientists from all over Europe to discuss recent trends in computer science and information technology. The workshop "Embedded Communication" featured talks from many ArtistDesign partners and industrial affiliates (for example Lothar Thiele, ETHZ, Markus Kampmann, Ericsson, Kees Goossens, NXP, Marco Bekooij, NXP, Marco Di Natale, Scuola Sup. di Sant' Anna, Luis Almeida, University of Porto, Kai Richter, Symtavision, Guido Stromberg, Infineon AG).

http://city.tu-braunschweig.de/index.php/en/events/symposium-2009/workshops/embedded-communication-

Tutorial: Networks on chip.
Short course at Fudan University,
Shanghai, China - June 2009,
Talk by A. Jantsch and Z. Lu, KTH

Seminar: Resource allocation for quality of service on-chip communication.
University of Cantabria Santander, Spain - February 2009,

Talk by A. Jantsch, KTH

Tutorial: Advanced Topics in Embedded Systems
DTU graduate course 02917 Advanced Topics in Embedded Systems
Technical University of Denmark, Denmark - June 24, 2009
Aske Brekling from DTU gave a tutorial on using MoVES followed by hands-on lab sessions.

Seminar: PhD-seminar at Tallinn Technical University
Tallinn Technical University - April 29, 2009
Michael R Hansen from DTU gave a seminar on efficient model checking for duration calculus

ARTIST Graduate Course: Automated Formal Methods for Embedded Systemsormal
Technical University of Denmark, Denmark – June 17- 25, 2009

DTU organized the yearly ARTIST graduate course. Lectures on UPPAAL by Alexandre Davids and Marius Mikucionis and lab sessions. In the lectures, the theory of timed automata, including priced timed automata and timed games, was introduced and lab exercises gave hands-on experience with the Uppaal tool suite. Lectures by Jüri Vain on model-based development and validation of multi-robot cooperative systems. Followed by Lab exercises based on the Uppaal tool suit. Lectures on MoVES and Duration Calculus by Michael R. Hansen, Jan Madsen and Aske Brekling with focus on analysis of systems with resource constraints.

Conference Organization Lothar Thiele (ETHZ, program chair): IEEE Symposium on Industrial Embedded Systems 2009
EPFL Lausanne, Switzerland - July 8 - 10, 2009.

Application domains have had a considerable impact on the evolution of embedded systems, in terms of required methodologies and supporting tools and resulting technologies. Systems-on-Chips (SoCs) are increasingly making inroads into the area of industrial automation to implement complex field-area intelligent devices which integrate the intelligent sensor/actuator functionality by providing on-chip signal conversion, data processing, and communication functions. There is a growing tendency to network field-area intelligent devices around industrial type of communication networks. Similar trends appear in the automotive electronic systems where the Electronic Control Units (ECUs), typically implemented as heterogeneous system-on-chip, are networked by means of one of safety-critical communication protocols such as FlexRay, for instance, for the purpose of controlling one of vehicle functions; electronic engine control, ABS, active suspension, etc. The design of this kind of networked embedded systems (this includes also hard real-time industrial control systems) is a challenge in itself due to the distributed nature of processing elements, sharing common communication medium, and safety-critical requirements, to mention some.

The aim of the symposium was to bring together researchers and practitioners from industry and academia and provide them with a platform to report on recent developments, deployments, technology trends and research results, as well as initiatives related to embedded systems and their applications in a variety of industrial environments.

Keynote Talks by Members of ARTISTDesign: Scaling in the Third Dimension: Communication Architectures and Memory Hierarchies in an Integrated 3D World, Luca Benini, DEIS Università di Bologna, Italy. System-Level Design Technologies for Heterogeneous Distributed Systems Giovanni de Micheli, EPFL, Switzerland. Embedded Systems Evolution - Design Complexity and the Timing Beast. Rolf Ernst, Technische Universität Braunschweig, Germany. http://sies2009.epfl.ch/ .

Workshop Organization Lothar Thiele (ETHZ): Workshop on Reconciling Performance with Predictability (RePP),
Grenoble, France - October 15, 2009, during the ESWEEK

The RePP workshop is concerned with embedded systems that are characterized by efficiency requirements on the one hand and critical constraints on the other. Such systems occur in many industry-relevant embedded application domains such as avionics, automotive, railway systems, power plants, construction machinery, and robotics. Offline guarantees for the satisfaction of critical constraints have to be derived by appropriate methods. The difficulty of deriving guarantees strongly depends on the predictability properties of the systems, in particular of the employed processor architecture, the software design discipline, the operating system including the scheduling strategy, the communication mechanism, and the used middleware. However, at the same time, system efficiency is measured by means of average-case behaviour under different criteria such as performance, utilization of resources, and power consumption. Unfortunately, it can be observed that in computer system design the gap between average-case and worst-case behaviour increases rapidly. The technical reasons for the limited time-predictability are well known, for example the variation and non-determinism of the system environment and the interference caused by the use of shared resources. The workshop will discuss approaches that atttack the combination of the two goals, the improvements of worst-case predictability and of average-case performance, on all system layers and in the layering principle itself. Predictable architectures, resource-aware compilers, scheduling considering worst-case and average-case performance will be considered. Of particular importance will be the abstraction mechanism used for structuring systems, which has to consider resources as first-class citizens. The workshop has been co-organized by ARTISTDesign participants Lothar Thiele (ETH Zurich) Reinhard Wilhelm (University Saarland), Bengt Jonsson (Uppsala). http://www.tik.ee.ethz.ch/~jchen/RePP/

-- The above is new material, not present in the Y1 deliverable --

3. Milestones, and Future Evolution

3.1 Problem to be Tackled over the next 12 months (Jan 2010 – Dec 2010)

Most of the activities started in Year 1 and continued in Year 2, will be continued in Year 3. A summary of the problems to be tackled and of the integration opportunities is summarized as follows.

System Level Temperature Modeling and Analysis
During the third year, the Linköping group will work on the elaboration of fast and sufficiently accurate analytical temperature models for the system level. Such an efficient approach to temperature analysis is extremely important as a component in a temperature aware optimisation framework for the design of energy efficient embedded systems.

Simulation-based and analytical methods for performance estimation of distributed real-time systems for control applications
During the third year the groups at Linköping, DTU, and Lund will continue their work on modeling and quality optimisation for control applications implemented on distributed embedded systems. Special emphasis will be placed on the issue of event based control and the related quality vs. resource utilisation tradeoffs.

TDMA arbitration policy on AMBA AHB protocol for MPSoC's system bus (UNIBO, Linköping)
The TDMA bus arbiter is 2-3 times bigger than the reference arbiter (i.e. Round Robin Arbiter), and can be clocked up to 330-400MHz (AHB protocol works at 200MHz, and the commercial solutions work at around 400MHz). These results are due to the bigger complexity of the hardware module compared to the reference and can be used to develop the new generations BSA algorithms. The main degree of freedom to improve complexity is the table size (at the moment they are very big since they have to handle all bus accesses) and the table row format (proportion of the number of the masters in the system; AMBA AHB set this to be 16), and to ensure compatibility with the bus protocol.

Future work will be focused on enhancing TDMA based protocols in order to improve the trade-off between performance and predictability.

New bus model for MPSoC's system bus analysis and optimization (UNIBO, ETHZ)
Enhancing the TDMA policy with a second round-robin level of arbitration represents a good trade-off between pure TDMA and pure round-robin, taking the best from each and hiding their drawbacks. Still it offers degrees of freedom (mainly concerning slot allocation) to improve performance.

Future work will be focused on modeling and analysing the FLASH memory sub-system of current and future MPSoC platforms.

Runtime layer design for many-cores architectures
THE CEA LIST and UNIBO will focus during year 2010 on the exploration and the development of dynamic management strategies for the deployment and the execution of multi-tasks application on many-cores architectures. Special attention will be paid on load-balancing and low-power management policies to take benefits from Dynamic Voltage and Frequency Scaling capabilities of the basic computing resources in many-core architectures. Also, smart deployment of application, taking care of potential hardware defauts in the device, will be explored.

In year 3, TU Braunschweig, ETHZ, and Linköping University will continue to work on providing real-time analyses for multiprocessor system with shared resources. These analyses can be supported by research in basically two different directions (which are followed in this cluster): One approach is to investigate and propose an appropriate design of such setups to increase their "predictability". Linköping University has already presented solutions to find optimal memory and bus schedules that allow a high predictability of the tasks on the individual cores in a multiprocessor system. Another approach is to derive upper bounds on the interference between the different cores, and derive the resulting impact on the task execution with formal methods. Analyses in this direction have already been investigated at TU Braunschweig. ETHZ is working on the same issues and the integration into the real-time calculus methodology.

Modeling and Verification of Embedded Systems

DTU will continue its efforts on analytical performance models for both system-level, such as ARTS and Duration Calculus, and low-level, such as a formalized version og the Gezel hardware description language. This will be done in cooperation with Oldenburg, AAU and Virginia Tech.

Contract based architecture dimensioning:

Much of the basic concepts have been built and a resource dimensioning method has been developed, larger experiments and a more systematic evaluation of the method are planned for next year. Within the next two years we will also study run-time re-negotiation of traffic contracts between IPs and the MPSoC infrastructure.

Integration of the communication architecture with the memory architecture:

During the second year Data Management Engine has been developed and implemented, that is programmable and can in principle support all types of MPSoC memory management functions and algorithm. In the third year, cache coherence protocols, memory consistency models, dynamic memory allocation alrgorithms will be developed, implemented and evaluated.

Modeling and analysis of heterogeneous systems:

KTH and DTU will continue their development of a comprehensive SystemC based modelling framework for heterogeneous systems. A few performance analysis tools will be integrated into the modeling framework.

-- Changes wrt Y1 deliverable --

Most of this is new text. It is an update based on the descripton from year 1.

3.2 Current and Future Milestones

Modeling and analysis of fault tolerant distributed embedded systems

During the second year Linköping and DTU will develop a reliability analysis approach for distributed and MPSoC systems considering various hardening degrees of the underlying hardware platform.

The above milestone has been fulfilled.

DTU will investigate "design for adaptivity". The question is how can a system be designed offline such that runtime adaptation is facilitated. We will identify a relevant case-study that can be used to motivate such an approach and propose design methods for adaptivity.

Simulation-based and analytical methods for performance estimation of distributed real-time systems for control applications

During the second year we will extend the analysis approach and make a step forward towards the actual application area. Instead of only looking after worst case execution and response times we will analytically derive quality of service figures that can be expected from an application running on a certain hardware platform. For the first we will look at control applications implemented on distributed embedded systems.

The above milestone has been fulfilled.

Scheduling-control co-analysis and optimisation for distributed applications with event-based control.

System Level Temperature Modeling and Analysis (LiU)

During the third year the focus is on development of fast and sufficiently accurate analytical temperature models for the system level.

Performance analysis of inter-task synchronization in multiprocessor systems (TU Braunschweig, Symtavision)

After the initial analysis has been proposed in year 1, in the 2nd year, the concept of shared resources in multiprocessor systems was to be systematically formalized to capture resource sharing in multiprocessor-systems-on-chips. For this, the previous results that apply to shared memory and MPCP shall be generalized into a framework that allows capturing the timing implication of shared resources, while keeping the composability of the analysis of each component.

This milestone has been fulfilled. The follow-up work [SNE09] allows to embed the analysis of a multicore system into a large-scale networked system. The synergies between the analysis of shared memory conflicts and inter-task synchronization have been investigated in [SNEJR09]. A unified approach to model the shared resource bound will be presented in [SNE10].

In the 3rd year, the work on unifying the methodologies to capture shared resource synchronization and shared memory accesses shall be continued. The framework shall be applied to new applications.

Modeling and Verification of Embedded Systems

In year 1 DTU will continue to formalize the ARTS system-level simulation model using timed automata based on UPPAAL. This work was started in ARTIST2. The aim is to make it usable for designers early in the design process. In order to support designers of industrial applications, the timed-automata model will be hidden for the user, allowing the designer to work directly with the abstract system-level model of embedded systems. The work will be carried out in cooperation with AAU.

The above milestone has been fulfilled, resulting in a prototype framework called MoVES, which allows to experiment with different models-of-computation.

During the second year this work will be continued with the aim to capture more aspects of both the application and the platform. A goal is to make a stronger link between the system-level model and a more detailed hardware platform model. DTU will refine its formal model to address modeling and verification issues closer to the hardware layer of the execution platform.

The above milestone has been fulfilled,

In the third year, DTU will extend the MoVES Framework in various ways, e.g. to incorporate more resource aspects and more advanced bus structures. Furthermore, the issue of scalability will be addressed.

Formal verification of design properties of hardware architectures

In year 1 DTU has worked on a formal language for hardware models based on the Gezel hardware description language developed and maintained by Virginia Tech, USA. The aim is to define a clear semantics of the language which allows to formulate the model-of-computation using timed automata, and hence, being able to formally reason about the hardware architecture.

The above milestone has been fulfilled.

In year 2 this work will be continued, with the aim to reason about non-functional properties such as power consumption and memory usage. A number of larger design cases will be carried out.

The above milestone has been fulfilled.

Initial experiments with a refinement framework for Gezel will been conducted. The framework will be elaborated taking resources into account. Furthermore, studies concerning a more semantically streamlined version of Gezel will be conducted.

Analysis tools for embedded systems

In year 1 DTU has established efficient methods for verification of resource constraints. One activity will focus on the real-time logic durations calculus.

The above milestone has been fulfilled. A model-checking result was established which has the potential of verifying strong timing constraints as well as other kinds of resource constraints. The work has been done in collaboration with University of Oldenburg.

Based on the encouraging results from a first prototype implementation, the plan for next year it to extend the theory and to advance the development of the tool.

The above milestone has been fulfilled.

In the third year, DTU will continue the Improvement of the Duration Calculus model checker with respect to both the theoretical aspects and the practical improvements of the prototype.

Energy Harvesting in Sensor Nodes

ETHZ and Bologna will continue to work on low power sensor nodes. In particular, the results so far will be extended towards application-level decisions.

The milestone has been fulfilled. Both the hardware and software of sensor nodes have

been analysed thoroughly to perform efficient application-level control.

It is planned to extend the current application model to different (e.g. distributed) application scenarios. Adaptive clustering and routing will be in the focus of this activity.

Integration of Symta/S - MPA and unifying approaches for hierarchical scheduling

The integration of methods and tools will be brought to a next level where the integrated tools result in a prototype that can be demonstrated.

Concerning the coupling of MPA with the original version of SymTA/s that applies standard event models (PJD models), the milestone has been completed. Since PJD models are a subset of the event models expressed by arrival curves as employed by MPA, the conversion of PJD event models to arrival curves is straight-forward. On the other hand, the (lossy) conversion of general arrival curves to PJD event models required the development of appropriate conservative approximation functions. Such functions have been implemented in the context of the RTC Toolbox.

More recent versions of SymTA/S employ more general event models (denoted here as delta-functions) which can be considered as the pseudo-inverses of arrival curves. The conversion of arrival curves to delta-functions has been completed. The conversion of delta-functions to arrival curves is still open and will be tackled in the next year.

Contract based architecture dimensioning

Based on the definition of performance contracts between IPs and the SoC infrastructure (done in year 1), in year 2 KTH will work on formulating the problem of dimensioning the infrastructure, given a set of contracted flows and proposing methods for solving it.

The above milestone has been fulfilled partially. The regulation spectrum has been defined, which defines the space of possible contract parameters and the the optimization opportunities for traffic shaping. An optimization algorithm has been developed and implemented and will hopefully be published in year 3.

During the third year we will further study different aspects of infrastructure dimensioning based on conracted flows, and develop optimization methods and algorithms.

Integration of the communication architecture with the memory architecture

KTH will develop a scalable, distributed memory architecture for MPSoCs. It will facilitate efficient handling of a virtual address space, cache coherence and memory consistency.

The above milestone has been fulfilled.

During year 3 we will develop and implement a programmable memory management handler that realizes many memory management functions efficiently. Empasis will be put on scalable performance for distributed memory system in MPSoCs.

Modeling and analysis of adaptive systems

Based on a developed framework for formal modeling of adaptivity (year 1), KTH will apply it to dynamically reconfigurable systems. In particular performance analysis to support design space exploration will be developed.

The above milestone has been fulfilled.

This activity will not be continued in year 3.

Modeling and refinement of heterogeneous systems

In this new activity, started during year 2, KTH and DTU will develop a SystemC based modeling framework for heterogeneous systems including untimed, synchronous time, discrete time and continuous time models of computation.

Hybrid approach combining Real-Time Analysis and Timed Automata

Concerning the hybrid approach combining Real-Time Analysis (RTC) and Timed Automata, CEA will try to extend the schedulability analysis of RTC to state-based schedulers by applying the event generator approach. For example, we are working on the feasibility analysis for adaptive DVS scheduling, to optimistically minimize the energy when the system is lightly loaded by executing at low speeds, and to pessimistically meet the timing constraints when the system is heavily loaded by executing at the maximum speed of the system. ETHZ will extend its framework for coupling timed automata with MPA and attempt to improve its scalability to large distributed embedded systems.

Reliability extensions for Variability Aware Modeling (IMEC)

In the 3rd year a research effort will start for the integration of reliability issues like Negative Bias Temperature Instability (NBTI), Hot Carrier Degradation (HCD), Soft Break Down (SBD in oxide) and Soft Errors in the VAM framework.

3.3 Main Funding

The ArtistDesign NoE funds integration and building excellence with the partners, and with the European research landscape as a whole. Beyond this “glue” for integration and excellence, during Year2 this activity has benefited from direct funding from:

Linköping University:

- Swedish Foundation for Strategic Research (SSF)

  Project name: “Fault-Tolerant and Secure Automotive Embedded Systems.”

- Swedish research Council

  Project name: “Predictability and Timeliness of Multiprocessor Applications in the Presence of Faults.”

DTU

- SYSMODEL (ARTEMIS JU). Period 2009-2011.
- DaNES (Danish Network for Embedded Systems, funded by the Danish Advanced Technology Foundation), Denmark. Period 2007-2010.

- MoDES (project on Model Driven Development of Intelligent Embedded Systems funded by the Danish Strategic Research Council), Denmark. Period 2006-2009.
- ProCell (project on programmable cell chip: culturing and manipulation of living cells with real-time reaction monitoring funded by the Danish Strategic Research Council),

CEA LIST

- **MC2H (ManyCore for Computing and Healing).** French R&D cooperation program (Nano 2012), focusing on the design of multi-core component and on the development of the SW layer allowing to manage it. In this project CEA LIST mainly focus on the SW runtime development in this project.

UNIBO

- ICT-Project PREDATOR
- ICT-Project Scalopes (Artemisia JU)
- Industrial funding on Sensor Networks from Telecom Italia spa

TUBS

- **COMBEST (IST STREP 215543)**
  This IST STREP project COMBEST provides a formal framework for component based design of complex embedded systems.
  http://www.combest.eu/home/

ETH Zurich

- PROD3D Programming for Future 3D Architecture with Many Cores (EU FP7)
- EURETILE Mapping Algorithms onto Tiled Multirocessor Arrays (EU, FP7)
- PREDATOR Predictable and Efficient Embedded Systems (EU, FP7)
- COMBEST Component Based Design of Embedded Systems (EU FP7)
- MICS Mobile Information and Communication Systems (Swiss National Science Foundation)

-- Changes wrt Y1 deliverable --

Each partner has updated the list of funding sources.

4. Internal Reviewers for this Deliverable

- **Dr. Raphaël DAVID** (CEA LIST)
- **Associate Professor Paul Pop** (DTU)