IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Transversal Activity Progress Report for Year 2

Transversal Activity:
Industrial Integration

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Policy Objective (abstract)
Each of the ArtistDesign Thematic Clusters (WP3-WP6) is important *per se* for advancing the state-of-the-art in embedded system design. However, if we wish to have a strong impact on industry and society at large, the results of the thematic clusters have to be harmonized in an overall design flow that can sustain the industrial embedded design chain from conception of the product to its implementation.This transversal activity is intended to define design flows and methodologies for two or three industrial segments leveraging the research carried out in the Thematic Clusters. This deliverable summarizes the achievements of the activity during Y2 of ArtistDesign.

Versions

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1. Overview

1.1 High-Level Objectives

Each of the ArtistDesign Thematic Clusters (WP3-WP6) is important *per se* for advancing the state-of-the-art in embedded system design. However, if we wish to have a strong impact on industry and society at large, the results of the thematic clusters have to be harmonized in an overall design flow that can sustain the industrial embedded design chain from conception of the product to its implementation.

The chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics).

Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, the system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company. The benefits of these flows and methods are obvious as they provide shorter time to market and better quality designs but require a will of the industrial segment to work together towards this goal. In the automotive domain, Autosar is an excellent step in that direction. Other industrial segments are less cohesive in searching for a unified approach to design. In addition, society concerns such as energy, health and environment conservation, are offering new business opportunities for emerging technologies such as wireless sensor networks. The difficulty in these new opportunities resides in lack of standards and of experience with new communication concepts and, last but not least, in security.

We believe that all the thematic clusters bring something important to all industrial segments, but we need to pay attention to the way the results obtained by the clusters are formulated. Integration is a matter of modelling and providing interfaces that guarantee that the properties of the components are maintained after integration. Integration takes two forms: an horizontal one where different IPs coming from different companies or from different design groups in the same company have to be assembled; a vertical one, where the requirements are clearly and possibly formally communicated from a higher level player to a lower level one and where the information about the capabilities and limitations of the IPs are unambiguously communicated from the lower level to the higher level. The ultimate goal of this activity is to provide the “meta rules” according to which the design transformations are carried out and interfaces are built and hence to provide strong guidance to the clusters to make their results more relevant and applicable. Understanding the roles and dynamics of an existing, well-established, vertical industrial segment is a complex task. We could only imagine the complexity of industrial segments that are coming together in these years. While we do target some industrial domain to be the driver for this activity, we understand that our research is going to be more relevant

and better quality if we can distil some common traits of these domains and work with those to choose at a later date which particular chains to address.

The transversal activity hence has two prongs:

- to dive into particular vertical industrial segments and package design methods out of the thematic cluster results for the segments;
- to identify some important common features among verticals and work towards developing methods to address these topics.

We note that the two concerns objects of the Transversal JPRAs (**predictability** and **adaptability**) are common to almost all industrial concerns: For this reason, they provide a framework to start the work on integration driven by industrial applications. Predictability has been a goal since the beginning of the modern industry: predicting the capabilities of existing components allows to come to market faster with new products and prevents taking dead ends, predicting the effort needed to develop parts of the design and to integrate it correctly prevents early recalls and associated costs. The faster is the dynamics of the industry, the more important is to have predictability in design.

Adaptability is the property of a design to be adapted to changing environments and working conditions. Reconfigurability, programmability, dynamic restructuring are all facets of adaptability. Novel approaches to communication could benefit greatly from adaptability. In fact, much research is being carried out to design devices that could sense available bandwidth and adapt the communication protocol to the most convenient band at the time.

We believe that it will be eventually easier to compose the vertical design industrial flows once these two sub-flows have been examined and results obtained. In addition, being generic concerns they do not require effort from the academic partners to understand the *modus operandi* of entire industrial segments and offer a shorter time to results.

The vertical industrial segment motivated prong will begin *by bringing up-to-speed the largest possible number of participants to the logic of the design chain by organizing workshops for discussion with the participants to the chain.*

We proposed at the onset of the activity to target Automotive, Nomadic and Health Applications as potential vertical segments where we have a range of maturity from well-established (automotive) to emerging (health). At the 2008 meeting in Rome of the ArtistDesign partners, the three vertical markets of interest were identified as:

1. Automotive/avionics since we noted a strong similarity in the overarching issues faced by these two industrial segments that are driven by safety concerns and have to consider distributed implementations;
2. Health applications with particular emphasis on equipment design and manufacturing;
3. Energy efficient buildings, a novel field of great interest to the European Community as well as to the rest of the world as 30% of energy consumption is considered to be in commercial buildings.

These applications address an established area of excellence of European Industry where international competition is fierce, an area of growth where again European Industry has a strong position but where the dynamics are fast and new applications are envisioned in strategic areas such as elderly care, and a new area with great potential where energy conservation concerns are going to place a great political emphasis. Given the nature of this work, the main participants in the cluster are the groups that have industrial vocation such as ESI, OFFIS, and IMEC.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.2 Industrial Sectors

This transversal activity is intended to funnel the results of the thematic clusters and of the other two transversal activities towards industry, thus maximizing the impact of DesignArtist findings. We expect the impact to be above and beyond the industrial segments identified above (automotive/avionics, health care and energy efficient buildings). In particular, we expect that the nomadic and consumer sectors be also impacted albeit some of the issues typical of these two vertical domains are substantially different from the others.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.3 Main Research Trends

The advancement of the embedded system research activities in Academia and research institutions has been gaining momentum over the past few years. Some industrial segments, typically avionics and automotive, have been also progressing in the use of tools and methodologies that have improved productivity and design quality albeit the advancements have not been uniform across companies and divisions inside the same company. In particular, *model-driven design* is becoming a standard. In this methodology, the design is captured and analyzed at the functional level with simulation tools and in some limited cases, with formal analysis techniques. The most used flow especially in the avionics/automotive domain is the Simulink Mathworks flow that uses Real Time Workshop (or dSpace, TargetLink) to generate implementation code on the most used single-processor platforms. Other industrial approaches are based on UML and the associated tools provided by IBM (Telelogic and Rational). There has been strong interest in defining UML profiles that are dedicated to real time embedded systems: in particular, SysML is gaining a broad attention. However, in both cases (but more visibly in the UML design flow), the semantics of the design has not been captured well enough to allow for formal analysis. The SPEEDS IP aims at improving substantially the quality of the embedded system design process by providing formal contract-based models that capture not only the functional aspects of the design but also the non functional ones such as power and timing with the Hierarchical Rich Component modelling approach. In this approach, the model can be mapped into the format accepted by advanced academic tools such as BIP so that formal analysis and simulation of the design can be carried out in a rigorous way. To capture the non functional aspects of the design novel timing analysis tools that are commercially available and that have been originally developed by ArtistDesign partners such as SymTA (Rolf Ernst) and AbsInt (Rheinhard Wilhelm), are being integrated into tool chains comprising model-based design tools, compilers, timing-analysis and schedulability tools. This tool integration will guarantee highest precision and thus avoid the need for over-commissioning.

We believe that the main issue is not one of modelling and tool usage but one of adopting and enforcing an appropriate methodology that could embrace advanced modelling and could use new generation tools. The aim of the transversal activity is indeed to study and propose to our industrial partners this approach. We do not expect to have an immediate success in having industry adapt the design flows since the tools and approaches are fairly sophisticated and require a quantum leap in the technical background of the designers.

The research trends in this domain is then to identify common layers of abstraction that favor the communication along the supply chain across company boundaries and the design chain inside each company. In addition, industry is pushing towards a better design capture methodology and formal model to allow for stronger verification and validation. In the case of the transportation and military industry, there is increased activity in design for certification. Certification is about design processes and not about the behavior of the artifact. We believe there will be a trend towards making the actual behavior of the artifact be certified which will in turn force companies to adopt rigorous methodologies for modeling and analysis.

Another important research trend to consider is how to accommodate the increased attention to energy efficiency. On October 21st, the US National Science and Technology Council (NSTC) released a report describing R&D activities that could decrease use of natural resources and improve indoor environments while reducing greenhouse gas emissions and other harmful pollutants from the building sector. The report, *Federal R&D Agenda for Net-Zero Energy, High-Performance Green Buildings*, was produced by the NSTC's Buildings Technology Research and Development Subcommittee under the auspices of the Office of Science and Technology Policy (OSTP) in the Executive Office of the President. Commercial and residential buildings consume about one-third of the world's energy. In particular, U.S. buildings account for more than 40 percent of total U.S. energy consumption, including 72 percent of electricity generation. If current trends continue, by 2025, buildings worldwide will be the largest consumer of global energy, consuming as much energy as the transportation and industry sectors combined. Building systems are characterized by uncertain process dynamics; time-varying behavior; multiple objectives (cost functions) that change over time (water usage for evaporative cooling, peak electrical power); and environmental effects (disturbances) such as ambient temperature and humidity, solar radiation, and user behavior. The challenges posed to the research community are large. The actual situation in bulding management is worrisome. The level of sophistication of building managers, of commissioning personnel and of building management companies is very low. Simple minded control laws are implemented on information systems that are under dimensioned with respect to the needs of a comprehensive design approach. The research agenda here is to tie together the various aspects of building management, e;g., Heating, Ventilation and Air Conditions (HVAC), lighting and safety (fire and intrusion alarms, egress systems) into an integrated monitoring and control system. This action must include research on hierarchical multi-objective control, distributed system design, sensor and actuator selection and positioning. The systems must be adaptive, predictable and fault tolerant. The research agenda in the design and operation of energy efficient buildings is fully consistent with the thematic clusters and with the transversal integration activities. The role of industry here is very relevant as the important aspects to take into consideration when developing algorithms and methodology cut across multiple domains and company boundaries. The industrial landscape is moving at an interesting pace: players are repositioning to take advantage of the concerns dictated by the political climate on energy issues. For example, equipment companies are now setting up new system divisions to address the integration problems. This situation offers this transversal activity a unique opportunity to influence the way industry is looking at the problem. There is a new term being used in the research community interested in this area: systems of systems, meaning that the level of integration needed here is one or more levels above what has been done today in other industrial sectors such as automotive. In the October 2009 SEEC meeting, the activities in energy efficiency by the leading industrial concerns and by selected academic groups were reviewed and potential for future collaboration identified. The Workshop was considered to be a success by the participants and we had a strong mandate to continue organizing similar workshops in the future.

-- Changes wrt Y1 deliverable --

The topic of energy efficiency and cyber-physical systems are coming rapidly to the center stage of the international research agenda and this is reflected in the activity that we have chosen to invest on.

2. State of the Integration in Europe

2.1 Brief State of the Art

As in the other transversal activities, it is almost impossible to provide a BRIEF state of the art of integration in Europe since this activity involves many different aspects in many different industrial segments. This transversal activity not only feeds from the thematic clusters but also from the other two transversal activities. Hence, the state of the art in each of the thematic clusters and transversal activities are propedeutic to this section and will not be repeated here.

In general, research activities tend to focus on specific problems and to develop techniques that are aimed at solving well defined aspects of these problems. This transversal activity is about integration at the industrial segment level transcending companies' boundaries and actually helping to integrate better the activities across the supply chain. In addition, the activity aims at providing inputs to the ArtistDesign community on how to interface methods and tools so that an overall methodology can be assembled. Today, integration at this level is vigorously pursued in Europe in some industrial segments (most notably the automotive domain) but it still needs years to come up with an agreed upon solution. In the energy efficient building domain achieving integration even inside single company boundaries is a difficult proposition. The potential impact of a research aimed at developing this overarching vision cannot be overemphasized. The objective is ambitious and it needs attention at the community level: a single research group does not have the breadth or the muscles to develop this vision.

The automotive industrial segment with the Autosar initiative has an important message about the integration of the design chain and advocates the adoption of standards in interfaces and operating systems. We actually believe that much more work needs to be done at the semantics level and at the non functional aspects of design. The work carried out in SPEEDS is an example of how to address these problems not only in the automotive domain but also in the avionics domain albeit limited to higher levels of abstraction. The CESAR Artemis project is about taking the work of SPEEDS to a new level of sophistication and to extend its reach to implementation issues. The large participation of industrial concerns in CESAR and SPEEDS that involve OEMs, Tier 1 suppliers and tool providers bodes well for the activity of this transversal activity.

The solidification of the Artemis JTI has been instrumental in driving the industrial interest in embedded systems. In particular, as quoted by the Artemis Web-site: "*The European Union recognises the strategic importance of Embedded Computing Systems and has launched the Artemis Joint Technology Initiative (JTI). The ARTEMIS JTI is implemented as a Joint Undertaking (JU) which is a public-private partnership between:*

- *The European Commission*
- *Member States*
- *ARTEMISIA, a non-profit Industrial Association*

ARTEMISIA is the ARTEMIS Industrial Association which represents the research commmunity including Industry (large, small and medium sized companies), universities and research institutes. The ARTEMIS JU is an organisation based in Brussels that was legally established in February 2008 and it is managed by an Executive Director."

Hence the links of the ArtistDesign community to Artemis and Artemisia are of paramount importance for the development of the deliverables of the Industrial Integration Transversal Activity. In particular, the steering Board of Artemisia counts three of the ArtistDesign Partners (Joseph Sifakis (CEA), Luca Benini (U. Bologna) and Rudi Lauwereins (IMEC)) among the 5 research representatives. Alberto Sangiovanni Vincentelli is a member of the Public Authority

Board and the Governing Board of Artemis. We expect the ties with Artemis and Artemisia to grow stronger in the future

The German competence cluster SafeTRANS (Safety in Transportation Systems,) including ArtistDesign members TU Braunschweig and OFFIS, concentrates research and development expertise in Germany in the area of the design of complex embedded systems for transport systems, to develop in cooperation with leading companies in the transport industry methodologies and processes for the development of safety critical embedded systems within the framework of a mutual research strategy. SafeTRANS and the French Pôles de Compétitivité SYSTEM@TIC-PARIS-REGION and Aerospace Valley allied to form the European institute EICOSE (European Institute for Complex and Safety Critical Embedded Systems Engineering). In the meantime EICOSE has become the first »Innovation Cluster« within the technology platform ARTEMIS.

In September 2008, the new KTH Centre in Embedded systems - ICES, joining forces from several research groups at KTH and industry (ABB, Enea, Ericsson, Scania, Stoneridge and ÅF) was founded. Key goals of the centre include acting as a catalyst for improved interactions between academia and industry, and between the member companies. The centre has a focus on embedded systems engineering and science, emphasizing system design, architecture and methodology. For this reason, KTH has been added to the core team for the Transversal Activity. We expect major contributions from this team.

-- Changes wrt Y1 deliverable --

More emphasis has been given to the relationship with Artemis and Artemisia.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

This transversal activity is intrinsically about integration. Integration is across the various partners who are active in it as well as across the different thematic clusters and other transversal activities. Since our aim is about integration of other groups in ArtistDesign we are depending on the delivery of their findings to build an effective approach to the design integration across industrial segments. We also aim at integrating our work with the work in other industrial and academic communities. The interaction with US companies and research organizations is documented in the activity report about the Forum on CyberPhysical Systems where industry, academia, and government agencies came together to discuss how to approach the new generation challenges posed by the closer interaction between the physical world and computing. Also the topical event in Trento saw the participation of companies that are not (yet) in the ArtistDesign community as well as US companies who are interested in exchanging notes and results with our community.

The industrial integration activity is intented to last beyond the period in which ArtistDesign will be funded. It does have important links with large European projects (SPEEDS and CESAR) and with industry independently. Partners OFFIS, ESI, IMEC and Trento are directly connected with industry in deep ways. They will provide the backbone of the activity of industrial integration during the years.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

2.3 Other Research Teams

The main teams in Europe who are active in industrial flows are all included in ArtistDesign. Of course, the teams do not cover all industrial domains with the same intensity as automotive. The historical Artist group had had their main focus placed on embedded software. In ArtistDesign the periphery has been augmented to include some teams that have architecture, SoC and control expertise that are a necessary complement to the core strength to address the industrial integration issues. Connections to the HYCON NoE (http://www.ist-hycon.org/) were present via PARADES who coordinated the industrial integration of this NoE. However, people involved in industrial integration activities based on control such ETH's Morari and Lygeros are not present in ArtistDesign. HYCON ended its operation last year and in 2009 it has been transformed into HYCON II with similar group of partners. We do have strong relations with Manfred Morari and John Lygeros of ETH who are instrumental in defining the next generation distributed architecture for control applications including wireless sensor networks and we have leveraged this contact.

The communication field is a main focus of parallel groups in the US especially in the area of military applications sponsored by DARPA (e.g., UCLA (Estrin), Berkeley (Culler, Pister, Rabaey), Washington (Borriello)). In Europe, research in wireless sensor networks and their applications is carried out in several academic and industrial research groups. In particular, University of L'Aquila, Politecnico di Torino and TU Berlin

Research groups in the US that work on the issue of industrial integration among others are CHESS (Berkeley), GSRC (multi-university program sponsored by the Semiconductor Industry Association and DARPA), MUSYC (MultiScale System Center, a new MARCO Focus Research Center Program headquartered in Berkeley) and ISIS (Vanderbilt). Teams at CMU have strong industrial program that culminated with the victory of the DARPA Urban Challenge of the GM-CMU team. The double appointment of Alberto Sangiovanni Vincentelli with Berkeley offers an opportunity to link tightly with these groups. In addition, the COMBEST project whose partners are for the large part participating to ArtistDesign has an international collaboration also at the industrial level (for example, UTC, GM, Intel, National Instruments, Mathworks, and Cadence) so that proficuous interactions are guaranteed.

-- Changes wrt Y1 deliverable --

The HYCON NOE has ended its operation and will be replaced by HYCON II NOE that will remain in close contact with us.

2.4 Interaction and Building Excellence between Partners

The core groups are internationally renowned in their area of industrial interest. A change with respect to the original proposal occurred in January 2009 when PARADES withdrew from the ArtistDesign Consortium and it has been replaced by Trento. Alberto Sangiovanni Vincentelli transitioned from the PARADES to the Trento team to provide the continuity in the management of the JPRA.

All have multiple industrial segment contacts (transportation, IC, printing, health care, entertainment, consumer, nomadic, security, buildings). They act as agents of change and of

spread of excellence in the ArtistDesign community with respect to relation with industry. The interactions with the other clusters and transversal activities are at their inception. Since we selected the final focus area recently, we expect to engage the cluster partners with additional impetus. The active collaboration within this project has also led to the identification of common problems and goals between the partners and national and European companies. This leads to new joint undertakings e.g. within the Artemis framework.

- Changes wrt Y1 deliverable --

A change with respect to Year 1 occurred in January 2009 when PARADES withdrew from the ArtistDesign Consortium and it has been replaced by Trento. Alberto Sangiovanni Vincentelli transitioned from the PARADES to the Trento team to provide the continuity in the management of the JPRA.

2.5 Interaction of the Transversal Activity with Other Communities

The partners for this activity are the majority of the partners in ArtistDesign. Their interactions with the communities are massive. Most of these interactions have been documented in the reports for the other sections. However, we would like to stress here the connection with HYCON that has not been reported elsewhere. The research communities that are connected with this activity include artificial intelligence, high-performance computing, wireless sensor networks, building optimization, IC design, and mechanical engineering. We are connected UC Berkeley, CMU, UCLA, Vanderbilt, University of Pennsylvania, Columbia University, Cadence, General Motors, Xilinx, Qualcomm, UTC and Stevens Institute in the US. In Asia, we are connected with Kyushu University, Hitachi, Toshiba, Panasonic, Samsung and Centre for Embedded Software Technology (CEST).

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

3. Summary of Activity Progress

3.1 Technical Achievements

The technical achievements are collected under four major subheadings reflecting the nature of the contribution and the industrial sector being impacted: General Frameworks for system-level design; Applications to the Automotive Sector, Applications to Chip Design; Applications to Buildings; Applications to Wireless communication technology.

3.1.1 General Frameworks for System Level Design

Platform-Based Design and Frameworks: Metropolis and Metro II

Participants: Cadence, Trento, UC Berkeley, Sun Microsystems, UTC, National Instruments and Intel.

System-Level Design (SLD) means many different things to many different people. In our view, system-level design is about the design of a whole that consists of several components where specifications are given in terms of functionality with additional:

- constraints on the properties the design has to satisfy and on the components that are available for implementation and
- objective functions that express the desirable features of the design when completed.

This definition is general since it relates to many different application domains, from semiconductors to systems such as cars and airplanes, buildings, telecommunication and biological systems. To deal with system-level problems, our view is that the issue to address is not developing new tools, albeit they are essential to advance the state of the art in design, rather it is the understanding of the principles of system design, the necessary change to design methodologies and the dynamics of the supply chain. Developing this understanding is necessary to define a sound approach to the needs of the system and component industry as they try to serve their customers better, to develop their products faster and with higher quality. This contribution was about principles and how a unified methodology together with a supporting software framework, as challenging as it may seem, can be developed to bring the embedded electronics industry to a new level of efficiency. To demonstrate this view, we first presented the challenges in design for the system of the future and a manifesto for the need of a unified methodology. We then summarized a methodology, Platform-Based Design (PBD), that has been developed over the past decade and that we believe can fulfil the needs. Further, we presented Metropolis, a software framework supporting the methodology and Metro II, a second generation framework built to alleviate the problems we encountered when applying Metropolis to industrial test cases. We concluded the paper with two test cases in two diverse domains: semiconductor chips (a UMTS single-chip design) and energy efficient buildings (an indoor air quality control system).

Embedded systems challenges and focus areas

Participants: KTH, ABB, Scania, Ericsson, ÅF, Enea, Stoneridge

During its first year of operation, the KTH Innovative Centre for Embedded Systems (ICES) has directed an effort to define the key focus of its activities. The Embedded systems area is wide, and there are also many possible activities which could be pursued by an embedded systems centre (ranging from continued education to research). In this first ICES Vision and Goals document, key challenges as perceived by the participating industries (telecom, automotive

and automation) and related scientific challenges are discussed. The guiding vision for ICES is established in the document: To achieve a flourishing eco-system for industry and academia excelling in embedded systems education, research and innovation. To reach this vision, ICES adopts the role of networker and catalyst with industry, KTH students and KTH faculty as the main stakeholders. The focal technical areas to be addressed by ICES are embedded systems architecture, software, verification and methodology. The Vision and goals document also defines concrete goals and activities for ICES the forthcoming years.

3.1.2 Automotive Applications

Dependable and Flexible Electrical Architecture 2020

Participants: Volvo car, KnowIT, Semcon, Mecel, Chalmers, Saab and KTH

This is a new automotive project, funded by the Swedish state, with the overall goals to suggest new embedded systems architectures that enable functional growth, are energy efficient and facilitate system verification. Topics of special concern include architecture evaluation methods, developing a reference architecture, model-based development methods, design for safety, and compliance with the upcoming safety standard ISO-26262. KTH has an industrial PhD student funded as part of the project, which connects well to KTH's ongoing research on architectural design, model-based development and design methodology.

Special Issue of the IEEE Trans on CAD on Automotive Applications

Participants: Trento, UC Berkeley, GM, TU Brauschweig, TU Vienna, Pirelli-Telecom Italia Berkeley Labs, Universitat des Saarlandes

Automotive systems are today the epitome of distributed complex embedded systems and, as such, offer an ideal domain to inspire research in methodologies and tools, as well as a rich test case for embedded system developers. The overall size of the software that is embedded in automobiles today is in the millions of lines of code, and it is forecast to significantly increase to accommodate additional functional content, from power train and chassis control, to infotainment. In addition to sheer software size, the complexity of automotive systems is constantly growing due to tight requirements for increased safety and performance, reduced pollution, and overall efficiency. Cost and time-to-market pressure pose additional burden to the designers for achieving an efficient use of system resources. Alongside the appetite for consumer electronics and communication devices that the car buyers are demonstrating, there is also a growing concern about the number of lives that are lost in our roads due to accidents. Both in the U.S. and Europe, regulatory pressures on safety are evident. Safety concerns are a major driving force for automakers. To cope with these problems, major advances are required at all levels in the architecture stack of automotive systems, from innovative chip architectures and sensors, to new standards for communications, to methods, tools, and standards for the development of middle-ware and application-level software components. One such advance is a fundamental shift in architecture design that is taking place. Today’s automobile electronic systems are based on the concept of federated architecture, where each function is deployed to an autonomous electronic control unit (ECU), which is developed as a black-box integrated subsystem by Tier-1 suppliers. Because of the increased complexity and distribution of active-safety and future safety-critical functions, including by-wire systems, and the interdependence of these functions that gives rise to unexpected and undesired emerging behaviors, systems are becoming very difficult to test and validate. Furthermore, there is limited understanding of how to control the nonfunctional behavior of interacting modules, including timing and reliability properties emerging from the composition. Last but not least, the number of ECUs and busses is growing to unreasonable levels due to the need of accommodating new functionalities in the

federated architecture paradigm, causing cost and reliability problems. This situation has interested the automotive industrial sector to look at integrated architectures, in which software components can be supplied from multiple sources, integrated on the same hardware platform or physically distributed and possibly moved from one CPU to another without loss of functional and time correctness and providing a guaranteed level of reliability. This shift decouples software design from the hardware platform and provides opportunities for the optimization of architecture configuration, increased extensibility, flexibility, and modularity. ECUs can physically be integrated, with significant cost and dependability benefits and a reduction in the number of communication wires and connection harnesses. The possibility of defining components (subsystems) at higher levels of abstraction and with well-defined interfaces also allows separation of concerns and improves modularity and reusability. Methods and tools are needed for the design–time analysis of the result of the system-level integration, including the verification of safety constraints and, in general, the capability of predicting system-level functional, reliability, and timing properties. To discuss these trends and to provide a glimpse at the future of automotive systems, we organized with **the support of ArtistDesign** a full special day at the DATE 08 Conference as shown in last year report for WP4. This Special Section on Automotive Systems collects some of the presentations given at the special day [SVD09]. The papers in this Special Section address several problems in the architecture stack, from physical (sensor device) designs, to software architectures, to methods and tools for timing and performance analysis.

PAPER LIST

1. Sinem Coleri Ergen, Alberto Sangiovanni-Vincentelli, Xuening Sun, Riccardo Tebano, Sayf Alalusi, Giorgio Audisio, and Marco Sabatini, *The Tire as an Intelligent Sensor*
2. Roman Obermaisser, Christian El Salloum, Bernhard Huber, and Hermann Kopetz, *From a Federated to an Integrated Automotive Architecture*
3. Reinhard Wilhelm, Daniel Grund, Jan Reineke, Marc Schlickling, Markus Pister, and Christian Ferdinand, *Memory Hierarchies, Pipelines, and Buses for Future Architectures in Time-Critical Embedded Systems*
4. Simon Schliecker, Jonas Rox, Mircea Negrean, Kai Richter, Marek Jersak, and Rolf Ernst, *System Level Performance Analysis for Real-Time Automotive Multi-Core and Network Architectures*

Model based engineering of automotive embedded systems, beyond Autosar

Participants: KTH, CEA, Volvo, CFR, TUB, Continental, Mentor, Univ. Hull, Mecel

As part of the FP7 ATESST2 project, technologies that complement Autosar - the automotive industry effort on software architecture - are being developed. The paper describes the EAST-ADL approach and how it complements Autosar. Autosar, is a large investment towards standardized automotive software platforms. An important role of Autosar is the strengthening the position of software development in the automotive industry. Autosar defines a complete software architecture and middleware that supports integration of third party software components into automotive electronic control units. While the standardization of software architecture is important, this does not however, solve the problems of dealing with requirements, product lines, mapping functions to software/hardware, and in meeting the needs of the upcoming safety standard, ISO26262. These goals correspond to the focal points in the ATESST2 project, where the EAST-ADL architecture description language, provides additional abstraction layers on top of Autosar and capabilities to reason about variability (product lines), and safety related issues. In addition, the TIMMO ITEA2 project, which has worked to establish complementary timing description techniques for Autosar, and ATESST2 have been carried out in close cooperation, such that results on timing descriptions for timing analysis are now fully integrated into the EAST-ADL.

Optimizing the implementation of communication in synchronous reactive models with time constraints

Participants: UC Berkeley, Trento, National Instruments

Model-based design methodologies are gaining attention in the industrial community because of the possibility of early and efficient functional validation and formal verification of properties at high levels of abstraction. The advantages of validating the design using high-level models can be lost entirely if errors and modifications that are not back-annotated to the higher abstraction levels are introduced when refining the design to lower levels of abstraction. To overcome this problem and to reduce design time, automatic synthesis has been used for the refinement process from Register Transfer Languages to logic gates for digital circuit design. This approach guarantees (assuming that the synthesis algorithms are correctly implemented) that the semantics of the RTL description are semantically equivalent to the semantics of the logic circuit. Automatic code generation is similar in intent and applicability. However, the software implementation of the abstract model must make efficient use of the platform resources that may not reflect all the assumptions of the code generation algorithms. The implementation of communication in a synchronous reactive model requires buffering and access procedures at the kernel level. In previous work, we obtained tight bounds on the size of communication buffers to maintain semantics equivalence. In real-time systems, however, because of the longer execution times of access procedures, an implementation with minimum buffer size may lead to the violation of deadlines. To solve this problem, we proposed a Mixed Integer Linear Programming (MILP)-based optimization approach that provides the minimum memory implementation of a set of communication channels while guaranteeing that the task deadline constraints are met [WDSV09]. The analysis is validated by an OSEK/VDX-compliant implementation that provides an estimate of actual run-time overheads. The approach is applied to a set of task graphs and an automotive case study.

Automatic Code Generation for Synchronous Reactive Communication

Participants: National Instruments, UC Berkeley, Trento, The Mathworks

Synchronous Reactive models are used in Model-Based Design to define embedded control applications. The advantage of Model-Based Design is that system properties can be verified on the model and apply to its software implementation if the translation of the model into code preserves its semantics. In this paper, we presented an automatic code generation framework for the semantics-preserving implementation of communication in multi-rate systems. The proposed solution applies to the widely used MATLAB and Simulink products. It leveraged the Target Language Compiler template language of Real-Time Workshop and extended the applicability of available commercial code generators. The overhead in memory of the presented solution was analyzed and compared with other implementations.

Optimizing Extensibility in Hard Real-Time Distributed Systems

Participants: Intel, UC Berkeley, Trento, UTC

Some applications such as the design of a car typically require upgrading an implementation platform to accommodate new functionality or to fix errors over a product life-time that may extend over a five year horizon. In this case, being able to adjust the design without undergoing a major re-design cycle is imperative for competitive advantage. We addressed the problem of defining the initial solution to the design problem so that it is as robust as possible with respect to addition of new tasks or modifications to existing ones. To do so, we introduce a robustness measure, the extensibility metric, and then develop an efficient algorithm that

optimizes this metric. In this paper, we focused on hard real-time distributed systems that collect data from a set of sensors, perform computations in a distributed fashion and based on the results, send commands to a set of actuators. The tasks must satisfy tight end-to-end deadline constraints. Extensibility is defined as the amount by which the execution time of tasks can be increased without changing the system configuration while meeting the deadline constraints. With this definition, a design that is optimized for extensibility not only allows adding future functionality with minimum changes, but is more robust with respect to the variance of task execution times. We considered systems based on run-time priority-based scheduling of tasks and messages. In particular, we assumed that input data (generated by a sensor, for instance) are available at one of the system's computational nodes. A periodically activated task on this node reads the input data, computes intermediate results, and writes them to the output buffer from where they can be read by another task or used for assembling the data content of a message. Messages - also periodically activated - transfer the data from the output buffer on the current node over the bus to an input buffer on a remote node. Local clocks on different nodes are not synchronized. Tasks may have multiple fan-ins and messages can be multi-cast. Eventually, task outputs are sent to the system's output devices or actuators. The extensibility optimization problem can be considered as part of the mapping stage in the Platform-Based Design (PBD) design flow, where the functionality of the design (what the system is supposed to do) and its architecture (how the system does it) are captured separately, and then "joined" together, i.e., the functionality is "mapped" onto the architecture. In the application, function blocks communicate through signals, which represent the data dependencies. The architectural description is a topology of computational nodes connected by buses. In this paper, buses and nodes can have different transmission and computation speeds. Mapping allocates functional blocks to tasks and tasks to nodes. Correspondingly, signals can be mapped into local communication or packed into messages that are exchanged over the buses. Task and message priorities are assigned and the mapping is performed in such a way that the end-to-end latency constraints are satisfied in the worst-case. Task allocation, signal to message packing, message allocation and priority assignment are the design variables considered in this paper that are chosen with the objective of optimizing task extensibility.

The first stage of the proposed algorithm is based on MILP programming, where task placement (the most important variable with respect to extensibility) is optimized within deadline and utilization constraints. The second phase features two heuristic algorithms, which iteratively optimize signal-to- message packing and priority assignment. This algorithm runs much faster than randomized optimization approaches (a 20x reduction with respect to simulated annealing in our case studies). Hence, it is applicable to industrial systems as the case studies, which are of size comparable with the typical case of deployment of a set of additional functionalities in a commercial car, demonstrate in the experimental section. The first case study is a set of active safety functions deployed on a vehicle bus-architecture, with 9 ECUs, 41 tasks, and 83 CAN signals. In this case, optimization takes less than 1800 seconds, compared to more than 12 hours needed by the randomized optimization method, with results of comparable quality. The second test case is a safety-critical distributed control system deployed within a small truck. The key features of this system are the integration of slow and very fast (power electronics) control loops using the same communication network. In this example, we are interested in redesigning an existing system to understand the effects of adding communication and computational resources to the system. The shorter running time of the proposed algorithm allows using the method not only for the optimization of a given system configuration, but also for architecture exploration, where the number of system configurations to be evaluated and subject to optimization can be large. A further advantage of an MILP formulation (even if used only for the first stage) with respect to randomized optimization, is the possibility of leveraging mature technology in solvers, the capability of detecting the actual optimum (when found in reasonable time), or, when the running time is excessive, to compute

at any time a lower bound on the cost of the optimum solution, which allows evaluating the quality of the best solution obtained up to that point.

Statistical Analysis of Controller Area Network Message Response Times

Participants: UC Berkeley, GM, Trento

Modern automobile architectures are composed by tens of Electronics Control Units (ECUs) connected by several buses, most of which are Controller Area Networks (CAN). The availability of multiple ECUs can be exploited by distributing control tasks of one domain (for example, power train) to several ECUs. In this case, a number of distributed functions are assigned to multiple tasks executing concurrently on different modules and communicating via messages transmitted on CAN. Distributed functions include time-critical controls, but most often, also functions that are characterized by requirements for average performance together with hard deadline constraints (as for most active-safety functions) and functions with soft real-time requirements (controls for enhanced driver comfort). The definition of a new architecture framework for one or more car product families is an extremely important step: ECUs, networks and the topology of connections must be defined and frozen years in advance of production. Later, during the architecture lifespan, functions are placed on ECUs and communication scheduled on the bus. This paper [ZDGSV09] presented a statistical approach to the early evaluation and selection of distributed embedded architectures for next-generation automotive controls, where the application performance depends on the end-to-end latencies of active-safety functions. Automobile architecture must be evaluated and selected having in mind that they will have a lifespan of 5 to 10 years and that during this lifespan the communication and computation load is partly unknown because new functions are still being decided on and have not been designed as yet. Hence, when verifying that the architecture is sufficiently robust with respect to constraints on latency and performance targets of present and future functionalities, loads can only be roughly estimated by looking at past trends or by exploiting early indications of designers. In this paper, we considered an application model that is currently deployed in GeneralMotors E/E architectures and is supported by the AUTOSAR standard. We described the use of statistical analysis to compute the probability distribution of Controller Area Network (CAN) message response times when only partial information is available about the electrical architecture of a vehicle as well as about its functionality. We provided results that showed our statistical inference allows predicting accurately the distribution of the response time of a CAN message, once its priority has been assigned, from limited information such as the bus utilization of higher priority messages.

This publication obtained the best paper award at the IEEE Symposium on Industrial Embedded Systems.

Optimizations of an application-level protocol for enhanced dependability in FlexRay

Participants: Trento, UC Berkeley, GM

FlexRay is an automotive standard for high-speed and reliable communication that is being widely deployed for next generation cars. The protocol has powerful error detection mechanisms, but its error-management scheme forces a corrupted frame to be dropped without any notification to the transmitter. In this paper, we analyzed the feasibility of and proposed an optimization approach for an application-level acknowledgment and retransmission scheme for which transmission time is allocated on top of an existing schedule. We formulated the problem as a Mixed Integer Linear Programming one. The optimization is comprised of two stages. The first stage optimizes a fault tolerance metric; the second improves scheduling by minimizing the latencies of the acknowledgment and retransmission messages. We demonstrated the effectiveness of our approach on a case study based on an experimental vehicle designed at General Motors.

3.1.3 Applications to Chip Design

UMTS MPSoC Design Evaluation Using Metro II

Participants: Trento, UC Berkeley, Intel

In the race for higher performance computing, multi-processor platforms offer flexibility and a wide range of alternative design solutions that are able to optimally trade-off the design metrics of interest. This is especially true for embedded applications, often faced with hard to satisfy real-time and energy requirements which are best addressed by a distributed implementation. This trend is also apparent in the design of modern microprocessors, where the use of multi-threaded cores is favored over faster clocks to speed up the software execution. The design of multi-core architectures is, however, made complex by a large design space, the difficulty of integrating heterogeneous components, and time-to-market pressures. We argued that only with a coherent and general design methodology can we address all these challenges. The methodology should be applicable during all phases of the design process from specification to implementation, it should support the design chain across divisional and company boundaries, it should favor re-use at all levels of abstraction and should be based on rigorous semantics foundations. Platform-based design (PBD) was developed with these goals in mind. A methodology can be applied even in the absence of supporting tools and flows. However, there is no question that the full leverage of the principles can be achieved only with appropriate design software. In this contribution [DSDP09], we discuss the use of a new event-based design framework, Metro II as presented above, for the simulation and design of multiprocessor platforms and present a non-trivial UMTS case study to show the results that can be obtained from architecture exploration. In particular, we show that this approach may be used to carry out quick design space exploration with accurate, low-overhead simulation.

A Methodology for Constraint-Driven Synthesis of On-Chip Communications

Participants: Trento, UC Berkeley, University of Columbia, UTC

With the advances of IC technology, global interconnects have become the dominant factor in determining chip performance: they are not only becoming responsible for a larger fraction of the overall delay and power dissipation but exacerbate also design problems such as noise coupling, routing congestion, and timing closure, thereby imposing severe limitations on design productivity. Because of these characteristics, most VLSI circuits can be considered **distributed systems**, a fact that challenges traditional design methodologies and the electronic design automation tools that are based on them. Systems-on-Chip (SoCs) are typically designed by assembling intellectual property (IP) components from different vendors and/or different divisions of the same company in the attempt of reducing time-to-market by reusing pre-designed and pre-verified elements. However, since these components are designed independently, the assembly step is often a challenging problem that requires *the design of communication interfaces to match different protocols and data parallelism, and the routing of global interconnect wires to meet the constraints imposed by the target clock period*. Borrowing from the communication networks literature, an NoC can be built through the combination of heterogeneous elements such as interfaces, routers, and links. The NoC design is a challenging problem because there are many degrees of freedom (e.g. network topologies, routing protocols, flow-control mechanisms, positions of the communication components and core interfaces) as well as multiple optimization goals (e.g. performance, power, area occupation and reliability). Hence, the problem had been simplified by limiting the number and types of components considered, by focusing on a subset of the relevant objectives, by constraining NoC topology and components positions, and by dividing the optimization process in successive stages. Limiting the degrees of freedom has also the important side effect of reducing implementation and layout complexity. While a rich set of interesting results exists in the literature, few are the examples of practical applications of NoCs. In fact, the debate

between those who favor standard bus architectures or variations thereof and those who advocate the adoption of NoC approaches ranging from constrained architectures to custom ones is vibrant. We do not take sides even though the NoC approach has undisputable fundamental merits that may make it successful in the long run. Instead, we propose a general methodology for the design of on-chip communication that can explore a large number of alternatives including as special cases NoCs, bus architectures and hybrid ones. Thanks to its generality our approach can be used to build a framework where different constrained solutions are compared using a number of evaluation factors. We addressed the synthesis of optimal heterogeneous networks by assembling components from a fine-grained library without enforcing any constraint on their topology other than the ones formally captured in the library. In particular, the network that we obtained need not be direct and not even connected if these constraints are not captured in the composition rules of the communication components.

Reliabiltiy Analysis with mixed-criticality workloads (see also Activity Report Hardware And MpSoC Design

Participants: TU Braunschweig, Toyota-ITC, Symtavision

In 2008 a research trilateral cooperation between TU Braunschweig, Toyota Information Technology Center (T-ITC), and Symtavision GmbH has been initiated, investigating the effects of errors on reliability and safety of real-time networks. Some of the results have been published in 2009 [SE09a], [SE09b].

A follow-up project has been started in 2009. In this context special focus has been put on reliability analysis for the CAN protocol, with special emphasis on the design of mixed criticality bus configurations. In this context several extensions of the analysis methodology have been developed. While the original approach addresses the occurrence of single bit errors only without any consideration of error correlations, in 2009 models have been proposed to describe interdependencies between errors, especially the occurrence of burst errors. Additionally analysis algorithms have been developed to integrate the burst error models into the original analysis approach.

Another subject of interest in this project is the extension of the message release model, which has been restricted to strictly periodic activations so far. The inclusion of release jitter enables the approach to be applicable to a wider variety of systems. For that purpose the analysis has been extended such that activation patterns with jitter can be incorporated.

Methods, Tools, and Platforms for cost-efficient certification of safety-critical multicore systems

Participants: TU Braunschweig, Intel, Infineon, Sysgo, Elektrobit, EADS IW, Delphi, TÜV Nord, and others

RECOMP is an ongoing project proposal submitted in response to the second call for proposals of the European JU Artemis. The goal of RECOMP is to develop methods, tools and platforms for enabling cost-efficient certification and re-certification of safety-critical multi-core systems, with special emphasis on the design of mixed-criticality systems. Additionally the integration of the developed techniques should be integrated into certification processes for different domains such as avionics, automotive or industrial automation. Commonly used safety standards for single-core systems like IEC 61508, ISO 26262 or DO 178B will provide the base for the certification of mixed-criticality multi-core systems. To enable the coverage of the complete safety-related development process a large consortium has been established to address most of the upcoming challenges. For example the consortium contains hardware (e.g. Intel, Infineon) and software (e.g. Sysgo, Elektrobit) vendors, system integrators (e.g. EADS IW, Delphi), certification authorities (TÜV Süd) and several research institutions.

Multi-processor design technology

Participants: IMEC, Toshiba

IMEC has extended in 2009 the research collaboration with Toshiba in the field of MPSoC mapping tools and flexible, energy efficient processors for MPSoC.

http://www2.imec.be/imec_com/adres-reconfigurable-processor-template.php

http://www2.imec.be/imec_com/imec__08217_s-multi-threaded-adres-processor-architecture-ready-for-licensing.php?year=2009&month=10

Component-based service model

Participants: DTU, B&O ICEpower

DTU and B&O ICEpower have continued the development of a modelling framework for system level performance estimation of embedded systems including Multi-Processor System on Chip (MPSoC) based configurations. The overall goal is to provide a framework which supports models described at multiple levels of abstraction which will allow designers to perform design space exploration at the various design stages ranging from initial high level specifications to detailed, bit true cycle accurate models.

During year 2, several refinements of the framework has been carried out resulting in minor changes of the modelling methodology. Substantial time and effort has been spent on this refinement implementing the changes in the current implementation of the framework. Also, a lot of time and effort has been put into the definition of a language used to specify models and automatically synthesize fast simulation models based on the specification. This shows promising results but is still work in progress. During year 2 DTU and B&O ICEpower has worked on an elaborate case-study, which has resulted in two publications [THM09a,THM09b].

3D Stacked IC Design using Through Silicon Vias - TSVs

Participants: IMEC, Qualcomm, Javelin

IMEC and Javelin developed in close collaboration with Qualcomm, a partner in IMEC's 3D integration program, 3D PathFinding toolflows, which extend the Javelin PathFinding methodology and j360 Silicon PathFinder platform to support virtual chip design for co-optimization of system design and 3D interconnect-packaging technologies. Designers of 3D ICs can use it to rapidly explore many potential 3D design implementations for their technical value propositions, and to identify and mitigate risks-benefits and optimize value.

http://www2.imec.be/imec_com/javelin-design-automation-and-imec-extend-javelin-pathfinding-design-technology-for-3d-stacked-ics.php?year=2009&month=02

Memory Aware Variability Modeling (VAM) for embedded SRAMs

Participants: IMEC, Samsung

IMEC successfully transferred MemoryVAM (Memory Variability Aware Modeling), the first EDA tool for statistical memory analysis, to Samsung Electronics. The tool predicts yield loss of SRAMs caused by the process variations of deep-submicron IC technologies. IMEC's MemoryVAM is an essential tool to avoid already at design time the most likely reasons for failure, anticipating and correcting weak design spots before tape-out, and hence avoiding redesign spins after processing. The tool also provides key help to memory and system designers to estimate yield loss due to changes of for example cycle time, access time and power consumption (static/dynamic) caused by process variations.

http://www2.imec.be/imec_com/imec-transferred-design-for-manufacturing-tool-for-embedded-srams-to-samsung-electronics.php?year=2009&month=04

RF Transceivers

Participants: IMEC, Renesas

Renesas continued in 2009 the strategic research collaboration with IMEC in the field of nanoelectronics, to perform research on 45nm RF transceivers targeting Gbit/s cognitive radios. To this end, Renesas has joined IMEC's software-defined radio (SDR) front-end program. This research program includes reconfigurable RF solutions, high-speed/low-power analog-to-digital converters (ADCs) and new approaches to digitize future RF architectures.

http://www2.imec.be/imec_com/renesas-collaborates-with-imec-on-reconfigurable-rf-transceivers.php?year=2008&month=04

3.1.4 Application to Smart Energy Efficient Buildings

Energy-neutral distributed sensing for proactive energy management in buildings and plants

Participant: University of Bologna, Telecom Italia
University of Bologna has designed the Energy Harvesting circuit which is the core of the power supply unit of the wireless sensor nodes of the Kaleidos framework developed by Telecom Italia (the main telephone company in Italy). The collaboration deeply exploits wireless sensor networks and wireless actuators to improve and simplify industrial and service operations. To this goal Kaleidos is a middleware platform to collect data and provide anf efficient management of electricity consumption in telecommunication switching plants. University of Bologna provided technology for powering the sensors and recharging the batteries exploiting the electromagnetic fields in the cable grid and using the same AC current sensors used for measurements and data logging.

Warehouse of the future

Participant: ESI, Vanderlande Industries

The Falcon project, set up by the Embedded Systems Institute and Vanderlande Industries, aims at overcoming the weaknesses of the existing centralized warehouse control systems. This so-called "warehouse of the future" can be achieved by defining appropriate (software) architecture for warehouse and (quantitatively) showing that such architecture eliminates the weaknesses of the centralized warehouse control system. Existing warehouses are controlled by centralized control systems, which are typically built around a centralized database containing all knowledge of the warehouse status. These warehouse control systems allow a high system performance, because all optimization information is available in one place. An additional strength of these systems is the persistency of information, which is handled automatically by the database. On the other hand, the scalability of such warehouse control systems is limited, because all event handling involves accessing a central database. Moreover, these centralized control systems are difficult to maintain, because it requires detailed knowledge of warehouse status in order to achieve the desired performance. Similarly, it is difficult to reuse warehouse controller functionality for other warehouses.

A main result of the project is a framework that allows holonic warehouse control systems to be set up from a description of the available warehouse equipment and a library of agent behaviors. This framework has been applied to the Compact Picking System (CPS) of the Plus Retail warehouse in Middenbeemster, the Netherlands. Moreover, a holonic prototype of a

High-Density Storage (HDS) system is being developed. Results of this work been published in [MCV09].

3.1.5 Application to Wireless Communication

Ambient Living with Embedded Networks

Participants: ESI, Free University Amsterdam, Devlab (Eindhoven)

ESI has started to work in the ALwEN project (Ambient Living with Embedded Networks) on the combination of Body Sensors, Ambient Sensors, Wireless Networks and Telemedicine. The ultimate goal is a set of concepts and methods for a novel care approach that will be implanted in a new generation low-cost integrated circuit (IC) with embedded computation and wireless communication. Key to the success of Wireless Sensor Network applications is the right balance between overall system-level properties such as dependability, power consumption, network and application performance, and robustness to adverse operating conditions. ESI focuses on improving, understanding and predicting capabilities of these system level properties. ESI intends to develop system-level, multi-disciplinary models to predict overall-system level properties, with high fidelity in typical home, office, and care environments. These models will be used also by project partners in support for system design evaluation methods, and system configuration methods to be developed in this project. The results of this work so far have been published in [BNH09], [NBB09a], [NBB09b].

Future wireless communications

Participants: IMEC, Panasonic

IMEC has extended in 2009 the research collaboration with Panasonic in the field of green radios.

http://www2.imec.be/imec_com/imec_and_panasonic_sign_comprehensive_joint_research_contract.php?year=2008&month=11

Green radio technology

Participants: IMEC, Samsung

IMEC collaborates in 2009 on technologies for green radios with Samsung. The research collaboration topics include cognitive reconfigurable radio baseband and millimeter-wave wireless communications technologies. Building on expertise in software-defined radios that support the major standards for wireless communications, IMEC pushes its research one step further towards cognitive radios (ICs with a radio that adapts itself to the changing environment, not only to the communication standard, but also to the available communication frequencies and conditions such as indoor/outdoor, signal strength, movement). IMEC is working on the control algorithms that take into account these changing environment parameters and user needs. As another cornerstone of its research into wireless communication, IMEC develops radio ICs for the wireless communication of massive data streams, for example for uncompressed high-definition television streams. Such data streams require a high throughput, in the order of Gbits per second. A suitable bandwidth for that communication is available around 60GHz. Therefore, IMEC works on cost-effective, low-power 60GHz radio ICs in standard CMOS, targeted at the consumer market,

http://www2.imec.be/imec_com/samsung-electronics-joins-imec-research-program-on-green-radios___.php?year=2009&month=05

3.1.6 Timing Analysis/Predictability

Static Analysis of Synthesized Code

Participants: Universität des Saarlandes, AbsInt, Daimler

The analysis of code synthesised from high-level models often can be improved by utilising model information. For example, code synthesized from the automata component of models often has complex control flow, not easily amenable to existing static analysis tools. The control logic implemented in automata also governs the control flow through the surrounding parts of the model. Information about the reachable states can be used to exclude infeasible paths in the model, potentially reducing the computed worst-case execution time.

Identification of Operating Modes

Participants: Universität des Saarlandes, AbsInt, Bosch

Embedded control often works in different operating modes with different timing constraints. Determining the overall worst-case execution time would be pessimistic for some of the modes. One goal of the cooperation between Universität des Saarlandes, AbsInt and Bosch is the development of a mode-specific timing analysis. This would determine a worst-case execution time for each mode. However, operating modes currently are not explicitly specified and therefore neither visible on the model level nor on the code level. Designers of components typically know them, but have no way to declare them. Upon composition of the components, this information is completely lost for the integrated system. A first step therefore consists of an analysis of the system on the model and/or the code level to identify operating modes.

3.1.7 Autonomous systems - Generation of Correct-by-construction Code

Project: Goal-Oriented Autonomous Controller (GOAC)

Participants: UJF/Verimag, GMV, LAAS, ISTC-CNR

Industrial Partner: GMV is a CMMI 3 certified company that has more than 20 years of experience in the aerospace field. for the space and ground segment, and has developed very different types of systems (safety/mission critical/aid tools/simulators/web systems/robotics) using a number of technologies (Linux/Unix, Win-dows, C++, .NET, Java, Matlab, Fortran, C, Multi-agent systems) in developments of varying size (ei-ther large, medium or small) and complexity. GMV, as the prime contractor for the proposal, will be in charge of the integration of the software, and it will design, develop and implement the executive layer, and the global framework for the GOAC. GMV will also develop the second use case, and will perform the testing of GOAC. GMV is already involved EXOMARS as well as in the EUROBOT Ground Prototype projects.

Application: The Goal Oriented Autonomous Controller (GOAC) is an autonomous controller using a sense-plan-act paradigm to provide increasing levels of autonomy for robotic task achievement. GOAC will generate plans in-situ, will deterministically dispatch activities for execution and will recover from off-nominal conditions. Underlying GOAC is a rich representation that deals with metric time and resources necessary for dealing with planning and execution time uncertainty in dynamic environments. It comes with a lower-level functional layer that is tightly integrated with an abstract decisional level all of which have a rich operational legacy with deployments in real-world environments. The system's higher levels of abstraction deal with long-term mission plans that are deliberative; lower levels of abstraction are increasingly reactive. The functional layer is purely reactive with fast reaction times necessary for failure recovery and command dispatch. Additionally a Verification and Validation

system ensures compositional correctness by guaranteeing global system properties of system components.

GOAC will comprise a set of coordinated concurrent control loops with each control loop embodied in a reactor that encapsulates all details of how to accomplish its control objectives. The controller will dynamically re-plan in the event of off-nominal situations by being context-aware of onboard resources and be responsive to human injected goals from the ground. Planning, Scheduling and Execution are interleaved, thereby ensuring responsiveness for control. With its representational richness using a timeline-based planning and scheduling approach, GOAC will simultaneously track a family of desired outcomes. The resultant controller will be robust to change, scalable for being embedded in space certified hardware and operable from ground control systems with selectable levels of autonomy. Further with its unified planning/scheduling and execution control language, GOAC will provide substantial economies in software development and in the process demonstrate advanced Artificial Intelligence-based control for space applications for future ESA missions.

GOAC has a rich legacy. Technology components of GOAC have been used for command and control (including failure recovery via replanning) of underwater, Earth-based mixed-initiative control of NASA's Spirit and Opportunity rovers at JPL, the first closed-loop AI-based control experiment in space with the Remote Agent, planning downlink/uplink activities of ESA's Mars Express orbiter and for functional layer control for autonomy testbeds which include rovers and terrestrial robots in challenging conditions.

UJF/Verimag's Role: The BIP (Behaviours, Interactions and Priorities) framework for the component-based construction of real time systems will be used to ensure interoperability of components guaranteeing correctness-by-construction for essential system properties such as deadlock-freedom, progress and liveliness, in order to reduce a-posteriori validation as much as possible.

The resulting system will be a robust, fully verifiable autonomous controller that will allow adjustable levels of goal-oriented commanding. And it will allow personnel to focus on what they want the robotic platform to do instead of laboriously working on how to satisfy science and engineering goals. The system will be proven looking at the requirements of two case studies including an embedded rover testbed.

Project: Méthode et Architecture Robuste pour l'Autonomie dans l'Espace (MARAE)

Participants: UJF/Verimag, LAAS, ASTRIUM

Description: The project addresses designing a software architecture for space systems, such as satellites, which must have a high level of autonomy. The consortium proposes a method for integrating functional and deliberative (planning and control execution) modules in a consistent and robust software architecture. The architecture relies on the BIP (Behaviours, Interactions and Priorities) framework for the component-based construction of real time systems will be used to develop a robust prototype, that will be evaluated experimentally by injecting faults.

3.1.8 Other System Applications

Code-generation Infrastructure

Participants: TU Dortmund, ICD, Siemens, Airbus, Bosch, Thales, Intracom, ELMOS, TUV, Raith, Vorwerk.

At Dortmund, most industrial activities are chanelled via the University's IT spin-off, ICD e.V. ICD has been providing a commercial code generation infrastructure to Infineon. This infrastructure is supporting a protocol processor optimized for processing internet packets. The infrastructure is based on the ICD-C compiler design tools. In 2009, the basic tool set as well as its applications have been extended. A cut-down version of ICD-C is now available for free downloads (see http://www.icd.de/es). ICD-C is offering support and maintenance for some terminated European research projects such as MORE, in cooperation with the original software developers. ICD is led by P. Marwedel, who also leads a group at TU Dortmund. Research results from Dortmund were presented at a visit to Samsung (Seoul) in August 2009. Dortmund is also cooperating with Airbus, Bosch, Thales (France), Intracom (Greece) via projects MNEMEE and PREDATOR. Also, the aiT tool for worst case timing analysis has been integrated into the experimental worst-case execution time aware C compiler WCC. Local contacts exist to ELMOS (a semiconductor manufacturer mostly for the automotive domain) and TÜV. Also, there was cooperation with Raith GmbH and with Vorwerk (on autonomous vacuum cleaners).

http://www.icd.de

Performance analysis of a top-range wafer stepper

Participant: ESI, ASML

In the Wings project ESI worked at ASML (http://www.asml.com) on a systematic approach for constructing executable models. The key of this approach is to separate the logic of the embedded control application from the execution platform on which it is deployed. The resulting executable models yield an overview and a system-wide insight in the timing bottlenecks. They further allow one to rapidly explore alternatives to optimize the timing performance, by adapting the application, the execution platform or the mapping.

The Wings project has demonstrated the effectiveness of the performance prediction and optimization method by applying it to a complex performance-critical subsystem of a wafer scanner. The application of the method within ASML has resulted in more than a dozen improvement proposals with an expected overall timing performance gain of more than 50%. The principles of this work were published in [FVT09], [GFV09], [LTS09].

-- The above is new material, not present in the Y1 deliverable --

3.2 Individual Publications Resulting from these Achievements

TRENTO

[SVSSYM09] A. Sangiovanni-Vincentelli, S. Shukla, J. Sztipanovits, G. Yang, D. Mathaikutty, "Metamodeling: An Emerging Representation Paradigm for System-Level Design", Special Section on Meta-Modeling, IEEE Design & Test, vol. 26, no. 3, pp. 54-69, May/June 2009.

[DSDP09] D. Densmore, A. Simalatsar, A. Davare, R. Passerone, and A. Sangiovanni-Vincentelli. “UMTS MPSoC design evaluation using a system level design framework”. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE09)*, Nice, France, April 20-24, 2009.

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[THM09b] Anders Tranberg-Hansen, Jan Madsen, A Compositional Modelling Framework for Exploring MPSoC systems, In *proceedings of the IEEE/ACM conference CODES+ISSS* 2009, Grenoble, France.

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[TWLR09]L. Tan, B. Wachter, P. Lucas and R. Wilhelm. Improving timing analysis for Matlab Simulink/Stateflow. In *Proceedings of the 2nd International Workshop on Model Based Architecting and Construction of Embedded Systems (ACES-MB)*, October 2009.

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-- The above are new references, not present in the Y1 deliverable --

3.3 Joint Publications Resulting from these Achievements

Trento, UCB, Verimag, INRIA, OFFIS, PARADES

[PBGB09] Roberto Passerone, Imene Ben Hafaiedh, Susanne Graf, Albert Benveniste, Daniela Cancila, Arnaud Cuccuru, Sèebastien Gèerard, Francois Terrier, Werner Damm, Alberto Ferrari, Leonardo Mangeruca, Bernhard Josko, Thomas Peikenkamp, and Alberto Sangiovanni-Vincentelli. “Metamodels in Europe: Languages, Tools, and Applications”. *IEEE Design and Test of Computers*, 26(3):38-53, May/June 2009.

Trento, Scuola di Sant’Anna, GM

[SVD09] A. Sangiovanni-Vincentelli, and M. Di Natale, Challenges and Solutions in the Development of Automotive Systems, *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, Volume: 28, Issue: 7, pp. 937-940, July 2009.

Trento, UC Berkeley, National Instruments

[WDSV09] G. Wang, M. Di Natale, A. Sangiovanni-Vincentelli, "Improving the Size of Communication Buffers in Synchronous Models With Time Constraints," *IEEE Transactions on Industrial Informatics*, Volume 5, Issue 3, Aug. 2009 Page(s):229 - 240.

Trento, UC Berkeley, National Instruments, Mathworks

[WDMSV09] G. Wang, M. Di Natale, P. J. Mosterman, A. Sangiovanni-Vincentelli, "Automatic Code Generation for Synchronous Reactive Communication*," ICESS*, pp.40-47, 2009 International Conference on Embedded Software and Systems, 2009.

Trento, UC Berkeley, UTC, Intel, Scuola di Sant’Anna

[ZYSDSV09] Q. Zhu, Y. Yang, E. Scholte, M. Di Natale and A. Sangiovanni-Vincentelli, "Optimizing Extensibility in Hard Real-Time Distributed Systems", *15th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*, San Francisco, CA, April, 2009.

Trento, UC Berkeley, GM, Scuola di Sant'Anna

[ZZDGG09] H. Zeng, W. Zheng, M. Di Natale, P. Giusto, A. Ghosal, A. Sangiovanni-Vincentelli. "Scheduling the FlexRay bus using optimization techniques". In *Proceedings of the 46th ACM/IEEE Design Automation Conference (DAC*), July 2009.

Trento, UC Berkeley, GM, Scuola di Sant'Anna

[ZDGSV09] H. Zeng, M. Di Natale, P. Giusto, A. Sangiovanni-Vincentelli. "Statistical Analysis of Controller Area Network Message Response Times". In *Proceedings of the IEEE Symposium on Industrial Embedded Systems (SIES*), July 2009. [Best Paper Award].

Trento, UC Berkeley, GM, Scuola di Sant'Anna

[LDZGSV09] W. Li, M. Di Natale, W. Zheng, P. Giusto, A. Sangiovanni-Vincentelli, and S.A. Seshia. "Optimizations of an application-level protocol for enhanced dependability in FlexRay," In *Procs. of the 2009 Design, Automation, and Test in Europe Conference and Exhibition (DATE'09*), pp.1076-1081, Nice, France, 2009.

Trento, UC Berkeley, Columbia, UTC

[PCVS09] A. Pinto, L.P. Carloni, and A. Sangiovanni-Vincentelli. "A Methodology for Constraint-Driven Synthesis of On-Chip Communications," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 28, No. 3, March 2009.

Braunschweig, Symtavision

[SR09] Simon Schliecker, Jonas Rox, Mircea Negrean, Kai Richter, Marek Jersak and Rolf Ernst, **"**System Level Performance Analysis for Real-Time Automotive Multi-Core and Network Architectures**,"***Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 28, No. 7, pp. 979-992, July 2009

KTH, Carmeq, Continental, ETAS, Volvo, Mentor

[CF09] Philippe Cuenot, Patrik Frey, Rolf Johansson, Henrik Lönn, David Servat, Ramin Tavakoli Kolagari, Matthias Weber, Martin Törngren. *ENGINEERING SUPPORT FOR AUTOMOTIVE EMBEDDED SYSTEMS – BEYOND AUTOSAR*. ATZ Autotechnology. Invited technical article. ATZautotechnology 2-2009 (April).

KTH, Volvo, Ericsson

[TE09] Martin Törngren, Tor Ericson, Barbro Claesson, Jan-Erik Frey, Axel Jantsch, Patric Jensfelt, Karl Henrik Johansson, Tony Sandberg, Hans Schmekel, Jan Wikander, Johnny Öberg. *Innovative Centre for Embedded Systems – ICES. Vision and goals towards world-class education and research at KTH in cooperation with industry.* KTH technical report to appear Dec. 2009 (http://www.kth.se/itm/centra/ices?l=en_UK).

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[GPH09] S.V. Gheorghita, M. Palkovic, J. Hamers, A. Vandecappelle, S. Mamagkakis, T. Basten, L. Eeckhout, H. Corporaal, F. Catthoor, F. Vandeputte, K. De Bosschere: A System Scenario based Approach to Dynamic Embedded Systems, ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 14, Number 1, (2009)

IMEC vzw. and UniBo

[FC09] Facchini, M.; Carlson, T.; Vignon, A.; Palkovic, M.; Catthoor, F.; Dehaene, W.; Benini, L. and Marchal, P.: System-level power/performance evaluation of 3D stacked DRAMs for mobile applications In Design, Automation and Test in Europe, DATE 2009, Nice, France, April 20-24, (2009).

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[BCA09] Christos Baloukas, José Luis Risco-Martín, David Atienza, Christophe Poucet, Lazaros Papadopoulos, Stylianos Mamagkakis, Dimitrios Soudris, José Ignacio Hidalgo, Francky Catthoor, Juan Lanchares: Optimization methodology of dynamic data structures based on genetic algorithms for multimedia embedded systems. Journal of Systems and Software 82(4): 590-602 (2009)

IMEC vzw. and NTNU

[MHM09] Narasinga Rao Miniskar, Elena Hammari, Satyakiran Munaga, Stylianos Mamagkakis, Per Gunnar Kjeldsberg, Francky Catthoor: Scenario Based Mapping of Dynamic Applications on MPSoC: A 3D Graphics Case Study. In Embedded Computer Systems: Architectures, Modeling, and Simulation, 9th International Workshop, SAMOS 2009, Samos, Greece, July 20-23, (2009)

-- The above are new references, not present in the Y1 deliverable --

3.4 Keynotes, Workshops, Tutorials

Keynote: Collaborate to Innovate, by Alberto Sangiovanni Vincentelli, annual customer meeting TSMC

San Jose', April 21st

This is the annual conference held by TSMC in United States. This year there were more than 2,000 attendants from all over the world. The key note addressed the issues of system level design and the novel direction of research in the area of advanced electronics and energy efficient buildings. The angle taken was that the new challenges for the electronic and system industry can only be tackled with rigorous design methodologies and tools that support collaboration.

Keynote: Integration means to achieve industry and academia collaboration, by Martin Törngren, Embedded Conference Scandinavia,

Stockholm, Sweden - October 13-14, 2009.

This conference originated as an industrial fair, but this year Swedish universities were invited both as presenters and to the exhibition, with the idea to stimulate a dialogue. Apart from the special session "A new economy and a new world" – there was also a well visited panel debate, discussing how to achieve improved collaboration between industry and academia. Various mechanisms and drivers to achieve this were discussed, including the role of funding agencies.

http://www.embeddedconference.se/index.php?Itemid=47

Keynote: S. Mamagkakis 'Adaptive solutions for the emerging reliability and multicore resource management challenges'

2nd Workshop on Adaptive and Reconfigurable Embedded Systems - APRES 2009

Grenoble, France, October 11th, 2009 within ESWEEK 2009

In this talk, the reliability and resource management challenges of the emerging multicore platforms were discussed and the proposed adaptive solutions were evaluated. As technology scaling approaches nanoscale dimensions, we expect integration to move even further, thus increasing dramatically the number of cores on a chip and enabling the mapping of a higher number of software applications. The main challenges that arise are related with run-time resource management of shared multicore platform resources and variability and reliability issues which are linked with nanoscale technology.

http://www.artist-embedded.org/artist/Keynote.html

Keynote: D. Verkest 'Multimedia systems in a changing technology landscape',

7th IEEE Workshop on Embedded Systems for Real-Time Multimedia

Grenoble, France, – October, 2009 within ESWEEK 2009

Silicon IC technology scaling delivers the required transistor densities to meet the computational needs of multimedia systems, however, at an ever increasing cost. Changes in the technology landscape influence multimedia systems architectures, resulting in design challenges and opportunities. In this presentation, we provided a glimpse of this technology-design interaction in the context of multimedia systems, touching upon multi-core architectures, 3D chip-stacking, and embedded MEMS technology.

http://www.science.uva.nl/events/ESTIMedia09/keynotes.html

Keynote: S. Mamagkakis 'Emerging multicore hardware platforms and their software support challenges'

21st Euromicro Conference on Real-Time Systems

Dublin, Ireland, – July, 2009

In this keynote talk, the latest developments and future directions of hardware MPSoC platforms for nomadic embedded applications were presented. Next to the hardware perspective, the software related challenges of these emerging MPSoC platforms were discussed and some of the proposed parallelization and memory hierarchy management

solutions were evaluated. This keynote is also relevant for the Scheduling and Resource Management activity.

http://ecrts09.dsg.cs.tcd.ie/keynote-speaker.php

Lectio Magistralis: **EDA: 40 years of innovation, by Alberto Sangiovanni Vincentelli**

Strathclyde University, Glasgow, August 10, 2009

This lecture was given to the members of the Royal Society of Edimburgh and to other invited guests in the occasion of the Maxwell Award ceremony. Alberto Sangiovanni Vincentelli presented how EDA was born and what were its early challenges. In addition, the raise of the EDA industry and the key contributions to the field were outlined.

Symposium: European Universities and Researchers as Sources of Innovation in Finland, Italy and Silicon Valley

European Entrepreneurship & Innovation Thought Leaders Seminar, Stanford Universit, April 20

Alberto Sangiovanni Vincentelli presented his view on the innovation scenarios in US and Europe and what can be done to improve the communication between the two innovation communities especially in the area of embedded systems.

Symposium: The how and why of Promoting Entrepreneurship Abroad,

Hoover Institution, Stanford University, May 21st

Alberto Sangiovanni Vincentelli moderated a panel and gave a speech on how US can use innovation as a foreign policy lever to increase its reach and positive impact. Participants to the seminar included Condoleeza Rice, George Schulz and four US ambassadors.

Workshop: Embedded Communication *(see also Activity 6.2 Platform and MpSoC Analysis)*
TUBS.city Symposium
Braunschweig, Germany – July 1-3, 2009

tubs.CITY, the TU Braunschweig Center for Informatics and Information Technology, was founded by 28 faculty members of computer science, electrical engineering, information technology, and economics to support and coordinate the research activities in the field. At the end of its first year, tubs.CITY organized a symposium inviting leading scientists from all over Europe to discuss recent trends in computer science and information technology. The workshop "Embedded Communication" featured talks from many ArtistDesign partners and industrial affiliates (for example Lothar Thiele, ETHZ, Markus Kampmann, Ericsson, Kees Goossens, NXP, Marco Bekooij, NXP, Marco Di Natale, Scuola Sup. di Sant' Anna, Luis Almeida, University of Porto, Kai Richter, Symtavision, Guido Stromberg, Infineon AG).

http://city.tu-braunschweig.de/index.php/en/events/symposium-2009/workshops/embedded-communication-

Workshop: Smart and Efficient Energy Council (SEEC'2009)
Invited talk: "Energy-neutral distributed sensing for proactive energy management in buildings and plants"
October 8-9, 2009 Trento, Italy
Speaker: Luca Benini
Luca Benini gave a talk on the system challenges of designing wireless sensor networks, particular emphasizing the challenges of making these systems self-powered using energy

harvesting tecniques. The focus of the workshop was on energy efficiency as a major contributor to the green economy.
http://www.artist-embedded.org/artist/Overview,1800.html

Tutorial: S. Mamagkakis and P. R. Panda 'Memory Architectures and Software Transformations for System Level Design'

15th Asia and South Pacific Design Automation Conference (ASP-DAC)

Yokohama, Japan, – January, 2009

In this tutorial a memory-aware system level design flow was presented that can address strict power and performance budgeting problems by customizing both the underlying memory architectures/organizations, as well as by transforming the system-level source code to generate an input for system-level design that is better tuned to the memory architectures and organizations. Such a "memory-aware" system level design flow can result in LSI designs exhibiting superior performance, power and memory footprint characteristics.

http://www.aspdac.com/aspdac2009/tutorial/

Conference: Industrial Embedded Systems
International Symposium on Industrial Embedded Systems (SIES)
Lausanne, Switzerland – 8-10 July, 2009

Anders Tranberg-Hansen from DTU gave a talk on "Exploration of a Digital Audio Processing Platform Using a Compositional System Level Perfromance Estimation Framework".

Conference: CODES+ISSS
Embedded Systems Week
Grenoble, France – 11-16 October, 2009

Jan Madsen from DTU gave a talk on "*A Compositional Modelling Framework for Exploring MPSoC systems".*

Symposium: ESI Symposium
Invited talk: Design-Space Exploration of High-Tech Embedded Systems
8 December 2009, Eindhoven, Netherlands
Speaker: Twan Basten
Twan Basten gave a talk outlining the development of a design-space exploration toolset that leverages the results of various formal modelling and analysis techniques to support the exploration of the large design-spaces of high-tech embedded systems.

Fall school: IPA Fall Days on Quantitative Methods for Embedded Systems
Invited talk: "Reliable Dynamic Embedded Data Processing Systems"
26 November 2009, Noordwijk aan Zee, Netherlands
Speaker: Twan Basten
Twan Basten gave a talk about ways to achieve reliable operation of data-intensive embedded systems, in a context with both intra- and inter-application dynamism. Dataflow analysis for models that capture the various operating modes of an application allows a model-driven design-space exploration, while compositional reasoning about trade-off configurations allows run-time adaptation to changing operating conditions.

Computer Engineering Seminar, University of Wisconsin
Invited talk: "Reliable Embedded Multimedia Systems?"
21 September 2009, Madison, Madison, WI, USA
Speaker: Twan Basten
Twan Basten gave a talk covering various throughput and buffer analysis techniques for dataflow graphs, exploring how these techniques can be used in a compilation flow for Chip

MultiProcessors (CMPs) that is able to cope with the increasingly dynamic nature of modern multimedia systems. The talk furthermore outlined a run-time adaptation solution for CMPs, that forms a basis for the reliable dynamic reconfiguration of the system.

Electrical & Computer Engineering Seminar, Carnegie Mellon University
Invited talk: "Reliable Run-time Adaptation in Resource-constrained Embedded Systems"
17 September 2009, Pittsburgh, PA, USA
Speaker: Twan Basten
Twan Basten gave a talk outlining how the concepts of Pareto algebra can be used to provide solutions for run-time adaptation problems. Two specific parameterized and compositional run-time adaptation solutions for Chip MultiProcessors (CMPs) and Wireless Sensor Networks (WSNs). The parametrization allows a trade-off between the quality of the result and the required computational resources. Compositionality ensures scalability of the solutions.

CSE seminar, KTH, Stockholm
Invited talk: "Reliable Run-time Adaptation in Resource-constrained Embedded Systems"
May 25, 2009, Stockholm, Sweden
Speaker: Twan Basten
Twan Basten gave a talk outlining how the concepts of Pareto algebra can be used to provide solutions for run-time adaptation problems. Two specific parameterized and compositional run-time adaptation solutions for Chip MultiProcessors (CMPs) and Wireless Sensor Networks (WSNs). The parametrization allows a trade-off between the quality of the result and the required computational resources. Compositionality ensures scalability of the solutions.

Workshop: "Dependable ICT Systems"
Invited talk: "Reliable Run-time Adaptation in Resource-constrained Embedded Systems"
April 24, 2009, Utrecht, Netherlands
Speaker: Twan Basten
Twan Basten gave a talk outlining how the concepts of Pareto algebra can be used to provide solutions for run-time adaptation problems. Two specific parameterized and compositional run-time adaptation solutions for Chip MultiProcessors (CMPs) and Wireless Sensor Networks (WSNs). The parametrization allows a trade-off between the quality of the result and the required computational resources. Compositionality ensures scalability of the solutions.

Seminar at ST-Ericsson, Netherlands
Invited talk: "Dataflow Analysis Revisited"
February 19, 2009, Eindhoven, Netherlands
Speaker: Twan Basten
Twan Basten gave a talk covering throughput and buffer analysis techniques for dataflow models, including parametric and scenario-aware techniques for throughput. The dataflow model of computation provides an interesting compromise between expressiveness and analyzability, that allows the use in a compilation flow for multiprocessor systems-on-chip that is able to cope with the increasingly dynamic nature of modern multimedia systems.

Conference: IEEE MASCOTS, Imperial College London
Keynote lecture: "Time for a change!"
Speaker: B.R. Haverkort
September 21-23, 2009, London
Boudewijn Haverkort gave a keynote address in which he discusses the achievements of 25 years of research in the area of model-based performance evaluation of computer and communication systems; what has been reached, but foremost, what has not been reached yet and what should be worked upon in the future.

Fall school: IPA Fall Days on Quantitative Methods for Embedded Systems
Invited tutorial: "Predictable Wafer Scanner Design"
Speakers: B.D. Theelen (J.P.M. Voeten, T. Hendriks, J. Schuddemat)
November 23-27, 2009, Noordwijk, Netherlands
Bart Theelen presented a case study performed at ASML, where formal performance modeling methods have been applied to identify bottlenecks in a critical subsystem of ASML's wafer scanner. The methods also helped in proposing various improvements to this subsystem.

Fall school: IPA Fall Days on Quantitative Methods for Embedded Systems
Invited tutorial: "A Performance Analysis Tool for Scenario-Aware Streaming Applications"
Speakes: B.D. Theelen
November 23-27, 2009, Noordwijk, Netherlands
Bart Theelen presented a model checking approach for computing the performance of dynamic dataflow models. The approach covers various types of worst/best-case and average-case performance metrics and relies on a very efficient generally applicable state-space reduction technique.

Symposium: ESI Symposium
Invited talk: "Model-Based Testing applied to an Electronic Passport"
8 December 2009, Eindhoven, Netherlands
Speaker: Jan Tretmans
Jan Tretmans gave a talk outlining the ideas and principles of model-based software testing. An an application he demonstrated how model-based testing was applied to the new electronic passport leading to fully automatically generated tests performing over 1,000,000 protocol steps on an actual passport.

Summer school: Ecole Jeunes Chercheurs en Programmation
Invited tutorial: "Software Testing"
Speaker : Jan Tretmans
June 3-12, 2009, Dinard/Rennes, France.
Jan Tretmans gave a one-day tutorial on software testing divided into two parts. The first part was devoted to general principles and the state of practice in software testing. The second part concentrated on the theory of model-based testing and how models of software can be used to algorithmically generate test suites.

Workshop: Chess IPS TechnoSessie
Invited talk: "Model-Based Testing applied to an Electronic Passport"
Speaker: Jan Tretmans,
October 20, 2009, Haarlem, Netherlands
Jan Tretmans presented the ideas and principles of model-based software testing where a specification model is used to automatically generate test cases. An an application he demonstrated how model-based testing was applied to testing the new electronic passport leading to fully automatically generated tests performing over 1,000,000 protocol steps on an actual passport.

Workshop on FP7 STREP Quasimodo at FMweek
Invited talk: "Model-Based Testing of Embedded Systems"
Speaker: Jan Tretmans
November 6, 2009, Eindhoven, Netherlands
Jan Tretmans presented the ideas and principles of model-based software testing where a specification model is used to automatically generate test cases. As an example he discussed conformance testing of an access protocol of a wireless sensor network. This presentation was part of a series of three presentations where the wireless sensor network itself, the verification

of the access protocol using model checking, and model-based testing of the access protocol were presented.

Workshop: Thales IVV Workshop
Speaker: Jan Tretmans
Invited talk: "Model-Based Testing"
March 16, 2009, Hengelo, Netherlands
Jan Tretmans presented the ideas and principles of model-based software testing where a specification model is used to automatically generate test cases, positioning model-based testing in the context of other model-based activities, such model-checking, model simulation, model analysis, model construction through process mining, etc.

Workshop on FP7/STREP Quasimodo at FMweek
Panelist: Jeroen Voeten
November 6, 2009, Eindhoven, Netherlands
The pannel discussed in what way industries could benefit best from the scientific innovations in quantitative formal methods.

Symposium: ESI Symposium
Invited talk: Performance and Flexibility for ASML Execution Platforms
8 December 2009, Eindhoven, Netherlands
Speaker: Jeroen Voeten

Jeroen Voeten presented a model-based performance prediction and optimization approach and its application to a performance-critical subsystem of an industrial wafer scanner.

-- The above is new material, not present in the Y1 deliverable --

4. Overall Assessment and Vision for the Transversal Activity

4.1 Assessment for Year 2

The level of energy at the CPS Forum and the SEEC09 meetings was excellent. In SEEC09 the change from Nomadic to Energy Efficient Building proposed in 2008 had a re-sounding success. This theme seems to be of increased interest to the European community in response to energy conservation concerns. In this respect, a detailed plan was drafted for meetings to be held in 2010 and a modus operandi that included international interaction. The meetings were very well attended (the CPS Forum had more than 500 attendants and the SEEC09 workshop reached max capacity) and strong positive feedback was received also from some of the companies involves. The funding model of a NoE does not allow substantial research work to be carried out under ArtistDesign umbrella. Most of the actual research is sponsored by other means. The meeting organization and support is indeed the only leverage we can utilize to direct researchers towards a common goal. However, the budget restrictions posed by the rules used for ArtistDesign force a continuous quest for additional resources. The budgeting process should be made more liberal in terms of support.

4.2 Overall Assesment since the start of the ArtistDesign NoE

The overall assessment is in line with Section 4.1 except that the workshop organizations run more smoothly as we learned better how to operate to obtain maximum results from a limited amount of resources. If we project in the future, we believe that the transversal activities can indeed play a fundamental role in ArtistDesign overall goals and as such, they should be strengthened.

4.3 Indicators for Integration

The indicators of integration are related to partners meetings with industry as well as joint papers with industrial participants. In the description of work we indicated meeting and workshops within the automotive, avionics, health-care and nomadic domains and in special sessions in conferences. Both have been achieved: In chronological order.

1. The CyberPhysicalSystem meeting in San Francisco was attended by ArtistDesign Partners who also presented and participated in the discussion. The presence of NSF representatives and EU ones was instrumental in aligning the research priorities across the Ocean, an important goal of the ArtistDesign community at large.
2. The Trento meeting put together the representatives of the energy efficient building industry with the ArtistDesign partners. In that meeting, the desire by industry to be involved was clearly articulated thus demonstrating the need to have a strong industrial program in ArtistDesign. This meeting is the first of a series of operational meetings intended to foster ideas in integration of design flows and energy efficiency policies.
3. The WSS09 meeting was a technical meeting intended to explore the impact and future outlook of software synthesis. Software design is at the core of the agenda of ArtistDesign and we believe it will have a major impact on the future of the industry. In particular, the presence of Mathworks and dSpace and their presentations gave an important input to the research community.

In addition, there have been quite a large number of joint papers with industrial partners addressing design flow issues. In particular, automotive design flows were examined by a number of different teams and compared in a special issue of the IEEE Transactions on CAD that collected the best papers of the ArtistDesign organized special day at DATE 08 thus demonstrating the continuity of the program.

4.4 Long-Term Vision

The industry-motivated transversal activity necessitates additional care as on one hand, we need to understand the concerns of companies that have been investing substantially in embedded system design such as the ones in automotive and aerospace domains; on the other hand, we need to understand the characteristics of emerging domains such as independent living and health, energy efficient buildings and nomadic. In the emerging sectors, the links among the different players are not clear as yet when we look at the promises of these markets. We believe that the activity in the more traditional segments will continue along a journey that has begun several years ago and we do not expect major surprises in corralling the industrial participants as well as the ArtistDesign partners. The emerging sectors represent significant new opportunities to impact the formation of new business models and approaches. We expect that the ArtistDesign community will have to dig deep into its accumulated expertise and into its research network to help industry find its path to profitable products and services.

5. Work Related to the Joint Programme of Integration Activities (JPIA)

5.1 Joint Technical Meetings

Meeting: Workshop: CyberPhysical Systems Forum, CPS Week

San Francisco, April 15, 2009

Objectives for the meeting:

The Cyber-Physical System Forum is the second edition of the event following the successful first edition held in St Louis, MO, in 2008 also co-sponsored by COMBEST. The Forum was held during the CPS week in San Francisco and was organized with the NSF and COMBEST sponsorship joint with the ArtistDesign NoE. The forum was structured into three panels addressing different aspects and challenges related to the design of cyber-physical systems. The objective was to **define with more clarity the research agenda** and how **to set up a sustained, multi-year research program with strong collaboration between the European and the US Community**. In particular, for each of the panel, there was one presenter from the European community either from Combest or from ArtistDesign.

Organizers: Bruce Krogh (CMU), Raj Rajikumar (CMU), Alberto Sangiovanni-Vincentelli (Berkeley, Trento).

Other participants: There were about 500 participants and 12 speakers, the European speakers (Alberto Sangiovanni Vincentelli, Christoph Kirsch, Karl Erik Arzen and Albert Benveniste) were all ArtistDesign Partners. In the participant list all or almost all ArtistDesign partners were represented.

Conclusions After the presentations, during the reception following the meeting, there was a a general consensus among the participants about the relevance of the field, research needs and the necessity to form joint teams among industry and academia **in Europe and US** for CyberPhysical Systems that are now a priority of NSF and of the Obama computing program. In particular, issues related to education and use of the results of the technology in novel application spaces were identified as crucial for the future of the field in general. Since then, NSF started a major research program:
http://www.nsf.gov/publications/pub_summ.jsp?ods_key=nsf08611
"*Congruent with the recommendations in the August 2007 report of the President's Council Scienceand Technology (PCAST), Leadership Under Challenge: Information Technolo Competitive World,NSF's Directorates for Computer and Information Science and Engineeri Engineering (ENG) arespear-heading the Cyber-Physical Systems (CPS) program because and technological importance as well as its potential impact on grand challenges in a nun critical to U.S. security and competitiveness, including aerospace, automotive, chemical p infrastructure, energy, healthcare,manufacturing, materials and transportation. By abstra particulars of specific applications in thesedomains, the CPS program aims to revea fundamental scientific and engineering principles that underpin the integration of cyber and ph across all application sectors*."

ArtistDesign partners continue being involved in the initiative with the intent of bridging the two research communities on the fundamental themes outlined in the ArtistDesign research

agenda. We expect that in the third edition of the CPS week to be held in Stockholm April 12-16, 2010 (http://www.cpsweek2010.se/web/page.aspx?pageid=57517) the involvement of ArtistDesign partners will be even more visible and we expect to present some of ArtistDesign achievements in that forum.

http://varma.ece.cmu.edu/CPS-Forum/index.html

Meeting: Workshop: Smart and Efficient Energy Council SEEC-09,

Trento, October 8-9, 2009.

Objectives for the meeting: The goal of the workshop was to discuss energy efficiency as a major contributor to the green economy. Data shows that alternative sources alone are insufficient to meet the increasing energy demand. Higher efficiency is therefore required to address the energy problem and to reduce the carbon footprint resulting in better environmental conditions. Many new initiatives for energy efficiency are afoot worldwide. The Workshop was intended to provide a forum where various initiatives were presented and discussed, results presented and open problems introduced. Emphasis was on addressing the problem from a system standpoint with deep discussions about the role of embedded systems and embedded control and relationship between Industry, Government and Academia. There was a wide participation from industry (22 out of the 78 participants, and 8 out of 15 presentations were from industry). In particular, there was a continuous interaction among the participants during break time to define follow-up activities in EU projects and continuation of the workshop.

The agenda was based on a two day event where ample time for discussions was allowed.

Organizers: Alberto Sangiovanni Vincentelli (UC Berkeley and Trento), Roberto Passerone (Trento)

Other participants: There were 78 participants of whom 27 were representing ArtistDesign partners (CEA, University of Trento, University of Bologna, TU Braunschweig, Politecnico di Milano, Politecnico di Torino, University of Verona, Scuola di Sant'Anna, TU Dortmund, CEA, University of Twente, and TU Denmark). 22 were industrial participants working in international corporations (UTC, Honeywell, Siemens, Fiat, Telecom Italia, ENEL) or in SMEs (Evidence, Optoelettronica, Yogitech, FARSystems, RDSystems, Gruner, Renience,SOFCPower, Fortiss). The participants and the presentations of the meeting are available on the ArtistDesign Web site. The meeting was very well received by the participants. Prof. Morari, Chair of EE of ETH, pointed out that this was probably the best workshop in years he participated to. This point of view expressed in the closing session of the meeting was echoed by most other participants.

Conclusions:
After the two-day presentation, there was a a general consensus among the participants about the relevance of the field, research needs and the necessity to form joint teams among industry and academia in Europe and across the Ocean to provide critical mass for a game changing approach to energy efficiency.
Energy-efficient smart buildings in particular were considered to be an area where there is an exponentially growing interest for traditional industry such as construction, HVAC, monitoring and energy optimization as well as ICT industry. During the meeting, it was emphasized that the key to efficiency is the use of advanced embedded system techniques including wireless sensor networks and embedded controllers. The European Community has started a fairly large effort in this area as documented by the November call of ICT in Framework 7 and the

US has declare the energy efficiency area as a top priority. There was an agreement among participants to make the conclusions of the meeting widely known via a Press Release and a special issue in a Journal to be determined. There was also an intense discussion about a major collaborative US-European program and a project was drafted to be presented to NSF, the Department of Energy, and the EU community. Several participants are collaborating to present a joint proposal to the EU. There was an explicit request by the participants to have a follow-up meeting in one year time frame. Some of the participants had strong interest in how to drive legislation, regulations and standards to favour energy efficiency. There was a mandate to organize a workshop/meeting with the same sponsorship involving Government, law, economics and engineering experts to discuss this important point. The European Institute of Technology call in the Energy and ICT fields were discussed and it was hoped that the ArtistDesign community would participate to define the technical agenda of the two Institutes once they will be assigned (January 2010).

http://www.artist-embedded.org/artist/SEEC-09.html

Meeting: Workshop*:* Workshop on Software Synthesis - WSS'09

October 16th, 2009, Grenoble, France (within ES Week)

Objectives for the meeting: An increasing amount of software is not written manually any more. Rather, software is synthesized from abstract models of the required functionality. As a result, the effort of generating software is reduced and software verification typically becomes easier. Software synthesis has been implemented in various disperse communities. The workshop aims at bringing these communities together and at identifying research problems which should be addressed by the scientific community.

Organizers: Peter Marwedel (Tu, Dortmund), Alberto Sangiovanni Vincentelli (Trento and UC Berkeley)

Other Participants: There were about 20 attendants mostly from ArtistDesign partners. The speakers were Ed Lee from UC Berkeley substituting for Alberto Sangiovanni Vincentelli, Karl-Erik Arzen (Lund), Emmanuel Roy (Mathworks), Markus Gros (dSpace), and Paul Caspi (Verimag).

Conclusions: The participants to the final panel discussed the status of the field and its potential directions.

Emmanuel Roy (Mathworks):

- Better bridge gap between algorithmic components and true software
- Mathworks: Better distribution to the processors in the network. e.g. in a car.

Christian Fabe (CEA):

- How to make sure that 1000 people can work on the same project?

Peter Marwedel (TU Dortmund)

- This is consistent with Markus Gros' (dSpace) view that handling of large scale models is a problem.

Tetsuya Tohdo (Denso):

- Look at the future, SOA for automotive? How to guarantee security?

Edward Lee (UCB):

- SOA too much rooted in OO-design, no time, no concurrency
- a single language will not work

Christian Fabe (CEA):

- At least a single intermediate representation should be there.

Paul Caspi (IMAG):

- Faithfulness is important, if you don't have it, you have lost the advantage of model-based design.

Edward Lee (UCB):

- If you have a way of encapsulating components, you achieve this.

Reinhard von Hanxleden (U. Kiel):

- Raise the level at which compiler writers are working.

http://www.artist-embedded.org/artist/Scope.html

Meeting: Workshop: ArtistDesign WP6 Cluster Meeting (*Activity 6.2 Platform and MpSoC Analysis)*
Braunschweig, Germany – June 25/26 2009

Objectives for the meeting: While the main objective of this meeting was a mutual update on the joint research progress of the WP6 cluster participants, speakers from the relevant industrial domains traditionally join.

Organizer: Rolf Ernst (TU Braunschweig)
Other participants: Matthias Gries, Gregor Stellpflug (Intel Labs), Nico Feiertag, Kai Richter (Symtavision), Fabian Wolf (Volkswagen)

Conclusions: The meeting has highlighted key problems in the design and analysis of upcoming embedded systems and suggested solutions in different stages of maturity. Topics included performance analysis, reliability, adaptivity, and early design space exploration. The industrial speakers have contributed talks about timing analysis in automotive applications. The meeting has shown that formal methods as developed in this project are increasingly adopted in the industrial design practice.

https://webmail.ida.ing.tu-bs.de/twiki/bin/view/Main/ArtistDesignClusterMeeting

Workshop: 2nd Annual ICES Conference Stockholm,

Sweden, Sept. 2nd, 2009

The conference celebrated the first year anniversary of the KTH based centre for Innovative Embedded Systems – ICES. The overallgoal of the conference was for ICES representatives from industry and KTH to present the drivers for ICES and accomplishments during the first year, as well as ICES vision, goals and concrete activities, including an inventory of Embedded Systems at KTH.

75 people from academia, industry, funding agencies and the press took part in this conference at the Norra Latin Conference Centre in Stockholm. The purpose of this all day conference was to present trends and challenges in embedded systems design, verification, architecting and integration from industrial and scientific viewpoints. The theme was addressed by a program including:

- A keynote talk by Prof. Werner Damm (Offis)
- Invited presentations from industry and KTH
- Presentations of ICES visions, goals, activities and accomplishments,
- addressing these challenges
- An exhibition, presenting ICES-related research projects, education
- and industrial products
- A panel debate discussing how to meet the challenges.

The Keynote Talk described trends and challenges from the viewpoint of the transportation sectors: Automotive, Aerospace and Railway. The three transportation domains share the need to develop advanced embedded systems to meet societal demands for increased mobility and accident reduction while reducing environmental load (CO2 emission and energy consumption) and maintaining high safety levels in spite of increasing traffic density and increased systems complexity. The domains are facing a highly competitive market and faces constraints imposed by (forthcoming) safety standards such as ISO CD 26262, Do178 B/C, CenelecEN 50128/50129, IEC 61508. Achieving continuous cost reduction, performance improvement and efficiently dealing with verification/certification will continue to be a challenge and a key focus in the domains. Werner Damm illustrated research efforts in the area by describing the SPEEDS and CESAR European projects, and their work to develop powerful and efficient supporting methods and tools for the development of safety critical embedded systems.

Invited industrial talks were given by:

- Micronic - addressing challenges in introducing model-based engineering into industrial development,
- Prevas - discussing challenges in embedded systems processes and testing with examples taken from the telecom and automotive domains, and
- Stoneridge in developing future human machine interfaces.

The KTH talks included overviews of trends and challenges in electronic computing platforms (multicore, terascale computing), wireless communication and automous robots.

http://www.kth.se/itm/centra/ices/ices-events/previous-events/1.44090?l=en_UK

Meeting : **Workshop: ICES Seminar: Platform Based Development in Practice**

Stockholm, Sweden, March 31, 2009

The ICES seminar “Platform Based Development in Practice” took place at ABB Corporate Research’s facilities in Västerås on Tuesday 31st March. The goal was to present Platform Based Development (PBD) from different angles and share experiences over domains.

About 50 people attended the seminar, around 10 of whom were from companies/institutions which are not (yet) ICES members. The seminar started with a Welcome from ICES Board member Jan-Erik Frey (ABB) and an introduction by ICES Director Martin Törngren (KTH) who discussed among other things the terminology around Platforms, in order to create a common understanding of the different concepts.

Speakers from ABB, ÅF, Enea and Microsoft presented their viewpoints on PBD, and gave the audience a good insight into both domain-specific issues as well as more general aspects such as organizational issues and impact on development time and cost.

After lunch and a demonstration of a new concept for wireless vibration monitoring on oil-platforms, Johannes Helander, a chief architect from Microsoft gave an inspiring presentation and shared his view of future development methods of embedded platforms.

In conclusion, PBD still remains a challenge in many respects. Design of embedded sytems platforms requires considerations over a large range of system variants including both software and hardware. Moreover, PBD poses a great challenge for testing, where the variability of products increase the state space.

http://www.kth.se/itm/centra/ices/ices-events/previous-events/1.36723?l=en_UK

Meeting: Workshop: ICES Seminar on Testing and verification

Stockholm, Sweden, Feb. 12, 2009

The ICES seminar on testing and verification was hosted by Scania in Södertälje. The seminar had about 55 participants representing a good blend of industrial domains (automotive, telecom, automation) and academic researchers.

The invited talks presented testing from several viewpoints, including safety standards; organizational integration and culture; process integration; and continuous improvement, as well as testing techniques. One of the conclusions from the seminar was that there are needs for improved education and intensified research in the area of testing. For industry, logging their performance and learning, was emphasized as a key point.

http://www.kth.se/itm/centra/ices/ices-events/previous-events/1.33317?l=en_UK

Meeting: Workshop: ICES-VINNOVA European Research Seminar, 28th January 2009

Stockholm, Sweden, January 28th, 2009

In collaboration with Vinnova (the Swedish governmental Research and Innovation Agency), KTH arranged a seminar on Themes, forms and funding relating to European research. The seminar arouse from the need to better disseminate opportunities for research on the European level, and to discuss similarities and differences among ITEA2, Artemis and FP7.

Around 45 people attended the ICES-VINNOVA open seminar "European Research in Embedded Systems: Themes, Forms and Funding", which took place at KTH on 28th January 2009.

The seminar was very successful, with interesting presentations, questions and discussions. The details of the ITEA2 (invited presentation by Rudolf Haggenmueller), FP7 (invited presentation by Philippe Reynert) and ARTEMIS (invited presentation by Alun Foster) programs were explained, including rationale and the directions for the current calls. Vinnova also presented the Swedish funding and support available.

In addition, industrial experiences and viewpoints were presented. A lot of the discussion focused on the relations between the programs and when to choose which. Among the conclusions, an overview of the current large project portfolios was called for.

http://www.kth.se/itm/centra/ices/ices-events/previous-events/1.32246?l=en_UK

Meeting : SMECY Project Proposal Face-to-Face Meeting
Paris, France - 2009-06-25
Objectives for the meeting: The goal of this meeting was to discuss the SMECY project proposal for "Smart Multicore Embedded Systems", which addresses the ARTEMIS Joint Undertaking Call 2009. The project envisions new programming technologies that enable the exploitation of many-core architectures in embedded systems.

Organizer: Francois Pacull (CEA), Ahmed Jerraya (CEA)
Other participants: Jonas Diemer (TU Braunschweig), Francois Pacull (CEA), Ahmed Jerraya (CEA), Joseph Sifakis (IMAG), Gilbert Edelin (Thales), and others (from over 20 institutions in total).

Conclusions : As a result, the 44 participants from industry and academia submitted the SMECY project proposal to the ARTEMIS JU. The project ranked high and was invited to funding negotiations, which are ongoing.

ArtistDesign Workshop on Embedded Systems in Healthcare 2009

Eindhoven, the Netherlands -- December, 7, 2009.
Objectives for the meeting: The goal of the Workshop on Embedded Systems in Healthcare is to strengthen the connections between academic research and industry, or to be more precise, to increase the understanding in the academic world of industrial issues in embedded systems engineering and together come to a shared agreement on research directions that seem worthwhile to pursue.
Organizers: Boudewijn Haverkort (ESI), Pierre America (Philips Research & ESI), Piërre van de Laar (ESI), Miranda Willems (ESI), Roland Mathijssen (ESI).

The speakers at the workshop work at different medical companies or are participants in the ArtistDesign network with extensive experience in healthcare. The topics include "How to design long lasting devices for a fast changing world?", "Cochlear Implant Systems: today's challenges in embedded firmware design", and "Embedded Contributions to an Intensive Care Safety Concept".
http://www.artist-embedded.org/artist/Overview,1831.html

SafeTRANS Industrial Days

Stuttgart, Germany, May 5, 2009 and Friedrichshafen, Germany, November 19, 2009

Within the context of SafeTRANS (including ArtistDesign members) two Industrial Days were organized in 2009. These workshops provide a platform for discussion and exchange of experiences in industry across application domains.

The first one on "Safety Management along the suppliers chain" was held in May 2009 in Stuttgart at Robert Bosch GmbH. Presentations from different application domains (avionics, automotive, rail) were given covering requirement management, development process in the context of ISO 26262, safety management in the development of safety critical rail systems as well as aspects of systems integration.

The second workshop took place on November 19 in Friedrichshafen at EADS on "Model-based testing and test automation". Presentations from industrial participants (Ford, Daimler, EADS, Siemens Validas) and academic participants cover verification of safety critical

automotive applications, deployment of model-based technologies to industrial testing, model-based testing for critical functions on architecture level – vision, concepts and way forwards in aeronautical engineering, Domain specific modeling and generation of test cases, model-based testing, risk oriented testing.
http://www.safetrans-de.org/de_6_Industrial_Day.php
http://www.safetrans-de.org/de_7_Industrial_Day.php

-- The above is new material, not present in the Y1 deliverable --

5.2 Staff Mobility and Exchanges

Visiting researcher : PhD, Lei Feng(Volvo)
Team visited: KTH led by Martin Törngren (KTH)
Approximate cost for travel and lodging: 2000 €
Reason for the visit: Since the spring 2009, Lei Feng, formerly a post-doc at KTH, started to work at Volvo. To maintain the cooperation, Lei spent two weeks at KTH during the spring.
Conclusions/objectives reached: To further strengthen the collaboration, it was decided that Lei would be employed 50% time at Volvo and 50% time at KTH, acting as a shared post-doc. During the autumn 2009, this has proven promising as a way to provide a bridge between KTH and Volvo.

-- The above is new material, not present in the Y1 deliverable --

5.3 Tools and Platforms

5.3.1 Tool or Platform: SymTA/S

Objectives

SymTA/S is a tool for the development and verification of embedded multiprocessor real-time systems. The existing technology is mainly suitable for event or time-driven systems with message passing as the main task interaction. The tool shall be extended to cover the timing implications of multicore processors, or multiprocessor-systems-on-chip.

Main Results

In several previous projects (funded by german DFG, “Sureal”, funded by german BMBF, ARTIST2, and others), the compositional analysis approach has been transferred into a tool framework which is now also commercially available. The available modelling options capture typical problems in todays automotive systems (CAN bus utilization, end-to-end deadlines,…). This addresses a growing need for formal methods in the industry. The topics currently under research (see below) address future problems which can be expected to become of increasing industrial interest in the future.

Current work

The research version of the tool framework is currently being developed into several new directions: Modeling of shared resources for multiprocessor-system-on-chips (see ArtistDesign Activity 6.2: Platform and MpSoC Analysis), the modelling of hierarchical event models (in the scope of the COMBEST project), the demonstrator platform for adaptive systems (see ArtistDesign 7.1: Design for Adaptivity), and the reliability analysis (as presented in Section 3.1 Technical Achievements of the Industry-driven integrtation activity 7.3). Besides the extension of the applicability into new domains driven by industrial applications, a major focus within ArtistDesign is the synergetic coupling of tools, as well as the corresponding development of models.

Participating partners:

- TU Braunschweig.

  TU Braunschweig investigates synergies in the coupling of methods and implements prototypical implementations of the research results.

- Symtavision GmbH.

  Symtavision is the commercial co-developer of the tool framework. A focus within ArtistDesign is the coupling of with other industrially available tools (such as aiT).

- ETHZ.

  Collaboration on the coupling of MPA and SymTA/S with respect to modelling of hierarchical event models.

- Absint GmbH.

  The aiT tool supplies task timing models, which are required for system level analysis.

Web

http://www.ida.ing.tu-bs.de/forschung/projekte/symtas/

http://www.symtavision.com/

Related Publications

- Simon Schliecker, Jonas Rox, Mircea Negrean, Kai Richter, Marek Jersak and Rolf Ernst, **"System Level Performance Analysis for Real-Time Automotive Multi-Core and Network Architectures,"***Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 28, No. 7, pp. 979-992, July 2009.
- Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst and Michael González Harbour, **"Influence of different abstractions on the performance analysis of distributed hard real-time systems,"** *Journal Design Automation for Embedded Systems*, vol. 13, No. 1, pp. 27-49, June 2009
- Mircea Negrean, Simon Schliecker and Rolf Ernst, **"Response-Time Analysis of Arbitrarily Activated Tasks in Multiprocessor Systems with Shared Resources,"** in *Proc. of Design, Automation, and Test in Europe (DATE)*, (Nice, France), April 2009

-- Changes wrt Y1 deliverable --

No change.

5.3.2 COSI

Objectives

COSI (Communication Synthesis Infrastructure) is a software framework for interconnect infrastructure analysis and synthesis

Main Results

The framework allows developing specialized flows and tools for communication synthesis as exemplified by the release of COSI-NOC (Communication Synthesis Infrastructure for Network-on-Chips), a software toolkit for the automatic synthesis of synchronous networks-on-chip based on the platform-based design paradigm, and by COSI-BAD, for building automation design.

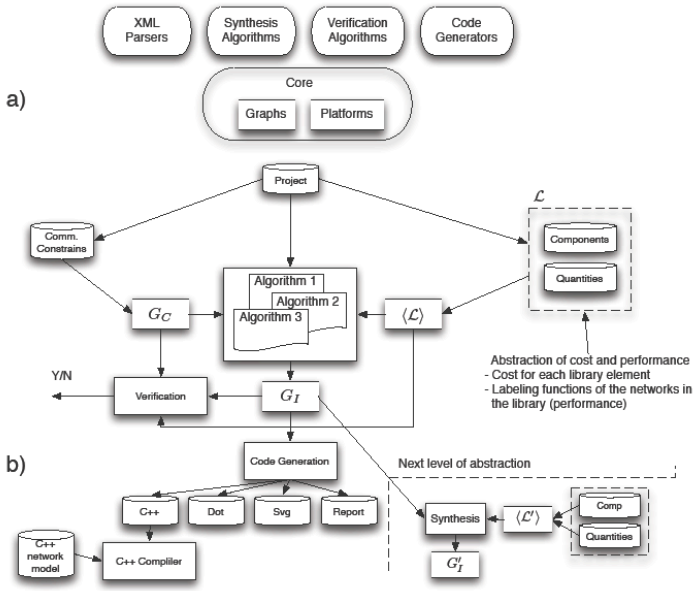


Figure 1. The COSI Platform-Based Design-like structure

	Quantities	CommStructs	Library	Models	Rules	Platforms	Environment	I/O	Algorithms
Core	Ports Bandwidth Flows...	Graphs							ShortestPath Tsp SpanningTree FacilityLocation Kmedian
On-Chip Communication	Interface IpGeometry NodeParam	Specification PltInstance Implementation	Router Link Bus	Ho-Area Ho-Power Orion	Critical length Deadlock	RouterLink BusNoc	Rectangle	Parsers SvgGen Parquet interface SyscGen	DegreeConstrained LatencyConstrained Hierarchical
Building Automation	Interface NodeParam Threads	Specification PltInstance Implementation	Sensor Actuator Controller TwistedPair	TokenRing 802.15.4	WiringRule NodePosition	DaisyChain TreeWireless	Walls CableLadder	BuildingParser SvgGen Desyre interface	DaisyChainPartition WirelessTree

Figure 2. How the COSI framework has been used to generate specific synthesis tools.

Current work

We continue to work towards expanding COSI capabilities, including better models for router delays, bus models, and support for the generation of synthesizable RTL description of the synthesized on-chip interconnection network. In this domain, we are integrating Metro with COSI. Meanwhile, we also plan to continue our work on the extension of the communication synthesis approach to the design of large-scale network for distributed embedded systems such as those that can be found in smart buildings and to airplane power distribution.

Participating partners:

- **Trento**
  Setting the directions of the framework. Methodology and theory. Integrating COSI with Metro.
- **UC Berkeley**
  Tool development and application to Network on Chip and intelligent buildings
- **Columbia**
  Participation in the development of the methodology.
- **UTC**

  Application to intelligent buildings and avionics.

Web
http://embedded.eecs.berkeley.edu/cosi/

Related Publications

[PCSV08] A. Pinto, L. Carloni and A. Sangiovanni Vincentelli, COSI: A Framework for the Design of Interconnection Networks, IEEE Design and Test of Computers, vol. 25, n. 5, Sept-Oct. 2008, pp. 402-415.

[PCVS09] A. Pinto, L.P. Carloni, and A. Sangiovanni-Vincentelli. "A Methodology for Constraint-Driven Synthesis of On-Chip Communications," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 28, No. 3, March 2009.

-- Changes wrt Y1 deliverable --

No change.

5.3.3 Metropolis and Metro II

Objectives

System-Level Design (SLD) means many different things to many different people. In our view, system-level design is about the design of a whole that consists of several components where specifications are given in terms of functionality with additional:

- constraints on the properties the design has to satisfy and on the components that are available for implementation and
- objective functions that express the desirable features of the design when completed.

This definition is general since it relates to many different application domains, from semiconductors to systems such as cars and airplanes, buildings, telecommunication and biological systems. To deal with system-level problems, our view is that the issue to address is not developing new tools, albeit they are essential to advance the state of the art in design, rather it is the understanding of the principles of system design, the necessary change to design methodologies and the dynamics of the supply chain. Developing this understanding is necessary to define a sound approach to the needs of the system and component industry as they try to serve their customers better, to develop their products faster and with higher quality.

Main Results

This contribution was about principles and how a unified methodology together with a supporting software framework, as challenging as it may seem, can be developed to bring the embedded electronics industry to a new level of efficiency. To demonstrate this view, we developed over the years Metropolis, a software framework supporting the methodology and Metro II, a second generation framework built to alleviate the problems we encountered when applying Metropolis to industrial test cases.

Current work

We are integrating this framework with the COSI framework to provide a full communication requirement capture, synthesis, verification and implementation. In parallel, we are interfacing Ptolemy to Metro II to offer a new way of entering designs using the graphical UI of Ptolemy II.

Participating partners:

- **Trento**

  Tool development, application of the framework to a UMTS case study.
- **UC Berkeley**

  Tool development, interface with Ptolemy II
- **Sun Microsystems**

  Application to multi-core development
- **UTC**

  Interface with COSI and application to smart buildings and avionics.
- **National Instruments**

  Industrial development of the ideas put forth by the frameworks
- **Intel**

Application to SoC design and development of architectural models

Web

http://chess.eecs.berkeley.edu/chess/forum/17.html

Related Publications

[DSDP09] D. Densmore, A. Simalatsar, A. Davare, R. Passerone, and A. Sangiovanni-Vincentelli. “UMTS MPSoC design evaluation using a system level design framework”. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE09)*, Nice, France, April 20-24, 2009.

[BDDD09] F. Balarin, A. Davare, M. D'Angelo, D. Densmore, T. Meyerowitz, R. Passerone, A. Pinto, A. Sangiovanni-Vincentelli, A. Simalatsar, Y. Watanabe, G. Yang and Q. Zhu. “Platform-Based Design and Frameworks: Metropolis and Metro II”. In *Model-Based Design for Embedded Systems,* chapter 10, page 259. CRC Press, Taylor and Francis Group, Boca Raton, London, New York, November 2009.

-- Changes wrt Y1 deliverable --

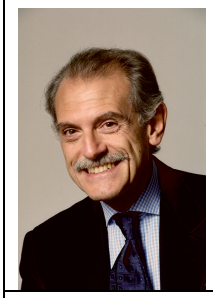
This is a new effort in ArtistDesign.

6. Transversal Activity Participants

-- Changes in the Cluster Participants wrt Y1 deliverable --

Alberto Sangiovanni Vincentelli is now with the University of Trento.

6.1 Core Partners

Transversal Activity Leader **Activity Leader for "Industrial Integration"**	
	Alberto Sangiovanni Vincentelli (Trento) www.eecs.berkeley.edu/~alberto/;
Technical role(s) within ArtistDesign	Bring in Expertise in embedded system modelling, validation, tools and methodologies and IC design. Deep involvement in cooperation with the industry: tools (co-founder Cadence and Synopsys), telecommunications (Telecom Italia), automotive (member of the GM STAB), avionics and energy efficient buildings (UTC)
Research interests	Embedded system design methodologies and tools including modelling, validation, synthesis and formal verification, semantic foundations.
Role in leading conferences/journals/etc in the area	Program Committee Member CODES and EMSOFT. Organizer of SEEC 09 Smart and Efficient Energy Council and of the 2009 CPS Forum Member of the ARTEMIS High-level Group, Governing Board, Public Authority Board and Steering Committee
Notable projects	SPEEDS - Speculative and Exploratory Design in Systems Engineering Provide a semantics based modelling methods with analysing techniques to support the construction of complex embedded systems by composing heterogeneous subsystems together with a speculative tool-supported design process. HYCON NoE: Taming Hybrid Systems Center for Hybrid and Embedded Software Systems

	(CHESS) co-director Gigascale System Research Center, Core theme leader MuSyC, Distributed Sense and Control Systems theme leader COMBEST
Awards/Decorations	IEEE Fellow, Member National Academy of Engineering, Kaufmann Award for pioneering contributions to EDA, IEEE Graduate Teaching Award, Gulliemin-Cauer Award, Darlington Award, Aristotle Award, University of California Distinguished Teaching Award, IEEE/RSE Wolfson James Clerk Maxwell Medal for groundbreaking contributions that have had an exceptional impact on the development of electronics and electrical engineering or related fields, EDAC R. Newton Impact Award

Team Leader	
	Boudewijn Haverkort (Embedded Systems Institute (ESI)) www.esi.nl
Technical role(s) within ArtistDesign	Model-based methods for embedded system engineering; collaborative research with industry
Research interests	Model-driven design and implementation of (embedded) computer-communication systems and the evaluation of their performance, dependability and performability.
Role in leading conferences/journals/etc in the area	Member of IFIP WG6.3 on "performance of communication systems" and of IFIP WG7.3 on "computer performance modelling and analysis" Fellow of the IEEE Member of the editorial board of the journal Performance Evaluation Chair of the steering committee of the IEEE Conference on Quantitative Evaluation of SysTems (QEST); http://www.qest.org/ Chair of the steering committee of the performability evaluation workshop series (PMCCS); http://www.pmccs.net/
Notable past projects	Rocks: Rigorous Dependability Analysis using Model Checking Techniques for Stochastic Systems (DFG/NWO) VOSS I and II: Validation of Stochastic Systems (DFG/NWO)

Team Leader	
	Prof. Dr. Werner Damm (OFFIS) http://www.offis.de
Technical role(s) within ArtistDesign	Bring in Expertise in embedded system modelling and validation. Deep involvement in cooperation with the automotive and avionics industry.
Research interests	His recent research covers foundational research on mathematical models of embedded systems, specification languages, hybrid systems, formal verification methods, and real-time and safety analysis. This is complemented by applied research with industrial partners in avionics, automotive, and train system application. The focus of this research is on enhancing model-based development processes with formal method-based approaches to verification, testing, and safety and real-time analysis, as well as on enabling component-based design for embedded systems.
Role in leading conferences/journals/etc in the area	Program Committee Member CAV2008 Member of the Editorial Board “Formal Methods in System Design” Chairman of the competence cluster SafeTRANS First Chairman of the ARTEMIS Innovation Cluster on Transportation
Notable projects	OMEGA - Correct Development of Real-time Embedded Systems Formal verification of embedded systems based on UML http://www-omega.imag.fr/ AVACS - Automatic Verification and Analysis of Complex Systems This project addresses the rigorous mathematical analysis of models of complex safety critical computerized systems. http://www.avacs.org/ SPEEDS - Speculative and Exploratory Design in Systems Engineering Provide a semantics based modelling method with analysing techniques to support the construction of complex embedded systems by composing heterogeneous subsystems together with a speculative tool-supported design process. http://www.speeds.eu.com/ COMBEST – Component-Based Embedded Systems design Techniques COMBEST will provide a formal framework for component based design of complex embedded systems: 1) formal integration of heterogeneous components; 2) encapsulation of components; 3) prediction of emergent key system characteristics; 4) corresponding certificates. http://www.combest.eu CESAR – Cost efficient methods and processes for safety relevant embedded systems CESAR is an ARTEMIS project which will provide

	innovations within the two engineering disciplines Requirements Engineering and Component-based Design. Furthermore, it will develop a customizable systems engineering "Reference Technology Platform" (RTP) making it possible to integrate or interoperate existing or emerging available technologies. http://www.cesarproject.eu SPES2020 – Software Platform Embedded Systems SPES2020 is a German Innovation Alliance dedicated to model-based design methods for embedded software systems across application domains. http:// www.spes2020.de

	Prof. Dr. Bernhard Josko (OFFIS) http://www.offis.de/
Technical role(s) within ARTIST2	Participating in several activities bringing in the expertise on real-time UML verification
Research interests	Modelling and analysis of embedded systems, formal verification, real-time UML, SysML
Notable projects	OMEGA - Correct Development of Real-time Embedded Systems Formal verification of embedded systems based on UML http://www-omega.imag.fr/ EASIS – Electronic Architecture and System Engineering for Integrated Safety Systems Within WP System Dependability provide formal verification guidelines http://www.easis.org SPEEDS - Speculative and Exploratory Design in Systems Engineering Provide a semantics based modelling methods with analysing techniques to support the construction of complex embedded systems by composing heterogeneous subsystems together with a speculative tool-supported design process. CESAR – Cost efficient methods and processes for safety relevant embedded systems CESAR is an ARTEMIS project which will provide innovations within the two engineering disciplines Requirements Engineering and Component-based Design. Furthermore, it will develop a customizable systems engineering "Reference Technology Platform" (RTP) making it possible to integrate or interoperate existing or emerging available technologies. Leader of sub project “Requirements Engineering” http:// www.cesarproject.eu

Core Teamleader	
	Prof. Dr.-Ing. Rolf Ernst (TU Braunschweig) http://www.ida.ing.tu-bs.de/en/home/faculty_and_staff/ernst/
Technical role(s) within ArtistDesign	Core Teamleader in Platform and MpSoC Design, Platform and MpSoC Analysis, Design for Adaptivity, Integration Driven by Industrial Applications. Affiliated Teamleader in Design for Predictability and Performance
Research interests	Research interests include embedded architectures, hardware-/software co-design, design automation, real-time systems, and embedded systems engineering.
Role in leading conferences/journals/etc in the area	Rolf Ernst chaired major international events, such as the International Conference on Computer Aided Design of VLSI (ICCAD), or the Design Automation and Test in Europe (DATE) Conference and Exhibition, and was Chair of the European Design Automation Association (EDAA). He is a founding member of the ACM Special Interest Group on Embedded System Design (SIGBED), and was a member of the first board of directors. He is an elected member (Fachkollegiat) and Deputy Spokesperson of the "Computer Science" review board of the German DFG (corresponds to NSF). He is an advisor to the German Ministry of Economics and Technology for the high-tech entrepreneurship program EXIST (www.exist.org).
Awards / Decorations	In 1995 he received the Jorck's Foundation Research Award for his research in hardware/software codesign

Team Leader	
	Dr. Stylianos Mamagkakis IMEC vzw. http://www.imec.be
Technical role(s) within ArtistDesign	Representing IMEC Nomadic Embedded Systems (NES) division in: -Cluster: SW Synthesis, Code Generation and Timing Analysis -Cluster: Operating Systems and Networks -Cluster: Hardware Platforms and MPSoC Design -Intercluster activity: Design for Adaptivity -Intercluster activity: Design for Predictability and Performance -Intercluster activity: Integration Driven by Industrial Applications
Research interests	Stylianos Mamagkakis received his Master and Ph.D. degree in Electrical and Computer Engineering from the Democritus Uni. Thrace (Greece) in 2004 and 2007, respectively. Since 2006, he coordinates a team of PhD students within the NES division at IMEC, Leuven, Belgium. His research activities mainly belong to the field of system-level exploration, with emphasis on MPSoC run-time resource management and system integration.
Role in leading conferences/journals/etc in the area	Stylianos Mamagkakis has published more than 35 papers in International Journals and Conferences. He was investigator in 9 research projects in the embedded systems domain funded from the EC as well as national governments and industry.
Notable past projects	Project leader of MNEMEE IST project www.mnemee.org Project leader of OptiMMA IWT project www.imec.be/OptiMMA Participation in: 1 international IMEC project (M4), 3 European IST projects (AMDREL, EASY, ARTIST2), 2 Greek projects (PRENED, DIAS)
Awards	1st prize in 'Technogenesis' Competition for Business Innovation, Greece, June'06 3rd prize in 'Otenet Innovation 2006' Competition for Business Innovation, Greece, November'06
Further Information	http://www2.imec.be/imec_com/nomadic-embedded-systems.php

Cluster Leader **Activity Leader & Team Leader**	
	Jan Madsen (Technical University of Denmark)
Technical role(s) within ArtistDesign	Member of the Strategic Management Board Leads Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Leader of the JPRA Activity: “Platform and MPSoC Analysis”
Research interests	Research interests include high-level synthesis, hardware/software codesign, System-on-Chip design methods, and system level modeling, integration and synthesis for embedded computer systems.
Role in leading conferences/journals/etc in the area	Program Chair and Vice-Chair of Design Automation and Test in Europe Conference. Tutorial Chair and Special Sessions Chair of Design Automation and Test in Europe Conference. General Chair, Program Chair and Workshop Chair of CODES+ISSS Conference Member of the editorial board of the journal “IEE Proceedings – Computers and Digital Techniques” Member of the technical program committee and organizing committee of several technical conferences, including the Design Automation and Test in Europe Conference, the Real-Time Systems Symposium, the Symposium on Hardware-Software Codesign, and the International Workshop on Applied Reconfigurable Computing. Danish delegate in the Governing Board of ARTEMIS JU
Awards / Decorations	In 1995 he received the Jorck's Foundation Research Award for his research in hardware/software codesign

Cluster and Team Leader	
	Prof. Dr. Dr. h. c. Reinhard Wilhelm (Saarland University) http://rw4.cs.uni-sb.de/people/wilhelm
Technical role(s) within ArtistDesign	Timing Analysis
Research interests	Compilers, Static Analysis, Timing Analysis
Role in leading conferences/journals/etc in the area	PC member of SCOPES, LCTES, MEMOCODE, RTSS etc. Steering committee member of EMSOFT, member at large of the steering committee of LCTES Member of the ACM SIGBED Executive Committee
Notable past projects	DAEDALUS
Awards / Decorations	Prix Gay-Lussac-Humboldt in 2007 Honorary doctorates of RWTH Aachen and Tartu University in 2008
Further Information	Co-founder of AbsInt Angewandte Informatik GmbH Scientific Director of the Leibniz Center for Informatics Schloss Dagstuhl

Team Leader **Activity Leader for "Software Synthesis and Code Generation"**	
	Prof. Dr. Peter Marwedel (TU Dortmund) http://ls12-www.cs.tu-dortmund.de/~marwedel/
Technical role(s) within ArtistDesign	Cluster leader, activity leader SW Synthesis and Code Generation Improved code quality for embedded applications is the main goal of the work at Dortmund University. Due to the widening gap between processor and memory speeds, emphasis has been on improving the efficiency of memory accesses, in terms of average and worst case execution time and in terms of the energy consumption.
Research interests	Peter Marwedel's Embedded Systems Group focuses on embedded software. Particular emphasis is on compilers for embedded processors. One of the very first publications in this area, the book "Compilers for Embedded Processors", edited by Peter Marwedel and Gert Goossens, was the result of the CHIPS project, funded by the European Commission. The group's current focus is on advanced optimizations for embedded processors (e.g. by using bit-level data flow analysis) and energy-aware compilation techniques. Current research also includes high-level transformations of algorithms as well as WCET-aware code generation.
Role in leading conferences/journals/etc in the area	Member of the EDAA (European Design and Automation Association) Main Board. Editorial Board Member of the Journal "Design Automation for Embedded Systems" Editorial Board Member of the Journal of Embedded Computing. Editorial Board Member of the Microelectronics Journal. Editor of the Springer series of books on Embedded Systems (http://www.springer.com/series/8563) Co-Founder and Steering Board Chair of the SCOPES Workshop (Software and Compilers for Embedded Systems) Series. >14 years of service for the DATE conference and its predecessors (program chair: 3 times, chairman of the steering committee, European representative to ASPDAC) Various other conferences
Notable past projects	MNEMEE: Memory maNagEMEnt technology for adaptive and efficient design of Embedded systems supported by the European Commission

	(http://www.mnemee.org) PREDATOR: Design for predictability and efficiency, supported by the European Commission (http://www.predator-projekt.eu) MORE: Network-centric Middleware for group communications and resource sharing across heterogeneous embedded systems, supported by the European Commission http://www.ist-more.org HiPEAC: European NoE on High-Performance Embedded Architecture and Compilation; http://www.hipeac.net MAMS: Multi-Access modular-services framework, national project funded by the German Federal Ministry of Education and Research (BMBF)Others: Various earlier projects supported by the EC, DFG etc.
Awards / Decorations	Teaching award, TU Dortmund, 2003 DATE fellow, 2008
Further Information	CEO of the Informatik Centrum Dortmund (ICD), a technology transfer centre founded in 1989. Chair of the Education Committee of TU Dortmund

Team Leader	
	Joseph Sifakis (VERIMAG) http://www-verimag.imag.fr/~sifakis/
Technical role(s) within ArtistDesign	Team Leader for Verimag. Contributes with expertise on component-based design, the BIP framework, platform-aware implementation of embedded systems, structural verification. Context-based analysis.

Team Leader	
	Saddek Bensalem (VERIMAG) http://www-verimag.imag.fr/~bensalem/
Technical role(s) within ArtistDesign	Team Leader for Verimag. Contributes with expertise on compositional modelling and verification

7. Internal Reviewers for this Deliverable

- **Jan Madsen**, Technical University of Denmark
- **Martin Törngren**, KTH
- **Roberto Passerone**, Trento