214373 ArtistDesign
Network of Excellence
on Embedded Systems Design

Project Management Report for Year 2

Executive Summary

Joseph Sifakis – ArtistDesign Scientific Coordinator
Bruno Bouyssounouse – ArtistDesign Technical Coordinator

ArtistDesign Consortium

1. Project Objectives

The ArtistDesign NoE is the visible result of the ongoing integration of a community.

The central objective for ArtistDesign is to build on existing structures and links forged in the ARTIST2 NoE, to become a virtual Centre of Excellence in Embedded Systems Design. This is achieved through tight integration between the central players of the European research community. Also, the consortium is smaller, and integrates several new partners. These teams have already established a long-term vision for embedded systems in Europe, which advances the emergence of Embedded Systems as a mature discipline.

ArtistDesign is becoming the main focal point for dissemination in Embedded Systems Design, leveraging on well-established infrastructure and links. It will extend its dissemination activities, including Education and Training, Industrial Applications, as well as International Collaboration. ArtistDesign will establish durable relationships with industry and SMEs in the area.

ArtistDesign builds on existing international visibility and recognition, to play a leading role in structuring the area.

The research effort aims to integrate topics, teams, and competencies, grouped into 4 Thematic Clusters: “Modelling and Validation”, “Software Synthesis, Code Generation, and Timing Analysis”, “Operating Systems and Networks”, “Platforms and MPSoC”. “Transversal Integration” covering both industrial applications and design issues aims for integration between clusters.

-- Changes wrt Y1 deliverable –

No changes with respect to Year 1.

2. Contact Details and Contractors Involved

2.1 Core Partners

For a complete description including web links, see:
http://www.artist-embedded.org/artist/-ArtistDesign-Participants-.html

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3	RWTH AACHEN	AACHEN	Germany
4	AALBORG UNIVERSITET	AALBORG	Denmark
6	ALMA MATER STUDORIUM - UNIVERSITA DI BOLOGNA	BOLOGNA	Italy
7	TECHNISCHE UNIVERSITAET BRAUNSCHWEIG	TUBS	Germany
8	UNIVERSIDAD DE CANTABRIA	CANTABRIA	Spain
9	COMMISSARIAT À L'ENERGIE ATOMIQUE	CEA	France
10	DANMARKS TEKNISKE UNIVERSITET	DTU	Denmark
11	UNIVERSITAET DORTMUND	DORTMUND	Germany
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32	IST Austria	IST_Austria	Austria
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-- Changes wrt Y1 deliverable –
Replaced Averio with UnivPorto, PARADES with Trento, added IST Austria.

2.2 Affiliated Partners

Affiliated partners play a very strong role in the Spreading Excellence from the core partners to the research and industrial communities at large.

Affiliated partners generally play an active role in the research activities, either participating directly in research, or transferring the results directly to industry.

Each of the JPRA and JPIA activities' deliverables provides the list of the corresponding affiliated partners and roles.

Affiliated Industrial Partners

The complete set of Affiliated Industrial partners, including web links, is available online, here: http://www.artist-embedded.org/artist/-Affiliated-Industrial-Partners-.html

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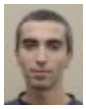
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3. Vision and Assessment of the Work Performed

ArtistDesign finances durable integration between teams and not the concrete elements of the JPA which most often belong to other projects. These specific technical objectives may or may not be attained (this is the essence of research as opposed to development), but we feel that the main product of ArtistDesign is the emergence of a lasting European research community, that has a significantly enhanced capacity for preparing Europe's future.

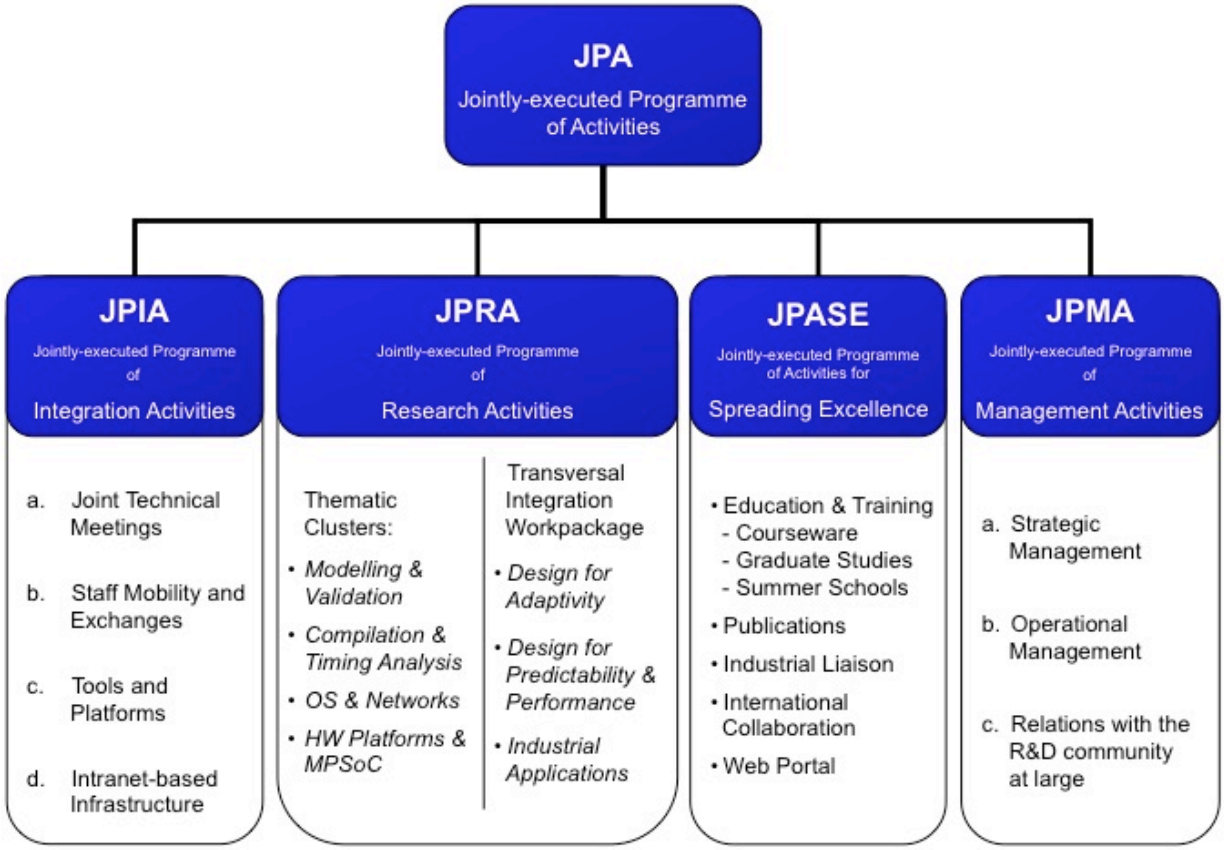
The research is completed by work in the JPIA (Jointly Executed Programme of Integration Activities) workpackage, which aim to transform research results in tangible tools and components, and bring teams closer together on a day to day basis.

We believe that the topics chosen provide a good coverage of the area, for embedded software and systems.

The ArtistDesign NoE is a complex construction assembled from world-leading communities, teams, and individuals. This is certainly an asset, but also a source of complexity in management. Each team has two essential characteristics: world-class excellence and strong interaction with top industrial players. ArtistDesign partners play a leading role in the different communities in embedded systems design, and they advance the state of the art in each of these.

It is difficult to abstract out a global synthesis of the overall technical achievements. This is due to the diversity and the low granularity of the actions to be covered (meetings, publications, attendance at workshops, visits, and platforms).

The following is a certainly non-exhaustive assessment of the work in the Joint Programme of Activities' 4 main branches.



No changes with respect to Year 1.

3.1 Joint Programme of Research Activities (JPRA)

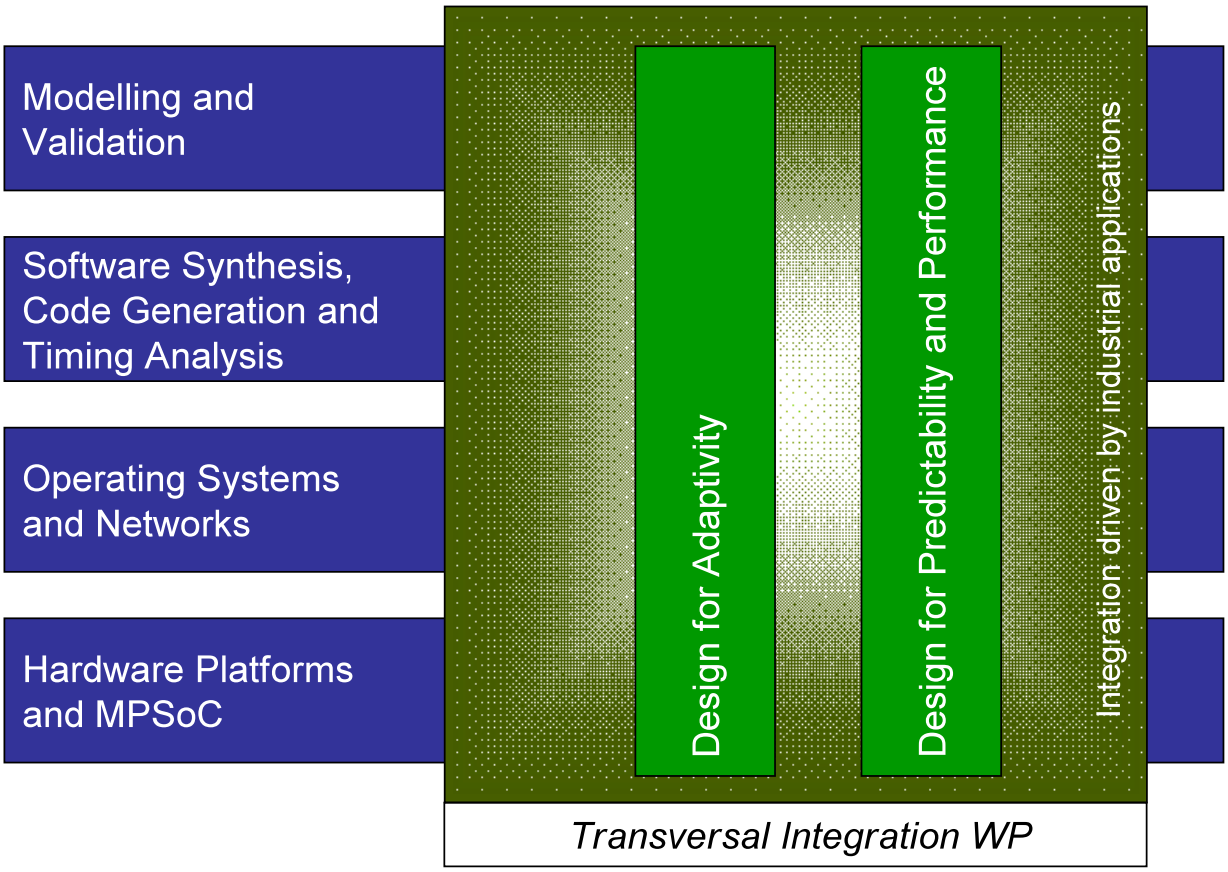
3.1.1 Structure of the Research Effort

The JPRA is composed of intra and inter-cluster research activities on cutting-edge topics in embedded systems design. While the main bulk of financing for these activities is taken up by outside programmes (Integrated Projects, National Programmes, Industrial Contracts, etc), the ArtistDesign NoE finances the extra burden due derived from integrating these into a single coherent research programme.

Thus, the essential ingredient within ArtistDesign is the JPRA, which motivates the participating research teams far more than the actual financing, which is tiny in comparison with the overall research aims. It is completed by the Joint Programme of Integrating Activities (JPIA), and the Joint Programme of Activities for Spreading Excellence (JPASE), and overseen by the Joint Programme of Management Activities (JPMA).

The structure of the research activities reflects the following decomposition of the embedded systems design flow.

This design flow is composed of the following cooperating activities, starting with component-based modelling and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality. Accordingly, we have structured the area of embedded systems design into the following topics.



Modelling and Validation. Unlike other computer systems, embedded systems are strongly connected with a physical environment. A scientific foundation for embedded systems must therefore deal simultaneously with software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based. The overall objective of this activity is develop model and component based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. The activity brings together the most important teams in the area of model and component based design in Europe.

SW Synthesis, Code Generation and Timing Analysis. There is a continuing demand for higher performance of information processing, which stimulates using a growing amount of parallelism (including using multiple processors). This trend affects the design of embedded systems. We address issues related to multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces. Such processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Timing analysis is also affected by the trend toward the new platforms. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Also, timing analysis beyond the single processor is required. Hence, timing analysis will also consider the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors.

Operating Systems and Networks. We investigate how current real-time operating systems have to be extended or modified to support emerging real-time embedded systems characterized by a high degree of complexity, highly variable resource requirements and parallel processing such as multicores. Most embedded systems are often characterized by scarce resources in terms of processing power, memory, space, weight, energy, and cost. Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, whilst guaranteeing isolation properties. Also, to support dynamic applications with variable resource requirements or to cope with unpredictable resource availability, feedback control techniques for resource management at the operating system and application level are also investigated.

Hardware Platforms and MPSoC Design. While hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application environments is much less clear. The consequence is fragmentation: while many research teams are working on one or more of these domains, there is little communication and integration, this leads to duplication of results and overall slow progress. The teams involved in this activity have a wide-ranging research experience which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ArtistDesign will help the participants to the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion.

Design for Adaptivity. An embedded hardware-software system is adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is a cross-cutting system characteristic that affects both hardware and software. At the software-level adaptivity is mainly concerned with flexible and adaptive resource scheduling, e.g., CPU time scheduling. At the hardware-level adaptivity includes both adaptation of operation modes, e.g., supply voltage and clock frequency, processor instruction sets, and dynamic management of hardware resources, e.g., processing elements and memory.

Design for Predictability and Performance. Many applications have strict requirements on timing, and limited resources (memory, processing power, power consumption, etc.). All systems also have increasing demands on (average) performance, which has motivated the introduction of features such as caching, pipelining, and (now becoming very prominent) multiprocessor platforms. Almost all such efficiency-increasing features drastically increase variability and decrease analyzability of response-times, etc. and thus have a detrimental effect on predictability. Since the introduction of new architectural features is inevitable, it is important to: a) develop technology and design techniques for achieving predictability of systems built on modern platforms, and b) investigate the trade-offs between performance and predictability.

Integration Driven by Industrial Applications. To have a strong impact on industry and society at large, the results of the Thematic Clusters need to be harmonized in an overall design flow that can sustain the embedded design chain from conception of the product to its implementation. The design chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics). Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, the system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company.

-- Changes wrt Y1 deliverable –

No changes with respect to Year 1.

3.1.2 Overview of the Year 2 Research Results

-- Changes wrt Y1 deliverable –
The texts in this section are entirely new.

3.1.2.1 Modeling and Validation

Modeling

The principal results obtained are:

- The development of modelling languages such as MARTE and Y-charts, as well as their application to non-trivial case studies.
- The foundations of a contract-based theory for components, as well as a theory for relational interfaces. These can be used for compositional verification of embedded systems.
- The development of model-based design methodologies for
  a) flight control systems,
  b) complex systems ranging from automobiles, buildings, and airplanes,
  c) multi-core systems.
- The development of resource modelling techniques based on languages and models that explicitly represent different resource types, such as processors, memories and energy.
- The study of a sound semantic basis for quantitative modelling, including
  a) performance models,
  b) quantitative generalisation of classical languages,
  c) synthesis of optimal controllers from quantitative high-level specifications.

Validation

The principal results obtained are:

- The development of compositional validation techniques, including:
  a) compositional verification of deadlock freedom,
  b) modular analysis for timed systems,
  c) compositional safety analysis,
  d) compositional verification of probabilistic systems.
- The development of quantitative validation techniques, including:
  a) the analysis of energy-related properties of sensor-networks,
  b) the verification of hybrid systems
  c) the study of multi-processor scheduling techniques and cache policies for ensuring timing predictability,
  d) the study of quantitative models and their associated verification techniques, such as timed automata, and stochastic automata,
  e) the verification of transactional memories, by model checking.
- The development of techniques for cross-layer validation, such as:
  a) control under partial observation,

b) adapting abstraction techniques to black-box analysis and learning,
c) test-case generation techniques, under partial observability.

3.1.2.2 Software Synthesis, Code Generation and Timing Analysis

Timing Analysis

The principal results obtained are:

- Using model identification and learning techniques for estimating WCET.
- Theory for ensuring timing predictability, as well as for timing composability.
- The development of a common annotation language for WCET analysis.
- The integration of Timing Analysis and Compilation, to achieve WCET-aware compilation.

Software Synthesis and Code Generation

The principal results obtained are:

- Techniques for mapping applications to MPSoCs, so as to meet a given set of non-functional properties.
- Code optimization techniques, taking into account WCET,
- Techniques for verifying code generation methods.

3.1.2.3 Operating Systems and Networks

Scheduling and Resource Management

The principal results obtained are on:

- resource management, including:
  a) the development of a taxonomy of resource management as a wiki,
  b) memory resource management techniques,
  c) adaptive resource management.
- scheduling, including:
  a) hierarchical scheduling,
  b) scheduling and placement algorithms for multi-processor systems,
  c) multi-resource contract-based scheduling,
  d) data-flow scheduling, using constraint programming.
- language support for programming real-time systems,
- sporadic event-based control.

Real-Time Networks

The principal results obtained are on:

- Timeliness in wireless sensor networks,
- Mobility issues in ad-hoc real-time wireless communication
- Robust communication with star topologies,
- Real-time support to middleware and composability,
- Applications of wireless networks in industrial environments, in intelligent transportation systems, and in health applications.

3.1.2.4 Hardware Platform and MPSoC Design

Platform and MPSoC Design

The principal results obtained are on:

- MPSoC design and programming, including the development of:
  a) modelling concepts, methods and tools allowing cost-efficient mapping of applications,
  b) run-time resource management techniques,
  c) architectures on chip communication, in future many-core processors,
  d) MPSoC mapping tools, for multi-media and wireless applications,
  e) MPSoC architecture exploration.
- The design of fault-tolerant distributed embedded systems,
- Resource-aware, system-level optimisation, including,
  a) power optimisation,
  b) performance optimisation in energy harvesting systems,
  c) optimisation-centric MPSoC design.

Platform and MPSoC Analysis

The principal results obtained are on:

- Modelling and analysis techniques for performance evaluation, including,
  a) performance estimation of distributed real-time systems, for control applications,
  b) unifying approaches for hierarchical scheduling,
  c) modelling of shared resources in multi-processor systems,
  d) modelling and analysis of adaptive systems,
  e) contract-based architecture dimensioning.
- Analytic real-time analysis and timed automata,
- Modelling and analysis of fault-tolerant distributed systems,
- Verification of design properties of hardware architectures.

3.1.2.5 Design for Adaptivity (Transversal Integration activity)

The principal results obtained are on:

- Analysis techniques for adaptive systems, including
  a) dynamic changes in real-time parameters,
  b) assignment of real-time parameters to control tasks,
  c) timing analysis and sampling mechanisms, for event-driven control systems.
- Adaptive design techniques, including:
  a) algorithms for QoS-aware, cooperative systems,
  b) adaptive topology management, to combine energy efficiency and QoS,
  c) in-system self-optimization for real-time systems,
  d) reconfigurable self-organizing and self-healing hardware platforms,
  e) adaptive energy management.
- Modeling and analysis of adaptive systems,
- Support for Adaptivity in distributed systems.

3.1.2.6 Design for Predictability and Performance (Transversal Integration activity)

The technical work on Predictability has intersected work in all the Thematic Clusters.

Modeling and Validation of component –based systems

- We studied the concept of predictability in relation with robustness, and this work is a continuation of work in Year 1. We identified two major challenges in embedded systems design. These challenges require a rethinking of the conventional, purely discrete and purely functional foundation of computing.
- We worked on methodologies for designing component-based systems, and participated in the standardisation of the MARTE-UML profile.

Timing Analysis and Compiler Techniques

- The main contribution is work on relations between Timing Analysis and Timing Predictability. We identified heuristics to derive operating mode candidates from source code and a procedure to exploit mode information to arrive at mode-specific WCET bounds. We also started to explore strategies for eliminating timing anomalies by different code generation techniques.
- We investigated WCET analysis techniques in the presence of context switches.
- Finally, we integrated Timing Analysis and Compilation techniques for optimizing code generation.

OS/MW/Networks

We developed the following results:

- Integrating scheduling analysis techniques and model checking.
- Partitioning the shared caches on multi-core processors for timing predictability. We have developed a sufficient schedulability test for non-preemptive fixed priority scheduling for multi-cores, with shared L2 cache, encoded as a linear programming problem. Furthermore, we have compared several scheduling models for multi-processor systems.

Architecture and System Design

- We studied techniques allowing predictability for fault-tolerant embedded systems and predictability for multi-processor MPSoC architectures. In particular, we developed power prediction algorithms for an energy harvester.
- We also developed a new bus model for MPSoC system bus analysis and optimisation.
- Finally, we developed the Precision Timed (PRET) language, which allows determinism and time predictability.

3.1.2.7 Industrial Integration (Transversal Integration activity)

This activity groups a set of industrial interactions and collaborations with ArtistDesign teams. The long-term goal is to understand industrial design methodologies and identify the research results that could be applied in these methodologies.

The work this year has consisted in :

- organising a few high-profile meetings with industry (eg: SEEC ’09, WESH ‘09,) as well as joint workshops and technical meetings. SEEC in particular was extremely successful, with a high international visibility far beyond European borders.
- a wide array of collaborations with industrial partners and ArtistDesign partners, including general frameworks for system-level design, automotive applications, applications for chip design, smart energy-efficient buildings, and wireless communication.

3.2 Joint Programme of Integration Activities (JPIA)

3.2.1 Structure of the Integration Effort

The JPIA activities promote integration of geographically dispersed teams and have long-lasting effects:

Joint Technical Meetings. Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

Staff Mobility and Exchanges. This is essential for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. Mobility is justified by and refers to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

Tools and Platforms. A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

The detailed information regarding the JPIA activities is available in the JPIA deliverable.

-- Changes wrt Y1 deliverable –

No changes with respect to Year 1.

3.2.2 Assessment

The ArtistDesign Network of Excellence is a significant evolutionary step for integrating the leading embedded systems design research teams in Europe. The clusters are more tightly woven together, and each represents a significantly greater critical mass than did the clusters in the Artist2 Network of Excellence, which ended Sept 30th 2008, and has nearly the same consortium.

Despite this strong overlap with the Artist2 NoE, the overall assessment for the WP at the end of ArtistDesign Y1 (Jan–Dec 2008) is positive - both in terms of impact on the overall structuring and lasting integration within the consortium and more generally within the area in Europe.

- The ArtistDesign clusters have been actively pursuing operational integration through joint meetings, staff mobility, and shared platforms and tools.
- The level of activity shows that the Cluster / Activity structure and research topics defined for ArtistDesign make sense, and are viable vehicles for integrating the area. In operational terms, they generate sufficient interest for the partners and individual researchers to participate actively in the joint meetings, to exchange personnel, and to orient the tools and platforms developed to make sense within this structure.
- There is clearly a greater level of maturity for tools and platforms than had been the case at the start of the Artist2 NoE – and the partner teams are actively pursuing a policy of implementing tools, demontrators, and in many cases their accompanying methodologies.
- Nonetheless, it is important to remember that these are tools and platforms for research. The aim is not necessarily always for these to lead to commercially viable tools and start-up companies. In general, they are the concrete realisation of the state-of-the-research, allowing to explore possibilities for future research and later tools (some of which may in turn lead to commercially viable products).
- The level of activity varies according to individual clusters / activities, which is normal. We believe this is partly due to the remaining overlap with Artist2 – which should no longer be the case in Y2.

-- Changes wrt Y1 deliverable –

No changes with respect to Year 1.

3.3 Jointly-executed Programme of Activities for Spreading Excellence *(JPASE)*

-- Changes wrt Y1 deliverable –
No significant changes with respect to Year 1.

ArtistDesign leverages on the worldwide visibility of its activities. It is progressively creating a European embedded systems design community and spreading the "Artist culture" in all major research institutions.

To ensure that the next generation of researchers will continue in this direction we, as a consortium, devote a great deal of effort to Spreading Excellence, in both academic and industrial circles. Furthermore, through our links with both core and affiliated partners, we actively set up permanent links between industry and public research, based on existing partner collaborations with major industrial players in the area.

The JPASE activities spread excellence and structure the community at large. They are planned by the Strategic Management Board, and are implemented by ArtistDesign core and affiliated partners.

The NoE leverages on its members and teams, who play a main role in the organisation of world-class scientific events, to disseminate results in the area. We expect that the NoE's structured and authoritative dissemination will have a strong effect on the community as a whole, for orienting and creating synergy for research.

3.3.1 Education and Training

- Courseware – The NoE has the ambition to serve as a resource and point of reference for the area, including by collecting and disseminating course materials for teaching embedded systems design.
- Graduate Studies – The NoE will provide support for selected graduate studies programmes, as the means for training engineers and researchers in embedded systems design.
- Summer Schools – The NoE will actively support and participate in summer schools and seminars in embedded systems design.
- International Workshop on Embedded Systems Education – We will continue this series of international workshops, started in ARTIST2. York has accepted to lead this activity.
- Implement a high-visibility International Summer School. The ArtistDesign NoE will organise each year a high-visibility international Summer School, drawing top European lecturers in Embedded Systems Design. The audience is researchers, PhD students, and engineers. The following group of core partners will lead this activity: Luca Benini (Bologna), Giorgio Buttazzo (SSSA-Pisa), Petru Eles (Linkoping), Kim Larsen (Aalborg), Peter Marwedel (Dortmund).
- Training Engineers – Many partners are already active in this area, such as IMEC, EPFL, ESI, and Aalborg's CSI. The ArtistDesign NoE will provide logistical, financial dissemination through the Web Portal and newsletter.

3.3.2 Publications in Conferences and Journals

The ArtistDesign consortium is very active in publishing in scientific journals and conferences, as attested by the list of significant publications by the partners' teams.

The NoE leverages on its members and teams, who are strongly implicated in collaboration with industry, to organize and structure industrial relations, and develop mutually beneficial interactions. Furthermore, through Industrial Liaison, ArtistDesign receives useful feedback about the relevance of work directions and priorities.

3.3.3 Links to Artemisia

ArtistDesign seeks a tight interaction with the Artemis community, through the **Artemisia Liaison Task Force**. This is composed of the following prominent ArtistDesign members, also active in ARTEMIS/ARTEMISIA: Luca Benini, Werner Damm, Rudy Lauwereins, and Joseph Sifakis. Amongst these, 3 are elected members of the ARTEMIS Steering Board.

ArtistDesign partners have been encouraged to join ARTEMISIA.

3.3.4 International Collaboration

The ArtistDesign "*International Collaboration*" activities allow ArtistDesign to be visible internationally, and to monitor the evolution of the state of the art in the area worldwide.

International Collaboration fits into a global win-win strategy for achieving the participants' long-range aims. Examples of activities include:

- **High-level meetings** gathering top representatives from industry, funding agencies, and research, to discuss avenues for International Collaboration, including on R&D and standards e.g. IST/NSF Workshop on Component-based Engineering (Paris, June 05).
- International Collaboration **Working Groups** for exploring possible avenues for research and education in a chosen topic and producing white papers and reports e.g. joint EU/US Working Groups: on Timing Validation, Adaptive Real-Time Systems for Dynamic Applications, Semantic Platform for Hard Real Time (2002 – 2003).
- Organization and sponsoring of international conferences and schools, to disseminate recent research results, and promote the emergence of embedded systems as a discipline e.g. Embedded Systems Week, New Jersey, October 2005.
- International Collaboration **Publications**.
- **Joint international projects**. Set up joint collaborative projects e.g. Columbus project or extend existing projects, by allotting them an extra budget.

International Collaborations is implemented mainly in collaboration with the USA, building on existing links between IST and the US funding agencies (mainly NSF).

ArtistDesign leverages on and extend the successful International Collaboration activities initiated in the ARTIST2 NoE.

3.3.5 Web Portal

The ArtistDesign Web Portal is a major tool for Spreading Excellence within the Embedded Systems Community. It aims to be the focal point of reference for events and announcements of interest to the embedded systems community.

This will play a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large. We believe the web portal will be an essential mechanism for achieving integration.

It acts as a repository of knowledge in the area, including courseware, information about standards, methods and tools, research publications and results. This web portal will be made available within the NoE core and affiliated partners, and to other parties.

This repository is to be the reference for the embedded systems design community. It builds on the existing ARTIST2 Portal, which includes several features that help keep it coherent and up to date:

- Authorised users (principally, the ARTIST2 partners) can access the back end of the site to modify and update information directly. The changes are immediately visible on the site, which greatly streamlines the updating process.
- It's possible to track changes and go back to previous versions of individual web pages.
- Events are automatically sorted by date, and transferred to 'Past Events'. When appropriate.
- Structural information (hierarchy of pages) is maintained automatically.
- Ergonomics are set for the entire site. The "look and feel" of the site is always homogeneous throughout the site. It's possible to change these ergonomics, and these changes are applied homogeneously throughout the site, via automated mechanisms.

The ArtistDesign Web Portal offers information about:

- **Workshops, Conferences, Schools and Seminars**
  Provide information about the main scientific events in the area, and in particular those organised by ArtistDesign.
- **International Collaboration**
  Advertise the ArtistDesign International Collaboration events, and provide pointers to the most visible International Projects (either about significant projects outside Europe, or joint International Collaboration projects.
- **Publications**
  Publications from core partners, with emphasis on Position Papers, White Papers, etc. that may have a particularly deep impact.
- **Course Materials Available Online**
  The web portal will centralize course materials from as many sources as possible, to make them available to the general public.

3.4 Managing the Network of Excellence (JPMA)

We believe that the current two-tiered Management structure - dividing the management amongst cluster leaders and the Strategic Management Board composed of both cluster leaders and a limited number of other selected prominent core partners – has been the right one for managing such a large research entity. It has provided the right combination of flexibility and accountability, while leaving room for innovation and evolution.

This management structure is reproduced with adaptations in the ArtistDesign NoE. The adaptations reflect the greater cohesion between partners, and move to capitalize on and strengthen the integration achieved in Artist2.

-- Changes wrt Y1 deliverable –

No significant changes with respect to Year 1.

4. End Results

We are achieving a significantly more integrated scientific community. Initially, there was a strong fragmentation by topics and communities, with little interaction between them. Over the course of the NoE, the clusters have evolved and merged. A gradually cohesion has taken place, through transversal “NoE Integration” activities, and more importantly through strategic alliances.

We are seeing a convergence of interests, and the gradual emergence of recognized leaders.

-- Changes wrt Y1 deliverable –

No changes with respect to Year 1.

214373 ArtistDesign
Network of Excellence
on Embedded Systems Design

Project Management Report for Year 2

Joseph Sifakis – ArtistDesign Scientific Coordinator
Bruno Bouyssounouse – ArtistDesign Technical Coordinator

ArtistDesign Consortium

Table of Contents

1. Overview

1.1 Project Objectives and Major Achievements

A detailed description of objectives, and particularly the main aims for integration, is provided for each cluster in the sections labelled « State of Integration in Europe ».

1.1.1 Historical Perspective: Artist FP5, then Artist2 in FP6

Within IST FP5, a subset of the current consortium implemented an Accompanying Measure, whose objectives were to:

- Coordinate the R&D effort in the area of Advanced Real-time Systems
- Improve awareness of academics and industry in the area
- Define innovative and relevant work directions

This was achieved through work along 3 axes:

- Roadmaps for selected actions: (Hard Real Time, Component-based Design, Adaptive Real Time, Execution Platforms)
- International Collaboration
- Education

Information about these results is publicly available:

http://www.artist-embedded.org/Roadmaps/

Within IST FP6, a consortium very similar to the current one implemented the highly successful ARTIST2 NoE. The main changes between Artist2 and ArtistDesign are :

- An evolution of the clusters to reflect the ongoing integration.
  There are now 4 clusters instead of 6, and they are significantly larger.
- Reinforced role of the Transversal Activities (called NoE Integration activities in Artist2). In ArtistDesign these now have nearly the same role and autonmy as did the clusters in Artist2.
- Tighter consortium. The number of partners in the consortium has been reduced by approximately 25%. The “departing” partners continue interaction with the NoE, as Affiliated Partners. This allows them to participate in the technical meetings and occasionally claim some costs for travel, but none for manpower.
- Tools and procedures continue to evolve. The tools (eg web) and procedures developed within Artist2 contionue to evolve within ArtistDesign.
- Change of Coordinator. The Financial and Legal Issues handled by the CDC in Artist2 are now handled by Floralis in ArtistDesign.

-- Changes wrt Y1 deliverable –

No changes with respect to Year 1.

1.2 Deliverables for the Reporting Period

WP0: Joint Programme of Management Activities (JPMA)

	D2-(0.2)-Y2	Project Management Report
UJF/Verimag	D2-(0.2a)-Y2	*ch. 1* - **Executive Summary and Overview**
Aalborg	D2-(0.2b)-Y2	*ch. 2* - **Modelling and Validation**
Dortmund	D2-(0.2c)-Y2	*ch. 3* - **SW Synthesis, Code Generation and Timing Analysis**
Pisa	D2-(0.2d)-Y2	*ch. 4* - **Operating Systems and Networks**
DTU	D2-(0.2e)-Y2	*ch. 5* - **Hardware Platforms and MPSoC Design**
UJF/Verimag, Floralis	D1-(0.1)-Y2	**Periodic Report**

WP1: Joint Programme of Integration Activities (JPIA)

UJF/Verimag	D3-(1.0)-Y2	**Integration Activities Report**

WP2: Joint Programme of Activities for Spreading Excellence (JPASE)

UJF/Verimag	D4-(2.0)-Y2	**Spreading Excellence Report**

WP3: Modeling and Validation (JPRA)

UJF/Verimag	D5-(3.1)-Y2	**Modelling**
Aalborg	D6-(3.2)-Y2	**Validation**

WP4: Software Synthesis, Code Generation and Timing Analysis (JPRA)

Dortmund	D7-(4.1)-Y2	**Software Synthesis, Code Generation**
Saarland	D8-(4.2)-Y2	**Timing Analysis**

WP5: Operating Systems and Networks (JPRA)

Pisa	D9-(5.1)-Y2	**Resource-aware Operating Systems**
York	D10-(5.2)-Y2	**Scheduling and Resource Management**
Univ. Porto	D11-(5.3)-Y2	**Embedded Real-Time Networking**

WP6: Hardware Platforms and MPSoC (JPRA)

Bologna	D12-(6.1)-Y2	**Platform and MPSoC Design**
DTU	D13-(6.2)-Y2	**Platform and MPSoC Analysis**

WP7: Transversal Integration (JPRA)

Lund	D14-(7.1)-Y2	**Design for Adaptivity**
Uppsala	D15-(7.2)-Y2	**Design for Predictability**
Trento	D16-(7.3)-Y2	**Integration Driven by Industrial Applications**

1.3 Consortium Management

-- Changes wrt Y1 deliverable –

No changes with respect to Year 1.

1.3.1 Governance Structure

Scientific Coordinator:	Technical Coordinator:
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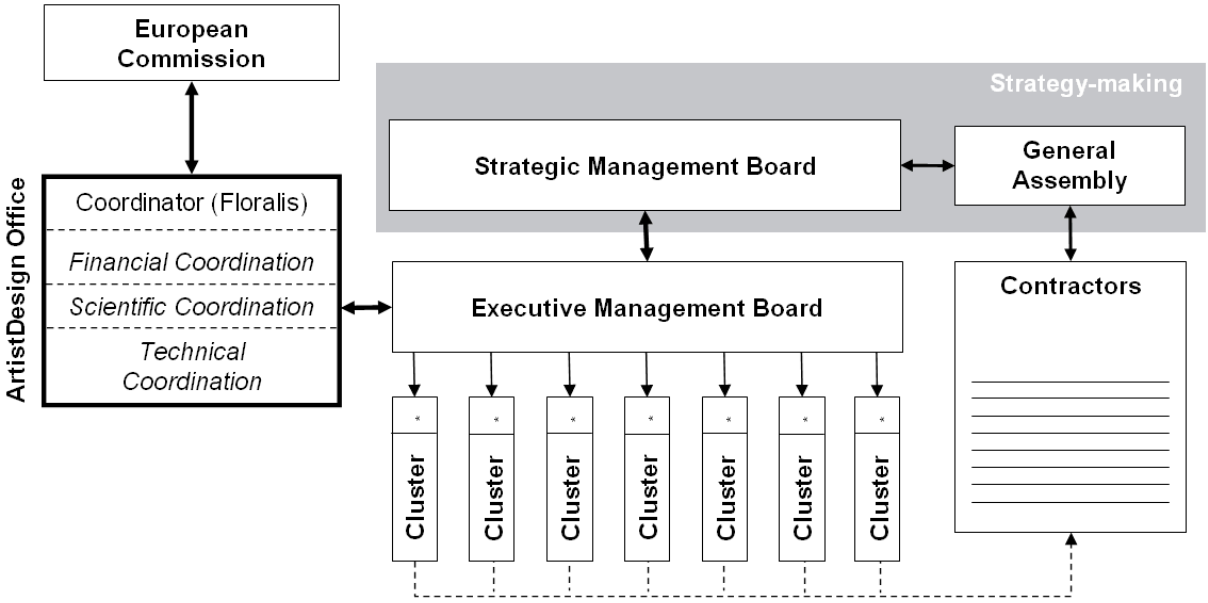
The methodology adopted for achieving the JPA objectives follows the same lines as for managing a laboratory. The activities, their objectives, their technical description, the partners involved, their roles, and the resources available have been clearly defined in the initial Description of Work, and updated in the deliverables. This will be monitored and guided by a tight and rigorous management, as defined in the diagram below:



The main governance bodies are:

The **General Assembly** is composed of one representative per core partner. It is convened at the beginning of the project and meets once per year. It is chaired by the Scientific Manager.

The **Strategic Management Board** is initially composed of the NoE cluster leaders, and a representative of the Coordinator – who attends, with no voting rights. It is chaired by the Scientific Manager, assisted by the Technical Manager. It meets at least once per year – close to the General Assembly meeting. Its members are elected by the General Assembly every two years, according to modalities to be determined in the Consortium Agreement.

The **Cluster Leaders** (who compose the Executive Management Board) are responsible for the overall coordination of the activities led by their cluster. A cluster functions as a virtual

team – with a degree of autonomy for defining its internal meetings and day to day management.

1.3.2 Partners Involved

This is provided in the publishable Executive Summary, in the first part of this document.

1.3.3 Contractors

There are no changes to the consortium at the end of Year 1.

1.3.4 Project Timetable

The JPA is organized into activities. The activities should not be considered as tasks of a workprogramme, with begin/end and synchronisation dependencies. Of course, the detailed description of an activity could be decomposed into sub-tasks and intermediate milestones, but this would imply a granularity that is too fine for research activities.

1.3.5 Other Issues

None

1.3.6 Plan for using and disseminating the knowledge

The main instruments for using and disseminating knowledge are:

- Workshops and Schools organised.
  The list is quite impressive, and is provided in the deliverable on “Spreading Excellence”.
- ArtistDesign Web Portal.
  Here also, the quantity of information made available to the greater embedded systems community is quite impressive, and continuously growing. This is possible through the efforts of the entire consortium, who now have direct access for updating the contents.
- Course Materials.
  There is a growing body of course materials made available via the Artist2 web portal.
- Publications.
  The ArtistDesign consortium is very prolific in publishing research articles, surveys, textbooks, roadmaps, and position papers.