IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Cluster Progress Report for Year 2

Cluster:
Software Synthesis, Code Generation and Timing Analysis

Cluster Leader:

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Policy Objective (abstract)

The objective of this activity is to provide software synthesis, code generation and timing analysis tools which are required for modern embedded architectures. A particular focus is on multi-processor systems. The parallelism and communication structures found in such architectures pose a particular challenge.

Versions

number	comment	date
1.0	First version delivered to the reviewers	December 18th 2009

Table of Contents

1. Overview

1.1 High-Level Objectives

There is a continuing demand for higher performance of information processing. This growing demand stimulates using a growing amount of parallelism (including using multiple processors), due to limitations of increasing clock speeds any further. This trend also affects the design of embedded systems. Hardware platforms, containing connected processors, are becoming increasingly parallel. Actually, there are various kinds of connectivity. In multi-processors in a system on a chip (MPSoC), processors are tightly connected and communication is fast. In other cases, networked processors may be less tightly connected and communication may be slower. In this project, we would like to address the issues resulting from the use of multiple processors, in particular in the form of multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces.

These processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Mapping techniques can be either based on task graphs or on sequential applications. The latter require the use of automatic parallelization techniques. In this cluster, we want to provide at least partial solutions to the problem of mapping specifications of embedded systems to networks of embedded processors. These networks will be characterized by different speed parameters reflecting the communication and memory architectures. These parameters will be considered during the mapping. We will focus on mappings from simple sequential code from C or C-like languages. However, we will also look at the generation of code from other specifications, being based, for example, on MATLAB or UML. Such languages could simplify the mapping since such specifications might be inherently parallel (and also more appropriate for embedded systems). In general, mapping techniques will be indispensable for using future architectures.

Timing analysis is also affected by the trend toward the new platforms. Also, timing analysis beyond single processors is required. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Hence, timing analysis will also consider the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors. In addition, overcoming the traditional separation between compilers and timing analysis continues being on the agenda.

The design of efficient embedded systems also requires additional work. In particular, minimizing the energy consumption, addressing the memory wall problem and customizing instruction sets are hot topics, for which integrated approaches from various partners are being extended and exploited.

Partners in this cluster also participate in the activities of the thematic activities of the Transversal Integration work package, where they address adaptivity and predictability of complex systems comprising MPSoCs. Predictability is also to be addressed in the cooperation between partners of the two activities of this cluster.

Partners are also contributing to orthogonal work, such as running workshops on embedded system education, writing text books, and editing a new series of books on embedded systems through Springer (see http://www.springer.com/series/8563).

It is understood that the current project can only help integrating work that provides potential solutions. The actual work on those solutions is mostly paid through other projects

- Changes wrt Y1 deliverable –
There is an increasing amount of work on orthogonal issues.

1.2 Industrial Sectors

Software Synthesis and Code Generation: The work performed in the cluster is relevant for all industrial sectors using embedded software. This includes semiconductor houses, system houses, companies working on audio processing, video processing, data streaming applications in the TV, Set Top boxes, DVD players and recorders, mobile phones, base stations, printers and disk drives. Efficiency of embedded software, in particular the efficiency of memories, is relevant for high-speed embedded systems. It is expected that most mobile devices will provide some kind of multimedia processing.

Timing Analysis: WCET estimations are relevant for all industrial sectors using hard real-time systems. Therefore, industrial sectors in this case include avionics, automotive, defence and some areas where control systems are applied. Especially in the automotive and the aeronautical domains, there is a need to have precise knowledge on the worst-case timing behaviour of safety critical software. Therefore, timing-analysis tools entered industrial practice and are in routine use in the aeronautics and automotive industry. This need is underlined by the fact that the worst-case timing of large parts of the software used within the new Airbus A380 has been analyzed using AbsInt's aiT. AbsInt's timing analysis tool, aiT, has been used in the certification of time-critical subsystems of the Airbus A380 and has thus acquired the status of a *validated* tool.

Link between timing analysis and compilers: Since the code of safety critical applications is typically generated by a compiler, the compiler should also be aware of worst-case timings. This work is relevant in all areas for which a physical environment is integrated with software. The focus is on sectors having safety critical applications.

-- Changes wrt Y1 deliverable --
No changes with respect to Year 1.

1.3 Main Research Trends

Mapping of applications to MPSoCs can be considered as an extension of scheduling. Traditionally, scheduling mostly focused on independent tasks. This assumption is not valid for most applications of embedded systems. Additional research is performed in the multi-core context. Multi-core processors are usually considered to be homogeneous. For embedded systems, this assumption is also not valid. Therefore, new mapping techniques are required. Some papers have been published in this area. It is a trend to combine the mapping problem with non-traditional objectives. For example, minimization of the operating temperatures, maximization of the life-time of processors, and dependability in the presence of failing processors etc are considered. However, these approaches mostly consider tasks as black boxes with little information, for example, on the memory access characteristics. This can lead to sub-optimum mappings. This trend is important in all industrial areas in which high performance embedded computing is required.

Taking the well-known (frequently negative) results on automatic parallelization in high-performance computing into account, automatic parallelization is being experimented with in a way which is appropriate for embedded systems. Results obtained (for example at the University of Edinburgh and the University of Passau) indicate that this parallelization is feasible within a restricted scope of applications and architectures. This trend is also important in all industrial areas in which high performance embedded computing is required.

Energy efficiency, initially mostly a topic considered for embedded systems, is now mainstream. Energy availability is continuing to be the most challenging constraint for embedded system design, but performance constraints also exist. Therefore, the design of efficient embedded systems continues being important. Constraints are most dominating for small, mobile products.

The importance of timing is slowly being recognized by larger groups of people. For example, there is increasing interest in the automotive domain. At the same time, researchers are also giving timing issues more attention. In-line with this, the first compiler including a fully integrated WCET estimator was designed recently. This research direction is finding more attention recently.

WCET analysis has so far almost exclusively dealt with sequential code running on uni-processors. The main trend has been towards managing more complex sequential hardware architectures. Increasing the level of automation, e.g., by more advanced analyses constraining the possible program flows, is also a topic of active research. As multi-core and MPSoC architectures arise, the research focus will have to shift towards analysis of parallel systems.

-- Changes wrt Y1 deliverable --
The IT-community pays more and more attention to the problem of compiling for multi-processor systems.

2. State of the Integration in Europe

2.1 Brief State of the Art

Software Synthesis and Code Generation: Mapping applications to MPSoCs is an important topic in various places in the world, due to its extreme relevance for industry. In Europe, Ed Deprettere (U. Leiden) performed significant work, working together with adjacent universities on the DEADALUS tool. Also, the group of Jürgen Teich from the University of Erlangen Nürnberg is proposing the SystemCoDesigner tool. In the automotive context, additional work has been performed at TU Braunschweig. METROPOLIS by Sangiovanni-Vincentelli et al. is a tool working on a global level. CHARMED by Bhattacharyya places emphasis on signal processing applications. Recent tools try to combine task allocation with non-standard cost functions such as energy (e.g. Chang at DAC 2008), temperature (e.g. Ciskun at DATE 2007), lifetime or dependability.

The design of efficient embedded systems is the target of numerous optimization tools. There are clearly too many tools to make any attempt to present a survey in limited space useful. Even within the more restricted area of optimization the memory structure, many approaches have been proposed by computer architects. Due to the increasing speed gap between processors and memories, efforts for improving the performance of systems have been predicted to hit the “memory wall”. Work was done in the context of caches (loop caches, filter caches etc.). However, these approaches have mostly focussed on hardware approaches for reaching the goals. For these approaches, compilers were considered to be black boxes and untouchable. Only few authors (e.g. Barua, Catthoor, Dutt, Kandemir, Egger) have taken a holistic approach, looking at hardware and software issues.

Timing Analysis: Several commercial WCET tools are available. They have experienced positive feedback from extensive industrial use in the automotive and aeronautics industry. The existing tools serve some particular and highly relevant points in this space. AbsInt’s tool for example has been used in the development and the certification of safety-critical systems in the Airbus A380. However, they currently do not serve distributed architectures well.

TU Dortmund demonstrated the **integration of compilers and timing analysis** and can be considered leading this research area.

-- Changes wrt Y1 deliverable --
The general impression is that compiling for multi-cores and timing predictability are receiving more attention, and so is the integration of compilers and timing analysis.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

The Compiler and Timing Analysis Cluster and the Execution Platforms Cluster aim at advancing the methodology for resource aware design and compilation and at increasing predictability while retaining a performant system. The main aim of using the ArtistDesign network is to get access to competences, knowledge and tools which are not available locally at each of the institutions. The cooperation provides the required size of research teams, necessary to handle the complexity of today’s technology. Furthermore, a major goal is the combination of areas of excellence of the different partners by defining and implementing interfaces between their design flows and tools in order to achieve compilation platforms applicable to a wider problem scope.

WCET analysis of parallel systems, including MPSoC, is a more or less novel research area. However, it is becoming rapidly important as MPSoCs become increasingly used. Therefore, it is urgently needed to initiate more research in this area, and the ArtistDesign network will be used for this. The network will also be used for research initiation activities within the WCET analysis area. Contacts with other clusters, such as the HW Platform and MPSoC design cluster, will also be of importance since the success of the cluster's activities depends critically on the properties of the underlying hardware design.

- Changes wrt Y1 deliverable – No major changes with respect to Year 1.

2.3 Other Research Teams

For mapping applications to MPSoCs, section 2.1 contains a brief description of the work of other research teams in this area. Ed Deprettere (U. Leiden), Jürgen Teich and some of their students participated in the working meeting at Düsseldorf in November 2008 as well as in the second workshop on "Mapping of applications to MPSoCs". Ed Deprettere helped to set up an activity on benchmarking. Jürgen Teich presented his advanced SystemCoDesigner concept. Both are clearly candidates for being added as affiliates. Fortunately, we were able to reach out beyond Europe as well. Soonhoi Ha of Seoul National University gave a keynote talk at the second Rheinfels workshop. His HOPES system is one of the leading systems worldwide. He has been proposed as a new ArtistDesign affiliate. Qiang Xu of the City University of Hong Kong considers the impact of mapping decisions on the reliability. His talk at the Rheinfels workshop was also well-received. Finally Tajana Simunic Rosing of UC San Diego presented her work on the consequences of mapping tasks on energy consumption and thermal management.

Essentially three more research teams have competed with Europe in the area of Timing Analysis, one at Seoul National University (SNU), one at Florida State University, now with some branches in North Carolina etc., and Singapore National University. Seoul has turned to power-aware computing, and flash memory based components research. Singapore and Florida have cooperated with the ArtistDesign partners in writing a survey paper. Singapore has participated in the WCET Tool Challenge, arranged within ArtistDesign, with their academic prototype. There is a continuous exchange of PhD students and PostDocs with the team of Prof. Sang Lyul Min at SNU.

Only few groups have been working on the integration of worst-case execution times and compilers. Smaller, apparently volatile efforts have been reported from Sweden and South Korea. Some work was performed in the group of David Whalley at the Computer Science Department of the Florida State University. However, only very simplified timing models and highly predictable processor architectures are considered at Florida. A larger effort takes place at the group of Abhik Roychoudhury from the National University of Singapore (NUS). Cooperation between TU Dortmund and NUS has been intensified through mutual visits from both teams.

WCET analysis for multi-core systems has been considered by Petru Eles et. al. at Linköping University (Artist-Design Core partner in the Hardware Platforms and MPSoC Design cluster), Their approach builds on a TDMA scheduling policy for the bus, which makes memory access times predictable and thus enables a more precise WCET analysis.

Additional work has been performed at INRIA by Isabelle Puaut et al. More information about the work of other teams is available in section 1.5 of the two related activity reports.

-- Changes wrt Y1 deliverable -- Cooperation between TU Dortmund and the National University of Singapore has been intensified.

2.4 Interaction of the Cluster with Other Communities

For mapping application to MPSoCs, links have been established with the execution platform cluster of ArtistDesign, where some related work is being performed, for example, at Zürich, Bologna and TU Denmark. For timing analysis, the same applies for the modelling and validation cluster. Cluster members Peter Marwedel and Rainer Leupers performed further teaching activities at ALARI, Lugano, together with ArtistDesign members like Luca Benini (Bologna), Rudy Lauwereins (IMEC) and Lothar Thiele (Zürich). Further links of ArtistDesign members existed to the SHAPES project and to the HiPEAC Network of Excellence.

For timing analysis, two joint meetings have been held with the Hardware Platforms and MPSoC Design cluster to discuss the impact of MPSoC design on timing predictability.

TU Dortmund:

The interaction with the local technology transfer centre ICD (see http://www.icd.de/index_eng.html) is key for interacting with industry. ICD is headed by Peter Marwedel. ICD is used for transferring research results to industry. ICD provides its development tool ICD-C to several partners, including TU Eindhoven and Saarland University.

The group promotes education in embedded systems through a published text book ("Embedded System Design"). Several other groups were asked to comment on upcoming second edition of the book, to be published in spring 2010. The group also organizes the WESE workshop on embedded system education. The group leader teaches at ALARI (Lugano) and is the European editor for the new Springer series on embedded systems (see http://www.springer.com/series/8563).

TU Dortmund organizes the SCOPES series of workshops on compilation for embedded systems, the workshop on the mapping of applications to MPSoCs and the workshop on software synthesis, held during the embedded systems week 2009.

TU Dortmund is working on the integration of timing analysis and compilation. The corresponding work on the WCC-Compiler led to a general interest in this type of work.

TU Dortmund works on resource-aware compilation. The main focus is on memory-architecture aware compilation, implemented through pre-pass compilation tools. This work also includes the mapping to multi-processors.

Work performed at Dortmund was presented in a visit to selected partners in Fukuoka, Seoul, Singapore and Delhi.

IMEC:

IMEC is integrated in European research networks, including HiPEAC. Moreover, IMEC is the central partner of a Marie Curie Host Fellowship project that involves more than 10 universities across Europe. IMEC also has many industry co-operations including most large European multi-media and communication systems oriented companies. Additionally, several news sites featured the launch of the CleanC tools for source code parallelization assistance. Articles talking about the launch of the tools could be found on sites like EETimes, EDN, Electronics Weekly, Azonano, EDACafé.com, EDA DesignLine, Electronic Design, Topix, SOCCentral, Ugens Erhverv, or Global-Electronics.net.

U. Passau:

The group at the University of Passau is internationally well connected in parallelism and programming methodology. This is most visibly documented by Christian Lengauer's chairmanship of the steering committee of the yearly international conference series Euro-Par (Parallel Computing in Europe) and the IFIP Working Group 2.11 on Program Generation. Here, the paradigm of feature orientation is receiving special interest.

Passau is also a member of the CoreGRID network of excellence which terminated in August 2008 but will continue as an informal interest group. Some of the software engineering and parallelization issue of CoreGRID are also relevant to ArtistDesign.

In the past year, Lengauer has spear-headed the submission of a proposal for a national research activity ("*Schwerpunktprogramm*") to the German Research Foundation ("*Deutsche Forschungsgemeinschaft*") with the title "Many cores for everyone". One of several application areas is the use of multi-cores and many-cores in embedded systems. The national research activity programme is highly competitive, and an acceptance of the proposal is not certain. If granted, funding of €10+ million can be expected for a period of 6 years, funding up to 25 research projects. A decision will have been made by May 2010.

RWTH Aachen:

A close cooperation existed with the ArtistDesign Execution Platforms cluster, in particular between Dortmund, Aachen, and Bologna University. RWTH Aachen participated in the HiPEAC network of excellence and worked on cooperations related to code optimization, e.g. with Edinburgh University and also on simulation techniques and computer architecture, e.g. with FORTH in Greece. Furthermore, Aachen maintained tight industry cooperations, e.g. with CoWare, ACE, and Infineon. ACE's CoSy framework was used in the MAPS Virtual Platform for high level exploration and profiling of embedded MPSoC software. A joint demo-booth highlighting the capabilities of CoSy in terms of providing efficient support for C code instrumentation and high-level code optimization was held in this year's DAC in San Francisco. Another collaboration work between Aachen and ACE was a joint Master thesis with the topic of generating C-code from a high-level intermediate representation of C compiler. RWTH Aachen also invites ACE to give a guest lecture every year in the course of "Compiler Construction" for Master-level students. On June 17, 2009, Dr. Marcel Beemster from ACE visited Aachen to give the guest lecture for this year. The topics covered the compiler backend techniques and new trends towards MPSoC compilation. Since Oct 2006, RWTH Aachen is running the UMIC research cluster (http://www.umic.rwth-aachen.de) of the German excellence initiative. In particular, the flagship project "Nucleus" in the "RF Subsystems and SoC Design" addresses the design challenges of heterogeneous MPSoC platforms for software-defined radio applications, which is in co-operation with TU Kaiserslautern.

Mälardalen:

The WCET analysis group maintains close contacts with several industrial partners, and has conducted a number of case studies using their production codes. The group also interacts heavily with the Component-based Software Engineering community, through the national centre PROGRESS for research on component-based software design for embedded systems. Björn Lisper is one of the founders of the Swedish Multicore Initiative (http://www.multicore.se/), whose purpose is to promote research and dissemination of knowledge in the area of multicore computing.

Saarland University:

Timing-Analysis activities in the cluster interacted closely with the Execution-Platform cluster in the area of increasing the timing-predictability of real-time systems. Saarland University is coordinating the FP7 project PREDATOR, which aims at reconciling performance with predictability. The project, in which several ArtistDesign partners also partake as well as Airbus and Bosch, started in February 2008 and lasts until January 2011. Saarland University works together with several partners, such as AbsInt on timing analysis and SSSA on cache-aware scheduling. Industrial partners such as Airbus, Bosch and Daimler provide further collaborations.

ACE:

ACE worked closely with ST and with Philips having both a commercial relationship with them as well as being co-members of EU project consortia – in one case along with Verimag. ACE has been working closely with Aachen in this domain for some time. One of the results of this cooperation has been the integration of compiler technology in a start-up company that span out of the university. Cooperation with Imperial College and Edinburgh has also started.

AbsInt:

Within the EmBounded Project (IST-510255), AbsInt was also involved in the development of the Hume compiler. Hume is a domain-specific high-level programming language for real-time embedded systems.

TU Berlin:

TU Berlin is generally involved in methods and tools for software engineering for embedded systems. TU Berlin has cooperated with Edinburgh University (Björn Franke) concerning the optimization of compilers based on machine learning techniques. Furthermore, TU Berlin has done research on the verification of embedded operating systems, also by cooperating with the Fraunhofer institute FIRST. Finally, TU Berlin visited and was visited by other cluster members, e.g. ACE, RWTH Aachen and TU Vienna.

Tidorum, York:

Tidorum (and partially York through Rapita Systems) were engaged in a project for the European Space Agency to study the timing and verification aspects of cache memories in space systems. The PEAL project ended in February 2007. An extension was started in late 2007 and ended with a final presentation in April 2009. The main partner from the aerospace domain was Thales Alenia Space, France.

TU Vienna:

TU Vienna worked on measurement-based timing analysis together with TU Munich. It also maintained a close interaction with the Lawrence Livermore National Laboratory, CA, USA, in optimizing high-level abstractions.

-- Changes wrt Y1 deliverable –
Interactions with affiliates and external groups have been intensified.

3. Overall Assessment and Vision for the Cluster

3.1 Assessment for Year 2

Using multi-processor systems continues being a major issue.

There has been progress on the mapping of applications to MPSoCs. The number and breadth of the attendance of this community at the Rheinfels workshop has increased. First tools are available (e.g. from RWTH Aachen and IMEC). The importance of this topic has been recognized on a world-wide basis. Any session on programming multi-cores and multi-processor systems is filled with people. The corresponding session at DATE clearly demonstrates this. Fortunately, ArtistDesign is active in this area. Also, the first workshop on software synthesis attracted a good number of internationally visible attendees. Year 2 will the the starting point for a new series of workshops in this direction.

Within the cluster, timing analysis and timing predictability have seen good progress. The PREDATOR project, which involves several partners of ArtistDesign, has entered its second year and continued the successful work of Year 1. Examples of collaborations include the worst-case execution time aware compiler wcc (Dortmund, AbsInt, USAAR) and cache-aware scheduling (USAAR, SSSA). Other collaborations on hardware design for multi-core systems are underway, but need to be strengthened in the next year: contacts have already been taken with the MPSoC design cluster in this matter.

Technically, the cluster has achieved good results advancing on the way towards timing predictability on multi-core platforms. Several partners have performed work concerning the influence of cache memories on timing predictability. Novel methods have been developed for timing analysis of multicore systems with shared caches, and to bound the context switch penalty due to cache effects in preemptive systems. Also, work on analysis on microarchitectural level has progressed, especielly regarding cache replacement policies and pipeline behaviour. Since the hardware timing models used for these analyses often are hard to derive manually, work has been undertaken to automate the derivation of timing models from VHDL specifications.

On the software side, USaar and AbsInt have studied the possibility to derive mode-specific WCET bounds by identifying operating modes from source code. Such bounds can be significantly sharper than general WCET bounds. TU Vienna has continued the work on timing-composable multicore architectures. Such architecture includes principles for the design of both software and hardware. A timing-composable architecture reclaims timing predictability for multiprocessor systems by allowing separate, accurate timing analyses for individual tasks on different cores.

During year 2, timing analysis activities regarding methods with elements of testing and measurements have picked up. These methods do not provide safe timing estimates in general, but can be appropriate in situations where such estimates are not strictly required. Since current multicore architectures are inherently very difficult to analyse by static, safe methods, this development is very interesting. MDH and York have developed novel methods to identify timing models from observations, based on machine learning and model identification. These methods reduce the need for fine-grain instrumentation of the code, and allow a larger flexibility in timing measurements. Criteria for when the models provide safe timing estimates have also been identified: when these are fulfilled, the methods have the same trustworthiness as methods based on static analysis. Furthermore, TU Vienna, York, and MDH have worked on test-case generation for measurement-based WCET analysis: two approaches have been pursued, where the first is based on segmentation of control flow, and

the second uses an input-sensitive static analysis to search for the input vector causing the longest path to be executed.

Concerning the goal of reconciling timing analysis with compilation as stated in item 2 of Section 1.2, the WCET-aware compiler WCC developed at TU Dortmund has matured in the past 12 months. The compiler is equipped with test-benches consisting of approx. 4000 benchmarks used to check the correctness of the compiler and to verify the effect of its WCET-aware optimizations. In ArtistDesign year 2, WCC has moved from academic research software to a compiler ready for commercialization. In the next 12 months, it is foreseen to extend WCC towards code generation and optimization for multi-process systems, including real-time operating systems. For this purpose, collaboration between TU Dortmund, AbsInt and the ArtistDesign Cluster on Operating Systems and Networks will be strengthened.

-- Changes wrt Y1 deliverable –
The above is new text, not present in the Y1 deliverable. Integration of compilers and timing analysis is also covered in the deliverable of predictability.

3.2 Overall Assessment since the start of the ArtistDesign NoE

The partners got the impression, that the importance of considering compiling for multi-cores, software synthesis and timing predictability is receiving even more attention than in year 1. In this respect, the work of the partners is urgently needed.

The cluster has made good progress advancing the state of the art in timing analysis and timing predictability. In this area, we have achieved significant results for single-core systems with single or multiple tasks. For multi-processor systems, important design principles for ensuring timing predictability have been formulated and are being evaluated. Work on more pragmatic, test-based methods has also progressed significantly.

The level of collaboration between partners is significant. In addition to collaborative research, tools and prototypes are developed and tools are integrated. This level of integration is indicative of the successful collaborative structure of the cluster.

-- Changes wrt Y1 deliverable –
The above is new text, not present in the Y1 deliverable.

3.3 Indicators for Integration

Partners promised the following Interactions:

- The partners promised organizing at least one open, internationally visible workshop on software generation, compilers and timing analysis per year. This promise was kept: the SCOPES workshop was held in April 2009. In addition, the WCET Workshop was held in July 2009. Cluster members also organized the second workshop on mapping applications to MPSoCs, the WESE workshop on embedded system education, the WSS workshop on software synthesis, and a workshop on predictability. So, in total, five instead of one workshop were organized.
- The partners promised integrating at least one timing analysis tool with an experimental compiler, to design optimizations within this compiler considering multiple objectives (including worst-case execution times) and to generate a detailed set of results demonstrating the advantages and limitations of such an integration. This promise was

kept: the integration of aiT and WCC has been completed. The results are being demonstrated in an increasing list of papers (see references). Tradeoffs between multiple objectives have not yet been studied.
http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/

- Partners announced an integration of techniques developed by the high-performance computing community and the compiler for embedded systems community. They predicted having at least one tool flow demonstrating the advantages of combining these approaches and having examples demonstrating the power of the integrated techniques for MPSoCs. According to the "description of the work", compilation techniques will be made available to the MPSoCs community. Along these lines, progress has been made.
- The partners promised publishing at least four joint papers per year. This promise was kept. There are four joint papers for the software synthesis and code generation activity (including submitted papers) and additional joint papers for the timing analysis activity (see section 2.4. of the activity report on timing analysis).
- The activity reports contain information about further cooperation between the partners. We prefer not to repeat it in this report.
- The partners also contributed to the transversal activities and dissemination.

-- Changes wrt Y1 deliverable --
The number of workshops organized was increased.

3.4 Long-Term Vision

The long term vision of the project is to have an impact on the tool landscape supporting embedded computing. We intend to contribute to programming tools for MPSoCs, to timing predictability for all kinds of platforms (including MPSoCs) and to resource-aware platform mapping techniques. We predict that an increasing amount of industrial areas will require a guaranteed timing. However, the trend toward higher performances and the use of multi-processor systems with shared resources is working in the opposite direction. It will be required to raise the awareness of timing issues.

-- Changes wrt Y1 deliverable --
Multi-cores and predictability remain key research trends which will be important in the years to come.

4. Cluster Participants

-- Changes in the Cluster Participants wrt Y1 deliverable --

None.

4.1 Core Partners

Cluster Leader **Activity Leader for "Software Synthesis and Code Generation"**	
	Prof. Dr. Peter Marwedel (TU Dortmund) http://ls12-www.cs.tu-dortmund.de/~marwedel/
Technical role(s) within ArtistDesign	Cluster leader, activity leader SW Synthesis and Code Generation Improved code quality for embedded applications is the main goal of the work at Dortmund University. Due to the widening gap between processor and memory speeds, emphasis has been on improving the efficiency of memory accesses, in terms of average and worst case execution time and in terms of the energy consumption.
Research interests	Peter Marwedel's Embedded Systems Group focuses on embedded software. Particular emphasis is on compilers for embedded processors. One of the very first publications in this area, the book "Compilers for Embedded Processors", edited by Peter Marwedel and Gert Goossens, was the result of the CHIPS project, funded by the European Commission. The group's current focus is on advanced optimizations for embedded processors (e.g. by using bit-level data flow analysis) and energy-aware compilation techniques. Current research also includes high-level transformations of algorithms as well as WCET-aware code generation.
Role in leading conferences/journals/etc in the area	Member of the EDAA (European Design and Automation Association) Main Board. Editorial Board Member of the Journal "Design Automation for Embedded Systems" Editorial Board Member of the Journal of Embedded Computing. Editorial Board Member of the Microelectronics Journal. Editor of the Springer series of books on Embedded Systems (http://www.springer.com/series/8563)

	Co-Founder and Steering Board Chair of the SCOPES Workshop (Software and Compilers for Embedded Systems) Series. >14 years of service for the DATE conference and its predecessors (program chair: 3 times, chairman of the steering committee, European representative to ASPDAC) Various other conferences
Notable past projects	MNEMEE: Memory maNagEMEnt technology for adaptive and efficient design of Embedded systems supported by the European Commission (http://www.mnemee.org) PREDATOR: Design for predictability and efficiency, supported by the European Commission (http://www.predator-projekt.eu) MORE: Network-centric Middleware for group communications and resource sharing across heterogeneous embedded systems, supported by the European Commission http://www.ist-more.org HiPEAC: European NoE on High-Performance Embedded Architecture and Compilation; http://www.hipeac.net MAMS: Multi-Access modular-services framework, national project funded by the German Federal Ministry of Education and Research (BMBF)Others: Various earlier projects supported by the EC, DFG etc.
Awards / Decorations	IEEE Fellow (class of 2010) DATE Fellow, 2008 Teaching award, TU Dortmund, 2003
Further Information	CEO of the Informatik Centrum Dortmund (ICD), a technology transfer centre founded in 1989. Chair of the Education Committee of TU Dortmund

Activity Leader for "Timing Analysis"	
	Prof. Björn Lisper (Mälardalen University) http://www.idt.mdh.se/personal/blr/
Technical role(s) within ArtistDesign	Activity for "Timing Analysis" Timing analysis, program analysis.

Research interests	Timing analysis, static program analysis, language design for embedded and real-time systems, program transformations, parallelism
Notable past projects	FP7 STREP ALL-TIMES, Integrating European Timing Analysis Technology (coordinator). http://www.all-times.org Several national projects, funded by Swedish Research Council, VINNOVA, KKS, SSF, Ericsson

	Dr. Stylianos Mamagkakis IMEC vzw. http://www.imec.be
Technical role(s) within ArtistDesign	Representing IMEC Nomadic Embedded Systems (NES) division in: -Cluster: SW Synthesis, Code Generation and Timing Analysis -Cluster: Operating Systems and Networks -Cluster: Hardware Platforms and MPSoC Design -Intercluster activity: Design for Adaptivity -Intercluster activity: Design for Predictability and Performance -Intercluster activity: Integration Driven by Industrial Applications
Research interests	Stylianos Mamagkakis received his Master and Ph.D. degree in Electrical and Computer Engineering from the Democritus Uni. Thrace (Greece) in 2004 and 2007, respectively. Since 2006, he coordinates a team of PhD students within the NES division at IMEC, Leuven, Belgium. His research activities mainly belong to the field of system-level exploration, with emphasis on MPSoC run-time resource management and system integration.
Role in leading conferences/journals/etc in the area	Stylianos Mamagkakis has published more than 35 papers in International Journals and Conferences. He was investigator in 9 research projects in the embedded systems domain funded from the EC as well as national governments and industry.
Notable past projects	Project leader of MNEMEE IST project http://www.mnemee.org Project leader of OptiMMA IWT project http://www.imec.be/OptiMMA Participation in: 1 international IMEC project (M4), 3 European IST projects (AMDREL, EASY, ARTIST2), 2 Greek projects (PRENED, DIAS)
Awards	1st prize in 'Technogenesis' Competition for Business Innovation, Greece, June'06 3rd prize in 'Otenet Innovation 2006' Competition for Business

	Innovation, Greece, November'06
Further Information	http://www2.imec.be/imec_com/nomadic-embedded-systems.php

	Prof. Dr. Christian Lengauer http://www.infosun.fim.uni-passau.de/cl/staff/lengauer
Technical role(s) within ArtistDesign	Strengthen link between high-performance computing and parallel programming and embedded systems
Research interests	Parallel systems, program analysis, programming methods
Role in leading conferences/journals/etc in the area	Journal editor for: *Parallel Processing Letters*, World Scientific Publ. Co. ; *Science of Computer Programming*, Elsevier Science B.V. ; *Scientific Programming*, IOS Press; *Int. J. of Parallel, Emergent and Distributed Systems*, Taylor & Francis; Chair of the Euro-Par steering committee, Chair of the IFIP WG 2.11 on Program Generation, programme committee member of various conferences
Notable present and past projects	LooPo: a loop parallelizer based on the polytope model (past and present DFG funding); FeatureFoundation: Feature-Oriented Program Synthesis (DFG: 2008-2010, renewable); Meta-Programming (DAAD: 2004-2005, EC FP6: from 2004) PolyAPM: abstract parallel machines for the polytope model (DFG: 2000-2002); HDC: a language for parallel higher-order divide & conquer (DFG: 1996-2000) ; SAT: performance-directed parallel programming (1994-98) ; PLR: parallel linear recursion (1994-98) ; OSIDRIS: object-oriented specification of distributed systems (DFG: 1993-97)

	Prof. Dr. Rainer Leupers http://www.iss.rwth-aachen.de
Technical role(s) within ArtistDesign	SW Synthesis and Code Generation, code optimization
Research interests	Compilers, ASIP design tools, MPSoC design tools
Role in leading conferences/journals/etc in the area	TPC member of DAC, DATE, ICCAD etc. Co-founder of SCOPES workshop General Co-Chair of MPSoC Forum 2008 (www.mpsoc-forum.org)
Notable past projects	HiPEAC NoE, SHAPES IP, several DFG-funded projects

	Industry-funded projects with Infineon, Philips, Microsoft, CoWare, ACE, Tokyo Electron etc.
Awards / Decorations	Several IEEE/ACM best paper awards
Further Information	Co-founder of LISATek Inc. (acquired by CoWare Inc.) European Commission expert in FP7 Editor of "Customizable Embedded Processors", Morgan Kaufmann, 2006 Steering committee member of UMIC (Ultra High-Speed Mobile Information and Communication) research cluster (www.umic.rwth-aachen.de)

	Prof. Dr. Dr. h.c. mult. Reinhard Wilhelm (Saarland University) http://rw4.cs.uni-sb.de/people/wilhelm
Technical role(s) within ArtistDesign	Timing Analysis
Research interests	Compilers, Static Analysis, Timing Analysis
Role in leading conferences/journals/etc in the area	PC member of SCOPES, LCTES, MEMOCODE, RTSS etc. Steering committee member of EMSOFT, member at large of the steering committee of LCTES Member of the ACM SIGBED Executive Committee
Notable past projects	DAEDALUS
Awards / Decorations	Prix Gay-Lussac-Humboldt in 2007 Honorary doctorates of RWTH Aachen and Tartu University in 2008 Konrad-Zuse Medal in 2009
Further Information	Co-founder of AbsInt Angewandte Informatik GmbH Scientific Director of the Leibniz Center for Informatics Schloss Dagstuhl

	Prof. Dr. Peter Puschner (TU Vienna) Real-Time Systems Group Institute of Computer Engineering Vienna University of Technology http://www.vmars.tuwien.ac.at/people/puschner.html
Technical role(s) within ArtistDesign	Peter Puschner and his group are participating in the Timing-Analysis activities of the Compilation and Timing Analysis cluster. Within ArtistDesign the contributions are in the area of path-description languages for static WCET analysis, compilation support for WCET analysis, methods and problems of measurement-based execution-time analysis, and on software and hardware architectures that support time predictability.
Research interests	Peter Puschner's main research interest is on real-time systems. Within this area he focuses on Worst-Case Execution-Time Analysis and Time-Predictable Architectures.
Role in leading conferences/journals/ etc in the area	Member of the Euromicro Technical Committee on Real-Time Systems, the steering committee of the Euromicro Conference on Real-Time Systems (ECRTS) Member of the advisory board and organizers committee of the IEEE International Symposium on Object- and Component-Oriented Distributed Computing (ISORC) conference series Chair of the Steering Committee of the Euromicro Workshop on Worst-Case Execution-Time Analysis (WCET) series
Notable past projects	DECOS - Dependable Embedded Components and Systems Develop the basic enabling technology to move from a federated distributed architecture to an integrated distributed architecture. http://www.decos.at MoDECS - Model-Based Development of Distributed Embedded Control Systems Model-based construction of distributed embedded control systems: shift from a platform-oriented towards a domain-oriented, *platform-independent* development of composable, distributed embedded control systems. http://www.modecs.cc NEXT TTA Enhance the structure, functionality and dependability of the

	time-triggered architecture (TTA) to meet the cost structure of the automotive industry, while satisfying the rigorous safety requirements of the aerospace industry. http://www.vmars.tuwien.ac.at/projects/nexttta/

	Dr. Iain Bate (University of York) http://www-users.cs.york.ac.uk/~ijb/
Technical role(s) within ArtistDesign	Responsible for the WCET cluster at University of York. Also involved in the Design for Adaptivity cluster.
Research interests	Worst-case execution time analysis. Design and certification of critical real-time systems. Design for flexibility. Search-based systems engineering. Use of novel computation techniques, e.g. Artificial Immune Systems.
Further Information	Also director of Origin Consulting (York) Ltd. a spin-off company providing consultancy on the design and certification of critical systems.

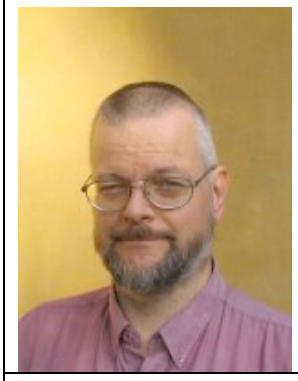
4.2 Affiliated Industrial Partners

	Joseph van Vlijmen (ACE, Netherlands)
Technical role(s) within ArtistDesign	The design and construction of extensions to CoSy required for ArtistDesign projects.
Research interests	The development and exploitation of compilation techniques and development systems in the wider contexts of SoC and EDA supported by descriptions of the system including application and target architectures. Particular interests include MPSoC and highly parallel system.
Role in leading conferences/journals/etc in the area	Programme Committees of SCOPES and DATE.
Notable past projects	COMPARE/PREPARE ESPRIT projects: These projects particularly COMPARE, were precursors for CoSy. PREPARE focused on retargetable compilation for Fortran 90 and High Performance Fortran using massively parallel MIMD machines. MESA/NEVA (ongoing): Framework IPs addressing the challenges of designing and

	constructing multi-processor systems.
Further Information	Principal architect of the CoSy. Previously, architect of ACE's shared memory heterogeneous multiprocessor UNIX OS.

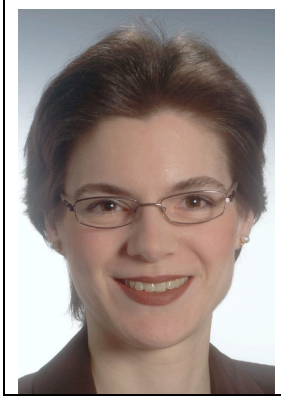
	Dr. Marco Bekooij (NXP)
Technical role(s) within ArtistDesign	Strengthen link to work on code synthesis and industry
Research interests	Design of predictable systems

	Dr.ir. Bart Kienhuis (Compaan Design B.V., Leiden) http://www.liacs.nl/~kienhuis/
Technical role(s) within ArtistDesign	Strengthen link to work on code synthesis and industry
Research interests	Design of predictable systems

	Dr. Niklas Holsti (Tidorum Ltd) http://www.tidorum.fi
Technical role(s) within ArtistDesign	Participate in the definition of the common WCET tool-set architecture, the analysis modules and the interchange representations (languages, file formats). Adapt Tidorum's WCET tool, Bound-T, to integrate with the architecture and interchange formats defined in ArtistDesign
Research interests	Static analysis of the worst-case execution time of embedded programs.

	Dr. Christian Ferdinand (AbsInt Angewandte Informatik GmbH) http://www.absint.com/
Technical role(s) within ArtistDesign	Christian Ferdinand coordinates the activities of AbsInt within Artist Design.
Research interests	Timing analysis, program optimization, and compiler construction.
Notable past projects	Transferbereich 14 "Run-time Guarantees for modern Processor Architectures" of the German DFG. DAEDALUS RTD project IST-1999-20527 of the European FP5 program on the validation of software components embedded in future generation critical concurrent systems by exhaustive semantic-based static analysis and abstract testing methods based on abstract interpretation. http://www.di.ens.fr/~cousot/projects/DAEDALUS/index.shtml INTEREST EU Framework VI Specific Targeted Research Project IST-033661 aiming at overcoming the lack of integration and interoperability of tools for developing Embedded Systems software. http://www.interest-strep.eu/
Awards / Decorations	Dr. Ferdinand received the Dr. Eduard Martin Preis in 1999 (award for best PhD Thesis in computer science at Saarland University). AbsInt has been awarded a 2004 European Information Society Technology (IST) Prize for its timing analyzer aiT.

4.3 Affiliated Academic Partners

	Prof. Dr. Sabine Glesner (Technical University of Berlin) www.pes.cs.tu-berlin.de

Technical role(s) within ArtistDesign	Activity Leader for Compiler Platform Compiler Verification
Research interests	Compilers, Verification, Embedded Systems and Software, Formal Semantics
Role in leading conferences/journals/etc in the area	PC Member of Compiler Construction 2007 Date'06, Design, Automation and Test in Europe, TPC Member of Topic B9 on Formal Verification Workshop Compiler Optimization meets Compiler Verification COCV, ETAPS Conferences, PC Member in 2005 and 2006, Program Co-Chair in 2007 Workshop Formal Foundations of Embedded Software and Component-Based Software Architectures (FESCA), ETAPS Conferences, PC Member 2005 and 2006 Editorial Board Member of "Informatik – Forschung und Entwicklung" by Springer, starting with Vol. 21, No. 1
Notable past projects	VATES (Verification and Transformation of Embedded Systems), funded by DFG Aktionsplan Informatik (Emmy Noether-Program), funded by DFG, support for young researchers to build a research group, with a focus on optimization and verification in the compilation of higher programming languages, from 2004 to 2009 Correct and Optimizing Compilers for Modern Processor Architectures, funded by a PostDocs excellence program of Baden-Württemberg, Germany, 2003-2005 Grant in the Wrangell-Habilitation Program of Baden-Württemberg, Germany, 2001-2005
Awards / Decorations	Award of the "Forschungszentrum Informatik" for one of the two best PhD theses of the Faculty for Computer Science, University of Karlsruhe, 1998/99 Member of the "Studienstiftung des deutschen Volkes", the German national scholarship organization, 1991-1996 Fulbright grant to study at the University of California, Berkeley, 1993-1994 Member of the Siemens Internationaler Studenten / Doktorandenkreis, 1993-1999

	Dr. Björn Franke (Lecturer, University of Edinburgh) http://homepages.inf.ed.ac.uk/bfranke/Welcome.html
Technical role(s) within ArtistDesign	Provide a link to work on program analysis and parallelization
Research interests	Compilers, embedded systems

	Prof. Paul Kelly (Imperial College, London) http://www.doc.ic.ac.uk/~phjk/
Technical role(s) within ArtistDesign	Provide a link to work on program analysis and parallelization
Research interests	Software performance optimization

Dr. Alain Darte

Scientific leader of Inria Project Compsys
(Compilation and Embedded Computing Systems)

Laboratoire de l'Informatique du Parallélisme

CNRS, Inria, UCBL, ENS-Lyon

http://perso.ens-lyon.fr/alain.darte	
Technical role(s) within ArtistDesign	Activity in automatic parallelization, source to source transformations for high-level synthesis of hardware accelerators,

	possibly WCET.
Research interests	Code optimizations for embedded computing systems: back-end code optimizations (SSA form, register allocation, static/JIT compilation), source-to-source code transformations for HLS tools (code rewriting, memory and communication optimizations).
Role in leading conferences/journals/etc in the area	Editorial board of ACM Transactions on Embedded Computing Systems (ACM TECS). Program committees in 2008-09: SCOPES 2009, PLDI 2008, CC 2008. Before 2008: many DATE, CASES, ASAP, ICS, CGO, etc.
Notable past projects	Minalogic project SCEPTRE Collaboration with STMicroelectronics, funded by French Ministry of Research and Région Rhône-Alpes
Awards / Decorations	Best paper awards: IPDPS 2002, CGO 2007

4.4 Affiliated International Partners

Prof. Abhik Roychoudhury

(Associate Professor, National University of Singapore) http://www.comp.nus.edu.sg/~abhik/	
Technical role(s) within ArtistDesign	Timing Analysis
Research interests	Software Analysis/Validation, Design Tools for Embedded Systems, Formal Methods in System Design.
Role in leading conferences/journals/etc	Recent Program Committee work includes:

in the area	Intl. Conf. on Software Engineering (ICSE) 2009 – Tools Track, Intl. Symp. on Automated Technology for Verification and Analysis (ATVA) 2009.
Notable past projects	"Timing Analysis of Behavioural System Models" (2007 -10) http://www.comp.nus.edu.sg/~abhik/projects/model-timing/ "EASEL: Engineering Architectures and Software for the Embedded Landscape" (2006-09), Funded by A*STAR Singapore under Embedded and Hybrid Systems Programme. "Chronos: Architectural Modelling for Timing Analysis of Embedded Software" (2003 – 07) http://www.comp.nus.edu.sg/~rpembed/chronos/
Awards / Decorations	Tan Kah Kee Young Inventor's Award 2008.

5. Internal Reviewers for this Deliverable

- Andreas Heinig (TU Dortmund)
- Prof. Dr. Olaf Spinczyk (TU Dortmund)