IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Cluster Progress Report for Year 2

Cluster:
Hardware Platform and MPSoC Design

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Policy Objective (abstract)

The purpose of this cluster is to integrate different view points and approaches to MPSoC design and programming. The cluster will consider the hardware architecture and software components in their interaction, investigate tools for accurate estimation of certain design parameters (power, performance), and provide the designer with adequate support for design space exploration and optimization.

Versions

number	comment	date
1.0	First version delivered to the reviewers	December 18th 2009

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1. Overview

In relation to the ArtistDesign network, it is the overall goal of the topic on hardware platforms and MPSoC design to extend the current state in composability towards issues like modeling of non-functional constraints, power and energy, end-to-end real-time behavior, timing and performance analysis and heterogeneous models of computation.

Many application domains require adaptive real-time embedded systems that can change their functionality over time. In such systems it is not only necessary to guarantee timing constraints in every operating mode, but also during the transition between different modes. Therefore, it is one of the goals to develop new methods for the design and analysis of adaptive multi-mode systems.

One of the most critical issues to be faced in the research on execution platform is their rapidly growing complexity. Complexity increase is pushed by Moore's law, and by the ever-increasing demand for high performance computing. In addition, the boundaries between hardware and software domains are getting more blurred (dynamically re-configurable hardware, adaptable embedded systems, breakthrough in power consumption and performance) and challenging questions are at the border (trade-offs in mapping applications to hardware and software components, re-configurable hardware, WCET, performance of distributed computer and communication systems).

The cluster attempts to combine the diverse knowledge and to integrate different approaches in the area of execution platforms for embedded systems available in Europe and beyond.

1.1 High-Level Objectives

The purpose of this cluster is to integrate different view points and approaches to MPSoC design and programming. Therefore, the work is based on existing and future hardware platforms and their expected properties as well as anticipated application domains. The cluster will consider the hardware architecture and software components in their interaction, investigate tools for accurate estimation of certain design parameters (power, performance) based on appropriate models for hardware and software components, and provide the designer with adequate support for design space exploration and optimisation.
The importance of resource awareness in embedded systems is growing very rapidly. One major aspect is predictability, in particular concerning the timing behaviour. With the growing software content in embedded systems, and the diffusion of highly programmable and re configurable platform, software is given an unprecedented degree of control on resource utilization. Therefore, the major focus of the combined activities is to establish a design methodology that;

- scales to massively parallel and heterogeneous multiprocessor architectures,
- allows for predictable system properties
- uses the available hardware resources in an efficient manner.

Promising approaches are based on increasing the adaptivity on various levels and on composable frameworks.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.2 Industrial Sectors

As hardware platforms are the backbone of embedded systems, the activities of this cluster spans all industrial sectors. A recent and accelerating trend is the move towards multicore platforms.

In the automotive domain, the increasing number of functions has led to automotive networks with a large number of distributed ECUs and increasing complexity with several busses and gateways that is difficult to handle. In next generation systems, large automotive OEMs are therefore proposing new structured hardware topologies, that focus on the application of powerful domain controllers connected over a high speed bus and several dedicated busses for the different functional domains. Multicore control units (MCUs) are perceived as a co-enabler for this technology, by allowing the integration of a large number of functions, at relatively low power and with various reliability and fail-safe options.

A similar trend can be observed in the aerospace domain, where multicore components need to be integrated into complex networks with commonly very high reliability requirements.

In the multimedia domain, the emerging trend for multimedia applications on mobile terminals, combined with a decreasing time-to-market and a multitude of standards have created the need for flexible and scalable computing platforms that are capable of providing considerable (application specific) computational performance at a low cost and a low energy budget. Platforms like TI OMAP, ST Nomadik, Philips Nexperia and IBM/Toshiba/Sonys CELL, contain multiple heterogeneous, flexible processing elements, a memory hierarchy and I/O components. All these components are linked to each other by a flexible on-chip interconnect structure. These architectures meet the performance needs of multimedia applications, while limiting the power consumption.

Also in the mechatronics domain, which traditionally was a rather sequential process, there is a trend towards multi-core platforms and the need to support the designer to make well-founded choices for an execution platform. Techniques from the multimedia domain are now being extended and adapted to deal with control-dominated high-tech applications as well.

Another clear trend is towards reconfigurable architectures, in general, and configurable processors, in particular. The generic goal is to achieve a high degree of flexibility (traditionally available only with software implementation) at an power consumption, which is much lower than achievable with a traditional software implementation using general purpose processors.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.3 Main Research Trends

Many embedded system applications are implemented today using distributed architectures, consisting of several hardware nodes interconnected in a network. Each hardware node can consist of a processor, memory, interfaces to I/O and to the network. The networks are using specialized communication protocols, depending on the application area. For example, in the automotive electronics area communication protocols such as CAN, FlexRay and TTP are used. One important trend today is toward the integration of multiple cores on the same chip, hence embedded systems are not only distributed across multiple boards or chips, but also within the same chip.

As the complexity of the functionality increases, the way it is distributed has changed. If we take as an example the automotive applications, initially, each function was running on a

dedicated hardware node, allowing the system integrators to purchase nodes implementing required functions from different vendors, and to integrate them into their system. Currently, number of such nodes has reached more than 100 in a high-end car, which can lead to large cost and performance penalties. Moreover, with the advent of poly-core (i.e. high cardinality multi-core) single-chip platforms, the effective number of processing nodes tends to grow in a "fractal" way, and future distributed systems with thousands of processing nodes are not a far away dream.

Not only the number of nodes has increased, but the resulting solutions based on dedicated hardware nodes do not use the available resources efficiently in order to reduce costs. For example, it should be possible to move functionality from one node to another node where there are enough resources (e.g., memory) available. Moreover, emerging functionality, such as brake-by-wire, is inherently distributed, and achieving an efficient fault-tolerant implementation is very difficult in the current setting.

Moreover, as the communications become a critical component, new protocols are needed that can cope with the high bandwidth and predictability required. The trend is towards hybrid communication protocols, such as the FlexRay protocol, which allows the sharing of the bus by event-driven and time-driven messages. Time-triggered protocols have the advantage of simplicity and predictability, while event-triggered protocols are flexible and have low cost. A hybrid communication protocol like FlexRay offers some of the advantages of both worlds. The need for scalable and predictable communication is not only a characteristic of automotive designs, but even multimedia and signal processing systems are increasingly communication dominated.

While computation and communication are clear targets, common consensus has been growing on the criticality of memory architecture and related memory management software challenges. Even predictable and efficient processors and communication fabrics are not sufficient to provide a predictable and efficient application level view of the platform if not adequately supported by a memory system.

The trend towards distributed architectures introduces a new challenge. A lot, if not most of the traditional software is sequential in nature. Major reason for this is that most modern programming languages are sequential and do not have adequate language-level concurrency support. Traditionally the timing performance of software increased as a result of the increase in clock speed of the individual processing cores. However, this free lunch is over because clock speeds have hardly increased since 2003. Multi-core and hyperthreading techniques are now used to boost platform performance. Modern compilers based on sequential programming languages are not able to sufficiently utilize these additional computational resources. New languages, techniques and tools are required that seamlessly match modern execution platforms, for instance by adequate application-level concurrency support. Although a number potential techniques already exist, getting more momentum in these directions is crucial to deal with future complexity and performance requirements.

With growing embedded system complexity more and more parts of a system are reused or supplied, often from external sources. These parts range from single hardware components or software processes to hardware-software (HW-SW) subsystems. They must cooperate and share resources with newly developed parts such that the design constraints are met. There are many software interface standards such as CORBA, COM or DCOM, to name just a few examples that are specifically designed for that task. Nevertheless in practice, software integration is not a solved but a growing problem. This is especially true when performance and energy efficiency can be achieved only if a sufficient degree of parallelism in application execution is achieved.

New design optimization tools are needed to handle the increasing complexity of such systems, and their competing requirements in terms of performance, reliability, low power

consumption, cost, time-to-market, etc. As the complexity of the systems continues to increase, the development time lengthens dramatically, and the manufacturing costs become prohibitively high. To cope with this complexity, it is necessary to reuse as much as possible at all levels of the design process, and to work at higher and higher abstraction levels, not only for specification of overall system functionality, but also for supporting communication among a number of parallel executing nodes.

One of the most significant achievements in the cultural landscape of low-power embedded systems design is the consensus on the strategic role of power management technology. It is now widely acknowledged that resource usage in embedded system platforms depends on application workload characteristics, desired quality of service and environmental conditions. System workload is highly non-stationary due to the heterogeneous nature of information content. Quality of service depends on user requirements, which may change over time. In addition, both can be affected by environmental conditions such as network congestion and wireless link quality.

Power management is viewed as a strategic technology both for integrated and distributed embedded systems. In the first area, the trend is toward supporting power management in multi-core architectures, with a large number of power-manageable resources. Silicon technology is rapidly evolving to provide an increased level of control of-on chip power resources. Technologies such as multiple power distribution regions, multiple power-gating circuits for partial shutdown, multiple variable-voltage supply circuits are now commonplace. The challenge now is how to allocate and distribute workload in an energy efficient fashion over multiple cores executing in parallel. Also, one open issue is how to cope with the increasing amount of leakage in nanometer technologies, which tends to over-emphasize the cost of inactive logic, unless it can be set in a low-power idle state (which in many cases implies storage losses and high wakeup cost).

In the area of distributed low-power systems, wireless sensor networks are the key technology drivers, given their tightly power constrained nature. One important trend in this area is toward “battery free” operation. This can be achieved through energy storage devices (e.g. super-capacitors) coupled with additional devices capable of harversting energy from environmental sources (e.g. solar energy, vibrational energy). Battery-free operation requires carefully balancing harvested energy and stored energy agains the energy consumed by the system, in a compromise between quality of service and sustainable lifetime.

The concept of Multiprocessors-on-a-chip (MPSoC) has been discussed since some years but it appears that recently, the area has gained much more interest. In terms of industrial support, an increasing number of companies are active in the design of corresponding architectures as well as introducing the first products in the market. Whereas there are major breakthroughs in terms of new hardware architectures, corresponding programming environment are still at their infancy. In particular, ease of application specification, scalability, predictability of the overall system, parallelization, low power operation, efficiency and support of legacy code are just some of the main problems the community is facing.

A major industrial concern that comes with the integration of previously independent functions onto a single multicore or multiprocessor-system-on-chip is the resulting reliability of the individual functions. Depending on the criticality of a function, OEMs and indirectly their suppliers deliver guarantees to lawmakers on the overall failure rate of the system or component, with higher cost associated with the certification of higher level of reliability. Integration of functions with different reliability levels is then not cost efficient, if the resulting system needs to be verified for the highest level of reliability. A major research direction is therefore the investigation of methods that allow the co-integration of such functions. The researchers in ArtistDesign investigate countermeasures to this problem, for example by orthogonalization of the shared memory (e.g. Linköping University), or conservative bounds on the use of shared resources (e.g. TU Braunschweig).

A new and emerging research field related to embedded systems is that of design optimization for digital microfluidic biochips. Microfluidic biochips (also referred to as lab-on-a-chip) represent a promising alternative to conventional biochemical laboratories, and are able to integrate on-chip all the necessary functions for biochemical analysis using microfluidics, such as, transport, splitting, merging, dispensing, mixing, and detection. Biochips offer a number of advantages over conventional biochemical procedures. By handling small amount of fluids, they provide higher sensitivity while decreasing the reagent consumption and waste, hence reducing cost. Moreover, due to their miniaturization and automation, they can be used as point-of-care devices, in areas that lack the infrastructure needed by conventional laboratories. Due to these advantages, biochips are expected to revolutionize clinical diagnosis, especially immediate point of care diagnosis of diseases. Other emerging application areas include drug discovery, DNA sequencing, tissue engineering and chemical detection. Biochips can also be used in monitoring the quality of air and water, through real-time detection of toxins.
The digital microfluidic biochip is based on the manipulation of discrete, individually controllable droplets, on a two-dimensional array of identical cells. Due to the analogy between the droplets and the bits in a digital system, where are many similarities between the design of digital systems and digital microfluidic systems. Biochips, consisting of hundreds and thousands of cells have already been successfuly designed and commercialized. The actuation of droplets is performed by software-driven electronic control, without the need of micro-structures. Since each cell in the array is controlled individually, cells can be reconfigured during the execution of an assay to perform differents operations. Digital microfluidic biochips are expected to be integrated with microelectronic components in next generation system-on-chips. Consequently, models and techniques for the analysis and design of such systems are needed, including “biochemical compilers” which are able to efficiently map a biochemical application onto a digital microfluidic biochip.

-- Changes wrt Y1 deliverable --

New paragraph on digital microfluidic biochips.

2. State of the Integration in Europe

2.1 Brief State of the Art

Modern embedded systems for multimedia, imaging, and signal processing are characterized by high performance requirements on the one hand and stringent power requirements on the other hand. Often, these requirements can no longer be satisfied by embedded system architectures based on a single processor. Thus, emerging embedded system-on-chip platforms are increasingly becoming multiprocessor architectures. To compensate the high nonrecurring costs for designing and manufacturing multiprocessor chips, however, they need to be flexible such that they can be reused in different systems. This flexibility calls for programmability and sometimes reconfigurability. As a result, embedded systems platforms often have a heterogeneous architecture consisting of fully dedicated hardware components and different programmable processor cores.

A considerable number of multi-processor design frameworks have been proposed in the past, such as Artemis, Distributed Operation Layer (DOL), Embedded System-Level Platform Synthesis and Application Mapping (ESPAM), Koski, or StreamIt. While all frameworks provide an automated path from application specification to system implementation, they focus on different aspects of the design flow. In ArtistDesign, we attempt to unify the approaches developed by the various partners and extend them towards new methods for performance analysis, design space exploration and adaptivity.

The past several years have seen an increasing interest in wireless sensor nodes that are scavenging energy from their environment. In [5], several technologies have been discussed how, e.g., solar, thermal, kinetic or vibrational energy may be extracted from a node‘s physical environment. In particular, techniques to harvest energy via photovoltaic cells have attracted the interest of the sensor network community [6]. Solar energy is certainly one of the most promising energy sources and typical environmental monitoring applications have access to solar energy. If sensor nodes are equipped with photovoltaic cells as energy transducers, the autonomy of sensor nodes is increased substantially since frequent recharging and replacement of the batteries becomes unnecessary. Ideally, sensor nodes once deployed in a harsh environment benefit from a drastically increased operating time and become virtually immortal.

Clearly, the power generated by small solar cells is limited. Sensor nodes executing a given application may frequently run out of energy in times with insufficient illumination. If one strives for predictable, continuous operation of a sensor node, common power management techniques have to be reconceived. In addition to perform classical power saving techniques, the sensor node has to adapt to the stochastic nature of solar energy. Goal of this adaptation is to maximize the utility of the application in a long-term perspective. The resulting mode of operation is sometimes also called energy neutral operation: The performance of the application is not predetermined a priori, but adjusted in a best effort manner during runtime and ultimately dictated by the power source. Therefore, storage devices like batteries are solely used as energy buffers to compensate the variations of the underlying energy source. It is the goal of the interaction in ArtistDesign to improve the state-of-the-art in energy scavenging and the corresponding algorithms to adapt the running applications so as to optimize a long-term reward function.

Design and analysis of biochip platforms from a computer science point of view is still largely inexplored in Europe. Only a few groups are working on CAD techniques for digital microfluidic based biochips. More groups are working on these biochips from the physical and materials science perspective.

-- Changes wrt Y1 deliverable --

Added a paragraph on biochips.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

Following the activities presented in the previous section, the cluster on execution platforms follows the following strategy and uses the following mechanisms to spread the knowledge and integration achieved so far:

- Summer Schools and Training Activities to distribute the knowledge acquired in ArtistDesign to (a) other countries, (b) other communities and (c) young researchers.
- Tutorials at major conferences to reach new and larger research communities.
- Joint publications between partners, which not only show the integration within the cluster but are an excellent instrument to disseminate the integration results.
- New research projects with industrial partners, which allow us to apply the obtained results at an industrial scale. This way, we also receive feedback and ideas for new research directions.
- Cooperation with other research groups, especially outside the EU (mostly USA and Asia). In this case, spreading excellence is not the only objective. The cluster participants can be exposed to new research problems and new approaches that can be then explored and improved within the cluster.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

2.3 Other Research Teams

It appears that main research groups in Europe dealing with execution platforms for embedded systems are in the ArtistDesign network, either as full or as affiliated partners. There are some exceptions though, caused by the fact that not all are accepting a European network of Excellence as a viable funding instrument. In the following, some of these groups are listed together with their relation to ArtistDesign.

The University of North Carolina at Chapel Hill, Sanjoy Baruah and Jim Anderson. Sanjoy Baruah and Jim Anderson are known in particular for their research in the domain of multiprocessor real-time scheduling.

University of Dresden, Hermann Härtig. Hermann Härtig is a leading researcher in the domain of micro-kernel based real-time operating systems.

Low power embedded systems design: In the area of low power embedded systems design, several new and relevant research thems are explored by other teams, not included in the ARTIST2 network. In particular research groups in the USA have a long tradition of excellence in low power research. We can mention the group lead by prof. Jan Rabaey in UC Berlely, which is carrying out ground-breaking work on hardware platforms for wireless sensor networks. In the same area, several other groups are performing top-level research, e.g.

Anantha Chandrakasan's group at MIT and David Blaauw's group at University of Michigan. Low power execution platforms are not relevant only for wireless sensor network, but also for mobile computing and even for servers and traditional computing infrastructure (e.g. servers). In these areas, the groups lead by Profs. Vijaykrishnan Narayanan, Mahmut Kandemir and Mary Jane Irwin at Penn State University, has produced a large number of interesting results in the last few years. We mention in particular their work on power issues for 3D integration and their analysis of power vs. reliability tradeoffs in high-performance computing. In this area, very interesting work is also performed by the group of prof. Kevin Skadron. The focus of this group is on thermal issues, which are very significant for high-performance system.

Universita degli Studi di Verona/Electronic Design Automation (EDA) group, Prof. Franco Fummi. Main research activities of the EDA group concern system verification, system synthesis and optimization, hardware description languages, power consumption, language abstraction, and system testing. Interactions with members of the execution platforms cluster are, for example, by participation in European projects (e.g. the STRP "Vertigo") together with the Linköping group.

University of Southampton,/Electronic Systems Design Group, Prof. Bashir Al Hashimi. The Electronic Systems Design (ESD) Research Group is internationally recognized in two main areas - the development of novel algorithms and methodologies for Electronic Design Automation to support the design and test of large systems, and for intelligent sensor micro-systems. The group is working in the areas of system modeling, simulation, and synthesis, SoC design and testing, as well as smart sensors. Several cooperation projects have been undertaken, in particular with the Linköping group.

Carnegie Mellon University/System Level Design Group/Prof. Radu Marculescu. The System Level Design group performs research on formal methods for system-level design of embedded applications. They, in particular, focus on fast methods for power and performance analysis that can guide the design process of portable information systems. Important results have been obtained with regard to the communication-centric SOC design, providing formal support for analysis and optimization of novel on-chip communication architectures. In particular, this work addresses fundamental research problems for defining scalable and flexible communication schemes via the Network-on-Chip (NoC) approach. Interaction has been by, for example, PhD student exchanges with the Linköping group.

Marco Caccamo (Univ. of Illinois at Urbana-Champaign): Real-time embedded systems are increasingly using Commercial-Off-The-Shelf (COTS) components in an effort to raise performance and lower production costs. In particular, fast multicore CPUs and high-performance DMA peripherals are required to service demanding applications such as video processing that are becoming more and more popular in markets such as automotive and avionic systems. Unfortunately, COTS components are not designed with timing predictability in mind, which makes it challenging to integrate them in real-time systems. In particular, most COTS architectures feature a single-port main memory that is shared among all CPU cores and peripherals. When a task suffers a cache miss, contention for access to main memory can significantly delay cache line fetch and greatly increase the worst case execution time (WCET) of the task. ETH Zuerich in cooperation with Marco Caccamo (Univ. of Illinois at Urbana-Champaign) developed a WCET analysis method for multi-core systems where tasks share a single memory. In particular, the joint work as published in DATE2010 provides the following contributions: (1) the computation of a curve bounding the memory traffic for each core, given a set of executed tasks. (2) an innovative algorithm that computes a delay bound for a task given traffic curves for all other cores and peripheral buses in the system. The algorithm is able to distinguish the behaviour of DMA peripherals, whose traffic is buffered, from the behaviour of CPU cores, which stall on cache misses. Overall this allows one to compute memory delay bounds for systems comprising any number of cores and any number of peripheral buses sharing a single main memory.

-- Changes wrt Y1 deliverable --

The research team of Marco Caccamo from Univ. of Illinois at Urbana-Champaign has been added.

2.4 Interaction of the Cluster with Other Communities

In terms of the design of highly reliable distributed embedded systems there is a close relationship to the Wireless Sensor Network Community. Especially ETH Zurich maintains close relations in terms of joint research activities and organization of conferences. One of the major conferences in this community, i.e. SENSYS, will be hosted by ETH Zurich in 2010. In terms of research, it is still an open issue how to design highly reliable and dependable sensor networks for applications in safty and security. The area of wireless sensor networks had a huge impact on the research in various fields related to electrical engineering and computer science. Spatially distributed sensor nodes are used as a new kind of measurement instruments to collect physical or environmental data. Examples of related research topics are low-power hardware design including wireless transceivers and microcontrollers, energy scavenging technologies, protocols for ad-hoc networks including multi-hop routing and topology control, operating systems and middleware, security, mobility, simulators and deployment support. Much of this work was driven by the early vision of SmartDust [JM Kahn, RH Katz and KSJ Pister: Next century challenges: mobile networking for “Smart Dust”, 1999] where the individual devices will eventually be the size of a grain of sand, or even a dust particle. As a result of this challenging and inspiring vision of self-contained sensing, computation, communication and power, research in several of the above themes has been concentrating on concepts that reach the overall functionally of sensing network by means of redundancy and basic concepts of self-organization. One of the corner stones to achieve the required quality of service in terms of sensing density in time and space is over-provisioning.

The field of wireless sensor networks is now in a stage where serious applications of societal and economical importance are in reach such as industrial process monitoring and control, environment monitoring, logistics, healthcare applications, home automation, and traffic control.

The above mentioned concept of ‘reliability via over-provisioning’ that underlies much of the wireless sensor networks research so far is not suited to application domains that require dependability. Instead, all measurements are precious and must not be lost, reliable data must arrive in real-time, sensors are relatively expensive, and deployment of a sensor network and repair/update are very labor-intensive and expensive. One can argue that in order to significantly advance application domains by using a wireless sensor network as a novel means of observation and interaction, it is inevitable that such a tool be created as a quality scientific instrument with known and predictable properties and not a research toy delivering average observations at best. As a result, a new path in wireless sensor network research must be entered that is clearly distinguished from classical approaches and opens up new perspectives and challenges.

Research and development of several advanced sensing technologies and their systemlevel integration via systems and software engineering will be necessary: (a) Model-based design to ensure dependable operation in a highly resource-constraint setting. (b) Optimized use of harvested solar energy through long-term reward maximization. (c) Multi-objective optimization of the multi-processor hardware platforms (signal processor for preprocessing and sensor

fusion, communication infrastructure) of a hierarchical system set-up. (d) Development of energy-efficient algorithms for real-time event detection. All of these research challenges are closely related to efforts in Cluster 2 of ARTISTDesign and a close relation to the WSN community is necessary for information exchange and joined research activities.

Participants of the MPSoC cluster (DTU, TU Braunschweig, Symtavision) and other ArtistDesign members (e.g. Aalborg University) are also contributing to the RECOMP project proposal, that was submitted in response to the second call for proposals of the European JU Artemis. Here, partners from automotive, avionics, and industrial automation (e.g. Intel, Infineon, Sysgo, Elektrobit, EADS IW, Delphi, TÜV Nord, and others) come together. The goal is to develop methods, tools and platforms for enabling cost-efficient certification and re-certification of safety-critical multi-core systems, with special emphasis on the design of mixed-criticality systems.

The research topics of this cluster with respect to multicore systems are mirrored by an increasing interest from industrial partner. For example, TU Braunschweig and GM Labs collaborate in the COMBEST project on the definition of methods and tools for the timing analysis of automotive systems based on a mix of complex communication protocols/software scheduling techniques. Already in 2008, a research cooperation between TU Braunschweig, Toyota Information Technology Center (T-ITC), and Symtavision GmbH has been initiated, investigating the effects of errors on reliability and safety of real-time networks.

KTH has a strategic and increasing collaboration with Fudan University in Shanghai and National University of Defense Technology in Changsha, China. It has been facilitated and fostered by visits of faculty, joint courses, exchange of students and joint research projects. At KTH the Electronic Systems department hosts and educates almost ten PhD students from these two Universities and we expect this number to grow further as part of exchange programs. KTH faculty has given many short and long courses at Fudan during the last five years and several joint research projects in the areas of NoC, low power techniques and RFIDs have been initated. We believe in the mutual benefit of these partnerships due to complementare competence profiles (NoC and MPSoC at KTH; computer architecture at NUDT; security and RFID at Fudan) and complementary application profiles (telecom and multimedia at KTH; high end computing at NUDT; distributed low power embedded systems at Fudan).

CEA, DTU, TUBS, UNIBO from the MPSoC cluster has together with other partners of ArtistDesign (e.g. Verimag) submitted a research proposal on Smart Multicore Embedded Systems (SMECY) to ARTEMIS JU. The project has been accepted for funding and is currently under contract negotiations. The mission of the SMECY project is to develop new programming technologies enabling the exploitation of many (100s) core architectures. Multi-core technologies are strategic to keep and win market shares in all areas of embedded systems.

DTU and TUBS from the MPSoC cluster has, together with TU Eindhoven, UNICA, Silicon Hives, ACE, ST and Compann, submitted a research proposal on Automatic Architecture Synthesis and Application Mapping (ASAM) to ARTEMIS JU. The project has been accepted for funding and is currently under contract negotiations. This project addresses a uniform process of automatic architecture synthesis and application mapping for heterogeneous adaptive multi-processor embedded systems, defining a new unified
multi-processor system design methodology, as well as, supporting synthesis and prototyping tools and tool-chains.

-- The above is new text, not present in the Y1 deliverable --

3. Overall Assessment and Vision for the Cluster

The research in embedded systems is still fragmented. This not only is true within a single subject but also between several sub-disciplines. It is one of the major goals of the cluster on 'Hardware Platforms and MPSoC Design' to establish closer links to the other communities and to take advantage of the scientific results and insights.

Cross-layer design is a key issue in embedded systems. The classical view of a strict layering according to chosen abstraction levels does not work any more because of the importance of non-functional constraints and limited resources. Therefore, completely new concepts are necessary that enable the integrated modelling and design under predictability and efficiency constraints. It is expected that this move towards a resource-aware design trajectory involves all current layers and a breakthrough can be obtained by integration only.

3.1 Assessment for Year 2

The MPSoC cluster received all 3 best paper awards at the Embedded Systems Week in Grenoble. ETHZ got the best paper award of EMSOFT, LINKÖPING got the best paper award of CODES+ISSS, and DTU got the best paper award of CASES.

LINKÖPING-DTU: Interaction between Linköping and DTU has been in the area of fault tolerant embedded systems. This has resulted in joint development and publications. Prof. Paul Pop from DTU has visited Linköping.

DTU-UNIBO: Interaction between DTU and UNIBO has been in the area of networked embedded systems. The work on power management in wireless sensor networks supported by energy harvesting, which were started in year 1 has been continued. Mikke Jakobsen from DTU has visited UNIBO.

DTU-KTH: Interaction between DTU and KTH has been in the area of system modelling. The work has been on development of a multi-MoC modelling framework for heterogeneous systems. Mikkel Jakobsen from DTU has visited KTH.

DTU-AAU: Interaction between DTU and AAU (Modeling and Validation cluster) has been on modelchecking using timed automata based on UPPAAL. The MoVES framework developed at DTU is one result of this interaction. A first version of the MoVES framework has been made public as a tool under ArtistDesign. Aske W. Brekling from DTU has visited AAU.

CEA LIST and UNIBO have started collaboration for the definition of a Software Runtime Architecture for the management of many-core components, and to analyze pros and cons of asymmetric and symmetric MPSOC approaches.

ETHZ-UNIBO: Interaction between ETH Zurich and University Bologna on linking the DOL (distributed operation environment) with the MPARM platform. This cooperation lead to a complete path from application specification (process network) to a software implementation running on a distributed ARM architecture. Thereby, tools for multiobjective mapping optimization (computation, communication and resource sharing), software generation, modular performance analysis (MPA), simulation using the MPARM platform and backannotation of results have been integrated.

ETHZ-UNIBO: Based on a successful cooperation in terms of energy harvesting sensor networks, several further joint investigations of application control and hardware implementation have been performed. Major extensions have been done in terms of harvesting in distributed settings and reward-based optimization strategies. These activities resulted in a large set of joint and individual publications on the subject, see section 3.2.1 .

ETHZ-VERIMAG: With ARTISTDesign partner VERIMAG (Joseph Sifakis), ETHZ linked the respective tools for MPSoC design, namely BIP and DOL. In particular, it is now possible to pass DOL specifications to the BIP environment for (a) software synthesis and (b) verification of functional and non-functional properties. This way, a semantic link between two completely different models of computation has been performed.

ETHZ-TUBS: ETH Zurich and University Braunschweig (Rolf Ernst) completed and extended the links between their performance analysis tools (SymTa/S and RTC/MPA). This way, components of a complex distributed embedded system can be analyzed with respect to their timing properties by means of different abstraction mechanisms. The combination of the tools allows short run-times while leading to a high accuracy of end-to-end system properties.

ETHZ-TUBS: ETH Zurich and University Braunschweig (Rolf Ernst) developed new methods to characterize and analyze hierarchical event streams in terms of their timing properties. To this end, new methods have been developed (such as event count curves and their transformations) as well as the respective tools have been extended. In addition, a realistic case study together with a large avionics industry partner has been undertaken that shows the effectiveness of the approach. Results have been submitted in form of a joint publication.

-- The above is new text, not present in the Y1 deliverable --

3.2 Overall Assesment since the start of the ArtistDesign NoE

The MPSoC cluster has continued its solid work on design and analysis of multi- and many-core system-on-chip, which was started during ARTIST2. Five of the current partners (ETHZ, UNIBO, DTU, Linkoping and TUBS) took participated in ARTIST2 and have continued and strengthened their collaboration in ArtistDesign. IMEC, KTH and CEA where not part of ARTIST2 and therefore had to be integrated with the others. Except from IMEC that already had a lot of interactions with partners of ArtistDesign, KTH and CEA had a slow start in the cluster, but have been fully integrated in year 2 with joint research and publications. In year 2 EPFL joint the cluster. They have primarily been collaborating with UNIBO, although other collaborations are being explored. EPFL are expected to be fully integrated during year 3.

Topicwise, the MPSoC cluster is focusing on platforms based on single-chip multicore SoC architectures and distributed architectures.

Within multicore SoC architectures the major themes are predictability, Network-on-Chip, programming models and resource awareness. The activities related to predictability have resulted in a better understanding of the subject of shared resource interference in multiprocessor systems, where the competition for e.g. a shared memory leads to a “feedback” on the task timing that breaks the predominant analysis approaches (in which the task timing is investigated in isolation). These problems have been identified also in joint meetings with members of the Timing Analysis cluster. First solutions have already been presented that allow circumnavigating this problem in a formal performance analysis. Collaboration among partners has resulted in a number of analysis tools to analyse resource usage and timeliness. A new direction within on-chip network structures is the use of 3D structures that allows the stacking of cores. These new structures need to be captured by the design and analysis tools. Effort in understanding how to program multicore SoC has been investigated. This covers both programming models and how to use the parallel architectures to support adaptivity, including task distribution and migration. Finally, initial exploration of new emerging biochip platforms has been explored. It is expected that one of the next integration steps for SoC is to include capabilities for biochemical analysis and “computation”.

Within distributed architectures the major themes are reliability and fault-tolerance, and resource awareness, in particular energy. The activities related to fault-tolerance have resulted in new techniques where hardware and software tolerance techniques are combined and where hard real-time and soft real-time tasks can coexist gauranteing that hard real-time task will meet their deadlines in case of faults, while soft real-time tasks will experiemnce a graceful degradation. The focus of the resource awareness has focused on the design of wireless sensor networks powered by energy harvesters. Emphasis has been on both node level energy awareness and network level (system level) energy awareness. Results have shown that dynamic adaptation can result in significantly extended lifetime of wireless sensor networks.

-- The above is new text, not present in the Y1 deliverable --

3.2.1 List of Joint Publications

The following list contains publications, where authors are in different research sites that are participating in the ArtistDesign network and where at least one author is in the cluster on Execution Platforms. It clearly shows the degree of integration that has been achieved. The following list collects all joint publications since the start of ArtistDesign:

Publications 2008

1. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Synthesis of Flexible Fault-Tolerant Schedules with Preemption for Mixed Soft and Hard Real-Time Systems”, 11th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN (DSD 2008), Parma, Italy, September 3-5, 2008, pp. 71-80.
2. Petru Eles, Viacheslav Izosimov, Paul Pop, Zebo Peng, “Synthesis of Fault-Tolerant Embedded Systems”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1117-1122.
3. Wu, K., Madsen, J., Kanstein, A., Mladen, B., *MT-ADRES: Multithreading on Coarse-Grained Reconfigurable Architecture*, Intel. Journal of Electronics (IJE), Volume 95, Issue 7, July 2008. Page(s): 761-776.
4. Anders Tranberg-Hansen, Jan Madsen, Bjørn Sand Jensen, A Service Based Estimation Method for MPSoC Performance Modelling, to appear in the proceedings of the 3rd International Symposium on Industrial Embedded Systems, June 2008.
5. A Reactive and Cycle-True IP Emulator for MPSoC Exploration Mahadevan, S.; Angiolini, F.; SparsSparso, J.; Benini, L.; Madsen, J. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 27, Issue 1, Jan. 2008 Page(s):109 – 122
6. ‘Enabling run-time memory data transfer optimizations at the system level with automated extraction of embedded software metadata information’, Bartzas, A.; Peon-Quiros, M.; Mamagkakis, S.; Catthoor, F.; Soudris, D. and Mendias, J., Asia and South Pacific Design Automation Conference - ASP-DAC, 2008
7. ‘Optimization Methodology of Dynamic Data Structures based on Genetic Algorithms for Multimedia Embedded Systems’, Baloukas, C.; Risco Martin, J.; Atienza, D.; Poucet, C.; Papadopoulos, L.; Mamagkakis, S.; Soudris, D.; Hidalgo, J.; Catthoor, F. and Lancares, J., Elsevier Journal of Systems and Software (JSS), 2008

8. 'MNEMEE: Memory management technology for adaptive and efficient design of embedded systems' S.Mamagkakis, P.Lemmens, D.Soudris, T.Basten, P.Marwedel, D.Kritharidis, G.Guilmin, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.
9. 'MOSART: Mapping Optimisation for Scalable multi-core ARchiTecture', B. Candaele, A. Jantsch, T. Ashby, K. Tiensyrjä, F. Ieromnimon, B. Vanthournout, P. Di Crescenzo, D. Soudris, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.
10. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, "Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints", Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, 915-920.
11. Traian Pop, Paul Pop, Petru Eles, Zebo Peng, Alexandru Andrei, "Timing Analysis of the FlexRay Communication Protocol", Real-Time Systems Journal, Volume 39, Numbers 1-3, August, 2008, pp 205-235.
12. Traian Pop, Paul Pop, Petru Eles, Zebo Peng, Alexandru Andrei, "Analysis and Optimisation of Hierarchically Scheduled Multiprocessor Embedded Systems", Intl. Journal of Parallel Programming, Volume 36, Number 1, February, 2008, pp. 37-67.
13. Bengt Jonsson, Simon Perathoner, Lothar Thiele, Wang Yi: Cyclic Dependencies in Modular Performance Analysis. ACM & IEEE International Conference on Embedded Software (EMSOFT), ACM Press, Atlanta, Georgia, USA, pages 179-188, October, 2008.
14. Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, 2008.
15. Davide Brunelli, Clemens Moser, Luca Benini, Lothar Thiele: An Efficient Solar Energy Harvester for Wireless Sensor Nodes. Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.
16. Clemens Moser, Lothar Thiele, Davide Brunelli, Luca Benini: Robust and Low Complexity Rate Control for Solar Powered Sensors Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.
17. Tolga Ovatman, Aske Brekling, and Michael R. Hansen. Cost analysis for embedded systems: Experiments with Priced Timed Automata. In proceedings of FESCA 2008.
18. 'Enabling run-time memory data transfer optimizations at the system level with automated extraction of embedded software metadata information', Bartzas, A.; Peon-Quiros, M.; Mamagkakis, S.; Catthoor, F.; Soudris, D. and Mendias, J., Asia and South Pacific Design Automation Conference - ASP-DAC, 2008
19. 'Storage estimation and design space exploration methodologies for the memory management of signal processing applications', Balasa, F.; Kjeldsberg, P.; Vandecappelle, A.; Palkovic, M.; Hu, Q.; Zhu, H. and Catthoor, F.Journal, Journal of VLSI Signal Processing Systems, 2008
20. Iyad Al Khatib, Francesco Poletti, Davide Bertozzi, Luca Benini, Mohamed Bech ara, Hasan Khalifeh, Axel Jantsch, and Rustam Nabiev, "A Multiprocessor System-on-Chip for Real-Time Biomedical Monitoring and Analysis: ECG Prototype Arc hitectural Design Space Exploration", ACM Transactions on Design Automation of Embedded Systems, vol. 13, no. 2, April 2008.

21. 'A System Scenario based Approach to Dynamic Embedded Systems', S.V. Gheorghita, M. Palkovic, J. Hamers, A. Vandecappelle, S. Mamagkakis, T. Basten, L. Eeckhout, H. Corporaal, F. Catthoor, F. Vandeputte, K. De Bosschere, ACM Transactions on Design Automation of Electronic Systems, ToDAES. To appear in 2009.
22. V. Izosimov, P. Pop, P. Eles, Z. Peng, "Design Optimization of Time- and Cost-Constrained Fault-Tolerant Embedded Systems with Checkpointing and Replication", IEEE Trans. on Very Large Scale Integrated (VLSI) Systems (accepted for publication).

Publications 2009

1. Clemens Moser, Lothar Thiele, Davide Brunelli and Luca Benini Adaptive Power Management for Environmentally Powered Systems, Accepted for publication in *IEEE Transactions on Computers*, 2009, regular papers.
2. Davide Brunelli, Clemens Moser, Lothar Thiele and Luca Benini Design of a Solar Harvesting Circuit for Battery-less Embedded Systems Accepted for publication in *IEEE Transactions on Circuits and Systems I*, 2009, regular papers.
3. 1. P. Pop, V. Izosimov, P. Eles, and Z. Peng. Design Optimization of Time- and Cost-Constrained Fault-Tolerant Embedded Systems with Checkpointing and Replication. IEEE Transactions on Very Large Scale Integrated (VLSI) Systems, 17(3):389-402. 2009.
4. 2. V. Izosimov, I. Polian, P. Pop, P. Eles, and Z. Peng. Analysis and Optimization of Fault-Tolerant Embedded Systems with Hardened Processors. Proceedings of DATE: Design Automation and Test in Europe, IEEE, 2009, pp. 682 – 687.
5. 3. S. Samii, P. Eles, Z. Peng, A. Cervin, "Quality-Driven Synthesis of Embedded Multi-Mode Control Systems," Design Automation Conference (DAC), San Francisco, California, USA, July 2009, pp. 864 - 869.
6. 4. S. Samii, A. Cervin, P. Eles, Z. Peng, "Integrated Scheduling and Synthesis of Control Applications on Distributed Embedded Systems," Design Automation and Test in Europe (DATE) Conference, Nice, 2009, pp. 57 - 62.
7. [MBT09] M. Magno, D. Brunelli, L. Thiele and L. Benini, "Adaptive Power Control for Solar Harvesting Multimodal Wireless Smart Camera", in proceedings of the 3rd ACM/IEEE International Conference on Distributed Smart Cameras ICDSC, 2009
8. [BMT09] Brunelli, D., Moser, C. Thiele, L. and Benini, L., Design of a Solar Harvesting Circuit for Battery-less Embedded Systems (2009), in: IEEE Transactions on Circuits and Systems I: Regular Papers,, 56:11(2519-2528)
9. [ZTB09] Zompakis, N.; Trautmann, M.; Bartzas, A.; Mamagkakis, S.; Soudris, D.; Van der Perre, L. and Catthoor, F.: Multi-granularity NoC simulation framework for early phase exploration of SDR hardware platforms . In 19th International Workshop on Power and Timing Modeling, Optimization and Simulation – PATMOS, Delft, Netherlands, (2009)
10. [ZAB09] Zanini, F.; Atienza, D.; Benini, L.; De Micheli, G.; Multicore thermal management with model predictive control. Circuit Theory and Design, 2009. ECCTD 2009. 23-27 Aug. 2009 Page(s):711 - 714
11. [SMBD09] Seiculescu, C.; Murali, S.; Benini, L.; De Micheli, G.; NoC topology synthesis for supporting shutdown of voltage islands in SoCs. Design Automation Conference, 2009. DAC '09. 46th ACM/IEEE; 26-31 July. 2009 Page(s):822 - 825

12. [SPBD09] Sathanur, A.; Pullini, A.; Benini, L.; De Micheli, G.; Macii, E.; Physically clustered forward body biasing for variability compensation in nanometer CMOS design. Design, Automation & Test in Europe Conference & Exhibition, 2009. DATE '09. 20-24 April 2009 Page(s):154 - 159

13. [SMB09] Seiculescu, C.; Murali, S.; Benini, L.; De Micheli, G.; SunFloor 3D: A tool for Networks On Chip topology synthesis for 3D systems on chips. Design, Automation & Test in Europe Conference & Exhibition, 2009. DATE '09. 20-24 April 2009 Page(s):9 - 14

14. [SRN+09] Simon Schliecker, Jonas Rox, Mircea Negrean, Kai Richter, Marek Jersak and Rolf Ernst, **"System Level Performance Analysis for Real-Time Automotive Multi-Core and Network Architectures**,"*Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 28, No. 7, pp. 979-992, July 2009

15. [PWT+09] Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst and Michael González Harbour, **"Influence of different abstractions on the performance analysis of distributed hard real-time systems,"** *Journal Design Automation for Embedded Systems (available as "online first", April 2008)*, vol. 13, No. 1, pp. 27-49, June 2009

16. Simon Perathoner, Tobias Rein, Lothar Thiele, Kai Lampka: FIFO Scheduling and Event Count Curves for Modeling Structured Event Streams in Modular Performance Analysis TIK Report Nr. 312, ETH Zurich, October, 2009.

17. Simon Perathoner, Tobias Rein, Lothar Thiele, Kai Lampka and Jonas Rox: Modeling Structured Event Streams in System Level Performance Analysis, submitted to Conference on Languages, Compilers, and Tools for Embedded Systems LCTES, Stockholm, Sweden, April 2010.

18. Facchini, M.; Carlson, T.; Vignon, A.; Palkovic, M.; Catthoor, F.; Dehaene, W.; Benini, L. and Marchal, P.: System-level power/performance evaluation of 3D stacked DRAMs for mobile applications In Design, Automation and Test in Europe, DATE 2009, Nice, France, April 20-24, (2009).

19. Christos Baloukas, José Luis Risco-Martín, David Atienza, Christophe Poucet, Lazaros Papadopoulos, Stylianos Mamagkakis, Dimitrios Soudris, José Ignacio Hidalgo, Francky Catthoor, Juan Lanchares: Optimization methodology of dynamic data structures based on genetic algorithms for multimedia embedded systems. Journal of Systems and Software 82(4): 590-602 (2009)

20. [SZJ+2009] Ingo Sander, Jun Zhu, Axel Jantsch, Andreas Herrholzy, Philipp A. Hartmanny, and Wolfgang Nebel. High-level estimation and trade-off analysis for adaptive real-time systems. In *Proceedings of the 16th Reconfigurable Architectures Workshop*, Rome, May 2009.

21. Martin Frãnzle and Michael R. Hansen. Efficient model checking for duration calculus. International Journal of Software and Informatics, Vol.3, no.2-3, pp. 171-196, 2009

22. William~P. Heise, Martin Fränzle and Michael R. Hansen. A prototype model checker for Duration Calculus. In proceedings of the 21st Nordic Workshop on Programming Theory (NWPT'09). DTU Informatics, 2009, pages 26-29.

23. Gerald Sauter, Henning Dierks, Martin Fränzle and Michael R. Hansen. Leight-weight hybrid model checking facilitating online prediction of temporal properties. In proceedings of the 21st Nordic Workshop on Programming Theory (NWPT'09). DTU Informatics, 2009, pages 20-23.

24. [MBT09] M. Magno, D. Brunelli, L. Thiele and L. Benini, "Adaptive Power Control for Solar Harvesting Multimodal Wireless Smart Camera", in proceedings of the 3rd ACM/IEEE International Conference on Distributed Smart Cameras ICDSC, 2009

25. R. Pellizzoni, A. Schranzhofer, J.-J. Chen, M. Caccamo, and L. Thiele., Worst case delay analysis for memory interference in multicore systems. In DATE, 2010.

3.3 Indicators for Integration

During year 2 we have done the following interactions between partners:

- *25 joint publications* have been produced. The plan was 10 Joint publications / year describing the results in terms of new methods and tools.
- Joint organization of workshops, tutorials, special sessions in international highly recognized conferences. In year 2 the following was accomplished:
  - Organized the 7th IEEE Workshop Embedded Systems for Real-Time Multimedia as part of the Embedded Systems Week, 2009.
  - Organized the Nordic Workshop on Programming Theory in Lyngby, Denmark, 2009
  - Organized the TUBS.city symposium, Braunschweig, Germany, 2009.
  - Organized the Embedded Software track at DATE 2009.
  - Organized the Industry Day at ESWeek, 2009.
  - Organized a PhD course on Advanced Topics in Embedded Systems, Lyngby, Denmark.
  - Gave tutorial at ASP-DAC in Japan, 2009.
  - Gave tutorial at the ARTIST Summer School in China, Tsing Hua, Beijing, China, 2009
  - Gave 10 keynotes and invited talks at conferences and workshops, including CAV, ESTIMedia, ECRTS and MPSoC.
- Yearly target is 1 workshop, 1 PhD course/school, 2-3 conference tutorials and special sessions.
- Integration of tools existing at the partner sites, and definition of tool flows integrating tools from the different partners.
  - The tool integration work is being continued. This covers both integration of tools within the cluster, between clusters of ArtistDesign and with external partners.
  - 6 tools have been produced by the cluster.
- Mobility, i.e. the number of PhD student and faculty exchanges. This integration activity will also introduce the concept of "student clusters", where more than two PhD students from different partners will work together in a single location.
  - 4 PhD student visits
  - 4 faculty/researcher visits
  - 3 focused meetings
- Impact on industrial practice in the area of MPSoC design and analysis. This objective will leverage student internships at associated industrial partner's sites.
  - Several PhD students have worked together with industry (and spent time in the companies) to apply tools and methods developed in the cluster in an industrial context.

-- Changes wrt Y1 deliverable --

The objectives are as for Year 1, but the text has been updated with the achivements of Year 2.

3.4 Long-Term Vision

Embedded systems are growing more software and communication centric. As a consequence, new models and new analysis and design space exploration tools are needed in order to support optimal implementation of applications on distributed embedded architectures such as MPSoC. Embedded systems are characterized by continuously increasing complexity and strong constraints on safety, performance, power consumption, and costs. To be able to design such systems, it is needed to (1) consider the hardware platform and software components of MPSoC systems in their interaction, in order to produce a system which satisfies the requirements at low cost, (2) support the designer with tools for accurate estimation of certain design parameters (power, performance) based on appropriate models for hardware and software components and (3) provide the designer with adequate support for design space exploration and optimisation.

Embedded architectures and heterogeneous distributed embedded systems have grown to extremely complex computation and communication patterns, and to an increasing level of reconfigurability (including adaptivity and run-time resource management). New performance models and a corresponding theory are urgently needed.

The long-term vision for this activity is to advance the theory, methods and tools for the modeling, analysis and design of embedded systems and to disseminate this to advance academic excellence, education and industrial innovation.

-- Changes wrt Y1 deliverable --

No changes

3.4.1 Tool: Analysis and optimisation framework for fault tolerant distributed embedded systems

Objectives

Linköping University and DTU are working on an environment and tool-set for the analysis and design optimisation of safety critical, fault tolerant real-time embedded applications. The emphasis is on the issue of transient faults and the goal is to develop tools for scheduling, mapping, and system optimisation.

Main results

A strategy for the synthesis of fault tolerant schedules has been developed. It can handle both hard and soft real-time tasks. The goal is to guarantee the deadlines for the hard processes even in the case of faults, while maximizing the overall utility. Time/utility functions are used to capture the utility of soft processes. Process re-execution is employed to recover from multiple

faults. A single static schedule computed off-line is not fault tolerant and is pessimistic in terms of utility, while a purely online approach, which computes a new schedule every time a process fails or completes, incurs an unacceptable overhead. Thus, a quasi-static scheduling strategy is used, where a set of schedules is synthesized off-line and, at run time, the scheduler will select the right schedule based on the occurrence of faults and the actual execution times of processes. An optimisation technique for the generation of schedule tables supporting such a quasi-static scheduling approach has been developed and implemented.

Current work

Ongoing work is towards development of cost-optimisation techniques by considering processors with various hardening levels and the associated tradeoffs.

During the second **year DTU** and **Linköping** have continued their cooperation related to the design and optimisation of fault tolerant mixed hard/soft real-time systems. During the second year the emphasis of the work has been on the analysis and optimisation of fault-tolerant hard real-time embedded systems, based on an approach in which hardware and software fault tolerance techniques are combined. The basic trade-off is between processor hardening in hardware and process re-execution in software which, together, have to provide the required levels of fault tolerance against transient faults with the lowest-possible system costs.

The goal for the third year is the development of new optimisation approaches for implementation of error detection techniques.

Participating partners

Linköping: Scheduling techniques, fault tolerant systems, design optimisation.

DTU: System level optimisation techniques

Publications

1. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Synthesis of Flexible Fault-Tolerant Schedules with Preemption for Mixed Soft and Hard Real-Time Systems”, 11th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN (DSD 2008), Parma, Italy, September 3-5, 2008, pp. 71-80.
2. Petru Eles, Viacheslav Izosimov, Paul Pop, Zebo Peng, “Synthesis of Fault-Tolerant Embedded Systems”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1117-1122.
3. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, 915-920.
4. P. Pop, V. Izosimov, P. Eles, and Z. Peng. Design Optimization of Time- and Cost-Constrained Fault-Tolerant Embedded Systems with Checkpointing and Replication. IEEE Transactions on Very Large Scale Integrated (VLSI) Systems, 17(3):389-402. 2009.
5. V. Izosimov, I. Polian, P. Pop, P. Eles, and Z. Peng. Analysis and Optimization of Fault-Tolerant Embedded Systems with Hardened Processors. Proceedings of DATE: Design Automation and Test in Europe, IEEE, 2009, pp. 682 – 687.

-- Changes wrt Y1 deliverable --

Updated description of current work and added two publications.

3.4.2 Tool: IMEC MPA + MH MPSoC mapping framework

Objectives

The main objectives of the framework is to offer an automatic source code parallelization (MPA tool) and memory hierarchy management (MH tool) in order to map efficiently embedded software application on MPSoC platforms.

Main Results

Prototype versions of the MPSoC Parallelization Assistant (MPA) and Memory Hierarchy (MH) management tools were developed and tested on video codec embedded sosftware applications (i.e., MPEG-4, AVC etc.).

Current work

Currently, the affiliated partners of IMEC (ie, DUTH/ICCS and TU/e) and core partners (TUDortmund/ICD and KTH) are trying to integrate their tool and design flows with the IMEC MPA + MH MPSoC mapping framework in the memory and interconnect specific context of the MNEMEE and MOSART FP7 projects, respectively.

Participating partners:

- DUTH/ICCS
  This partner is integrating the dynamic data type and dynamic memory management tools and design flows with the IMEC MPSoC mapping tool flows.
- TUDortmund/ICD
  This partner is integrating its pre-compiler and compiler framework to the static MH tool of IMEC.
- TU/e
  This partner is integrating its SDF3 framework in the context of system scenarios with the IMEC MPSoC mapping tool flows.
- KTH
  This partner is integrating its NoC simulation and exploration framework with the MPA tool of IMEC.

Web

http://www.mnemee.org/
http://www.mosart-project.org/

Related Publications

IMEC vzw. & TU/e

- 'A System Scenario based Approach to Dynamic Embedded Systems', S.V. Gheorghita, M. Palkovic, J. Hamers, A. Vandecappelle, S. Mamagkakis, T. Basten, L. Eeckhout, H. Corporaal, F. Catthoor, F. Vandeputte, K. De Bosschere, ACM Transactions on Design Automation of Electronic Systems, ToDAES. To appear in 2009.

IMEC vzw. & TU/e & DUTH & TU Dortmund (at ICD)

- 'MNEMEE: Memory management technology for adaptive and efficient design of embedded systems' S.Mamagkakis, P.Lemmens, D.Soudris, T.Basten, P.Marwedel, D.Kritharidis, G.Guilmin, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

IMEC vzw. & KTH & DUTH

'MOSART: Mapping Optimisation for Scalable multi-core ARchiTecture', B. Candaele, A. Jantsch, T. Ashby, K. Tiensyrjä, F. Ieromnimon, B. Vanthournout, P. Di Crescenzo, D. Soudris, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

-- Changes wrt Y1 deliverable --

No changes.

3.4.3 Tool: MoVES - Modelling and Verification of Embedded Systems

Objectives

The MoVES framework is being developed to assist in the early phases of embedded systems design. The framework can be used to conduct schedulability analysis and has the potential to reason about different types of resource usage such as memory usage and power consumption.

Main Results

In several projects (MoDES, DaNES, ARTIST2, ArtistDesign) a model-based approach to analysis of embedded systems has been analyzed. This has resultet in the MoVES framework, which is now available online. The framework consists of a model- and a trace generator. From a system specification MoVES builds a model suitable for verification using an external verification back-end. In the case of e.g. verified non-schedulability, the trace generator provides the user with an understandable trace that leads to a missed deadline of the system.

Current work

The current version of the framework is based on a simple specification language where a system is modelled as an application running on an execution platform. The application is modelled through the individual tasks, and the execution platform is modelled through the processing elements, including the operating systems, and their interconnections. The tasks and processing elements are characterized by their real-time properties. Currently, verification can be conducted using two different verification back-ends, a) the original Uppaal model-checker for timed-automata models and b) a developmental Uppaal model-checker for stop-watch automata.

Participating partners:

- DTU: Provides the MoVES development environment.
- AAU: Provides the UPPAAL verification engine

Web
http://www.imm.dtu.dk/moves

Related Publications

1. Aske Brekling, Michael R. Hansen, Jan Madsen, MoVES - A Framework for Modelling and Verifying Embedded Systems, The 21st International Conference on Microelectronics, Marrakech, Morocco, 2009
2. Jan Madsen, Michael R. Hansen, Aske W. Brekling, A Modelling and Analysis Framework for Embedded Systems, Model-Based Design of Heterogeneous Embedded Systems, CRC Press, 2009
3. Aske Brekling, Michael R. Hansen, Jan Madsen, Analysis of Quantitative Properties of Hardware Specifications, The 21st Nordic Workshop on Programming Theory, Technical University of Denmark, 2009

-- Changes wrt Y1 deliverable --

This is new text.

3.4.4 Tool: MPA (Modular Performance Analysis)

Objectives

The tool MPA (modular performance analysis) is based on an extension of network calculus that is termed real-time calculus (RTC). The purpose of the tool is to perform an end-to-end real-time analysis of complex distributed embedded systems. The implementation is based on a Java mathematical library for max-+ algebra with an associated Matlab interface.

Main Results

Within ARTISTDesign, the MPA tool box has been (a) extended towards the new results together with University Braunschweig (TUBS) related to hierarchical event streams and (b) it has been linked to the Symta/S tool suite as described above. In addition, the toolbox has been used in the context of various application studies from avionic and automotive domain.

Current work

We are currently working towards linking the toolbox to other performance analysis frameworks, e.g. UPPAAL from Uppsala University (Wang Yi, Bengt Jonsson). Some first promising results are available already. In addition, we are intending to use the method to investigate the interaction between memory access and computations in MPSoC platforms. This will be continued together with University Saarland (Reinhard Wilhelm).

Participating partners

ETHZ: Provides and maintains the MPA toolbox

TUBS: Link to the Symta/S tool suite, development of algorithms and methods for hierarchical event stream analysis.

Web

http://www.mpa.ethz.ch/

Related Publications

ETHZ: Kai Lampka, Simon Perathoner, Lothar Thiele: Analytic Real-Time Analysis and Timed Automata: A Hybrid Method for Analyzing Embedded Real-Time Systems. 8th ACM & IEEE International conference on Embedded software, EMSOFT 2009, CD edition, ACM, Grenoble, France, pages 107-116, October, 2009.

ETHZ: Lothar Thiele, Nikolay Stoimenov: Modular Performance Analysis of Cyclic Dataflow Graphs. EMSOFT 09: Proceedings of the 9th ACM international conference on Embedded software, Grenoble, France, pages 127-136, October, 2009.

ETHZ & TUBS: Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, Vol. 13, No. 1, pages 27-49, June, 2009.

ETHZ & TUBS: Simon Perathoner, Tobias Rein, Lothar Thiele, Kai Lampka and Jonas Rox: Modeling Structured Event Streams in System Level Performance Analysis, submitted to Conference on Languages, Compilers, and Tools for Embedded Systems LCTES, Stockholm, Sweden, April 2010

-- Changes wrt Y1 deliverable --

This is new text.

3.4.5 Tool: DOL (Distributed Operation Layer)

Objectives

The DOL environment is a complete high-level compilation environment for MPSoC platforms. It consists of a graphical input specification interface for (a) application and (b) platform, a link to analytic performance analysis based on MPA, a simulation environment based on MPARM (Univeristy Bologna, Luca Benini) and a multi-objective optimization environment based on PISA (http://www.tik.ethz.ch/~sop/pisa/) for mapping (binding of application components to computation resources and communication links to paths on the platform). The environment has been successfully used to map complex applications to various platforms such as IBM Cell, MPARM (UNIBO) and ATMEL Diopsys.

Main Results

In the framework of ARTISTDesign, the DOL environment has been successfully linked and coupled to the MPARM simulation and design environment from University Bologna. This way, DOL could be used for ARM-based MPSoC architectures and extended with a state-of-the-art simulation environment. Main results are the comparison of analytic performance analysis with simulation-based performance numbers.

Current work

In the future, the coupling between MPARM and DOL will be used in order to investigate new concepts for predictable and efficient communication fabrics, including intelligent DMA controllers, scratchpad memories and flexible TDMA scheduling policies.

Participating Partners

ETH: Provides the DOL software development environment.

UNIBO: Provides the MPARM environment, including simulation capabilities and new concepts for predictable communication fabrics.

Web

http://www.tik.ee.ethz.ch/~shapes/dol.html

Related Publications

W. Haid, K. Huang, I. Bacivarov, and L. Thiele. Multiprocessor SoC Software Design Flows. IEEE Signal Processing Magazine, vol. 26, no. 6, pp. 64—71, Nov. 2009.

W. Haid, L. Schor, K. Huang, I. Bacivarov, and L. Thiele. Efficient Execution of Kahn Process Networks on Multi-Processor Systems Using Protothreads and Windowed FIFOs. In Proc. IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia), pages 35—44, Grenoble, France, Oct. 2009.

W. Haid, M. Keller, K. Huang, I. Bacivarov, and L. Thiele. Generation and Calibration of Compositional Performance Analysis Models for Multi-Processor Systems. In Proc. Int'l Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), pages 92—99, Samos, Greece, July 2009. Awarded the Stamatis Vassiliadis Best Paper Award.

K. Huang, I. Bacivarov, J. Liu, and W. Haid. A Modular Fast Simulation Framework for Stream-Oriented MPSoC. In IEEE Symposium on Industrial Embedded Systems (SIES), pages 74—81, Lausanne, Switzerland, July 2009.

-- Changes wrt Y1 deliverable --

This is new text.

4. Cluster Participants

-- Changes in the Cluster Participants wrt Y1 deliverable --

Raphaël David has replaced Thierry Collette as the team leader for CES LIST

Professor Giovanni De Micheli has been added as team leader for EPFL (new cluster member)

Morten Kragh has replaced Bjørn Sand Jensen as the representative foraffiliated industrial partner B&O ICEpower

4.1 Core Partners

Cluster Leader Activity Leader & Team Leader	
	Jan Madsen (Technical University of Denmark)
Technical role(s) within ArtistDesign	Member of the Strategic Management Board Leads Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Integration Driven by Industrial Applications Leader of the JPRA Activity: “Platform and MPSoC Analysis”
Research interests	Research interests include high-level synthesis, hardware/software codesign, System-on-Chip design methods, and system level modeling, integration and synthesis for embedded computer systems.
Role in leading conferences/journals/etc in the area	Program Chair and Vice-Chair of Design Automation and Test in Europe Conference. Tutorial Chair and Special Sessions Chair of Design Automation and Test in Europe Conference. General Chair, Program Chair and Workshop Chair of CODES+ISSS Conference Member of the editorial board of the journal “IEE Proceedings – Computers and Digital Techniques” Member of the technical program committee and organizing committee of several technical conferences, including the Design Automation and Test in Europe Conference, the Real-Time Systems Symposium, the Symposium on Hardware-Software Codesign, and

	the International Workshop on Applied Reconfigurable Computing. Danish delegate in the Governing Board of ARTEMIS JU
Awards / Decorations	In 1995 he received the Jorck's Foundation Research Award for his research in hardware/software codesign

Team Leader	
	Lothar Thiele (ETH Zurich)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems and Software Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance
Research interests	Research interests include models, methods and software tools for the design of embedded systems, embedded software and bioinspired optimization techniques.
Awards / Decorations	In 1986 he received the "Dissertation Award" of the Technical University of Munich, in 1987, the "Outstanding Young Author Award" of the IEEE Circuits and Systems Society, in 1988, the Browder J. Thompson Memorial Award of the IEEE, and in 2000-2001, the "IBM Faculty Partnership Award". In 2004, he joined the German Academy of Natural Scientists Leopoldina. In 2005-2006, he was the recipient of the Honorary Blaise Pascal Chair of University Leiden, The Netherlands.

Team Leader	
	Prof. Luca Benini, University of Bologna http://www-micrel.deis.unibo.it/%7Ebenini/
Technical role(s) within ArtistDesign	Member of the Strategic Management Board Co-leads Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance

	Leader of the JPRA Activity: "Platform and MPSoC Design"
Research interests	(i) Development of power modeling and estimation framework for systems-on-chip. (ii) Development of optimal allocation and scheduling techniques for energy-efficient mapping of multi-task applications onto multi-processor systems-on-chips. (iii) Development of energy-scavenging techniques for ultra-low power sensor network platforms.
Role in leading conferences/journals/etc in the area	▪ Program chair and vice-chair of Design Automation and Test in Europe Conference. ▪ Member of the 2003 MEDEA+ EDA roadmap committee 2003. ▪ Member of the IST Embedded System Technology Platform Initiative (ARTEMIS): working group on Design Methodologies ▪ Member of the Strategic Management Board of the ARTIST2 Network of excellence on Embedded Systems ▪ Member of the Advisory group on Computing Systems of the IST Embedded Systems Unit. ▪ Member of the technical program committee and organizing committee of several technical conferences, including the Design Automation Conference, International Symposium on Low Power Design, the Symposium on Hardware-Software Codesign. He is Associate Editor of the IEEE Transactions on Computer-Aided Design of Circuits and Systems and of the ACM Journal on Emerging Technologies in Computing Systems. ▪ Fellow of the IEEE.
Notable past projects	ICT-Project **REALITY - *Reliable and variability tolerant system-on-a-chip design in more-moore technologies.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.1 Next-Generation Nanoelectronics Components and Electronics Integration. Start date: 01/01/2008; Duration: 30 months; Contract Type: Collaborative project; Project Reference: 216537; Project Cost: 4.45 million euro; Project Funding: 2.9 million euro. ICT-Project **PREDATOR - *Design for predictability and efficiency.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.3 Embedded Systems Design. Start date: 01/02/2008; Duration: 36 months; Contract Type: Collaborative project; Project Reference: 216008; Project Cost: 3.93 million euro; Project Funding: 2.8 million euro. ICT-Project **GALAXY - *interface for complex digital system integration.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.3 Embedded Systems Design. Start date: 01/12/2007; Duration: 36 months; Contract Type: Collaborative project; Project Reference: 214364; Project Cost: 4.08 million euro; Project Funding: 2.9 million euro. ICT-Project **DINAMICS - *Diagnostic Nanotech and Microtech Sensors.*** Funded under 6th FWP (Sixth Framework Programme). FP6-NMP 'Nanotechnologies and nanosciences, knowledge-based multifunctional materials and new production processes and devices'. Contract Type: Integrated project; Project Reference:IP

	026804-2. Start date: 01/04/2007. Duration: 18 + 30 months. Project Cost:7276856 Euro. Project Funding: 4499542 Euro. http://www.dinamics-project.eu/ ICT-Project **SHARE - *Sharing open source software middleware to improve industry competitiveness in the embedded systems domain.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.7 Network embedded and control systems. Start date: 01/05/2008; Duration: 24 months; Contract Type: Coordination and support actions; Project Reference: 224170; Project Cost: 1.1 million euro; Project Funding: 590000.00 euro.

Team Leader	
	Rolf Ernst (TU Braunschweig)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Participates in Intercluster activity: Integration Driven by Industrial Applications
Research interests	Research interests include embedded architectures, hardware-/software co-design, real-time systems, and embedded systems engineering.
Role in leading conferences/journals/etc in the area	He chaired major international events, such as the International Conference on Computer Aided Design of VLSI (ICCAD), or the Design Automation and Test in Europe (DATE) Conference and Exhibition, and was Chair of the European Design Automation Association (EDAA), which is the main sponsor of DATE. He is a founding member of the ACM Special Interest Group on Embedded System Design (SIGBED), and was a member of the first board of directors. He is an elected member (Fachkollegiat) and Deputy Spokesperson of the "Computer Science" review board of the German DFG (corresponds to NSF). He is an advisor to the German Ministry of Economics and Technology for the high-tech entrepreneurship program EXIST (www.exist.org).

Team Leader	
	Petru Eles (Linköping University)
Technical role(s) within Artist2	Main areas of research: Embedded Systems Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Participates in Intercluster activity: Integration Driven by Industrial Applications
Research interests	Research interests include electronic design automation, hardware/software co-design, real-time systems, design of embedded systems and design for testability.
Role in leading conferences/journals/etc in the area	- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; - Associate Editor, IEE Proceedings - Computers and Digital Techniques; - TPC Chair and General Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS). - Topic chair, Design Automation and Test in Europe (DATE). - Topic Chair, Int. Conference on Computer Aided Design (ICCAD). - Program chair of the Hw/Sw Codesign track, IEEE Real-Time Systems Symposium (RTSS). - TPC Chair IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia). - Steering Committee Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS).
Awards / Decorations	- Best paper award, European Design Automation Conference (EURO-DAC), 1992. - Best paper award, European Design Automation Conference (EURO-DAC), 1994. - Best paper award, Design Automation and Test in Europe (DATE), 2005. - Best presentation award, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS), 2003. - IEEE Circuits and Systems Society Distinguished Lecturer, for 2004 - 2005.

Team Leader	
	Dr. Stylianos Mamagkakis IMEC vzw. http://www.imec.be
Technical role(s) within ArtistDesign	Representing IMEC Nomadic Embedded Systems (NES) division in: -Cluster: SW Synthesis, Code Generation and Timing Analysis -Cluster: Operating Systems and Networks -Cluster: Hardware Platforms and MPSoC Design -Intercluster activity: Design for Adaptivity -Intercluster activity: Design for Predictability and Performance -Intercluster activity: Integration Driven by Industrial Applications
Research interests	Stylianos Mamagkakis received his Master and Ph.D. degree in Electrical and Computer Engineering from the Democritus Uni. Thrace (Greece) in 2004 and 2007, respectively. Since 2006, he coordinates a team of PhD students within the NES division at IMEC, Leuven, Belgium. His research activities mainly belong to the field of system-level exploration, with emphasis on MPSoC run-time resource management and system integration.
Role in leading conferences/journals/etc in the area	Stylianos Mamagkakis has published more than 35 papers in International Journals and Conferences. He was investigator in 9 research projects in the embedded systems domain funded from the EC as well as national governments and industry.
Notable past projects	Project leader of MNEMEE IST project www.mnemee.org Project leader of OptiMMA IWT project www.imec.be/OptiMMA Participation in: 1 international IMEC project (M4), 3 European IST projects (AMDREL, EASY, ARTIST2), 2 Greek projects (PRENED, DIAS)
Awards	1st prize in 'Technogenesis' Competition for Business Innovation, Greece, June'06 3rd prize in 'Otenet Innovation 2006' Competition for Business Innovation, Greece, November'06
Further Information	http://www2.imec.be/imec_com/nomadic-embedded-systems.php

Team Leader	
	Professor Axel Jantsch KTH http://web.it.kth.se/~axel/
Technical role(s) within ArtistDesign	A. Jantsch contributes to KTH participation and to the work on formal models of computation and communication and the ForSyDe framework. Furthermore, he also contributes to Hardware Platforms and MPSOC Design with focus on run-time environments and analysis techniques.
Research interests	A. Jantsch's main research topics are models of computation, modelling and analysis of embedded systems and SoCs, networks on chip.
Role in leading conferences/journals/etc in the area	TPC cochair of NoC Symposium 2009 Guest editor for IEEE Transactions on CAD TPC member of NOCS, DATE, CODES
Notable past projects	**ANDRES** (Analysis and Design of run-time Reconfigurable, heterogeneous Systems) Project) – EU FP6 (http://andres.offis.de/) **SPRINT** (Open SoC Design Platform for Reuse and Integration of IPs): EU FP6 (http://www.ecsi-association.org/sprint) **MOSART** (Mapping Optimization for Scalable multi-core ARchiTecture) – EU FP7 (http://www.mosart-project.org/)

Team Leader	
	Raphaël David, Ph.D (CEA LIST)
Technical role(s) within ArtistDesign	Participates in Hardware Platforms and MPSoC Design
Research interests	Main research interests are related to the exploration of new execution models for multiprocessing System-on-Chip and on development of exploration framework for multi- and many-core architectures. He is also studying advance strategies for the deployment and the management of multi-task applications onto multi- and many-core devices. He is also involved in the implementation of dynamically reconfigurable processors for image processing and low power design.

Team Leader	
	Professor Giovanni De Micheli EPFL http://si2.epfl.ch/~demichel/
Technical role(s) within ArtistDesign	Giovanni De Micheli contributes to EPFL participation and to the work on models of computation for 3D integrated circuits, as well as on models as policies for thermal evaluation and control
Research interests	De Micheli's research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis, hw/sw codesign and low-power design, as well as systems on heterogeneous platforms including electrical, micromechanical and biological components.
Role in leading conferences/journals/etc in the area	General Chair of DATE 2010
Notable past projects	**Nano-tera.ch** (Engineering Complex Systems for Health, Security and the Environment) Swiss Federal grant (http://www.nano-tera.ch/) **PROD3D (**Programming for Future 3D Architecture with Many Cores): *EU FP7 starting project*

4.2 Affiliated Industrial Partners

	Daniel Karlsson (Volvo Technology Corporation)
Technical role(s) within ArtistDesign	Architecture and Design of Automotive Embedded Systems

	Kai Richter (SymTAVision GmbH)
Technical role(s) within ArtistDesign	Formal Performance Analysis and Optimization of Embedded Systems, Reliable System Integration, Early Architecture Exploration

	Dr. Arne Hamann (Robert Bosch GmbH)
Technical role(s) within ArtistDesign	Automotive Software Architectures

	Matthias Gries (Intel Germany)
Technical role(s) within ArtistDesign	Microprocessor Technology Lab, new computer architecture for embedded systems

	Rune Domsteen (Prevas A/S)
Technical role(s) within ArtistDesign	Embedded systems platform development

	Morten Kragh (Bang & Olufsen ICEpower)
Technical role(s) within ArtistDesign	Execution platforms for audio signal processing

	Dr. Valter Bella (Telecom Italia Lab)
Technical role(s) within ArtistDesign	Architecture and Design of Wireless Sensor Networks and Embedded Systems for Ambient Intelligence

4.3 Affiliated Academic Partners

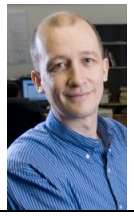
	Ass. Professor Dimitrios Soudris (NTUA/ formerly DUTH) www.microlab.ntua.gr www.ee.duth.gr
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	Dimitrios Soudris received his Diploma in Electrical Engineering from the University of Patras, Greece, in 1987. He received the Ph.D. Degree in Electrical Engineering, from the University of Patras in 1992. He is currently working as Assistant Professor in Electrical and Computer Engineering, National Technical University of Athens (NTUA), Greece. His research interests include low power design, parallel architectures, embedded systems design, and VLSI signal processing. He was leader and principal investigator in numerous research projects funded from the Greek Government and Industry as well as the European Commission (ESPRIT II-III-IV and 5th, 6th and 7th IST). He is a member of the IEEE, the VLSI Systems and Applications Technical Committee of IEEE CAS and the ACM.
Role in leading conferences/journals/etc in the area	Dimitrios Soudris has (co-)authored over 180 papers in international journals and conferences, and has coauthored and edited 4 text books. He has served as General Chair and Program Chair for PATMOS' 99 and 2000 and General Chair IEEE/CEDA VLSI-SOC 2008. He received an award from INTEL and IBM for the project results of LPGD #25256 (ESPRIT IV) and 4th position in ASP-DAC 2005 Design Contest for AMDREL IST-34793.
Notable past projects	LPGD project Design of a low power GFSK/GMSK modulator/demodulator for DECT receivers. AMDREL project Development of dynamic memory management design methodologies for emebedded syetems. Design of a low energy FPGA and a software supported design flow.
Awards / Decorations	Dimitrios Soudris received an award from INTEL and IBM for the project results of LPGD #25256 (ESPRIT IV) and 4th position in ASP-DAC 2005 for AMDREL IST-34793.
Further Information	Dimitrios Soudris is also member at the Institute of Communications and Computer Systems

	Prof. David Atienza (EPFL, Switzerland, and Complutense University of Madrid, Spain) http://esl.epfl.ch/
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	David Atienza received his MSc and PhD degrees in Computer Science from Complutense University of Madrid (UCM), Spain, and Inter-University Micro-Electronics Center (IMEC), Belgium, in 2001 and 2005, respectively. Currently he is Professor and Director of the Embedded Systems Laboratory (ESL) at Ecole Polytechnique Fédérale de Lausanne, Switzerland, and Adjunct Professor at the Computer Architecture and Automation Department of UCM. His research interests focus on design methodologies for high-performance embedded systems and Systems-on-Chip (SoC), including new thermal management techniques for Multi-Processor SoCs, dynamic memory management and memory hierarchy optimizations for embedded systems, novel architectures for logic and memories in forthcoming nano-scale electronics, Networks-on-Chip interconnection design, and low-power design of embedded systems.
Role in leading conferences/journals/etc in the area	In these fields, David Atienza is co-author of more than 90 publications in prestigious journals and international conferences, such as, IEEE TCAD, IEEE Micro, IEEE T-VLSI Systems, ACM TODAES, Elsevier-Integration: The VLSI Journal, DAC, ICCAD, DATE, ASP-DAC, etc. Also, he is part of the Technical Program Committee of the DATE, ICCAD, GLSVLSI, VLSI-SoC, RTAS, SBCCI and PATMOS conferences, and Associate Editor of IEEE Transactions on CAD (in the area of System-Level Design) and Elsevier Integration: The VLSI Journal. He is the general chair of VLSI-SoC 2010 and organizer of several conferences including GLSVLSI '09, ISVLSI '09 and SBCCI '09.
Notable past projects	MDDTNSB-B22: "Materials, Devices and Design Technologies for Nanoelectronic Systems Beyond 22 nm CMOS" project *Development of reliability-aware design methodologies for emerging nano-scale electronics.* CMOSAIC project *Design of design 3D stacked processing architectures with interlayer cooling.* TIN2005-ARCHITECT project *HW/SW technologies for the design of high-performance processing systems*
Awards / Decorations	David Atienza received the nomination as co-author for the "2004 DAC Best Paper Award" and the "2006 ICCAD Best Paper Award". In September 2008 he was named IEEE Young Gold Member Coordinator in the area of EDA.
Further Information	Since 2008, he an elected member of the Executive Committee of the IEEE Council of Electronic Design Automation (CEDA).

	Associate Professor Per Gunnar Kjeldsberg (NTNU) www.iet.ntnu.no/en
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	Per Gunnar Kjeldsberg received his Sivilingeniør degree (MSc) in electrical engineering in 1992 from the Norwegian Institute of Technology. In 2001 he received the degree of Doktor ingeniør (PhD) from the same institution (now Norwegian University of Science and Technology, NTNU). During his doctoral studies, he focused on storage requirement estimation and optimization for data intensive applications. The research was performed in close cooperation with IMEC, in Leuven, Belgium, where he was a visiting researcher for nine months in all. His research interests are embedded hw/sw systems, with a focus on multi-media and digital signal processing applications. Between October 2005 and June 2006, Kjeldsberg was a visiting researcher at University of California, Irvine, Center for Embedded Computer Systems.
Role in leading conferences/journals/etc in the area	Kjeldsberg has (co-)authored a large number of conference and journal papers, and has been coauthor of a book in his field of interest. He is frequently used as reviewer for several international journals and conferences.
Notable past projects	CUBAN project Co-optimized Ubiqutious Broadband Access Networks with focus on cross-layer optimized implementation of DSP algorithms. CoDeVer/Embla Codesign, verification, and languages for embedded systems in close cooperation with industry partners
Further Information	Between 1992 and 1996 Kjeldsberg worked as a design engineer at Eidsvoll Electronics, designing communication control equipment based on embedded hw/sw solutions. Currently he is an Associate Professor at the Department of Electronics and Telecommunications, NTNU. Here he teaches several extensive undergraduate and graduate courses, and supervises a number of students at master and PhD level. Kjeldsberg is and has been a member of the board of directors both at the Faculty and in private companies.

4.4 Affiliated International Partners

	Prof. Krishnendu (Krish) Chakrabarty, Department of Electrical and Computer Engineering, Duke University, USA
Technical role(s) within ArtistDesign	Collaboration with DTU on microfluidics-based biochips. Contributions to the Hardware Platforms and MPSoC cluster.
Research interests	Design and test of system-on-chip integrated circuits, microfluidics-based biochips (digital microfluidics, microelectrofluidics), and wireless/sensor networks.
Role in leading conferences/journals/etc in the area	He is an Editor of the Journal of Electronic Testing: Theory and Applications (JETTA), an Associate Editor of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on VLSI Systems, IEEE Transactions on Biomedical Circuits and Systems, and ACM Journal on Emerging Technologies in Computing Systems. He serves on the editorial board of IEEE Design & Test of Computers. During 2006-2007, he served as an Associate Editor of IEEE Transactions on Circuits and Systems I, and before that as an Associate Editor of IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing.
Awards / Decorations	Prof. Chakrabarty is currently serving as an ACM Distinguished Speaker. He served as a Distinguished Visitor of the IEEE Computer Society for 2005-2007, and a Distinguished Lecturer of the IEEE Circuits and Systems Society for 2006-2007. He is also a recipient of the Humboldt Research Fellowship, awarded by the Alexander von Humboldt Foundation, Germany, in 2003.
Further Information	http://people.ee.duke.edu/~krish/

	Assist. Prof. Patrick Schaumont, Department of Electrical and Computer Engineering, Virginia Tech, USA
Technical role(s) within ArtistDesign	Collaboration with DTU on hardware description languages for MPSoC platforms. Contributions to the Hardware Platforms and MPSoC cluster.
Research interests	Design methods and architectures for secure embedded systems.
Further Information	http://www.ece.vt.edu/schaum/

5. Internal Reviewers for this Deliverable

- **Professor Bengt Jonsson** (Uppsala University)
- **Associate Professor Paul Pop** (DTU)