IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Workpackage Progress Report for Year 2

Jointly-executed Programme of Integrating Activities (JPIA) Report

With input from all clusters.

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Policy Objective (abstract)

Each ArtistDesign research activity has work within both the JPIA and the JPRA workpackages. The JPIA activities are carried out on a global, NoE level, transcending the clusters. They form the supporting background for integration of the NoE, and are executed in phase and in interplay with the JPRA research activities. For instance, funds for staff mobility will be allocated taking into account the needs for research.

The activities listed here will promote integration of geographically dispersed teams. All these activities will have long-lasting effects, well beyond the duration of the initial EC funding.

These activities include Joint Technical Meetings, Staff Mobility and Exchanges, Tools and Platforms.

Versions

number	comment	date
1.0	First version delivered to the reviewers	December 18th 2009

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1. Overview of the Workpackage

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.1 ArtistDesign Participants and Affiliated Partners

Each ArtistDesign research activity contributes to achieving both research and integration goals. Thus, each has work within both the JPIA and the JPRA workpackages, and all partners and affiliated partners participate in the Joint Programme of Integration Activities.

1.2 Starting Date, and Expected Ending Date

These activities are intimately related to the JPRA (Joint Programme of Research Activities) and run for the entire duration of the NoE.

1.3 Policy Objective

The JPIA activities are carried out on a global, NoE level, transcending the clusters. They form the supporting background for integration of the NoE, and are executed in phase and in interplay with the JPRA research activities. For instance, funds for staff mobility will be allocated taking into account the needs for research.

The activities listed here will promote integration of geographically dispersed teams. All these activities will have long-lasting effects, well beyond the duration of the initial EC funding.

These activities include Joint Technical Meetings, Staff Mobility and Exchanges, Tools and Platforms.

2. Joint Technical Meetings

Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

They are often organized around the annual General Assembly and Review, or around some of the main conferences in the area (most of which are piloted by a majority of ArtistDesign partners).

Depending on the context and in particular on the maturity of the topics under discussion, these Joint Technical Meetings may be open to the public, or by invitation (which implicitly includes all interested ArtistDesign partners).

-- Changes wrt Y1 deliverable --

All new text: this entire chapter pertains only to activity in Year 2.

2.1 Modelling and Validation Cluster

Workshop : ArtistDesign Workshop on Embedded Systems in Healthcare 2009
Eindhoven, The Netherlands, 7 December 2009.
The goal of the Workshop on Embedded Systems in Healthcare is to strengthen the connections between academic research and industry, or to be more precise, to increase the understanding in the academic world of industrial issues in embedded systems engineering and together come to a shared agreement on research directions that seem worthwhile to pursue. The speakers at the workshop work at different medical companies or are participants in the ArtistDesign network with extensive experience in healthcare. The topics include "How to design long lasting devices for a fast changing world?", "Cochlear Implant Systems: today's challenges in embedded firmware design", and "Embedded Contributions to an Intensive Care Safety Concept".

http://www.artist-embedded.org/artist/WESH-2009.html

Workshop : 2nd International Workshop on Model Based Architecting and Construction of Embedded Systems (ACES^{MB} 2009)
ACM/IEEE 12th Int. Conf. on Model Driven Engineering Languages and Systems
Denver, Colorado, USA – October 6th, 2009

The development of embedded systems with real-time and other critical constraints raises distinctive problems. In particular, development teams have to make very specific architectural choices and handle key non-functional constraints related to, for example, real-time deadlines and to platform parameters like energy consumption or memory footprint. In this context, the last few years have seen an increased interest in using model-based engineering (MBE) techniques. MBE techniques are interesting and promising for the following reasons: They allow to capture dedicated architectural and non-functional information in precise (and even formal) domain-specific models, and they support a layered construction of systems, in which the (platform independent) functional aspects are kept separate from architectural and non-functional (platform specific) aspects, where the final system is obtained by combining these aspects later using model transformations. The topics handled in the workshop were:

Architecture description languages (ADLs); Domain specific design and implementation languages; Languages for capturing non-functional constraints; Component languages and system description languages.
http://www.artist-embedded.org/artist/Overview,1706.html

Workshop : Second IEEE International workshop UML and Formal Methods
11th International Conference on Formal Engineering Methods
Rio de Janeiro, Brasil – December 8th, 2009

Many interest groups from a research perspective are in favour of the creation of this workshop. For more than a decade now, the two communities of UML and formal methods have been working together to produce a simultaneously practical (via UML) and rigorous (via formal methods) approach to software engineering. UML is the de facto standard for modelling various aspects of software systems in both industry and academia, despite the inconvenience that its current specification is complex and its syntax imprecise. The fact that the UML semantics is too informal have led many researchers to formalize it with all kinds of existing formal languages, like OCL, Z, B, CSP, VDM, Petri Nets, UPPAAL, HOL, Coq, PVS etc. This second workshop will be open to various subjects as the main objective is to encourage new initiatives of building bridges between informal, semi-formal and formal notations.
http://www.artist-embedded.org/artist/Overview,1663.html

Workshop : Fourth IEEE International workshop UML and AADL
14th International International Conference on Engineering of Complex Computer Systems
Potsdam, Germany – June 2nd, 2009

New real-time systems have increasingly complex architectures because of the intricacy of the multiple interdependent features they have to manage. They must meet new requirements of reusability, interoperability, flexibility and portability. These new dimensions favour the use of an architecture description language that offers a global vision of the system, and which is particularly suitable for handling real-time characteristics. Due to the even more increased complexity of distributed, real-time and embedded systems (DRE), the need for a model-driven approach is more obvious in this domain than in monolithic RT systems. The purpose of this workshop is to provide an opportunity to gather researchers and industrial practitioners to survey existing efforts related to behaviour modelling and model-based analysis of DRE systems.
http://www.artist-embedded.org/artist/Overview,1579.html

Workshop: Dagstuhl Seminar "Design and Validation of Embedded Systems"
Dagstuhl -- September 30 – October 4*, 2009*
The aim of this seminar was to discuss topics related to systems with concurrency in a broad set of application domains. We had a broad participation reflecting the various approaches to the problem, including language design, compiler construction, program analysis, formal methods, and testing. To focus the discussions, the seminar also included participants from application areas (embedded reactive systems, robotics, middleware, operating systems, and virtual machines) who have strong interests in verification. We hope these discussions inspired researchers to come up with long-term and practical solutions for the design and verification of concurrent systems. The seminar gathered almost 50 participants.
http://www.dagstuhl.de/de/programm/kalender/semhp/?semnr=09361

Workshop: 2nd International Workshop on Verification and Validation of Planning and Scheduling Systems
Toulouse -- September 29th, 2009

This ARTIST workshop is held in conjunction with ICAPS 2009. Verification techniques, such as model checking, and planning techniques have many commonalities. Planning and scheduling (P&S) systems are finding increased application in safety- and mission-critical systems that require a high level of assurance. Experience has shown that most errors are in domain models, which can be inconsistent, incomplete or inaccurate models of the target domains. However tools and methodologies for verification and validation (V&V) of P&S systems have received relatively little attention. The objective of this workshop is to maintain an interaction between the V&V and P&S communities, to identify specialized and innovative V&V tools and methodologies that can be applied to P&S. Topics of interest include: V&V of domain models, using technologies such as static analysis, theorem proving, and model checking; consistency and completeness of domain models; domain model coverage metrics; regression, stress and boundary testing; runtime verification of plan executions; generation of robust plans; compositional verification of domain models; how to structure domain models which are more amenable to static analysis; inspection methods; the relationship between timed automata and domain models; investigations of the impact wrt. V&V of procedural versus declarative plan models; etc..
http://www-vvps09.imag.fr/

Workshop: 9th International Workshop on Runtime Verification

Grenoble – June 26th- June 28th, 2009

This ARTIST workshop is held in conjunction with CAV 2009, the objective of RV'09 is to bring scientists from both academia and industry together to debate on how to monitor and analyze the execution of programs, for example by checking conformance with a formal specification written in temporal logic or some other form of history tracking logic. The purpose might be testing a piece of software before deployment, detecting errors after deployment in the field and potentially triggering subsequent fault protection actions, or the purpose can be to augment the software with new capabilities in an aspect oriented style. The longer-term goal is to investigate whether the use of lightweight formal methods applied during the execution of programs is a viable complement to the current heavyweight methods proving programs correct always before their execution, such as model checking and theorem proving. This year's workshop is organized as a satellite event of CAV.

http://www-rv2009.imag.fr/

Automatic test generation of Reactive and timed systems, T. Jéron MSR'09 (http://msr09.irccyn.ec-nantes.fr/), Nantes, France French colloquium on modelling, analysis and command of reactive and real-time systems.

Automatic test generation of Reactive and timed systems, T. Jéron ETR'09 summer school (Ecole d'été Temps réel, http://etr09.telecom-paristech.fr/), Paris, France, 31/08-04/09. Summer school on methods, techniques and tools for real-time systems.

EJCP (Ecole Jeunes Chercheurs en Programmation, http://ejcp2009.inria.fr/) Rennes, France, June 2009. Summer school organized by V. Rusu on modelling, analysis of computer systems.

GASICS Workshop on Games for Design, Verification and Synthesis. Co-located with CAV'09, Grenoble, June 28, 2009. *www.lsv.ens-cachan.fr/Events/gasics09/*

GASICS is an ESF project of the EUROCORES programme LogICCC (Modeling intelligent interaction – Logic in the Humanities, Social and Computational Sciences). It studies game theoretic formalizations of interactive computational systems and algorithms for their analysis

and synthesis. Our aim is to extend the existing notions of games played on graphs introduced by computer scientists. Currently, most of the games played on graphs are of the sort "two-player zero-sum", we aim to extend them to "multiple-player non-zero-sum", and show the applicability of the new theory to the analysis and synthesis of interactive computational systems. The aim of this workshop is to bring together researchers working on game-related subjects, and to discuss on various aspects of game theory in the fields where it is applied.

QUANTLOG Workshop on Quantitative Logics July 11, 2009, Rhodes, Greece Satelite event of ICALP 2009 *quantlog09.web.auth.gr/*

The Workshop on Quantitative Logics (QUANTLOG 2009) will take place in Rhodes, Greece, July 11, 2009 as a satellite event of the 36th International Colloquium on Automata, Languages and Programming (ICALP 2009). It is organized under the auspices of the Department of Mathematics of the Aristotle University of Thessaloniki. The aim of the workshop is to provide a forum for researchers interested in the topic of quantitative logics to present their new results and to combine their efforts in the further development of the topic, with emphasis to its connection with automata theory as well as to practical applications.

2.2 Software Synthesis, Code Generation and Timing Analysis cluster

Tutorial: S. Mamagkakis and P. R. Panda: Memory Architectures and Software Transformations for System Level Design, ASP-DAC 2009
Yokohama, Japan, – January, 2009
In this tutorial a memory-aware system level design flow was presented that can address strict power and performance budgeting problems by customizing both the underlying memory architectures/organizations, as well as by transforming the system-level source code to generate an input for system-level design that is better tuned to the memory architectures and organizations. Such a "memory-aware" system level design flow can result in LSI designs exhibiting superior performance, power and memory footprint characteristics.
http://www.aspdac.com/aspdac2009/tutorial/

Joint Computer Architecture Seminar (RWTH Aachen and Edinburgh)
Aachen, Germany – Feb. 11, 2009
Objectives for the meeting: During the seminar, different subjects from the research areas of both groups were presented and intensively discussed.
Organizer: This event was organized by RWTH Aachen
Other participants: a research group from the Edinburgh Institute for Computing Systems Architecture (ICSA)
Conclusion: The major focus was on processor customization for embedded applications, fast simulation, advanced profiling, and multi-core programming. Approaches were discussed.

Invited Talk: Predictable Multi-Cores
Verimag – February 13, 2009
Objective: To explain the PROMPT design principles on predictable multi-core architectures.
Presenter: Reinhard Wilhelm (Saarland U.)

Course: Retargetable Compilation
Lugano, Switzerland, Feb. 16-19 & Feb 23-25, 2009
Objectives: Spreading excellence in memory-architecture aware compilation and processor retargetability beyond ArtistDesign partners.

Presenters: Peter Marwedel (TU Dortmund), Rainer Leupers (RWTH Aachen)
Other participants: about 20 students
Conclusion: The new, extended format turned out to be very useful.
http://www.alari.ch

Invited talk: From Embedded Systems to Cyber-Physical Systems: Does the Name Change Matter? – Inauguration of the Uppsala Programming for Multicore Architectures Research Center (UPMARC)
Uppsala, Sweden, March 26, 2009
Objectives: Providing an overview over Embedded Systems Research at Dortmund
Speaker: Peter Marwedel (TU Dortmund)
http://www.it.uu.se/research/upmarc/inauguration

SPECIAL SESSION – Programming MPSoC Platforms: Roadworks Ahead! (Multi-core Applications Special Day) DATE 2009
Nice, France, – April 23, 2009
Objectives for the meeting: To consolidate today's different MPSoC programming approaches, and to provide focus for future R&D activities.
Organizer: This panel session was organized by R. Leupers (RWTH Aachen) and moderated by M. de Lange (ACE).
Other participants: M. Bekooij from NXP, regular DATE attendees
http://www.date-conference.com/date09/conference/date09-session-12-1

Meeting: Joint TA/MPSoC meeting at DATE
Nice, France, April 23, 2009
Objectives for the meeting: To discuss the problem of timing predictability for MPSoC and multi-core from both an analysis and system design perspective.
Organizer: Björn Lisper (MDH)
Other participants: Peter Puschner (Vienna), Abhik Roychoudhury (N.U. Singapore), Simon Schliecker (TU Braunschweig), Mircea Negrean (TU Braunschweig)
Petru Eles (Linköping), Stylianos Magmakakis (IMEC), Paolo Burgio (Bologna), Paul Pop (TU Denmark), Reinhard Wilhelm (USaar), Niklas Holsti (Tidorum)
Conclusions: A number of presentations were given, reflecting the state of the art for timing models and timing analysis both for the system design level and for the code level. The impact of the design on predictability, for both these levels, was discussed, and some possible solutions were presented. It was decided to have a follow-up meeting in the fall.

Workshop: Software & Compilers for Embedded Systems (SCOPES) 2009
Nice, France – April 23-24, 2009
Objectives for the meeting: SCOPES focuses on the software generation process for embedded systems.
Organizer: Heiko Falk (TU Dortmund)
Conclusions: There were many discussions between cluster members at SCOPES (starting already on the eve before the sessions), at DATE, making the entire week the key joint event in spring.

http://www.scopesconf.org/scopes-09

Keynote: Reinhard Wilhelm – The PROMPT Design Principles for Predictable Multi-Core Architectures, SCOPES 2009
Nice, France – April 24, 2009
Objectives: The precision of the results and the efficiency of timing-analysis methods are highly dependent on the predictability of the execution platform. The possibility of proving the safety

of embedded systems is seriously compromised by architectural developments aiming exclusively at improving average-case performance.
Presenter: Reinhard Wilhelm (Saarland University)
Conclusions: We propose design principles for multi-core architectures to provide efficiently predictable good worst-case performance as needed for embedded control in the aeronautics and automotive industries supporting the Integrated Modular Avionics (IMA) and the Automotive Open System Architecture (AUTOSAR) development trends.
http://www.scopesconf.org/scopes-09

Meeting: Technical Meeting within Predator
Pisa, Italy – 23rd June, 2009
Objectives for the meeting: Discussing interferences, in particular regarding memory.
Participants: Researchers from SSSA, ETHZ, USAAR, UDORT and ABSINT
Conclusions: We clarified notions of memory interference models based on the real-time calculus, timing guarantees for pre-emptive schedules, cache-related context switch costs and the status of the ERIKA operating system. This provided the starting point for the cooperation of USAAR with SSSA on cache-aware scheduling.

Invited Talk: Timing Analysis of Real-Time Software - Workshop on Quantitative Analysis of Software
Grenoble, France – June 28, 2009
Objective: Gaving insights into the principles of worst-case execution time analysis and explained current challenges, including transformation of flow information and hardware modelling in the presence of timing anomalies. Further, research on measurement-based timing analysis was presented.
Presenter: Raimund Kirner.
http://www.eecs.berkeley.edu/~sseshia/qa09/

Meeting: 2nd Workshop on Mapping Applications to MPSoCs, 2009
St. Goar*, Germany – June 29-30, 2009*
Objectives for the meeting: This is the flagship workshop of this cluster. The goal of this workshop is to establish links between leading researchers in the area and to stimulate advanced research.
Organizer: Peter Marwedel (TU Dortmund)
Other participants: About 50
Conclusions: We are reaching out far beyond the ArtistDesign network. The workshop is now a key forum for discussions in this area. Attendees expressed their strong interest to continue this series of informal workshops as a platform for discussions.
http://www.artist-embedded.org/artist/-map2mpsoc-2009-.html

Meeting: 9th International Workshop on Worst-Case Execution Time Analysis, 2009
Dublin*, Ireland – June 30, 2009, in connection with ECRTS 2009*
Objectives for the meeting: To present and discuss recent work in WCET analysis of all kinds of systems by static or dynamic methods.
Organizer: Niklas Holsti (Tidorum Ltd)
Other participants: About 35
Conclusions: Most of the reported work still deals with single-processor systems where the growing complexity of programs and processors is a continuing challenge. However, an invited talk by Prof. Petru Eles (Linköping University) addressed MPSoCs and somewhat similar ideas were presented in a workshop paper by Martin Schoeberl and Peter Puschner (Vienna University of Technology).
http://www.artist-embedded.org/artist/-WCET-2009-.html

Keynote: Emerging multi-core hardware platforms and their software support challenges, ECRTS 2009
Dublin, Ireland, – July 1-3, 2009
Objectives: In this keynote talk, the latest developments and future directions of hardware MPSoC platforms for nomadic embedded applications were presented. This keynote was also relevant for the Scheduling and Resource Management activity.
Speaker: S. Mamagkakis (IMEC)
Conclusions: Next to the hardware perspective, the software related challenges of these emerging MPSoC platforms were discussed and some of the proposed parallelization and memory hierarchy management solutions were evaluated.
http://ecrts09.dsg.cs.tcd.ie/keynote-speaker.php

Invited Tutorial: WCET Analysis: Problems, Methods and Time-Predictable Architectures - Acaces 2009. Fifth International Summer School on Advanced Computer Architecture and Compilation for Embedded Systems
Terrassa (near Barcelona), Spain – July 12-18, 2009
Objectives: Providing an overview over WCET analysis and time-predictable hardware/ software architectures.
Presenter: Peter Puschner (TU Vienna)
http://www.hipeac.net/acaces2009/

Special Series of presentations: Overview of research results from Dortmund
Samsung and SNU, Seoul (Korea), Kyushu U., Fukuoka (Japan), NTU and NUS, Singapore, IIT, Delhi (India), – Aug. 3-14, 2009
Objectives for the meeting: These talks provided an overview over research activities in the "Design Automation for Embedded Systems" group at TU Dortmund, including results from the ArtistDesign NoE and the work on the WCC compiler.
Presenter: Peter Marwedel (TU Dortmund)
Conclusions: This tour through parts of Asia was a very efficient way of strengthening the ties with top research groups in Asia.

Tutorial : Multicore and Hard Real-Time Systems - Swedish Multicore Day
Kista, Sweden – Sept 4, 2009
Objectives: Describing the inherent problems with timing predictability for conventional multicore architectures, and gaving an account for ongoing research in the area to practicioners in industry.
Presenter: Björn Lisper (Mälardalen U.)
http://www.sics.se/multicoredays

Keynote : From Performance to Time-Predictability
9th Architectures and Compilers for Embedded Systems (ACES) Symposium
Edegem, Belgium – September 7-8, 2009
Objectives: Outlining the problems of building predictable hardware/software systems and discussing strategies for constructing systems that provide both temporal predictability and performance.
Presenter: Peter Puschner (TU Vienna)
http://www.elis.ugent.be/aces/index.php?page=activities

ARTIST Summer School in Europe 2009
Autrans – Sept. 7-11, 2009
Objectives: Disemination of research results
Presenters: Invited presenters include Jan Beutel, and Lothar Thiele
http://www.artist-embedded.org/artist/Overview,1633.html

Invited Talk: 7th IEEE East-West Design & Test Symposium – EWDTS'09
Moscow, Russia, - Sept. 19.2009
Objectives for the meeting: This talk provided an overview over research activities in the "Design Automation for Embedded Systems" group at TU Dortmund, including results from the ArtistDesign NoE.
Presenter: Peter Marwedel (TU Dortmund)
Conclusions: There is a huge interest in Russia to stay up-to-date with recent research in Western Europe.
http://www.ewdtest.com/conf/

Meeting: Static WCET Analysis of multi-process and Multi-processor systems
Saarbrücken, Germany – 25th of September, 2009
Objectives for the meeting: To discuss possible approaches for safe WCET analysis of multi-task / multi-core systems, and how to use such possible approaches to do WCET-aware code optimization for such systems.
Organizer: Christian Ferdinand (AbsInt)
Other participants: Reinhard Wilhelm (Saarland U.), Sebastian Altmeyer (Saarland U.), Claire Burguiere (Saarland U.)), Daniel Grund (Saarland U.), Jan Reineke (Saarland U.), Henrik Theiling (AbsInt), Christoph Cullmann (AbsInt), Heiko Falk (TU Dortmund), Jan Kleinsorge (TU Dortmund), Sascha Plazar (TU Dortmund)

Workshop: Shape Analysis, Timing Analysis - PUMA Workshop
San Servolo Island, Venice – Oct. 5 and 6, 2009
Objectives: Providing an overview over Shape Analysis and on Timing Analysis at the PUMA workshop. This workshop is an annual event held by the PUMA Graduate School of LMU and TU Munich.
Presenter: Reinhard Wilhelm (Saarland U.)
http://puma.in.tum.de/wiki/Venice_2009

Workshop on Reconciling Performance with Predictability (RePP)
Grenoble, France, – October 15, 2009
Objectives for the meeting: The RePP workshop is concerned with embedded systems that are characterized by efficiency requirements on the one hand and critical constraints on the other. Offline guarantees for the satisfaction of critical constraints have to be derived by appropriate methods.
Organizers: Lothar Thiele (ETH Zürich), Reinhard Wilhelm (Saarland U.), Theo Ungerer (U. of Augsburg), Bengt Jonsson (Uppsala U.), Jian-Jia Chen (ETH Zürich)
Conclusions: The discussion included the abstraction mechanism used for structuring systems, which has to consider resources as first-class citizens.

Workshop: 5th Workshop on Embedded Systems Education, 2009
Grenoble, France, – October 15, 2009
Objectives for the meeting: Embedded system education is still a very young area and frequently restricted to teaching the details of microcontroller programming. A long-term objective of this workshop is to improve the visibility of work in the area and to stimulate the introduction of broader curricula.
Organizer: Peter Marwedel (TU Dortmund)
Other participants: About 30
Conclusions: Visibility was improved by the inclusion of the proceedings in the ACM digital library. Presenters included top researchers from the US and Asia. Attendees were extremely satisfied with the quality of the presentations.
http://www.artist-embedded.org/artist/-WESE-09-.html

Meeting: Joint TA/MPSoC meeting at ESWEEK

Grenoble, France, October 16, 2009
Objectives for the meeting: to foster the contacts between the MPSoC design and timing analysis communities, and build the ground for future research collaborations, by working together on a concrete design example.
Organizer: Björn Lisper (Mälardalen)
Other participants: Raimund Kirner (Vienna), Peter Puschner (Vienna), Simon Schliecker (TU Braunschweig), Stylianos Magmakakis (IMEC), Praveen Raghavan (IMEC), Iain Bate (York), Claire Burguière (USaar), Daniel Grund (USaar), Francesco Paterna (Bologna)
Conclusions: A concrete design example was presented. The example is a safety-critical avionics system with different parts for control, avionics bus interface, and health monitoring of the system. The different parts of the system have different levels of integrity, and different real-time constraints. Different HW/SW system designs, supporting the requirements on the system, were discussed. It was concluded that the example should be further refined in order to support further joint work in system design for timing predictability.

Workshop: 1st Workshop on Software Synthesis, 2009
Grenoble, France, – October 16, 2009
Objectives for the meeting: An increasing amount of software is not written manually any more. Rather, software is synthesized from abstract models of the required functionality. Software synthesis has been implemented in various disperse communities. The workshop aimed at bringing these communities together.
Organizer: Peter Marwedel (TU Dortmund); Alberto Sangiovanni-Vincentelli
Other participants: About 20
Conclusions: Presenters at this workshop presented industrial as well as academic results. Attendees agreed on the necessity of more work in this area.
http://www.artist-embedded.org/artist/-WSS-09-.html

Keynote: Embedded Systems - Trends, Successes, Challenges
10th Anniversary of the Hasso-Plattner Institute
Potsdam – Nov. 18, 2009
Objectives: To celebrate its 10th anniversary, the Hasso-Plattner-Institiute holds a conference "Informatik-Impulse".
Presenter: Reinhard Wilhelm (Saarland University)
Conclusions: outlook onto future developments.

Invited Talk: P. Marwedel: IP – Embedded Systems Conference,
Grenoble, France, - Dec. 3, 2009
Objectives: The objective of this presentation is to spread the results from the first two Rheinfels workshops on mapping applications to MPSoCs.
Presenter: Peter Marwedel (TU Dortmund)
Other participants: Unknown at the time of writing this deliverable
Conclusions: Unknown at the time of writing this deliverable
http://www.design-reuse.com/ipesc09/program/

Keynote: Timing Analysis and Timing Predictability - Tag der Informatik
RWTH Aachen – December 4, 2009
Objectives: Presenting the current challenges and existing algorithms in timing analysis, covering also the additional challenges posed by multi-core systems and approaches to achieve predictability for them.
Presenter: Reinhard Wilhelm (Saarland U.)
http://www.nets.rwth-aachen.de/content/current_events/tdi/pro/index.html

2.3 Operating Systems and Networks Cluster

Meeting: Cluster Meeting
April 2-3, 2009 – Pisa (Italy)

Objectives for the meeting: Coordinating the future work of the Cluster activities.

Organizer: Giorgio Buttazzo, RETIS Lab, Scuola Superiore Sant'Anna (Pisa).

Participants: Giorgio Buttazzo (SSSA, Italy), Karl-Erik Årzén (Univ. of Lund, Sweden), Alan Burns (Univ. of York, UK), Iain Bate (Univ. of York, UK), Stylianos Mamagkakis (IMEC, Belgium), Luis Almeida (Univ. of Porto, Portugal), Magnus Persson (KTH, Sweden), Tahir Naseer (KTH, Sweden), Pau Marti (Univ. of Catalonia, Spain), Alejandro Alonso (Univ. of Madrid, Spain), Lucia Lo Bello (Univ. of Catania, Italy), Emanuele Toscano (Univ. of Catania, Italy), Michael Gonzalez Harbour (Univ. of Cantabria, Spain), Liesbeth Steffens (NXP, The Netherlands), Stefan Petters (Univ. of Porto, Portugal)

Meeting: Cache-aware scheduling
June 22, 2009 – Pisa (Italy)

Objectives for the meeting: Discussing on the effects of preemptive scheduling on cache memories and worst-case execution times, and identifying new research directions and possible collaborations.

Organizer: Giorgio Buttazzo, RETIS Lab, Scuola Superiore Sant'Anna (Pisa).

Other participants: Giorgio Buttazzo (SSSA), Marco Caccamo (UIUC), Marko Bertogna (Pisa), Francesco Esposito (Pisa), Mauro Marinoni (Pisa), Gang Yao (Pisa), Christoph Cullmann (Absint), Sebastian Altmeyer (Saarland), Claire Burguiere (Saarland), Sascha Plazar (TU Dortmund), Jan Kleinsorge (TU Dortmund), Andreas Schranzhofer (ETHZ), Jian-Jia Chen (ETHZ), Luca Benini (Bologna), Martino Ruggiero (Bologna).

Meeting: Graduate Course on Embedded Control Systems: Theory and Practice
June 8-12, 2009 – Pisa (Italy)

Objectives for the meeting: Providing the fundamentals concepts of real-time computing systems, including scheduling, resource management and timing analysis; Introducing the OSEK/VDX standards, taking as a reference implementation the Erika Enterprise kernel; Showing how to apply such concepts in practice, with examples based on the Flex platform and the Microchip dsPIC DSC microcontrollers.

Organizers: Giorgio Buttazzo (Pisa), Karl-Erik Arzen (Lund), Luis Almeida (Porto).

Other participants: Tesnim Abdellatif (Verimag), Simon Aittamaa (LTU), Gaetano Anastasi (Pisa), Claudia Barberis (Torino), Imene Ben Hafaiedh (VERIMAG), Irene Bicchierai (DSI), Torsten Bruns (University Paderborn), Laura Carnevali (Firenze), Jacques Combaz (Verimag), Johan Eriksson (LTU), Francesco Esposito (Pisa), Cyril Faure (IFP), Stefano Fontanelli (Pisa), Nadereh Hatami (Torino), Benjamin Kuch (Pisa), Rom Langerak (U.Twente), Holger Nahrstaedt (TU Berlin), Christian Nastasi (Pisa), Moritz Neukirchner (TU Braunschweig), Simon Perathoner (ETH Zurich), Sophie Quinton (Verimag), Lorenzo Ridi (Firenze), Andreas Schranzhofer (ETH Zurich), Vassiliki Sfyrla (Verimag), Colin Shaw (BCIT), Gang Yao (Pisa).

URL: http://www.artist-embedded.org/artist/ARTIST-Embedded-Control-2009.html

Meeting: OSPERT 2009 - Fifth International Workshop on Operating Systems Platforms for Embedded Real-Time Applications
Dublin, Ireland – June 30th, 2009

Objectives for the meeting: This workshop was intended as a forum for researchers and practitioners of RTOS to discuss the recent advances in RTOS technology and the challenges that lie ahead. The workshop consisted of submitted papers as well as invited presentations about academic state-of-the-art and industrial state-of-practice within the area of real-time operating systems architectures and services.

Organizers:

- Stefan M. Petters, IPP-Hurray, ISEP-IPP, Polytechnic Institute of Porto, Portugal

URL: http://ospert09.cister-isep.info/

Meeting: WCET 2009: Worst Case Execution Time Analysis
Dublin, Ireland – June 30th, 2009

Objectives for the meeting: The goal of the workshop was to bring together people from academia, tool vendors and users in industry interested in all aspects of timing analysis for real-time systems. The workshop fostered a highly interactive format with ample time for in-depth discussions. It provided a relaxed forum to present and discuss new ideas, new research directions, and to review current trends in this area. The presentations were kept short to leave plenty of time for interaction of attendees.

Organizers:

- - Niklas Holsti, Tidorum Ltd., Tiirasaarentie 32, 00200 Finland.

URL: http://www.artist-embedded.org/artist/WCET-2009.html

Meeting: RTN 2009: Real-Time Networks
Dublin, Ireland – June 30th, 2009

Objectives for the meeting: The Real Time Networks (RTN, formerly RTLIA) workshop was the seventh on the series of workshops that started at the 2002 ECRTS conference. RTN focuses on the current technological challenges of developing communication infrastructures that are real-time, reliable, pervasive and interoperable. The goal of this workshop was to bring together people from industry and academia that are interested in all aspects of real-time communication. The workshop provided a relaxed forum to present and discuss new ideas, new research directions and to review current trends in this area.

Organizers:

- - Eduardo Tovar, Polytechnic Institute of Porto, Portugal
- Jean-Dominique Decotignie, Swiss Center for Microtechnology CSEM, Switzerland.

URL: http://www.hurray.isep.ipp.pt/rtn09/index.php

Meeting between York and Aachen
York, UK – October 26th, 2009

Objectives for the meeting: Meeting with Prof Anke Schmeink, presentation of Aachen's UMIC Cluster (Ultra High-Speed Mobile Information & Communication) and its activities on the systematic design of mobile communication systems, presentation of York's research in evaluating performance and power dissipation of on-chip multiprocessor platforms

Meeting: 4.1.1: STANDRTS 2009 - Workshop on the Definition, Evaluation, and Exploitation of Modelling and Computing Standards for Real-Time Embedded Systems
Dublin, Ireland – June 30th, 2009

Objectives for the meeting: The main focus of the workshop is the identification of modelling constructs and usage styles that may lead to the better exploitation and/or evolution of the standards for the RTES domain in general.

Organizers:

- Sebastien Gerard, CEA LIST, France
- Henrik Lonn, Volvo Technology, Sweden
- Julio Medina, Universidad de Cantabria, Spain
- Laurent Rioux, THALES Research and Technology, France
- Ramin Tavakoli Kolagari, Volvo Technology, Sweden

URL: http://www.adams-project.org/standrts09/

2.4 Hardware Platforms and MPSoC Cluster

Meeting : ArtistDesign WP6 Cluster Meeting on Hardware Platforms and MpSoC
Braunschweig, Germany – June 25/26 2009
Objectives for the meeting: The main objective of this meeting was a mutual update on the joint research progress of the WP6 cluster participants, but speakers from the relevant industrial domains traditionally join (in tradition to previous years).
Organizer: Rolf Ernst (TUBS)
Other participants: All cluster members were present with several people. Other participants included Matthias Gries, Gregor Stellpflug (Intel Labs), Nico Feiertag, Kai Richter (Symtavision), Fabian Wolf (Volkswagen).
Conclusions : The meeting has highlighted key problems in the design and analysis of upcoming embedded systems and suggested solutions in different stages of maturity. Topics included performance analysis, reliability, adaptivity, and early design space exploration. The industrial speakers have contributed talks about timing analysis in automotive applications. The meeting has shown that formal methods as developed in this project are increasingly adopted in the industrial design practice.

https://webmail.ida.ing.tu-bs.de/twiki/bin/view/Main/ArtistDesignClusterMeeting

Meeting : Cluster meeting
Nice, France – April 25-26, 2009
Objectives for the meeting: Alignment and planning of cluster activities.
Organizer: Petru Eles (Linkoping)
Other participants: Most of the cluster partners were participating.
Conclusions : Discussions on collaboration and planning of the yearly cluster meeting.

Meeting : MP-MH MPSoC parallelization assistant and memory hierarchy assignment for MPSoC
Objectives for the meeting: The main objectives of the framework is to offer an automatic source code parallelization (MPA tool) and memory hierarchy management (MH tool) in order to map efficiently embedded software application on MPSoC platforms. This toolsuite is also used in the Software Synthesis, Code Generation and Timing Analysis cluster.
Organizer: IMEC

Other participants: NTUA/ICCS, TUDortmund
Conclusions: After the prototype versions of the MPSoC Parallelization Assistant (MPA) and Memory Hierarchy (MH) management tools were developed and tested, we proceeded in their integration as a single MP-MH tool, thus solving interdependency and exploration optimization issues. Currently, the affiliated partners of IMEC (ie, NTUA/ICCS) and core partners (TUDortmund/ICD) are trying to integrate their tool and design flows with the IMEC MP-MH framework in the memory assignment context of the MNEMEE FP7 project.
http://www.mnemee.org/ <http://www.mnemee.org/>
http://www.imec.be/cleanc <http://www.imec.be/cleanc>

2.5 Design for Adaptivity in Embedded Systems (Transversal Integration WP)

Workshop : Fourth International Workshop on Feedback Control Implementation and Design in Computing Systems and Networks (FeBID 2009), Cyber-Physical Systems Week,2009

San Francisco, US – April 16, 2009

Traditional practice in performance modeling focuses on using a variety of techniques including mathematical modeling, simulation, and analysis to understand the behavior of systems for the purpose of better design and evaluation. As IT systems, networks, and services become increasingly complex, this task becomes ever more difficult. In recent years, there has been considerable success in applying feedback control theory to analyzing and designing run-time IT control systems. Feedback control theory complements traditional modeling by providing formal mechanisms to dynamically control behavior of systems at run-time.

The FeBID series of workshops offer a unique opportunity for researchers and practitioners to discuss recent and innovative results in applying control theory to controlling performance of computing systems and networks. It provides a forum to exchange ideas and experiences on practical control system design and implementation and to identify future directions and challenges in aligning feedback control techniques with traditional performance modeling and simulation. The workshop program consisted of one invited plenary talk and 12 submitted papers. The workshop was co-chaired by Karl-Erik Årzén (ULUND) and several of the members of this activity participated in the PC. The workshop was co-funded by Artist.

http://controlofsystems.org/febid2009/

Workshop : Second Workshop on Adaptive and Reconfigurable Embedded Systems (APRES 09), Embedded Systems Week, 2009

Grenoble, France – October 11, 2009

This was the second workshop in the APRES series which is co-funded by Artist. It aims at discussing new and on-going research in the development and use of adaptive and reconfigurable embedded systems and gathering feedback from the embedded systems community at large. Of particular interest are new concepts and ideas for modeling and analyzing tradeoffs of embedded and real-time systems, novel algorithms and mechanisms to realize adaptation and reconfigurability, and experience reports with practical or industrial case studies. The workshop was co-organized by Luis Almeida, Karl-Erik Årzén (members of the activity), and Sebastian Fischmeister, Insup Lee, and Juilan Proenza (non-members), with several of the Artist partners in the programming committee. The workshop contained 12 submitted paper and Stylianos Mamagkakis of IMEC gave a very appreciated plenary presentation. The number of participants at the workshop was around 25. The papers of the workshop will be published by SIGBED Review.

http://www.artist-embedded.org/artist/Overview,1765.html

Course: ARTIST Graduate Course on Embedded Control Systems
Pisa, Italy – June 8-12, 2009
The fifth annual ARTIST Graduate Scool on Embedded Control Systems was organized and delivered by Giorgio Buttazzo and Mauro Marinoni (SSSA), Karl-Erik Årzén and Anton Cervin (ULUND), Paolo Gai (Evidence), Luis Almeida (UPorto), and Paulo Pedreiras (UAveiro).

The objectives of the course were to:

- Introduce the most important concepts and methodologies used to develop a real-time embedded system, including fundamentals of real-time scheduling, control and distributed systems;
- Show how to apply these concepts to develop simple real-time control applications using an embedded platform specifically developed for education.

http://www.artist-embedded.org/artist/Overview,1673.html

Meeting: Annual Activity Meeting
Pisa, Italy - April 2-3, 2009
Objectives for the meeting: Organize the activities during Year 2. Present the adaptive resource management related activities in FRESCOR, ACTORS, DysCAS together with the work at UPC/SSSA, DTU, and IMEC.
Organizer: Karl-Erik Årzén (ULUND) & Giorgio Buttazzo (SSSA)
Participating groups: ULUND, SSSA, TUKL, University of York, IMEC, UPorto, KTH, UPC, UPM, UCatania, DTU, UCantabria, Universidad Carlos III de Madrid, NXP, IPP
Conclusions:

- The structure for a wiki-based white paper on embedded system adaptivity was outlined and set up. Initial contents were added.

- It was decided that the activity should take the initiative to an one-day workshop on adaptive resource management to be held in conjunction with the Cyber-Physical Systems Week in Stockholm, Sweden in April 2010. This should also constitute the annual activity meeting for 2010.

Web site:http://www2.control.lth.se/ArtistAdapt/index.php/Main_Page/Meetings/Pisa_Apr_2009

Meeting : BIP – DOL, 13th Oct. 2009
Grenoble, France
Objectives for the meeting: The main goal of this meeting was to introduce the available execution platforms of the DOL framework and try to find a suitable one for BIP.
Organizer: Verimag
Other participants: Verimag, ETHZ
Conclusions : There are three execution platforms available from the DOL framework, i.e., the SHAPES platform, the broad band cell engine, and the DOL/MPARM simulator. It was concluded that the DOL/MPARM is suitable for the BIP timed model.

Meeting: Real-time Parameters, 1st Oct. 2009
Zurich, Switzerland
Objectives for the meeting: Establish a set of server-based resource-reservation strategies and their suitability for dynamic reconfigurations in resource-constraint systems.

Organizer: ETHZ
Other participants: ETHZ, SSSA
Conclusions: The well-known server-based resource-reservation strategies are not designed to be adaptive therefore, new methods and strategies are needed that can guarantee resource-reservations during configuration changes. A new server-based strategy and a mechanism for reconfiguration have been proposed. This is currently investigated jointly by ETHZ and SSSA.

Meeting : DySCAS Open Workshop
Brussels, Belgium – February 18, 2009
Objectives for the meeting: Dissemination of the results of the "Dynamically Self-configuring Automotive Systems" (DySCAS) FP6 project
Organizer: Volvo (coorganised and funded by Artist)
Conclusions : http://www.artist-embedded.org/docs/Events/2009/DySCAS/DySCAS%20workshop%20February%2018%20-%20Summary_MT.pdf
Web site: http://www.artist-embedded.org/artist/DySCAS-2009,1555.html

In addition KTH has had several meetings within the context of of the Dyscas project with Offis (ArtistDesign partner), Volvo (affiliated ArtistDesign partner), and Bosch, Daimler, Enea and Univ. of Grenwich.

2.6 Design for Predictability (Transversal Integration WP)

Meeting : Static WCET Analysis of multi-process and Multi-processor systems
Saarbrücken, Germany – 25th of September, 2009
Objectives for the meeting: To discuss possible approaches for safe WCET analysis of multi-task / multi-core systems, and how to use such possible approaches to do WCET-aware code optimization for such systems.
Organizer: Christian Ferdinand (AbsInt)
Other participants: Reinhard Wilhelm (Saarbrücken), Sebastian Altmeyer (Saarbrücken), Claire Burguiere (Saarbrücken), Daniel Grund (Saarbrücken), Jan Reineke (Saarbrücken), Henrik Theiling (AbsInt), Christoph Cullmann (AbsInt), Heiko Falk (Dortmund), Jan Kleinsorge (Dortmund), Sascha Plazar (Dortmund)

Meeting: Technical Meeting within Predator
Pisa, Italy – 23th June, 2009
Objectives for the meeting: Discussing interferences, in particular regarding memory.
Participants: Researchers from SSSA, ETHZ, USAAR, UDORT and ABSINT
Conclusions : We clarified notions of memory interference models based on the real-time calculus, timing guarantees for preemptive schedules, cache-related context switch costs and the status of the ERIKA operating system. This provided the starting point for the cooperation of USAAR with SSSA on cache-aware scheduling.

2.7 Integration Driven by Industrial Applications (Transversal Integration WP)

Meeting: Workshop: CyberPhysical Systems Forum, CPS Week

San Francisco, April 15, 2009

Objectives for the meeting:

The Cyber-Physical System Forum is the second edition of the event following the successful first edition held in St Louis, MO, in 2008 also co-sponsored by COMBEST. The Forum was held during the CPS week in San Francisco and was organized with the NSF and COMBEST sponsorship joint with the ArtistDesign NoE. The forum was structured into three panels addressing different aspects and challenges related to the design of cyber-physical systems. The objective was to **define with more clarity the research agenda** and how **to set up a sustained, multi-year research program with strong collaboration between the European and the US Community**. In particular, for each of the panel, there was one presenter from the European community either from Combest or from ArtistDesign.

Organizers: Bruce Krogh (CMU), Raj Rajikumar (CMU), Alberto Sangiovanni-Vincentelli (Berkeley, Trento).

Other participants: There were about 500 participants and 12 speakers, the European speakers (Alberto Sangiovanni Vincentelli, Christoph Kirsch, Karl Erik Arzen and Albert Benveniste) were all ArtistDesign Partners. In the participant list all or almost all ArtistDesign partners were represented.

Conclusions After the presentations, during the reception following the meeting, there was a a general consensus among the participants about the relevance of the field, research needs and the necessity to form joint teams among industry and academia **in Europe and US** for CyberPhysical Systems that are now a priority of NSF and of the Obama computing program. In particular, issues related to education and use of the results of the technology in novel application spaces were identified as crucial for the future of the field in general. Since then, NSF started a major research program:
http://www.nsf.gov/publications/pub_summ.jsp?ods_key=nsf08611
"*Congruent with the recommendations in the August 2007 report of the President's Council Scienceand Technology (PCAST), Leadership Under Challenge: Information Technolo Competitive World,NSF's Directorates for Computer and Information Science and Engineeri Engineering (ENG) arespear-heading the Cyber-Physical Systems (CPS) program because and technological importance as well as its potential impact on grand challenges in a nun critical to U.S. security and competitiveness, including aerospace, automotive, chemical p infrastructure, energy, healthcare,manufacturing, materials and transportation. By abstra particulars of specific applications in thesedomains, the CPS program aims to revea fundamental scientific and engineering principles that underpin the integration of cyber and ph across all application sectors*."

ArtistDesign partners continue being involved in the initiative with the intent of bridging the two research communities on the fundamental themes outlined in the ArtistDesign research agenda. We expect that in the third edition of the CPS week to be held in Stockholm April 12-16, 2010 (http://www.cpsweek2010.se/web/page.aspx?pageid=57517) the involvement of ArtistDesign partners will be even more visible and we expect to present some of ArtistDesign achievements in that forum.

http://varma.ece.cmu.edu/CPS-Forum/index.html

Meeting: Workshop: Smart and Efficient Energy Council SEEC-09,

Trento, October 8-9, 2009.

Objectives for the meeting: The goal of the workshop was to discuss energy efficiency as a major contributor to the green economy. Data shows that alternative sources alone are insufficient to meet the increasing energy demand. Higher efficiency is therefore required to address the energy problem and to reduce the carbon footprint resulting in better environmental conditions. Many new initiatives for energy efficiency are afoot worldwide. The Workshop was intended to provide a forum where various initiatives were presented and discussed, results presented and open problems introduced. Emphasis was on addressing the problem from a system standpoint with deep discussions about the role of embedded systems and embedded control and relationship between Industry, Government and Academia. There was a wide participation from industry (22 out of the 78 participants, and 8 out of 15 presentations were from industry). In particular, there was a continuous interaction among the participants during break time to define follow-up activities in EU projects and continuation of the workshop.

The agenda was based on a two day event where ample time for discussions was allowed.

Organizers: Alberto Sangiovanni Vincentelli (UC Berkeley and Trento), Roberto Passerone (Trento)

Other participants: There were 78 participants of whom 27 were representing ArtistDesign partners (CEA, University of Trento, University of Bologna, TU Braunschweig, Politecnico di Milano, Politecnico di Torino, University of Verona, Scuola di Sant'Anna, TU Dortmund, CEA, University of Twente, and TU Denmark). 22 were industrial participants working in international corporations (UTC, Honeywell, Siemens, Fiat, Telecom Italia, ENEL) or in SMEs (Evidence, Optoelettronica, Yogitech, FARSystems, RDSystems, Gruner, Renience,SOFCPower, Fortiss). The participants and the presentations of the meeting are available on the ArtistDesign Web site. The meeting was very well received by the participants. Prof. Morari, Chair of EE of ETH, pointed out that this was probably the best workshop in years he participated to. This point of view expressed in the closing session of the meeting was echoed by most other participants.

Conclusions:
After the two-day presentation, there was a a general consensus among the participants about the relevance of the field, research needs and the necessity to form joint teams among industry and academia in Europe and across the Ocean to provide critical mass for a game changing approach to energy efficiency.
Energy-efficient smart buildings in particular were considered to be an area where there is an exponentially growing interest for traditional industry such as construction, HVAC, monitoring and energy optimization as well as ICT industry. During the meeting, it was emphasized that the key to efficiency is the use of advanced embedded system techniques including wireless sensor networks and embedded controllers. The European Community has started a fairly large effort in this area as documented by the November call of ICT in Framework 7 and the US has declare the energy efficiency area as a top priority. There was an agreement among participants to make the conclusions of the meeting widely known via a Press Release and a special issue in a Journal to be determined. There was also an intense discussion about a major collaborative US-European program and a project was drafted to be presented to NSF, the Department of Energy, and the EU community. Several participants are collaborating to present a joint proposal to the EU. There was an explicit request by the participants to have a follow-up meeting in one year time frame. Some of the participants had strong interest in how

to drive legislation, regulations and standards to favour energy efficiency. There was a mandate to organize a workshop/meeting with the same sponsorship involving Government, law, economics and engineering experts to discuss this important point. The European Institute of Technology call in the Energy and ICT fields were discussed and it was hoped that the ArtistDesign community would participate to define the technical agenda of the two Institutes once they will be assigned (January 2010).

http://www.artist-embedded.org/artist/SEEC-09.html

Meeting: Workshop: Workshop on Software Synthesis - WSS'09

October 16th, 2009, Grenoble, France (within ES Week)

Objectives for the meeting: An increasing amount of software is not written manually any more. Rather, software is synthesized from abstract models of the required functionality. As a result, the effort of generating software is reduced and software verification typically becomes easier. Software synthesis has been implemented in various disperse communities. The workshop aims at bringing these communities together and at identifying research problems which should be addressed by the scientific community.

Organizers: Peter Marwedel (Tu, Dortmund), Alberto Sangiovanni Vincentelli (Trento and UC Berkeley)

Other Participants: There were about 20 attendants mostly from ArtistDesign partners. The speakers were Ed Lee from UC Berkeley substituting for Alberto Sangiovanni Vincentelli, Karl-Erik Arzen (Lund), Emmanuel Roy (Mathworks), Markus Gros (dSpace), and Paul Caspi (Verimag).

Conclusions: The participants to the final panel discussed the status of the field and its potential directions.

Emmanuel Roy (Mathworks):

- Better bridge gap between algorithmic components and true software
- Mathworks: Better distribution to the processors in the network. e.g. in a car.

Christian Fabe (CEA):

- How to make sure that 1000 people can work on the same project?

Peter Marwedel (TU Dortmund)

- This is consistent with Markus Gros' (dSpace) view that handling of large scale models is a problem.

Tetsuya Tohdo (Denso):

- Look at the future, SOA for automotive? How to guarantee security?

Edward Lee (UCB):

- SOA too much rooted in OO-design, no time, no concurrency
- a single language will not work

Christian Fabe (CEA):

- At least a single intermediate representation should be there.

Paul Caspi (IMAG):

- Faithfulness is important, if you don't have it, you have lost the advantage of model-based design.

Edward Lee (UCB):

- If you have a way of encapsulating components, you achieve this.

Reinhard von Hanxleden (U. Kiel):

- Raise the level at which compiler writers are working.

http://www.artist-embedded.org/artist/Scope.html

Meeting: Workshop: ArtistDesign WP6 Cluster Meeting (*Activity 6.2 Platform and MpSoC Analysis)*
Braunschweig, Germany – June 25/26 2009

Objectives for the meeting: While the main objective of this meeting was a mutual update on the joint research progress of the WP6 cluster participants, speakers from the relevant industrial domains traditionally join.

Organizer: Rolf Ernst (TU Braunschweig)
Other participants: Matthias Gries, Gregor Stellpflug (Intel Labs), Nico Feiertag, Kai Richter (Symtavision), Fabian Wolf (Volkswagen)

Conclusions: The meeting has highlighted key problems in the design and analysis of upcoming embedded systems and suggested solutions in different stages of maturity. Topics included performance analysis, reliability, adaptivity, and early design space exploration. The industrial speakers have contributed talks about timing analysis in automotive applications. The meeting has shown that formal methods as developed in this project are increasingly adopted in the industrial design practice.

https://webmail.ida.ing.tu-bs.de/twiki/bin/view/Main/ArtistDesignClusterMeeting

Workshop: 2nd Annual ICES Conference Stockholm,

Sweden, Sept. 2nd, 2009

The conference celebrated the first year anniversary of the KTH based centre for Innovative Embedded Systems – ICES. The overallgoal of the conference was for ICES representatives from industry and KTH to present the drivers for ICES and accomplishments during the first year, as well as ICES vision, goals and concrete activities, including an inventory of Embedded Systems at KTH.

75 people from academia, industry, funding agencies and the press took part in this conference at the Norra Latin Conference Centre in Stockholm. The purpose of this all day conference was to present trends and challenges in embedded systems design, verification, architecting and integration from industrial and scientific viewpoints. The theme was addressed by a program including:

- A keynote talk by Prof. Werner Damm (Offis)
- Invited presentations from industry and KTH
- Presentations of ICES visions, goals, activities and accomplishments,
- addressing these challenges
- An exhibition, presenting ICES-related research projects, education
- and industrial products
- A panel debate discussing how to meet the challenges.

The Keynote Talk described trends and challenges from the viewpoint of the transportation sectors: Automotive, Aerospace and Railway. The three transportation domains share the need to develop advanced embedded systems to meet societal demands for increased mobility and accident reduction while reducing environmental load (CO2 emission and energy consumption) and maintaining high safety levels in spite of increasing traffic density and increased systems complexity. The domains are facing a highly competitive market and faces constraints imposed by (forthcoming) safety standards such as ISO CD 26262, Do178 B/C, CenelecEN 50128/50129, IEC 61508. Achieving continuous cost reduction, performance improvement and efficiently dealing with verification/certification will continue to be a challenge and a key focus in the domains. Werner Damm illustrated research efforts in the area by describing the SPEEDS and CESAR European projects, and their work to develop powerful and efficient supporting methods and tools for the development of safety critical embedded systems.

Invited industrial talks were given by:

- Micronic - addressing challenges in introducing model-based engineering into industrial development,
- Prevas - discussing challenges in embedded systems processes and testing with examples taken from the telecom and automotive domains, and
- Stoneridge in developing future human machine interfaces.

The KTH talks included overviews of trends and challenges in electronic computing platforms (multicore, terascale computing), wireless communication and automous robots.

http://www.kth.se/itm/centra/ices/ices-events/previous-events/1.44090?l=en_UK

Meeting : **Workshop: ICES Seminar: Platform Based Development in Practice**

Stockholm, Sweden, March 31, 2009

The ICES seminar “Platform Based Development in Practice” took place at ABB Corporate Research’s facilities in Västerås on Tuesday 31st March. The goal was to present Platform Based Development (PBD) from different angles and share experiences over domains.

About 50 people attended the seminar, around 10 of whom were from companies/institutions which are not (yet) ICES members. The seminar started with a Welcome from ICES Board member Jan-Erik Frey (ABB) and an introduction by ICES Director Martin Törngren (KTH) who discussed among other things the terminology around Platforms, in order to create a common understanding of the different concepts.

Speakers from ABB, ÅF, Enea and Microsoft presented their viewpoints on PBD, and gave the audience a good insight into both domain-specific issues as well as more general aspects such as organizational issues and impact on development time and cost.

After lunch and a demonstration of a new concept for wireless vibration monitoring on oil-platforms, Johannes Helander, a chief architect from Microsoft gave an inspiring presentation and shared his view of future development methods of embedded platforms.

In conclusion, PBD still remains a challenge in many respects. Design of embedded sytems platforms requires considerations over a large range of system variants including both software and hardware. Moreover, PBD poses a great challenge for testing, where the variability of products increase the state space.

http://www.kth.se/itm/centra/ices/ices-events/previous-events/1.36723?l=en_UK

Meeting: Workshop: ICES Seminar on Testing and verification

Stockholm, Sweden, Feb. 12, 2009

The ICES seminar on testing and verification was hosted by Scania in Södertälje. The seminar had about 55 participants representing a good blend of industrial domains (automotive, telecom, automation) and academic researchers.

The invited talks presented testing from several viewpoints, including safety standards; organizational integration and culture; process integration; and continuous improvement, as well as testing techniques. One of the conclusions from the seminar was that there are needs for improved education and intensified research in the area of testing. For industry, logging their performance and learning, was emphasized as a key point.

http://www.kth.se/itm/centra/ices/ices-events/previous-events/1.33317?l=en_UK

Meeting: Workshop: ICES-VINNOVA European Research Seminar, 28th January 2009

Stockholm, Sweden, January 28th, 2009

In collaboration with Vinnova (the Swedish governmental Research and Innovation Agency), KTH arranged a seminar on Themes, forms and funding relating to European research. The seminar arouse from the need to better disseminate opportunities for research on the European level, and to discuss similarities and differences among ITEA2, Artemis and FP7.

Around 45 people attended the ICES-VINNOVA open seminar "European Research in Embedded Systems: Themes, Forms and Funding", which took place at KTH on 28th January 2009.

The seminar was very successful, with interesting presentations, questions and discussions. The details of the ITEA2 (invited presentation by Rudolf Haggenmueller), FP7 (invited presentation by Philippe Reynert) and ARTEMIS (invited presentation by Alun Foster) programs were explained, including rationale and the directions for the current calls. Vinnova also presented the Swedish funding and support available.

In addition, industrial experiences and viewpoints were presented. A lot of the discussion focused on the relations between the programs and when to choose which. Among the conclusions, an overview of the current large project portfolios was called for.

http://www.kth.se/itm/centra/ices/ices-events/previous-events/1.32246?l=en_UK

Meeting : SMECY Project Proposal Face-to-Face Meeting

Paris, France - 2009-06-25

Objectives for the meeting: The goal of this meeting was to discuss the SMECY project proposal for "Smart Multicore Embedded Systems", which addresses the ARTEMIS Joint Undertaking Call 2009. The project envisions new programming technologies that enable the exploitation of many-core architectures in embedded systems.

Organizer: Francois Pacull (CEA), Ahmed Jerraya (CEA)
Other participants: Jonas Diemer (TU Braunschweig), Francois Pacull (CEA), Ahmed Jerraya (CEA), Joseph Sifakis (IMAG), Gilbert Edelin (Thales), and others (from over 20 institutions in total).

Conclusions : As a result, the 44 participants from industry and academia submitted the SMECY project proposal to the ARTEMIS JU. The project ranked high and was invited to funding negotiations, which are ongoing.

ArtistDesign Workshop on Embedded Systems in Healthcare 2009

Eindhoven, the Netherlands -- December, 7, 2009.
Objectives for the meeting: The goal of the Workshop on Embedded Systems in Healthcare is to strengthen the connections between academic research and industry, or to be more precise, to increase the understanding in the academic world of industrial issues in embedded systems engineering and together come to a shared agreement on research directions that seem worthwhile to pursue.
Organizers: Boudewijn Haverkort (ESI), Pierre America (Philips Research & ESI), Piërre van de Laar (ESI), Miranda Willems (ESI), Roland Mathijssen (ESI).

The speakers at the workshop work at different medical companies or are participants in the ArtistDesign network with extensive experience in healthcare. The topics include "How to design long lasting devices for a fast changing world?", "Cochlear Implant Systems: today's challenges in embedded firmware design", and "Embedded Contributions to an Intensive Care Safety Concept".
http://www.artist-embedded.org/artist/Overview,1831.html

SafeTRANS Industrial Days

Stuttgart, Germany, May 5, 2009 and Friedrichshafen, Germany, November 19, 2009

Within the context of SafeTRANS (including ArtistDesign members) two Industrial Days were organized in 2009. These workshops provide a platform for discussion and exchange of experiences in industry across application domains.

The first one on "Safety Management along the suppliers chain" was held in May 2009 in Stuttgart at Robert Bosch GmbH. Presentations from different application domains (avionics, automotive, rail) were given covering requirement management, development process in the context of ISO 26262, safety management in the development of safety critical rail systems as well as aspects of systems integration.

The second workshop took place on November 19 in Friedrichshafen at EADS on "Model-based testing and test automation". Presentations from industrial participants (Ford, Daimler, EADS, Siemens Validas) and academic participants cover verification of safety critical automotive applications, deployment of model-based technologies to industrial testing, model-based testing for critical functions on architecture level – vision, concepts and way forwards in aeronautical engineering, Domain specific modeling and generation of test cases, model-based testing, risk oriented testing.
http://www.safetrans-de.org/de_6_Industrial_Day.php
http://www.safetrans-de.org/de_7_Industrial_Day.php

3. Staff Mobility and Exchanges

From the Description of Work:
Staff Mobility and Exchanges between teams are essential for integration within and beyond the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams.

Mobility should be justified by and refer to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

-- Changes wrt Y1 deliverable --

All new text: this entire chapter pertains only to activity in Year 2.

3.1 Modelling and Validation Cluster

Oded Maler visited ETH Zurich and Aalborg University where he collaborated with Kim Larsen on probabilistic semantics for timed automata.

The collaboration between VERIMAG and EPFL lead to the recruitment of Barabara Jobstmann as a permanent researcher at VERIMAG.

Sandeep Shukla, (associate professor at Virginia Tech))
Team visited: INRIA Rennes. The visit of Sandeep Shukla for his sabbatical was jointly funded by the University of Rennes, INRIA Rennes-Bretagne-Atlantique, the Scientific Board of INRIA and the Artist-Design Network of Excellence. The main objective of the sabbatical was to jointly investigate the state of the art to modeling multi-clocked synchronous embedded systems, as in Polychrony, for instance, and to explore alternatives modeling, analysis and compilation techniques.

Uli Fahrenberg (CISS, Aalborg University) visited LSV, Cachan for 2 weeks during Year 2 as an invited research fellow.

Vaclav Kaczmarczyk PhD student at the Brno University of Technology in Czech Republic visiting CISS, Aalborg University twice for 1 week to collaborate on a timed automata concrete time simulator.

Extensive collaboration between INRIA and CISS Aalborg on development of prorbabilistic and timed specification formalisms involving a large number of exchange visits, including:

- Kim G Larsen visiting INRIA during a COMBEST meeting in spring 2009.
- Benoit Delay, PhD student at INRIA, visiting CISS, Aalborg University for 2 month
- Axel Legay, research fellow at INRIA, visiting CISS Aalborg multiple times Mikkel Pedersen Larsen, PhD student at CISS visiting INRIA for 3 weeks. Axel Legay will visit CISS again as a research fellow in 2010.
- Visits to CISS by Benoit Caillaud, INRIA.

Aachen has been visited by a number of researchers from Aalborg interacting on games and controller synthesis as well as on probabilistic extensions of priced timed automata.

Alexandre David and Kim G Larsen visiting Uppsala to coordinate plans for future development of UPPAAL.

Exchange visits between IST and CFV, IST and Salzburg, IST and Saarlandes University as well as IST and ETHZ.

Exchange visits between Uppsala and ETHZ collaborating on combinations of real-time calculus and timed automata.

Exchange visits between INRIA and LSV Cachan collaborating on analysis of timed systems.

Exchange visits between INRIA and ULB Brussels collaborating on controller synthesis.

Professor Alberto Sangiovanni Vencentelli has been award Doctor Honoris Causa at Aalborg University acknowledging his numerous research contributions to computer science and engineering. The award ceremony will take place on February 29, 2010.

Several visits of researcers from ETHZ and EPFL at Verimag.

Radu Iosif and Barbara Jobstmann from Verimag have been invited to give regular courses on Artist related topics at EPFL

3.2 Software Synthesis, Code Generation and Timing Analysis cluster

Visiting student: Artur Wiebe (RWTH Aachen)
Team visited: Compaan, led by Dr. Bart Kienhuis (Compaan)
Amsterdam, Netherlands – August 17, 2009 to August 21, 2009
Approximate cost for travel and lodging: 500 €
Reason for the visit: Learn Compaan tools
Conclusions/objectives reached: This visit was in the context of a joint Master thesis between RWTH Aachen and Compaan. Artur Wiebe spent one week in the Compaan office in Amsterdam to learn how to use the Compaan tools and extend the tools to generate code for a target backend.

Visiting researcher: Dr. Sander Stuijk (TU Eindhoven)
Team visited: Design Automation of Embedded Systems, led by P. Marwedel (TU Dortmund)
Dortmund, Germany - March 9th to May 28th, 2009.
Approximate cost for lodging: about 1400 €
Reason for the visit: TU Dortmund and TU Eindhoven are cooperating to develop a novel solution for mapping applications cost-efficiently to the memory hierarchy of any MPSoC platform. Both groups have in the past developed their own approach. The objective of the visit is to align both approaches in order to develop a mapping flow that combines best practices of both approaches.
Conclusions/objectives reached: A common mapping flow has been defined during the visit. Both groups have continued to work on this flow after the visit ended.

Visiting student: Aurore Junier (ENS Rennes)
Team visited: Design Automation of Embedded Systems, led by P. Marwedel (TU Dortmund)

Dortmund, Germany – June 1-July 6, 2009.
Approximate cost for travel and lodging: about 700 €
Reason for the visit: This visit aimed at extending an existing ILP-based register allocator of the WCC compiler such that it uses precise WCET timing models. Using this WCET timing data, the compiler tries to avoid spill code generation along the critical path defining a program's WCET.
Conclusions: an experimental modified WCET-oriented register allocator has been developed. Preliminary results on a small set of benchmarks indicate an average improvement of the WCET of 5%.

Visiting Researcher: Prof. Abhik Roychoudhury (NUS)
Team visited: Design Automation of Embedded Systems, led by P. Marwedel (TU Dortmund)
Dortmund, Germany - August 25, 2009
Reason for visit: To foster collaboration between TU Dortmund and NUS
Conclusions: The NUS and Dortmund groups can collaborate on several topics in multi-core timing analysis. The Dortmund group has developed a robust infra-structure for WCET-directed compilation. The NUS group has recently studied timing analysis of multi-cores with shared cache, as well as scratchpad allocation for concurrent software. We discussed plans for collaborating on shared scratchpad allocation mechanisms for multi-cores with the aim of WCET reduction.

Visiting researcher: Christos Baloukas (Institute of Communication and Computer Systems (ICCS, associated to the National Technical University of Athens))
Team visited: Design Automation of Embedded Systems, led by P. Marwedel (TU Dortmund)
Dortmund, Germany –Sept. 8th – Oct. 5th.
Approximate cost for lodging: about 300 €
Reason for visit: The reason for the visit was to get acquainted with the MACC framework used at Dortmund for the integration of memory-architecture aware pre-pass optimization tools, both at TU Dortmund and its spin-off ICD, including work in the MNEMEE-project.
Conclusions/objectives reached: The ICCS-tools were successfully integrated into the MACC framework.

Visiting researcher: Dr. Iain Bate (York)
Team visited: Mälardalen, led by Björn Lisper
Västerås, Sweden, March 9-10, 2009
Approximate cost for travel and lodging: 700 €
Reason for the visit: to foster the collaboration between York and Mälardalen within the timing analysis activity.
Conclusions: both groups are now doing related work applying machine learning and model identification techniques to timing analysis. There is a clear potential for collaboration. The most promising topic seems to be parametric WCET analysis, where the machine-learning based methods for parametric loop bounds analysis provide an interesting alternative to the static analysis methods developed by Mälardalen.

Visiting researcher: Dr. Mike Bartlett (York)
Team visited: Mälardalen, led by Björn Lisper
Västerås, Sweden, March 9-10, 2009
Approximate cost for travel and lodging: 700 €
Reason for the visit: see above
Conclusions: see above

3.3 Operating Systems and Networks Cluster

- Doct. Pedro Samuel Nunes da Silva, from University of Aveiro (Portugal) to University of Pavia, working on the powerline communication for automotive applications. Pavia, March 3, 2009 - June 9, 2009.

- Doct. Pedro Samuel Nunes da Silva, from University of Aveiro (Portugal) to University of Pavia, working on the powerline communication for automotive applications. Pavia, July 14, 2009 - July 18, 2009.

- Tom A. Henzinger, from EPFL (Switzerland) visited University of York (UK) in April 2009 to give a seminar on model checking and interface-based design.

- Rainer Leupers, from RWTH Aachen (Germany) visited University of York (UK) on October 26, 2009 to give a seminar on timing analysis techniques.

- Tarek Abdelzhaer, from UIUC (USA), visited University of Catania (affiliated to Pisa) from 22 March 2009 to 27 March 2009, to collaborate on wireless sensor networks and distributed embedded systems. During his visit, he also gave a talk on “Research Challenges in Composable Distributed Cyber-Physical Systems”.

- Lucia Lo Bello, from University of Catania (affiliated to Pisa), visited Univ. of Catalonia in Barcelona, on 4-5 December 2008, for a collaboration on distributed control systems using wireless sensor networks.

- Lucia Lo Bello, from University of Catania (affiliated to Pisa), visited the Scuola Superiore Sant’Anna of Pisa on April 1, 2009, for a collaboration on distributed monitoring systems using wireless sensor networks.

- Luca Santinelli, from the Scuola Superiore Sant’Anna of Pisa, visited ETH in Zurich (Switzerland) from November 2008 to August 2009, for a collaboration on component based design of embedded systems.

- Yifan Wu, from the Scuola Superiore Sant’Anna of Pisa, visited Univ. of Lund (Sweden) from March 2009 to July 2009, for a collaboration on integrated design and analysis of real-time control systems.

3.4 Hardware Platforms and MPSoC Cluster

Visiting researcher : Dr. Zhonghai Lu (KTH)
Team visited: Fudan University, Shanghai, China, led by Prof. X. Zeng (Fudan University) Shanghai, China, - June 15-July 8, 2009
Approximate cost for travel and lodging: 4600 €
Reason for the visit:
KTH has a long standing collaboration with Fudan in both research and education. For instance, KTH is giving a 2 years Master program on SoC Design at Fudan.
Recently, KTH and Fudan are initiating a collaboration on Network on Chip architectures. This work is overlapping to a large extent with the KTH activities in the WP6 of ArtistDesign.

Conclusions/objectives reached: The visit of Dr. Lu at Fudan has increased the mutual understanding of the respective activities in MPSoC and NoC research. It has been decided to jointly aply for grant from the Chinese government for developing NoC based architectures for security applications.

Visiting researcher : Prof. Paul Pop (DTU)
Team visited: Linköping, led by Petru Eles (Linköping University)
Several short visits during 2009
Reason for the visit: Common research on predictable fault tolerant systems.
Conclusions/objectives reached: Elaborated several approaches. Written two common publications for 2009.

Visiting researcher : Aske W. Brekling (DTU)
Team visited: CISS/AAU, led by Kim G. Larsen (AAU)
Ålborg, Denmark – September 14 – 25, 2009
Reason for the visit: Planing joint research on model-based verification
Conclusions/objectives reached: Meetings with relevant researchers. Attended presentations on different AAU research projects. Presented current research on Hardware specification language (Gezel). Presented current research on verification framework (MoVES)

Visiting researcher : Mikkel Jakobsen (DTU)
Team visited: KTH, led by Prof. Axel Jantsch (KTH)
Kista, Stockholm, Sweeden – June 8 to 12, 2009
Reason for the visit: Planing joint research on the ForSyDe modelling framework
Conclusions/objectives reached: Definition of an extension of the ForSyDe models-of-conputation for discrete time and synchronous models. Initial definition of SystemC templates.the different ForSyDe MoCs.

Visiting student : Anders Tranberg-Hansen (DTU)
Team visited: , EESC led by Prof. Alberto Sangiovanni-Vincentelli (UC Berkeley)
Berkeley, California, USA – September 1, 2009 to December 4, 2009
Reason for the visit: Study of system modelling methodologies.
Conclusions/objectives reached: The modelling framework for system level performance estimation of embedded systems including Multi-Processor System on Chip (MPSoC) based configurations developed at DTU, has been refined and a language used to specify models and automatically synthesize fast simulation models based on the specification has been developed.

Visiting researcher : Prof. Krishnendu Chakrabarty (Duke University)
Team visited: ESE, led by Jan Madsen (DTU)
Lyngby, Denmark – October 27, 2009
Reason for the visit: Planing joint research collaboration.
Conclusions/objectives reached: Definition of research directions for two PhD students at DTU working on microfluidic biochips.

Visiting researcher: Dr. Zhonghai Lu (KTH)
Team visited: ETH Zurich (Lothar Thiele), Zurich from July 2008 – January 2009.
Approximate cost for travel and lodging: 10000 €
Reasons for the visit: KTH has a long standing experience in the design of NoC and their analysis. Recently, Dr. Lu has been applying network calculus for the analysis of those systems. On the other hand, ETH Zurich has been developing an extended version of network calculus that can be used to investigate real-time properties of computation and communication systems. The visit should lead to new results concerning (a) the relation between the various approaches and (b) new concepts for predictable and efficient

communication fabrics.
Conclusions/objectives reached: The visit of Dr. Lu at ETHZ is still ongoing.

Visiting researcher: Michele Magno (UNIBO)
Team visited: ETH Zurich (Lothar Thiele), Zurich from Nov. 2009 – February 2010.
Approximate cost for travel and lodging: 4500 €
Reasons for the visit: UNIBO and ETHZ have been very successfully cooperating in the area of energy harvesting. The visit of Michele Magno continued this cooperation. In particular, we have been investigating possibilities to design a distributed application control algorithm that takes advantage of different amounts of harvested energy in different computation/communication nodes.
Conclusions/objectives reached: An new algorithm based on integer linear programming has been developed and a joint paper has been accepted in 2009.

3.5 Design for Adaptivity in Embedded Systems (Transversal Integration WP)

Visiting researcher : Michele Magno (UoB)
Team visited: TIK, ETHZ, led by Lothar Thiele (ETHZ)
Zurich, Switzerland – *2008 to January, 2009*
Approximate cost for travel and lodging: 3000 €
Reason for the visit: Michele Magno has concluded his visit in ETHZ, where he worked adaptive algorithms and power management of smart cameras and embedded systems equipped with energy harvesting capabilities.
Conclusions/objectives reached: Michele developed power management algorithms its outcome turned into a joint publication.

Visiting researcher : Yifan Wu (SSSA)
Team visited: ULUND led by Karl-Erik Årzén
March 09 – July 09
Approximate cost for travel and lodging: 4500€
Reason for the visit: Joint work on scheduling of dataflow programs on multicore platform
Conclusions/objectives reached: Yifan developed a scheduling tool for dataflow-based control algorithms within the ACTORS project.

Visiting researcher : Raphael Guerra (TUKL)
Team visited: UNC led by John Anderson
Oct 09 to Dec 09
Reason for the visit: PhD student visit focused on Adaptive Scheduling on Multicore Systems

Visiting researcher : Lei Feng (KTH)

Team visited: Volvo led by Martin Sanfridson

Moved from KTH to Volvo and then became 50%/50% employed as an Industrial Post-doc where some of the work involved follow-up research related to the DySCAS project.

3.6 Design for Predictability (Transversal Integration WP)

Visiting researcher : Aurore Junier (IRISA, France / ENS Cachan, France)
Team visited: WCC Compiler Team, led by Heiko Falk (TU Dortmund)
Dortmund, Germany – June 1st,, 2009 to July 6th , 2009
Approximate cost for travel and lodging: 702.50 €
Reason for the visit: This visit aims at extending an existing ILP-based register allocator of the WCC compiler such that it uses precise WCET timing models. Using this WCET timing data, the compiler tries to avoid spill code generation along the critical path defining a program's WCET.
Conclusions/objectives reached: Objectives unfortunately not reached due to health problems of Ms. Junier and her premature departure from Dortmund.

Visiting researcher : Prof. Paul Pop (DTU)
Team visited: Linköping, led by Petru Eles (Linköping University)
Several short visits during 2009
Reason for the visit: Common research on predictable fault tolerant systems.
Conclusions/objectives reached: Elaborated several approaches. Written two common publications for 2009.

3.7 Integration Driven by Industrial Applications (Transversal Integration WP)

Visiting researcher : PhD, Lei Feng(Volvo)
Team visited: KTH led by Martin Törngren (KTH)
Approximate cost for travel and lodging: 2000 €
Reason for the visit: Since the spring 2009, Lei Feng, formerly a post-doc at KTH, started to work at Volvo. To maintain the cooperation, Lei spent two weeks at KTH during the spring.
Conclusions/objectives reached: To further strengthen the collaboration, it was decided that Lei would be employed 50% time at Volvo and 50% time at KTH, acting as a shared post-doc. During the autumn 2009, this has proven promising as a way to provide a bridge between KTH and Volvo.

4. Tools and Platforms

From the description of work :
A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

4.1 Modelling and Validation Cluster

Here we list some of the stable, downloadable tools and platforms of the cluster. The cluster partners are working on several other tools and platforms. For more and detailed information we refer to the reports of the activities *Modeling* and *Validation*.

- **AMT**
  - AMT (Analog Monitoring Tool) is a tool for checking the correctness of analogue and mixed-signal simulation traces with respect to a formal specification expressed as an assertion. The specification language supported by the tool is STL/PSL, an extension of the temporal logic inspired by the PSL language, which allows expressing properties of real-valued continuous-time behaviors.
  - http://www-verimag.imag.fr/~nickovic/index.php?id=nickovic&page=amt

- **IF TOOLBOX**
  - IF is a language for the structured representation of concurrent real-time systems and a set of tools allowing the analysis and verification of requirements on such systems. The tool evolved from the CADP toolset. Its development was motivated by the need for a structured representation of systems, allowing the application of simplifications for avoiding state explosion before its translation into a global (symbolic) transition relation. In particular, IF has frontends allowing the verification and analysis of models of real-time systems represented in SDL and UML.
  - http://www-if.imag.fr./

- **MARTE**

- MARTE consists in defining foundations for model-based description of real time and embedded systems. These core concepts are then refined for both modeling and analyzing concerns. Modeling parts provides support required from specification to detailed design of real-time and embedded characteristics of systems. MARTE concerns also model-based analysis. In this sense, the intent is not to define new techniques for analyzing real-time and embedded systems, but to support them. Hence, it provides facilities to annotate models with information required to perform specific analysis. Especially, MARTE focuses on performance and schedulability analysis. But, it defines also a general framework for quantitative analysis which intends to refine/specialize any other kind of analysis.

http://www.omgmarte.org/

- **METROPOLIS**

The aim of this tool environment is

- Establishing formal design methodologies is imperative to effectively
- Managing complex design tasks required in modern-date system designs. It involves defining levels of abstraction to formally represent systems being designed, as well as formulating problems to be addressed at and across the abstraction levels. This calls for a design environment in which systems can be unambiguously represented throughout the abstraction levels, the design problems can be mathematically formulated, and tools can be incorporated to solve some of the problems automatically. Developing such an environment is precisely the goal of Metropolis.

  Metropolis consists of an infrastructure, a tool set, and design methodologies for various application domains. The infrastructure provides a mechanism such that heterogeneous components of a system can be represented uniformly and tools for formal methods can be applied naturally.

- http://embedded.eecs.berkeley.edu/metropolis/index.html

- **PHAVER**
  - PHAVer is a tool for verifying safety properties of hybrid systems. It stands out from other tools with the following features:
    - exact and robust arithmetic with unlimited precision,
    - on-the-fly over-approximation of piecewise affine dynamics
    - improved algorithms and termination heuristics
    - support for compositional and assume-guarantee reasoning.
  - http://www-verimag.imag.fr/~frehse/phaver_web/index.html

- **UPPAAL**
  - Uppaal is an integrated tool environment for modeling, validation and verification of real-time systems modeled as networks of timed automata, extended with data types (bounded integers, arrays, etc.).

    The tool is developed in collaboration between the Department of Information Technology at Uppsala University, Sweden and the Department of Computer Science at Aalborg University in Denmark.

  - www.uppaal.com

- **UPPAAL TIGA**
  - UPPAAL TIGA (Fig. 1) is an extension of UPPAAL [BDL04] and it implements the first efficient on-the-fly algorithm for solving games based on timed game automata with respect to reachability and safety properties. Though timed games for long have been known to be decidable there has until now been a lack of efficient and truly on-the-fly algorithms for their analysis.
  - http://www.cs.aau.dk/~adavid/tiga/

- UPPAAL TRON
  - Uppaal TRON is a testing tool, based on Uppaal engine, suited for black-box conformance testing of timed systems, mainly targeted for embedded software commonly found in various controllers. By online we mean that tests are derived, executed and checked simultaneously while maintaining the connection to the system in real-time.
  - http://www.cs.aau.dk/~marius/tron/

- **SARTS**
  - SARTS is a model based schedulability analysis tool used for hard real-time systems. SARTS is used to translate hard real-time systems, implemented in Java, to a finite state machine in the modeling tool Uppaal.

    The system being analyzed must be implemented in SCJ2, a safety critical profile for Java developed in this project, based on SCJ. The target hardware is the time predictable Java processor JOP, developed specifically for hard real-time systems.

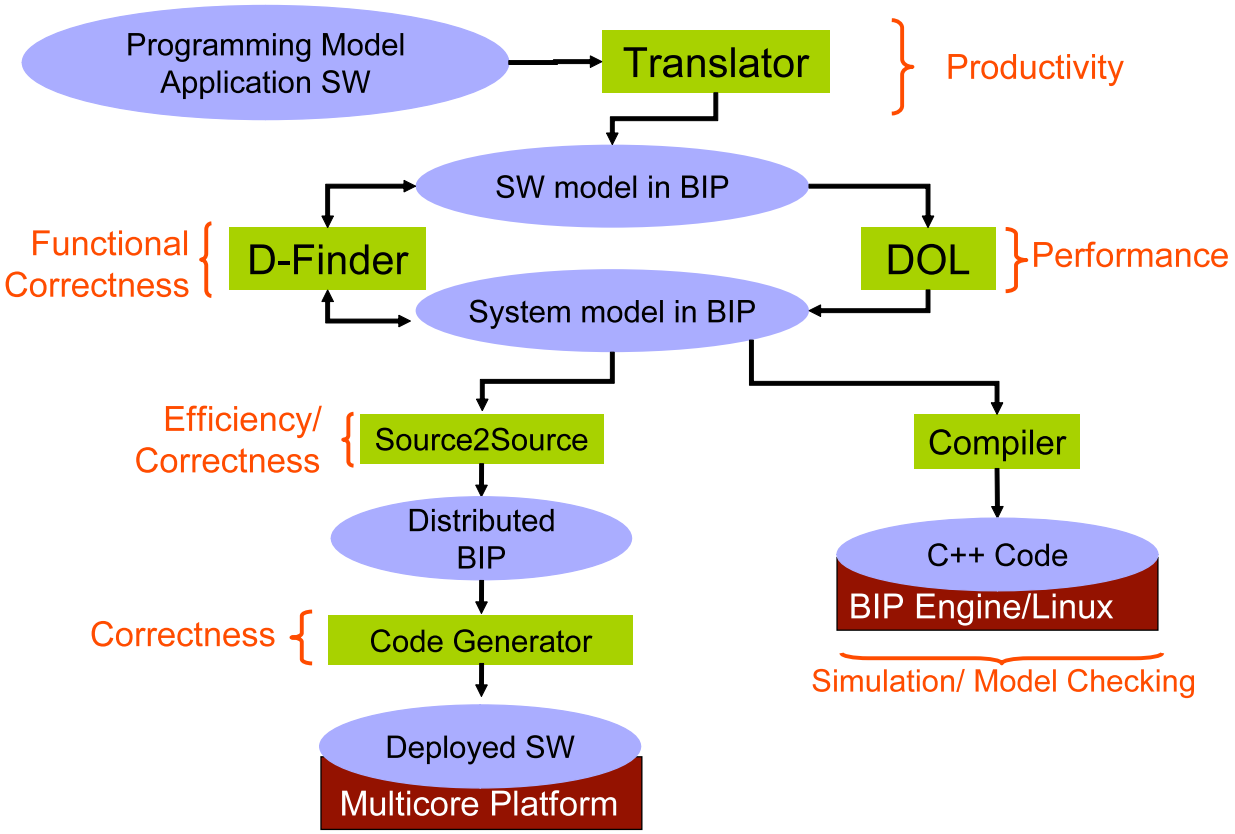
    Several experiments have been conducted to illustrate the accuracy of SARTS compared to existing tools. It is shown how the model based approach can result in a more accurate analysis, than possible with traditional analyses.
  - http://sarts.boegholm.dk/

- **STG**
  - STG (Symbolic Test Generator) generates conformance tests, based on this framework:
- Implementation: black-box, only input/output behavior is observable.
- Specification: IOSTS(input/output behavior + internal structure)
- Test Purpose: IOSTS, tells which part of the specification is to be tested
- Test Case: IOSTS generated by STG from a specification and a test purpose
    - Test Cases are symbolic, and possibly parameterized by constants
    - They take into account possible non-determinism of the Spec;
    - They include a verdict (no manual interpretation needed)
  - http://www.irisa.fr/prive/ployette/stg-doc/stg-web.html

- **TIMES**
  - TIMES is a **T**ool for **M**odeling and **I**mplementation of **E**mbedded **S**ystems. It is a tool set for modelling, schedulability analysis, synthesis of (optimal) schedules and executable code. It is appropriate for systems that can be described as a set of tasks which are triggered periodically or sporadically by time or external events.

- http://www.timestool.com/

- **BIP Design and Validation platform**
  - **objectives**: The vision is to use BIP as a unifying semantic model used along a complete and rigorous (model-based) system design flow. We have already implemented a significant part of this vision such as encompassing heterogeneous programming paradigms and scalable constructive verification techniques. The focus for the long term is to complete ongoing work on correct-by-construction transformations allowing to get from an application software model its implementation on some target platform, in particular multicore platforms.
  - **Main results**: The BIP toolset supports a design flow for the development of heterogeneous real-time systems and their correct implementation. It starts from application software written in domain-specific languages, e.g. synchronous, data flow, event driven languages. Different translators generate a unique BIP model of the application This BIP model can be analyzed by checking deadlock-freedom with **D-Finder**.
  - The transformation of the BIP model into an application is achieved by progressively enriching the model with information about the resources of the target platform. The process of modification of the model in order to take into account physical resource is still under study. It is driven by architectural constraints provided by the **DOL** tool (ETHZ) used for performance analysis. DOL provides a partitioning of the BIP model as well as a mapping of high level primitives into their implementation. To the BIP model, are then applied source-to-source transformations to obtain a functionally equivalent distributed BIP model. The latter differs from the initial model in that multiparty interaction, strong synchronization in particular, is expressed by using protocols based on asynchronous message passing. The distributed BIP model is obtained by application of a set of syntactic transformations that are shown to be correct. http://www-verimag.imag.fr/~async/bip.php



-- Changes wrt Y1 deliverable --

All new text: this pertains only to activity in Year 2.

4.2 Software Synthesis, Code Generation and Timing Analysis cluster

4.2.1 Tool or Platform: WCC

Objectives

WCC is the leading tool for exploring the integration of worst-case execution time-aware analysis into compilers.

Main Results

In a previous project, aiT was integrated with an experimental worst-case execution time aware compiler called WCC. During the last year, this integrated tool set was continued to be used for exploring the optimization potential for compiler optimizations using WCETs as the objective function. Work on multi-objective optimization was started.

Current work

The current work explores the optimization potential of WCC further.

Participating partners:

- TU Dortmund
  TU Dortmund designs WCC and explores the optimization potential.
- AbsInt, Saarbrücken
  AbsInt provides aiT.

Web
http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/

Related Publications

Paul Lokuciejewski, Fatih Gedikli, Peter Marwedel, and Katharina Morik: Automatic WCET Reduction by Machine Learning Based Heuristics for Function Inlining, In: *Proceedings of the 3rd Workshop on Statistical and Machine Learning Approaches to Architectures and Compilation*, pages 1-15, Paphos / Cyprus, January 2009.

Paul Lokuciejewski, Daniel Cordes, Heiko Falk, and Peter Marwedel: A Fast and Precise Static Loop Analysis based on Abstract Interpretation, Program Slicing and Polytope Models, In: *International Symposium on Code Generation and Optimization (CGO)*, pages 136-146, Seattle / USA, March 2009.

Paul Lokuciejewski, Fatih Gedikli, and Peter Marwedel: Accelerating WCET-driven Optimizations by the Invariant Path - a Case Study of Loop Unswitching, In: *The 12th International Workshop on Software & Compilers for Embedded Systems (SCOPES)*, pages 11-20, Nice / France, April 2009.

Sascha Plazar, Paul Lokuciejewski, and Peter Marwedel: WCET-aware Software Based Cache Partitioning for Multi-Task Real-Time Systems, In: *The 9th International Workshop on Worst-Case Execution Time Analysis (WCET)*, pages 78-88, Dublin / Ireland, June 2009.

Paul Lokuciejewski and Peter Marwedel: Combining Worst-Case Timing Models, Loop Unrolling, and Static Loop Analysis for WCET Minimization, In: *The 21st Euromicro Conference on Real-Time Systems (ECRTS)*, pages 35-44, Dublin / Ireland, July 2009.

Heiko Falk: WCET-aware Register Allocation based on Graph Colouring, In: *The 46th Design Automation Conference (DAC)*, pages 726-731, San Francisco / USA, July 2009.

Heiko Falk and Jan C. Kleinsorge: Optimal Static WCET-aware Scratchpad Allocation of Program Code, In: *The 46th Design Automation Conference (DAC)*, pages 732-737, San Francisco / USA, July 2009.

Paul Lokuciejewski, Timon Kelter, Peter Marwedel: Superblock-Based Source Code Optimizations for WCET Minimization, submitted to RTAS 2010

Paul Lokuciejewski, Marco Stolpe, Katharina Morik, Peter Marwedel: Automatic Selection of Machine Learning Models for Compiler Heuristic Generation, submitted to CGO 2010

-- Changes wrt Y1 deliverable --

The potential of using WCET as a cost function has been explored further.

4.2.2 MAPS

Objectives

MAPS (MPSoC Application Programming Studio) is proposed and developed in ISS, RWTH Aachen to tackle the challenge of programming future heterogeneous MPSoC platforms. It targets efficient code generation for multiple applications at a time and predefined heterogeneous MPSoC platforms.

Main Results

This year, a high-level virtual platform for early MPSoC SW development (the MVP (MAPS Virtual Platform) has been proposed and developed in the context of the MAPS project. It allows the SW developers to quickly experiment with different mappings of task-to-PE (Processing Element) as well as different scheduling policies using an easy-to-configure virtual prototype, in order to examine the functional correctness and non-functional properties such as deadline misses. ACE's CoSy framework was used in the MVP for C code instrumentation and high-level code optimization.

Current work

MAPS is currently under development in many aspects to enhance its capabilities, such as multi-application RT scenario, high-level simulation environment, dedicated task dispatching/scheduling, code-generation for HW back-ends, etc. MAPS is part of RWTH Aachen's Ultra high speed Mobile Information and Communication (UMIC) research cluster. RWTH Aachen has been actively discussing MAPS with ArtistDesign partners at the Rheinfels workshop.

Participating partners:

- RWTH Aachen
  RWTH Aachen is designing and developing the MAPS tools.
- ACE
  ACE provides the CoSy compiler framework for use in the MAPS tools.

Web
http://www.iss.rwth-aachen.de/Projekte/Tools/MPSoC%20Application%20Programming%20Studio.html

Related Publications

Jianjiang Ceng, Jeronimo Castrillon, Weihua Sheng, Hanno Scharwächter, Rainer Leupers, Gerd Ascheid, Heinrich Meyr (RWTH Aachen Univ.), Tsuyoshi Isshiki, Hiroaki Kunieda (Tokyo Institute of Tech.), "MAPS: An Integrated Framework for MPSoC Application Parallelization", in 45th Design Automation Conference, Anaheim, CA, USA, June 2008

Ceng, J., Sheng, W., Castrillon, J., Stulova, A., Leupers, R., Ascheid, G., and H. Meyr: A High-Level Virtual Platform for Early MPSoC Software Development, In: International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS 2009), Grenoble, France, 2009.

Anastasia Stulova, Jianjiang Ceng, Weihua Sheng, Jeronimo Castrillon and Rainer Leupers: A Co-simulation Framework for MPSoC Run-Time Behavior Analysis in Early System Design, MCC 2009

R. Leupers, S. Ha, A. Vajda, R. Doemer, M. Bekooij and A. Nohl: Programming MPSoC Platforms: Road Works Ahead, DATE 2009

-- Changes wrt Y1 deliverable –

The MAPS toolset has been extended in cooperation with other partners.

4.2.3 CoSy

Objectives

CoSy is a mature commercial development compiler platform.

Main Results

RWTH integrated additional optimizations into CoSy. TU Berlin used CoSy for its research on compiler verification. IMEC used CoSy as a platform for generating compilers. RWTH Aachen used CoSy for its MAPS tools.

Current work

Work on additional optimizations continues at RWTH Aachen and so does the work at TU Berlin and IMEC. There is the trend toward using MPSoCs as the target platform.

Participating partners:

- RWTH Aachen
- TU Berlin
- IMEC vzw

Web
http://www.ace.nl/compiler/cosy.html

Related Publications

See 4.3.2.

-- Changes wrt Y1 deliverable --

CoSy is now also used as the platform for MAPS.

4.2.4 ICD-C

Objectives

ICD-C is a development platform with special support for source-to-source transformations. Source-to-source transformations can be implemented without loosing any information about the original C program. It can also be used in cases where full control over the libraries is required.

Main Results

ICD-C was used for the integration of compilers with timing analysis and the impact of optimizing the WCET was studied in a number of cases. Also, it was used for memory-architecture aware pre-pass compilation tools. For their mode analysis on C code, Saarland University uses the ICD-C compiler infrastructure developed at ICD / TU Dortmund. This semi-automatic mode derivation from C code tries to superimpose a mode structure on code which may be generated from automata, from other control models or may be handwritten.

Current work

Current work is extending the support for caches and aims at reducing the number of calls of the WCET estimator in order to speed-up optimization. Machine-learning techniques are being tried as a promising approach. Mnemee partners are using ICD-C. For their mode analysis on C code, Saarland University uses the ICD-C compiler infrastructure developed at Dortmund.

Participating partners:

- TU Dortmund
- Saarland University (via the PREDATOR project)
- U. Passau
- ICD Dortmund (via the Mnemee project)
- TU Eindhoven (via the Mnemee project)
- IMEC (via the Mnemee project)
- ICCS (via the Mnemee project)

Web

http://www.icd.de/es/index.html

-- Changes wrt Y1 deliverable --

Additional partners are using ICD-C for source-to-source transformations.

4.2.5 MP-MH MPSoC parallelization assistant and memory hierarchy assignment for MPSoC

Objectives

The main objectives of the framework is to offer an automatic source code parallelization (MPA tool) and memory hierarchy management (MH tool) in order to map efficiently embedded software application on MPSoC platforms. This tool suite is also used in the Platform and MPSoC Design cluster.

Main Results

After the prototype versions of the MPSoC Parallelization Assistant (MPA) and Memory Hierarchy (MH) management tools were developed and tested, we proceeded in their integration as a single MP-MH tool, thus solving interdependency and exploration optimization issues.

Current work

Currently, the affiliated partners of IMEC (i.e., NTUA/ICCS) and core partners (TU Dortmund/ICD) are integrating their tool and design flows with the IMEC MP-MH framework in the memory assignment context of the MNEMEE FP7 project.

Participating partners:

- NTUA/ICCS
  This partner is integrating the dynamic data type and dynamic memory management tools and design flows with the IMEC MPSoC mapping tool flows.
- TU Dortmund/ICD
  This partner is integrating its pre-compiler and compiler framework to the static MH tool of IMEC.

Web

http://www.mnemee.org/
http://www.imec.be/cleanc

Related Publications

Baert, R.; Brockmeyer, E.; Wuytack, S. and Ashby, T.: Exploring parallelizations of applications for MPSoC platforms using MPA. In Design, Automation and Test in Europe, DATE 2009, Nice, France, April 20-24, 2009. IEEE 2009

Mignolet, J.; Baert, R.; Ashby, T.; Avasare, P.; Jang, H. and Son, J.: MPA: Parallelizing an application onto a multi-core platform made easy. In IEEE Micro journal p.31-39, Vol.29, Issue 3, (2009)

-- Changes wrt Y1 deliverable --

This is the first listing of the tool.

4.2.6 aiT

Objectives

aiT is the leading tool for computing worst case execution times (WCETs).

Main Results

A prototype implementation of the UCB computation as developed by Saarland University has been integrated by AbsInt into the aiT Timing Analyzer. The analysis is implemented for the ARM7 and has been tested on smaller benchmark programs.

Current work

Current work is concerned with optimising the performance of the analysis and exploring its potential on larger examples. Implementations for other processors are also underway.

Participating partners:

- AbsInt, Saarbrücken
  AbsInt provides aiT and support for aiT.
- TU Dortmund
  TU Dortmund uses aiT.

Web
http://www.absint.com

-- Changes wrt Y1 deliverable --

This is the first listing of the tool. For Y1, it was just mentioned as a component of WCC.

4.2.7 Bound-T

Objectives

Bound-T is a tool for computing worst case execution time bounds (WCETs) by static analysis of machine code.

Current work and main results

Work on Bound-T in this period focused on extending the model of the computations in the program under analysis to include the finite size (number of bits) of storage elements and the bit-precise semantics of integer arithmetic and other operations on binary words. This will increase the safety of the analysis and also allow a better translation between Bound-T's models and the ARTIST2/Artist-Design common interchange languages, in particular the ALF language from Mälardalen. Unfortunately, these model extensions proved to exceed the abilities of the main analysis tool that Bound-T has used so far (Presburger Arithmetic as implemented in the Omega Calculator program) which means that other methods of analysis must be chosen and implemented. Thus the extensions are not yet completed.

Participating partners:

- Tidorum, Helsinki
  Tidorum provides Bound-T and support for Bound-T.
- Mälardalen
  Mälardalen University is defining the ALF language for modelling computations and

control flow. Discussions on ALF between Tidorum and Mälardalen have been very useful.

Web
http://www..bound-t.com

-- Changes wrt Y1 deliverable --

This is the first listing of the tool.

4.2.8 SWEET

Objectives

SWEET (SWEdish Execution time analysis Tool) is a prototype WCET analysis tool developed at MDH. In particular, SWEET serves as an environment for the development and evaluation of advanced methods for automatic program flow analysis. This makes the program flow analysis component of SWEET an interesting candidate to use as plug-in with other WCET analysis tools, since it can reduce the need for manual annotations.

Main Results

SWEET has been equipped with different interfaces for its program flow analysis, including the ALF code format for representing code on different levels, a novel "Flow Fact" format for expressing precise program flow constraints, and an alternative backend producing program flow constraints in the AIS annotation format for aiT.

Current work

SWEET is now being integrated with other tools. It is currently being equipped with a C front-end through the SATIrE tool from TU Vienna. This allows SWEET to perform program flow analysis on source code level. The AIS interface to aiT is being refined to allow the export of more sophisticated program flow constraints.

Partners

- Mälardalen University
- AbsInt
- TU Vienna

Related Publications

Jan Gustafsson, Andreas Ermedahl, Björn Lisper, Christer Sandberg, and Linus Källberg: ALF – A Language for WCET Flow Analysis. Proc. 9th International Workshop on Worst-Case Execution Time Analysis (WCET'09), Dublin, Ireland, June 2009

-- Changes wrt Y1 deliverable --

This is the first listing of the tool.

4.3 Operating Systems and Networks Cluster

4.3.1 Platform: Educational kit for Real-Time Embedded Systems

Objectives

The goal of this initiative is to develop of an educational kit for embedded systems, based on Microchip dsPIC technology, consisting of a number of modules that can easily be composed depending on specific application purposes. The modules consist of:

1. The main processing platform (the FLEX mother board) with the dsPIC 16-bit microcontroller. It is designed to be composable with other boards (daughter boards) designed for specific applications and connected in a piggy-back fashion.
2. A set of dauther boards for specific applications, with specific sensors and actuators. Available special boards include a multi-bus connection board, an intertial system for flight control, a 4 axis motor controller, and a sound localization board.
3. A set of libraries to simplify the access to the hardware devices (sensors, servomotors, wireless modules),
4. A number of sample real-time control applications that can be easily replicated by the users.

All applications are developed in C language and run on the Erika operating system, which is an OSEK compliant real-time kernel for small embedded microcontrollers.

Main Results

In this second year, the system was used to develop additional real-time control applications under severe resource constraints. The following control applications have been developed using Erika Enterprise as a real-time kernel and Flex as a hardware platform.

Ball and plate balancing. An additional two-degrees-of-freedom ball-and-plate balancing device has been built at the Universtiy of Pavia (affiliated to the Scuola Superiore Sant'Anna) using infrared sensors as sensing devices. The trajectory of the ball on the plate was controlled by two servomotors.

Low-cost Cartesian Robot for Neurorehabilitation. A low-cost 2-DOF Cartesian Robot for Neurorehabilitation was developed by the ARTS Lab of the Scuola Superiore Sant'Anna, Evidence Srl, Humanware Srl, and SO.GE.Il s.r.l.

Segway. A small segway was controlled using Erika and the FLEX board at the Retis Lab of the Scuola Superiore Sant'Anna of Pisa. A special purpose board containing a 3-axis accelerometer, 3 gyroscopes, and the servomotor drivers was developed and connected to the FLEX.

Educational experiments. An embedded control systems was developed with the Erika+Flex platform at the Automatic Control Department of the Technical University of Catalonia (Spain), with the purpose of setting a laboratory experiment for educational purposes. A real-time control of dynamical system was designed to drive students to a better understanding and integration of the diverse theoretical concepts that often come from different disciplines such as real-time and control systems.

Current work

The current work includes the development of:

- new dauther boards for specific sensors and real-time control applications;
- operating system support for energy management;
- real-time communication protocols for wireless sensor networks;
- new code generation modules for the Scilab/Scicos environment;

Participating partners:

RETIS Lab - Scuola Superiore Sant'Anna, Pisa – Giorgio Buttazzo (http://retis.sssup.it/)
Role: Design of real-time algorithms, applications and sensor interfaces.

Evidence s.r.l. – Paolo Gai (http://www.evidence.eu.com/)
Role: Support for the Erika operating system.

Embedded Solutions – Daniele Sartorello (http://www.es-online.it/)
Role: Hardware design, board production, and testing.

Microchip Technology – Antonio Bersani (http://www.mchip.it/)
Role: Hardware components, support for the compiler and device libraries, dissemination.

University of Catalonia – Pau Marti (http://paginespersonals.upcnet.es/~pmc16/)
Role: Development of control applications.

University of Pavia – Tullio Facchinetti (http://robot.unipv.it/toolleeo/)
Role: Development of robotic applications.

Web

ERIKA: http://www.evidence.eu.com/content/view/27/254/

FLEX: http://www.evidence.eu.com/content/view/114/204/

Applications: http://www.evidence.eu.com/content/blogsection/6/266/

http://www.youtube.com/group/flexboards

Related Publications

1. Pau Marti, Manel Velasco, Josep M. Fuertes, and Giorgio Buttazzo, "Design of an embedded control systems laboratory experiment", IEEE Transactions on Industrial Electronics, to appear.
2. Enrico Bini, Giorgio Buttazzo, and Giuseppe Lipari, "Minimizing CPU energy in real-time systems with discrete speed management", ACM Transactions on Embedded Computing Systems, Vol. 8, Issue 4, July 2009.

4.3.2 Platform: RTNS simulation package

Simulation plays a key role, together with analytical models, for validating a system against the QoS it must guarantee. Pisa is continuing to work on RTNS a publicly available free tool to simulate Operating System (OS) aspects in wireless distributed applications. The tool extends the well-known NS-2 simulator with models of the CPU, RealTime OS and application tasks, to take into account delays introduced by computation and I/O from peripherals. This package can be used to efficiently co-design the kernel and network profiles before deployment, especially when the number of nodes is such that analytical analysis is inapplicable.

URL: http://rtns.sssup.it

-- Changes wrt Y1 deliverable --

New applications were developed on the FLEX platform and new software has been written to support wireless real-time communication, power-aware scheduling and control systems.

4.4 Hardware Platforms and MPSoC Cluster

4.4.1 Tool: SymTA/S

Objectives

SymTA/S is a tool for the development and verification of embedded multiprocessor real-time systems. The existing technology is mainly suitable for event or time-driven systems with message passing as the main task interaction. The tool shall be extended to cover the timing implications of multicore processors, or multiprocessor-systems-on-chip.

Main Results

In several previous projects (funded by german DFG, “Sureal”, funded by german BMBF, ARTIST2, and others), the compositional analysis approach has been transferred into a tool framework which is now also commercially available. The available modelling options capture typical problems in todays automotive systems (CAN bus utilization, end-to-end deadlines,…). This addresses a growing need for formal methods in the industry. The topics currently under research (see below) address future problems which can be expected to become of increasing industrial interest in the future.

Current work

The research version of the tool framework is currently being developed into several new directions: Modeling of shared resources for multiprocessor-system-on-chips (see ArtistDesign Activity 6.2: Platform and MpSoC Analysis), the modelling of hierarchical event models (in the scope of the COMBEST project), and the demonstrator platform for adaptive systems (see ArtistDesign 7.1: Design for Adaptivity). Besides the extension of the applicability into new domains, a major focus within ArtistDesign is the synergetic coupling of tools, as well as the correspoinding development of models.

Participating partners:

- TU Braunschweig.

  TU Braunschweig investigates synergies in the coupling of methods and implements prototypical implementations of the research results.

- Symtavision GmbH.

  Symtavision is the commercial co-developer of the tool framework. A focus within ArtistDesign is the coupling of with other industrially available tools (such as aiT).

- ETHZ.

  Collaboration on the coupling of MPA and SymTA/S with respect to modelling of hierarchical event models.

- Absint GmbH.

  The aiT tool supplies task timing models, which are required for system level analysis.

Web
http://www.symtavision.com/
http://www.ida.ing.tu-bs.de/index.php?id=symtas
http://www.ida.ing.tu-bs.de/en/research/projects/accord/

Related Publications

Simon Schliecker and Arne Hamann and Razvan Racu and Rolf Ernst. "Formal Methods for System Level Performance Analysis and Optimization." In *Proc. of the Design Verification Conference (DVCon)*, San José, CA, February 2008.

Jonas Rox and Rolf Ernst. "Modeling Event Stream Hierarchies with Hierarchical Event Models." In *Proc. Design, Automation and Test in Europe (DATE 2008)*, March 2008.

-- Changes wrt Y1 deliverable --

No changes.

4.4.2 Tool: Analysis and optimisation framework for fault tolerant distributed embedded systems

Objectives

Linköping University and DTU are working on an environment and tool-set for the analysis and design optimisation of safety critical, fault tolerant real-time embedded applications. The emphasis is on the issue of transient faults and the goal is to develop tools for scheduling, mapping, and system optimisation.

Main results

A strategy for the synthesis of fault tolerant schedules has been developed. It can handle both hard and soft real-time tasks. The goal is to guarantee the deadlines for the hard processes even in the case of faults, while maximizing the overall utility. Time/utility functions are used to capture the utility of soft processes. Process re-execution is employed to recover from multiple faults. A single static schedule computed off-line is not fault tolerant and is pessimistic in terms of utility, while a purely online approach, which computes a new schedule every time a process fails or completes, incurs an unacceptable overhead. Thus, a quasi-static scheduling strategy is used, where a set of schedules is synthesized off-line and, at run time, the scheduler will select the right schedule based on the occurrence of faults and the actual execution times of processes. An optimisation technique for the generation of schedule tables supporting such a quasi-static scheduling approach has been developed and implemented.

Current work

Ongoing work is towards development of cost-optimisation techniques by considering processors with various hardening levels and the associated tradeoffs.

During the second **year DTU** and **Linköping** have continued their cooperation related to the design and optimisation of fault tolerant mixed hard/soft real-time systems. During the second

year the emphasis of the work has been on the analysis and optimisation of fault-tolerant hard real-time embedded systems, based on an approach in which hardware and software fault tolerance techniques are combined. The basic trade-off is between processor hardening in hardware and process re-execution in software which, together, have to provide the required levels of fault tolerance against transient faults with the lowest-possible system costs.

The goal for the third year is the development of new optimisation approaches for implementation of error detection techniques.

Participating partners

Linköping: Scheduling techniques, fault tolerant systems, design optimisation.

DTU: System level optimisation techniques

Publications

1. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Synthesis of Flexible Fault-Tolerant Schedules with Preemption for Mixed Soft and Hard Real-Time Systems”, 11th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN (DSD 2008), Parma, Italy, September 3-5, 2008, pp. 71-80.
2. Petru Eles, Viacheslav Izosimov, Paul Pop, Zebo Peng, “Synthesis of Fault-Tolerant Embedded Systems”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1117-1122.
3. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, 915-920.
4. P. Pop, V. Izosimov, P. Eles, and Z. Peng. Design Optimization of Time- and Cost-Constrained Fault-Tolerant Embedded Systems with Checkpointing and Replication. IEEE Transactions on Very Large Scale Integrated (VLSI) Systems, 17(3):389-402. 2009.
5. V. Izosimov, I. Polian, P. Pop, P. Eles, and Z. Peng. Analysis and Optimization of Fault-Tolerant Embedded Systems with Hardened Processors. Proceedings of DATE: Design Automation and Test in Europe, IEEE, 2009, pp. 682 – 687.

-- Changes wrt Y1 deliverable --

Updated description of current work and added two publications.

4.4.3 Tool: IMEC MPA + MH MPSoC mapping framework

Objectives

The main objectives of the framework is to offer an automatic source code parallelization (MPA tool) and memory hierarchy management (MH tool) in order to map efficiently embedded software application on MPSoC platforms.

Main Results

Prototype versions of the MPSoC Parallelization Assistant (MPA) and Memory Hierarchy (MH) management tools were developed and tested on video codec embedded sosftware applications (i.e., MPEG-4, AVC etc.).

Current work

Currently, the affiliated partners of IMEC (ie, DUTH/ICCS and TU/e) and core partners (TUDortmund/ICD and KTH) are trying to integrate their tool and design flows with the IMEC MPA + MH MPSoC mapping framework in the memory and interconnect specific context of the MNEMEE and MOSART FP7 projects, respectively.

Participating partners:

- DUTH/ICCS
  This partner is integrating the dynamic data type and dynamic memory management tools and design flows with the IMEC MPSoC mapping tool flows.
- TUDortmund/ICD
  This partner is integrating its pre-compiler and compiler framework to the static MH tool of IMEC.
- TU/e
  This partner is integrating its SDF3 framework in the context of system scenarios with the IMEC MPSoC mapping tool flows.
- KTH
  This partner is integrating its NoC simulation and exploration framework with the MPA tool of IMEC.

Web
http://www.mnemee.org/
http://www.mosart-project.org/

Related Publications

IMEC vzw. & TU/e

- 'A System Scenario based Approach to Dynamic Embedded Systems', S.V. Gheorghita, M. Palkovic, J. Hamers, A. Vandecappelle, S. Mamagkakis, T. Basten, L. Eeckhout, H. Corporaal, F. Catthoor, F. Vandeputte, K. De Bosschere, ACM Transactions on Design Automation of Electronic Systems, ToDAES. To appear in 2009.

IMEC vzw. & TU/e & DUTH & TU Dortmund (at ICD)

- 'MNEMEE: Memory management technology for adaptive and efficient design of embedded systems' S.Mamagkakis, P.Lemmens, D.Soudris, T.Basten, P.Marwedel, D.Kritharidis, G.Guilmin, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

IMEC vzw. & KTH & DUTH

'MOSART: Mapping Optimisation for Scalable multi-core ARchiTecture', B. Candaele, A. Jantsch, T. Ashby, K. Tiensyrjä, F. Ieromnimon, B. Vanthournout, P. Di Crescenzo, D. Soudris, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

-- Changes wrt Y1 deliverable --

No changes.

4.4.4 Tool: MoVES - Modelling and Verification of Embedded Systems

Objectives

The MoVES framework is being developed to assist in the early phases of embedded systems design. The framework can be used to conduct schedulability analysis and has the potential to reason about different types of resource usage such as memory usage and power consumption.

Main Results

In several projects (MoDES, DaNES, ARTIST2, ArtistDesign) a model-based approach to analysis of embedded systems has been analyzed. This has resultet in the MoVES framework, which is now available online. The framework consists of a model- and a trace generator. From a system specification MoVES builds a model suitable for verification using an external verification back-end. In the case of e.g. verified non-schedulability, the trace generator provides the user with an understandable trace that leads to a missed deadline of the system.

Current work

The current version of the framework is based on a simple specification language where a system is modelled as an application running on an execution platform. The application is modelled through the individual tasks, and the execution platform is modelled through the processing elements, including the operating systems, and their interconnections. The tasks and processing elements are characterized by their real-time properties. Currently, verification can be conducted using two different verification back-ends, a) the original Uppaal model-checker for timed-automata models and b) a developmental Uppaal model-checker for stop-watch automata.

Participating partners:

- DTU: Provides the MoVES development environment.
- AAU: Provides the UPPAAL verification engine

Web

http://www.imm.dtu.dk/moves

Related Publications

1. Aske Brekling, Michael R. Hansen, Jan Madsen, MoVES - A Framework for Modelling and Verifying Embedded Systems, The 21st International Conference on Microelectronics, Marrakech, Morocco, 2009
2. Jan Madsen, Michael R. Hansen, Aske W. Brekling, A Modelling and Analysis Framework for Embedded Systems, Model-Based Design of Heterogeneous Embedded Systems, CRC Press, 2009
3. Aske Brekling, Michael R. Hansen, Jan Madsen, Analysis of Quantitative Properties of Hardware Specifications, The 21st Nordic Workshop on Programming Theory, Technical University of Denmark, 2009

-- Changes wrt Y1 deliverable --

This is new text.

4.4.5 Tool: MPA (Modular Performance Analysis)

Objectives

The tool MPA (modular performance analysis) is based on an extension of network calculus that is termed real-time calculus (RTC). The purpose of the tool is to perform an end-to-end real-time analysis of complex distributed embedded systems. The implementation is based on a Java mathematical library for max-+ algebra with an associated Matlab interface.

Main Results

Within ARTISTDesign, the MPA tool box has been (a) extended towards the new results together with University Braunschweig (TUBS) related to hierarchical event streams and (b) it has been linked to the Symta/S tool suite as described above. In addition, the toolbox has been used in the context of various application studies from avionic and automotive domain.

Current work

We are currently working towards linking the toolbox to other performance analysis frameworks, e.g. UPPAAL from Uppsala University (Wang Yi, Bengt Jonsson). Some first promising results are available already. In addition, we are intending to use the method to investigate the interaction between memory access and computations in MPSoC platforms. This will be continued together with University Saarland (Reinhard Wilhelm).

Participating partners

ETHZ: Provides and maintains the MPA toolbox

TUBS: Link to the Symta/S tool suite, development of algorithms and methods for hierarchical event stream analysis.

Web

http://www.mpa.ethz.ch/

Related Publications

ETHZ: Kai Lampka, Simon Perathoner, Lothar Thiele: Analytic Real-Time Analysis and Timed Automata: A Hybrid Method for Analyzing Embedded Real-Time Systems. 8th ACM & IEEE International conference on Embedded software, EMSOFT 2009, CD edition, ACM, Grenoble, France, pages 107-116, October, 2009.

ETHZ: Lothar Thiele, Nikolay Stoimenov: Modular Performance Analysis of Cyclic Dataflow Graphs. EMSOFT 09: Proceedings of the 9th ACM international conference on Embedded software, Grenoble, France, pages 127-136, October, 2009.

ETHZ & TUBS: Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, Vol. 13, No. 1, pages 27-49, June, 2009.

ETHZ & TUBS: Simon Perathoner, Tobias Rein, Lothar Thiele, Kai Lampka and Jonas Rox: Modeling Structured Event Streams in System Level Performance Analysis, submitted to

Conference on Languages, Compilers, and Tools for Embedded Systems LCTES, Stockholm, Sweden, April 2010

-- Changes wrt Y1 deliverable --

This is new text.

4.4.6 Tool: DOL (Distributed Operation Layer)

Objectives

The DOL environment is a complete high-level compilation environment for MPSoC platforms. It consists of a graphical input specification interface for (a) application and (b) platform, a link to analytic performance analysis based on MPA, a simulation environment based on MPARM (Univeristy Bologna, Luca Benini) and a multi-objective optimization environment based on PISA (http://www.tik.ethz.ch/~sop/pisa/) for mapping (binding of application components to computation resources and communication links to paths on the platform). The environment has been successfully used to map complex applications to various platforms such as IBM Cell, MPARM (UNIBO) and ATMEL Diopsys.

Main Results

In the framework of ARTISTDesign, the DOL environment has been successfully linked and coupled to the MPARM simulation and design environment from University Bologna. This way, DOL could be used for ARM-based MPSoC architectures and extended with a state-of-the-art simulation environment. Main results are the comparison of analytic performance analysis with simulation-based performance numbers.

Current work

In the future, the coupling between MPARM and DOL will be used in order to investigate new concepts for predictable and efficient communication fabrics, including intelligent DMA controllers, scratchpad memories and flexible TDMA scheduling policies.

Participating Partners

ETH: Provides the DOL software development environment.

UNIBO: Provides the MPARM environment, including simulation capabilities and new concepts for predictable communication fabrics.

Web

http://www.tik.ee.ethz.ch/~shapes/dol.html

Related Publications

W. Haid, K. Huang, I. Bacivarov, and L. Thiele. Multiprocessor SoC Software Design Flows. IEEE Signal Processing Magazine, vol. 26, no. 6, pp. 64—71, Nov. 2009.

W. Haid, L. Schor, K. Huang, I. Bacivarov, and L. Thiele. Efficient Execution of Kahn Process Networks on Multi-Processor Systems Using Protothreads and Windowed FIFOs. In Proc. IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia), pages 35—44, Grenoble, France, Oct. 2009.

W. Haid, M. Keller, K. Huang, I. Bacivarov, and L. Thiele. Generation and Calibration of Compositional Performance Analysis Models for Multi-Processor Systems. In Proc. Int'l Conf.

on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), pages 92—99, Samos, Greece, July 2009. Awarded the Stamatis Vassiliadis Best Paper Award.

K. Huang, I. Bacivarov, J. Liu, and W. Haid. A Modular Fast Simulation Framework for Stream-Oriented MPSoC. In IEEE Symposium on Industrial Embedded Systems (SIES), pages 74—81, Lausanne, Switzerland, July 2009.

-- Changes wrt Y1 deliverable --

This is new text.

4.5 Design for Adaptivity in Embedded Systems (Transversal Integration WP)

4.5.1 SWEET (SWEdish Execution Time tool)

Objectives

SWEET is a WCET analysis tool. It is an academic prototype: the main objective is to use it as a test bench for methods in WCET analysis, and then mainly flow analysis to produce program flow constraints (upper bounds on # of loop iterations, information about infeasible paths, etc.).

Main Results

SWEET has been used to develop and test various methods for constraining program flow. It has also been used in industrial case studies. The results indicate that the developed methods do improve on the number of automatically detected program flow constraints, as well as on the precision of the resulting WCET bound.

Current work

SWEET is currently being reengineered to use new interface formats for code to analyze and resulting program flow constraints. A version of SWEET that performs parametric WCET analysis will also be created: this work is of relevance to the adaptivity activity since parametric WCET bounds can be used by adaptive scheduling methods.

Participating partners:

- Mälardalen University
  Maintains and develops SWEET, develops methods for parametric WCET analysis.
- Saarland University
  Collaboration partner for parametric WCET analysis.

Web
http://www.mrtc.mdh.se/projects/wcet/sweet.html

Related Publications

- [BEL09] Stefan Bygde, Andreas Ermedahl, and Björn Lisper. An Efficient Algorithm for Parametric WCET Calculation. in Patrick Kellenberger, ed. Proc. 16th International Conference on Real-Time Computing Systems and Applications (RTCSA'09), pages 13-21. Beijing, China, Aug 2009. Best paper award.

4.5.2 Multicore Partitioni

A tool has been developed at the Scuola Superiore Sant'Anna of Pisa to partition parallel real-time applications on a multicore platform. The method handles sporadic real-time applications with timing and precedence constraints and allocate them to a set of virtual processors to make the allocation process independent of the physical platform. The tool allows the user to specify two objective functions for minimizing either the overall bandwidth consumption or the maximum degree of parallelism. A graphic interface is also provided to facilitate user interaction, as well as evaluating the outcomes of the search algorithm.

4.5.3 *Hardware setup to demonstrate self-protection and adaptability of embedded Real-Time Systems*

Objectives
A demonstrator for self-protection and adaptability in real-time systems is being developed. It demonstrates the feasibility and cost of run-time adaptation and protection with respect to performance metrics such as end-to-end latencies. Furthermore, the demonstrator acts as a platform to evaluate performance of the proposed methodologies.

Main Results
During the previous year, the concepts of an encompassing framework to the analysis engine enabling performance analysis of the compound system before actually starting an update on the embedded system were developed. The key concept of this framework is that applications are annotated with a contract specifying their timing behaviour and constraints. Once an application is accepted by the framework, it is guaranteed to adhere to its constraints if it adheres to its behavioural descriptio

In this year, the framework has been integrated into a hardware demonstrator setup consisting of two microcontroller boards interconnected by a CAN bus and surrounding hardware. As an application, a ball-and-beam setup with distributed control has been implemented. A second application merely induces load on the CAN bus disturbing the distributed control application.

The demonstrator shows that the second application, if started, renders the control application useless. The implemented framework rejects the start of the second application after analysis assuring adherence to the contract of the control application. This demonstrator has been presented at the University Booth at DATE'09.

The microcontroller boards have been extended by a time sensitive control application, in order to show effects of self-protection and adaptation with respect to performance metrics.

Current work

Currently, work is being done on integration of framework components in the demonstrator. Furthermore, the time-sensitive control application is being implemented.

Participating partners:

- TU Braunschweig
  Symtavision GmbH
- Universität Erlangen

Related Publications

[NSSE10] Moritz Neukirchner, Steffen Stein, Harald Schrom and Rolf Ernst. A software Update Service with Self-Protection Capabilities. In Proceedings of the conference on Design, Automation and Test in Europe (DATE), Dresden, Germany, March 2010 (to appear)

4.5.4 TrueTime

Objectives

To provide a flexible simulation platform for networked embedded real-time systems with a particular focus on control applications. TrueTime implements simulation models for a multi-tasking real-time kernel and data link layer network protocols that execute embedded in the Matlab/Simulink environment. Using TrueTime it is possible to experiment with adaptive resource management and network protocols and investigate how this influence application performance.

Main Results

TrueTime has been continuously developed since 1999. During Y2 four new versions have been released:

- 2009-01-14 – TrueTime 2.0 Beta 1 was released. The most important change was that the simulator was released under the GPL license. Other changes include:
  - Automatic connections between Kernel and Network blocks
  - Improved configuration of the Kernel block via the mask dialogue
  - New syntax for several real-time primitives
  - New implementation of handlers
  - New Ultrasound Network block (for simulation of mobile robot localization)
  - Improved stand-alone network blocks to handle vector signals
  - Full built-in support for CBS scheduling
- 2009-05-11 – TrueTime 2.0 Beta 2 was released. Bug fixes.
- 2009-09-18 – TrueTime 2.0 Beta 3 was released. Bug fixes and more examples included.
- 2009-10-15 – TrueTime 2.0 Beta 4 was released. The following issues were included:

- Bug fixes
- Support for FlexRay networks.
- Support for PROFINET IO fieldbus networks.
- Additional examples were added.

- In addition to this the network part of TrueTime has been ported to the Modelica/Dymola platform within the ITEA 2 project EUROSYSLIB.

Current work
The current not yet released development version also supports partitioned multicore scheduling and hierarchical schedulers. This is currently being used in the ACTORS project.

Participating partners:

- ULUND
  Toolbox development.
- SSSA, TUKL, Aveiro, KTH ...
  Users of the toolbox

Web
http://www.control.lth.se/truetime/

Related Publications

- [CHO09] Anton Cervin, Dan Henriksson, Martin Ohlin, TrueTime 2.0 beta – Reference Manual, Technical report, Department of Automatic Control, Lund University, January 2009
- [CÅ09] Anton Cervin, Karl-Erik Årzén, TrueTime: Simulation tool for performance analysis of real-time embedded systems, In Model-Based Design for Embedded Systems, Eds. G. Nicolescu, P. Mosterman, Routledge Taylor & Francis Group, 2009

-- Changes wrt Y1 deliverable --

The text above only contains the tools / platforms for which something significant has changed with respect to Year 1. Tools such as SHARK or ForSyDe mentioned in the Year 1 deliverable are still of relevance to this activity.

4.6 Design for Predictability (Transversal Integration WP)

4.6.1 Tool or Platform: aiT

Objectives

aiT is the leading tool for computing worst case execution times (WCETs).

Main Results

A prototype implementation of the UCB computation as developed by Saarland University has been integrated by AbsInt into the aiT Timing Analyzer. The analysis is implemented for the ARM7 and has been tested on smaller benchmark programs.

Current work

Current work is concerned with optimising the performance of the analysis and exploring its potential on larger examples. Implementations for other processors are also underway.

Web
http://www.absint.com

4.6.2 Tool or Platform: aiT / WCC

<USaar: Update this section>

Objectives

aiT is the leading tool for computing worst case execution times (WCETs). It has been integrated with a worst-case execution time-aware compiler.

Main Results

In a previous project, aiT was integrated with an experimental worst-case execution time aware compiler called WCC. During the last year, this integrated tool set was used for exploring the optimization potential for compiler optimizations using WCETs as the objective function.

Current work

The current work explores the optimization potential of WCC.

Participating partners:

- AbsInt, Saarbrücken
  AbsInt provides aiT.
- TU Dortmund
  TU Dortmund integrates aiT into WCC and explores the optimization potential.

Web
http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/

Related Publications

[LGMM09] P. Lokuciejewski, F. Gedikli, P. Marwedel and K. Morik. *Automatic WCET Reduction by Machine Learning Based Heuristics for Function Inlining*. Proceedings of SMART '09: 3rd Workshop on Statistical and Machine Learning Approaches to Architectures and Compilation, January 2009, pp. 1-15.

[LCFM09] P. Lokuciejewski, D. Cordes, H. Falk and P. Marwedel. *A Fast and Precise Static Loop Analysis based on Abstract Interpretation, Program Slicing and Polytope Models*. Proceedings of CGO '09: International Symposium on Code Generation and Optimization, March 2009, pp. 136-146.

[LGM09] P. Lokuciejewski, F. Gedikli and P. Marwedel. *Accelerating WCET-driven Optimizations by the Invariant Path – a Case Study of Loop Unswitching*. Proceeding of SCOPES '09: 12th International Workshop on Software & Compilers for Embedded Systems, April 2009, pp. 11-20.

[PLM09] S. Plazar, P. Lokuciejewski and P. Marwedel. *WCET-aware Software Based Cache Partitioning for Multi-Task Real-Time Systems*. Proceedings of WCET '09: 9th International Workshop on Worst-Case Execution Time Analysis, June 2009, pp. 78-88.

[LoMa09] P. Lokuciejewski and P. Marwedel. *Combining Worst-Case Timing Models, Loop Unrolling, and Static Loop Analysis for WCET Minimization*. Proceedings of ECRTS '09: 21st Euromicro Conference on Real-Time Systems, July 2009, pp. 35-44.

[Falk09] H. Falk. *WCET-aware Register Allocation based on Graph Coloring*. Proceedings of DAC '09: 46th Design Automation Conference, July 2009, pp. 726-731.

[FaKl09] H. Falk and J. C. Kleinsorge. *Optimal Static WCET-aware Scratchpad Allocation of Program Code*. Proceedings of DAC '09: 46th Design Automation Conference, July 2009, pp. 732-737.

4.6.3 Tool: MPA (Modular Performance Analysis)

Objectives

The tool MPA (modular performance analysis) is based on an extension of network calculus that is termed real-time calculus (RTC). The purpose of the tool is to perform an end-to-end real-time analysis of complex distributed embedded systems. The implementation is based on a Java mathematical library for max-+ algebra with an associated Matlab interface.

Main Results

Within ARTISTDesign, the MPA tool box has been (a) extended towards the new results together with University Braunschweig (TUBS) related to hierarchical event streams and (b) it has been linked to the Symta/S tool suite as described above. In addition, the toolbox has been used in the context of various application studies from avionic and automotive domain.

Current work

We are currently working towards linking the toolbox to other performance analysis frameworks, e.g. UPPAAL from Uppsala University (Wang Yi, Bengt Jonsson). Some first promising results are available already. In addition, we are intending to use the method to investigate the interaction between memory access and computations in MPSoC platforms. This will be continued together with University Saarland (Reinhard Wilhelm).

Participating partners

ETHZ: Provides and maintains the MPA toolbox

TUBS: Link to the Symta/S tool suite, development of algorithms and methods for hierarchical event stream analysis.

Uppsala: Provides knowledge and links to model checker UPPAAL

Web

http://www.mpa.ethz.ch/

Related Publications

ETHZ: Kai Lampka, Simon Perathoner, Lothar Thiele: Analytic Real-Time Analysis and Timed Automata: A Hybrid Method for Analyzing Embedded Real-Time Systems. 8th ACM & IEEE International conference on Embedded software, EMSOFT 2009, CD edition, ACM, Grenoble, France, pages 107-116, October, 2009.

ETHZ: Lothar Thiele, Nikolay Stoimenov: Modular Performance Analysis of Cyclic Dataflow Graphs. EMSOFT 09: Proceedings of the 9th ACM international conference on Embedded software, Grenoble, France, pages 127-136, October, 2009.

ETHZ & TUBS: Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, Vol. 13, No. 1, pages 27-49, June, 2009.

ETHZ & TUBS: Simon Perathoner, Tobias Rein, Lothar Thiele, Kai Lampka and Jonas Rox: Modeling Structured Event Streams in System Level Performance Analysis, submitted to Conference on Languages, Compilers, and Tools for Embedded Systems LCTES, Stockholm, Sweden, April 2010

4.6.4 Tool or Platform : MPARM

Objectives
MPARM is a virtual SoC platform almost written in SystemC, which could be used to model both HW and SW of a system. The MPARM virtual platform is highly modular and capable of simulating at cycle-accurate level an entire MPSoC, including cores, L1 and L2 caches, L3 memories and system buses.

Current work
We are working on defining and implementing new ways to enhance the predictability of MPSoC systems. We will consider both SW and HW techniques, applied to the CPU, bus and memory sub-systems.

-- Changes wrt Y1 deliverable --

The section has been updated.

4.7 Integration Driven by Industrial Applications (Transversal Integration WP)

4.7.1 Tool or Platform: SymTA/S

Objectives

SymTA/S is a tool for the development and verification of embedded multiprocessor real-time systems. The existing technology is mainly suitable for event or time-driven systems with message passing as the main task interaction. The tool shall be extended to cover the timing implications of multicore processors, or multiprocessor-systems-on-chip.

Main Results

In several previous projects (funded by german DFG, “Sureal”, funded by german BMBF, ARTIST2, and others), the compositional analysis approach has been transferred into a tool framework which is now also commercially available. The available modelling options capture typical problems in todays automotive systems (CAN bus utilization, end-to-end deadlines,…). This addresses a growing need for formal methods in the industry. The topics currently under

research (see below) address future problems which can be expected to become of increasing industrial interest in the future.

Current work

The research version of the tool framework is currently being developed into several new directions: Modeling of shared resources for multiprocessor-system-on-chips (see ArtistDesign Activity 6.2: Platform and MpSoC Analysis), the modelling of hierarchical event models (in the scope of the COMBEST project), the demonstrator platform for adaptive systems (see ArtistDesign 7.1: Design for Adaptivity), and the reliability analysis (as presented in Section 3.1 Technical Achievements of the Industry-driven integrtation activity 7.3). Besides the extension of the applicability into new domains driven by industrial applications, a major focus within ArtistDesign is the synergetic coupling of tools, as well as the corresponding development of models.

Participating partners:

- TU Braunschweig.

  TU Braunschweig investigates synergies in the coupling of methods and implements prototypical implementations of the research results.

- Symtavision GmbH.

  Symtavision is the commercial co-developer of the tool framework. A focus within ArtistDesign is the coupling of with other industrially available tools (such as aiT).

- ETHZ.

  Collaboration on the coupling of MPA and SymTA/S with respect to modelling of hierarchical event models.

- Absint GmbH.

  The aiT tool supplies task timing models, which are required for system level analysis.

Web

http://www.ida.ing.tu-bs.de/forschung/projekte/symtas/

http://www.symtavision.com/

Related Publications

- Simon Schliecker, Jonas Rox, Mircea Negrean, Kai Richter, Marek Jersak and Rolf Ernst, **"System Level Performance Analysis for Real-Time Automotive Multi-Core and Network Architectures,"** *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 28, No. 7, pp. 979-992, July 2009.
- Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst and Michael González Harbour, **"Influence of different abstractions on the performance analysis of distributed hard real-time systems,"** *Journal Design Automation for Embedded Systems*, vol. 13, No. 1, pp. 27-49, June 2009
- Mircea Negrean, Simon Schliecker and Rolf Ernst, **"Response-Time Analysis of Arbitrarily Activated Tasks in Multiprocessor Systems with Shared**

Resources," in *Proc. of Design, Automation, and Test in Europe (DATE)*, (Nice, France), April 2009

-- Changes wrt Y1 deliverable --

No change.

4.7.2 COSI

Objectives

COSI (Communication Synthesis Infrastructure) is a software framework for interconnect infrastructure analysis and synthesis

Main Results

The framework allows developing specialized flows and tools for communication synthesis as exemplified by the release of COSI-NOC (Communication Synthesis Infrastructure for Network-on-Chips), a software toolkit for the automatic synthesis of synchronous networks-on-chip based on the platform-based design paradigm, and by COSI-BAD, for building automation design.

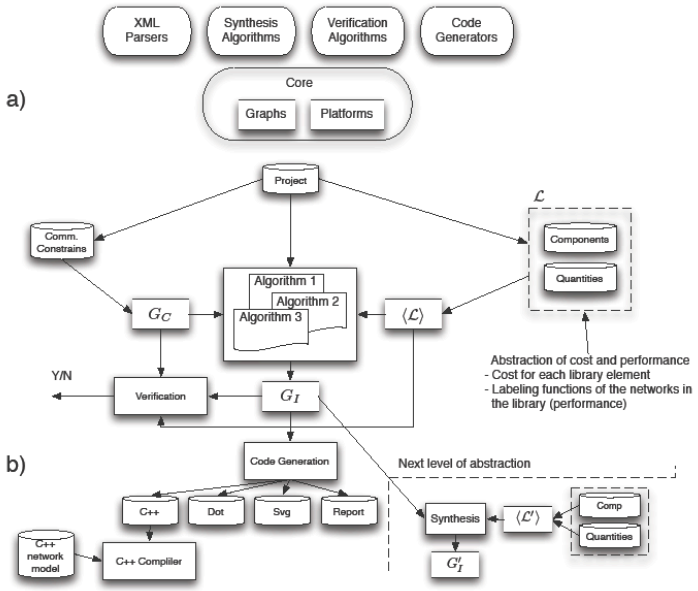


Figure 1. The COSI Platform-Based Design-like structure

	Quantities	CommStructs	Library	Models	Rules	Platforms	Environment	I/O	Algorithms
Core	Ports Bandwidth Flows...	Graphs							ShortestPath Tsp SpanningTree FacilityLocation Kmedian
On-Chip Communication	Interface IpGeometry NodeParam	Specification PItInstance implementation	Router Link Bus	Ho-Area Ho-Power Orion	Critical length Deadlock	RouterLink BusNoc	Rectangle	Parsers SvgGen Parquet interface SyscGen	DegreeConstrained LatencyConstrained Hierarchical
Building Automation	Interface NodeParam Threads	Specification PItInstance implementation	Sensor Actuator Controller TwistedPair	TokenRing 802.15.4	WiringRule NodePosition	DaisyChain TreeWireless	Walls CableLadder	BuildingParser SvgGen Desyre interface	DaisyChainPartition WirelessTree

Figure 2. How the COSI framework has been used to generate specific synthesis tools.

Current work

We continue to work towards expanding COSI capabilities, including better models for router delays, bus models, and support for the generation of synthesizable RTL description of the synthesized on-chip interconnection network. In this domain, we are integrating Metro with COSI. Meanwhile, we also plan to continue our work on the extension of the communication synthesis approach to the design of large-scale network for distributed embedded systems such as those that can be found in smart buildings and to airplane power distribution.

Participating partners:

- **Trento**
  Setting the directions of the framework. Methodology and theory. Integrating COSI with Metro.
- **UC Berkeley**
  Tool development and application to Network on Chip and intelligent buildings
- **Columbia**
  Participation in the development of the methodology.
- **UTC**

  Application to intelligent buildings and avionics.

Web

http://embedded.eecs.berkeley.edu/cosi/

Related Publications

[PCSV08] A. Pinto, L. Carloni and A. Sangiovanni Vincentelli, COSI: A Framework for the Design of Interconnection Networks, IEEE Design and Test of Computers, vol. 25, n. 5, Sept-Oct. 2008, pp. 402-415.

[PCVS09] A. Pinto, L.P. Carloni, and A. Sangiovanni-Vincentelli. "A Methodology for Constraint-Driven Synthesis of On-Chip Communications," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 28, No. 3, March 2009.

-- Changes wrt Y1 deliverable --

No change.

4.7.3 Metropolis and Metro II

Objectives

System-Level Design (SLD) means many different things to many different people. In our view, system-level design is about the design of a whole that consists of several components where specifications are given in terms of functionality with additional:

- constraints on the properties the design has to satisfy and on the components that are available for implementation and
- objective functions that express the desirable features of the design when completed.

This definition is general since it relates to many different application domains, from semiconductors to systems such as cars and airplanes, buildings, telecommunication and biological systems. To deal with system-level problems, our view is that the issue to address is not developing new tools, albeit they are essential to advance the state of the art in design, rather it is the understanding of the principles of system design, the necessary change to design methodologies and the dynamics of the supply chain. Developing this understanding is necessary to define a sound approach to the needs of the system and component industry as they try to serve their customers better, to develop their products faster and with higher quality.

Main Results

This contribution was about principles and how a unified methodology together with a supporting software framework, as challenging as it may seem, can be developed to bring the embedded electronics industry to a new level of efficiency. To demonstrate this view, we developed over the years Metropolis, a software framework supporting the methodology and Metro II, a second generation framework built to alleviate the problems we encountered when applying Metropolis to industrial test cases.

Current work

We are integrating this framework with the COSI framework to provide a full communication requirement capture, synthesis, verification and implementation. In parallel, we are interfacing Ptolemy to Metro II to offer a new way of entering designs using the graphical UI of Ptolemy II.

Participating partners:

- **Trento**

  Tool development, application of the framework to a UMTS case study.

- **UC Berkeley**

  Tool development, interface with Ptolemy II
- **Sun Microsystems**

  Application to multi-core development
- **UTC**

  Interface with COSI and application to smart buildings and avionics.
- **National Instruments**

  Industrial development of the ideas put forth by the frameworks
- **Intel**

  Application to SoC design and development of architectural models

Web

http://chess.eecs.berkeley.edu/chess/forum/17.html

Related Publications

[DSDP09] D. Densmore, A. Simalatsar, A. Davare, R. Passerone, and A. Sangiovanni-Vincentelli. “UMTS MPSoC design evaluation using a system level design framework”. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE09)*, Nice, France, April 20-24, 2009.

[BDDD09] F. Balarin, A. Davare, M. D'Angelo, D. Densmore, T. Meyerowitz, R. Passerone, A. Pinto, A. Sangiovanni-Vincentelli, A. Simalatsar, Y. Watanabe, G. Yang and Q. Zhu. “Platform-Based Design and Frameworks: Metropolis and Metro II”. In *Model-Based Design for Embedded Systems,* chapter 10, page 259. CRC Press, Taylor and Francis Group, Boca Raton, London, New York, November 2009.

-- Changes wrt Y1 deliverable --

This is a new effort in ArtistDesign.

5. Assessment of the Workpackage at the end of Y2

The ArtistDesign Network of Excellence is a significant evolutionary step for integrating the leading embedded systems design research teams in Europe.

The overall assessment for the WP at the end of ArtistDesign Y2 (Jan–Dec 2009) is positive - both in terms of impact on the overall structuring and lasting integration within the consortium and more generally within the area in Europe.

- The ArtistDesign clusters have been actively pursuing operational integration through joint meetings, staff mobility, and shared platforms and tools.
- The level of activity shows that the Cluster / Activity structure and research topics defined for ArtistDesign make sense, and are viable vehicles for integrating the area. In operational terms, they generate sufficient interest for the partners and individual researchers to participate actively in the joint meetings, to exchange personnel, and to orient the tools and platforms developed to make sense within this structure.
- There is clearly a growing level of maturity for tools and platforms – and the partner teams are actively pursuing a policy of implementing tools, demontrators, and in many cases their accompanying methodologies.
- Nonetheless, it is important to remember that these are tools and platforms for research. The aim is not necessarily always for these to lead to commercially viable tools and start-up companies. In general, they are the concrete realisation of the state-of-the-research, allowing to explore possibilities for future research and later tools (some of which may in turn lead to commercially viable products).

In particular, we have had XX joint technical meetings, bringing together a wide audience. These meetings have covered a broad spectrum of topics, including XXXXXX.

The NoE has facilitated the mobility of YYYY researchers, for a total period of HHH in Year 2. This is widely considered to be the best way to integrated research teams, through the phyical transfer of persons and competencies. They lead to lasting collaboration and synergy.

The level of effort started in Year 1 has been maintained. We currently have XXX platforms developed in collaboration with ArtistDesign, covering the technical domains of the NoE.