IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Activity Progress Report for Year 2

Software Synthesis and Code Generation

Clusters:

SW Synthesis, Code Generation and Timing Analysis

Activity Leader:

Prof. Dr. Peter Marwedel (TU Dortmund)
http://ls12-www.cs.tu-dortmund.de/~marwedel

Policy Objective (abstract)

The objective of this activity is to provide software synthesis and code generation tools which are required for modern embedded architectures. Due to the constraints of such architectures, the tools have to generate very efficient code. A particular focus is on the mapping of applications to multi-processor systems on a chip (MPSoCs). The parallelism found in such architectures poses a particular challenge. In addition, other selected tools (linking, for example, timing analysis and compilation) are also considered.

Versions

number	comment	date
1.0	First version delivered to the reviewers	December 18th 2009

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1. Overview of the Activity

1.1 ArtistDesign participants and their role within the Activity

Prof. Dr. Peter Marwedel – TU Dortmund, Dortmund (Germany)
Prof. Marwedel's role is to lead this activity. His team works on resource aware compilation, worst-case execution time (WCET) aware compilation and provides results on compilation for MPSoCs.

Dr. Stylianos Mamagkakis – IMEC, Leuven (Belgium)
The team led by Dr. Mamagkakis will introduce novel source code parallelization and memory source-to-source optimizations for MPSoC platforms.

Prof. Dr. Christian Lengauer – U. Passau, Passau (Germany)
Prof. Lengauer's team has advanced knowledge in program analysis techniques. This knowledge was initially generated in the context of high-performance computing and shall now be used for compilation to MPSoCs.

Prof. Dr. Rainer Leupers – RWTH Aachen, Aachen (Germany)
The team led by Prof. Leupers works on compiler platforms, adaptive compilation, and MPSoC compilation. The group's MAPS project provides a reference for tools mapping algorithms to MPSoCs.

-- Changes wrt Y1 deliverable --

Only stylistic changes with respect to Year 1.

1.2 Affiliated participants and their role within the Activity

Joseph van Vlijmen – ACE, Amsterdam (Netherlands)
ACE (including van team member van Vlijmen) is a key player in the compiler domain in Europe and the world. This partner provides a view on industrial requirements and practices.

Dr. Björn Franke – University of Edinburgh, Edinburgh (UK)
Dr. Franke's team has advanced knowledge in program analysis techniques. This knowledge was initially generated in the context of high-performance computing and shall now be used, for example, for compilation to MPSoCs.

Prof. Dr. Sabine Glesner – TU Berlin, Berlin (Germany)
The team led by Prof. Glesner provides its expertise on program verification and compiler optimization to the network. This expertise will help verifying transformations as well as developing optimizing compiler transformations of single programs and applications.

Prof. Dr. Paul Kelly – Imperial College, London (UK)
Prof. Kelly's team has advanced knowledge in program analysis techniques. This knowledge was initially generated in the context of high-performance computing and shall now be used, for example, for compilation to MPSoCs.

Prof. Dr. Alain Darte – ENS, Lyon (France)
Prof. Darte's team has advanced knowledge in program analysis techniques. This knowledge was initially generated in the context of high-performance computing and shall now be used, for example, for compilation to MPSoCs.

Dr. Marco Bekooji, Ruben van Royen – NXP, Eindhoven (Netherlands)

The team led by Dr. Bekooji has advanced knowledge in software synthesis from non-imperative models of computation. Within its area of expertise, the team has already designed tools mapping applications to multi-processors.

Dr. Bart Kienhuis – Compaan Design B.V., Leiden (Netherlands)

This partner's team has advanced knowledge in software synthesis from non-imperative models of computation. Within its area of expertise, the team has already designed tools mapping applications to multi-processors.

-- Changes wrt Y1 deliverable --

Only stylistic changes with respect to Year 1.

1.3 Starting Date, and Expected Ending Date

This activity started with day 1 of the network. This activity includes the difficult problem of mapping applications to MPSoCs. We cannot expect that this problem will be completely solved at the end of the funding period. Therefore, work on this problem will be required for a number of years, even though the activity will formally be finished at the end of the funding period.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.4 Policy Objective

Software synthesis, code generation, and timing analysis tools provide the necessary link between embedded execution platforms and applications. The recent trend toward multi-processor systems has amplified the need for research in this area.

In order to achieve the required critical mass without increasing the number of partners beyond a manageable number, affiliated partners are added. These affiliated partners complement the work done by the core partners. For the same reason, external partners from outside the project have been integrated into the work of the network. At some time, some external partners might become affiliated partners.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.5 Background

Software synthesis and code generation tools are indispensable tools for developing embedded systems. They are frequently assumed to be available. New architectural features are introduced all the time, assuming that "somebody" will provide the expected tools. However, the design of such tools poses many very difficult challenges. There is always the risk of major losses of investments if the expected tools cannot be designed in the available time.

Existing compilers represent very valuable software components which cannot be easily replaced by new methods. Many companies hesitate to replace their existing proven compilers by less well-debugged research results. Therefore, this cluster is extensively considering software synthesis and pre-pass source-to-source optimization tools, which can be used with several standard compilers. Pre-pass optimizers decouple the process of code generation and that of particular optimizations for certain architectural features.

The following is an enumeration of the background in the various areas of this activity:

1. Parallelism as available in MPSoCs is a particularly challenging new architectural feature. Significant effort on automatic parallelization has been spent in the context of high performance computing. Due to this effort, automatic parallelization has become feasible provided certain assumptions about the applications are met. The same results are not yet available for embedded systems. For embedded systems, the situation is different in various respects. MPSoCs, for example, are characterized by communication speeds which are comparable to the speeds of larger on-chip memories. As a result, communication based on the message-passing interface (MPI) is completely ill-designed, since it uses memory buffers extensively. Due to its limitations, special variants of MPI exist. Also, embedded system applications are different from general purpose or high performance computing. They are typically more “well-behaved” in that features like recursion, dynamic loop bounds, dynamic memory allocation, pointers, dynamic class loading etc. are much less frequent, simplifying the analysis. However, heterogeneity of processing elements, real-time constraints, streaming data, limited communication resources and energy awareness impose additional restrictions.
2. Most embedded systems are integrated into a physical environment. In such an environment, time is frequently the most critical resource. It has been found that the lack of timing in the core abstraction of computer science is a serious flaw (see, for example, Edward A. Lee, http://ptolemy.eecs.berkeley.edu/publications/papers/05/APOT/APOT.pdf). Reconciling code generation and timing models should therefore receive more attention.
3. Efficiency of embedded systems is a main concern. Therefore, optimized architectures are required and resource allocation has to be handled with care. There are many proposals for optimizing architectures. For example, customized instruction sets, exploitation of attached FPGAs and multimedia instructions have been suggested. Most of these features require special consideration in compilers and code generation. Resource allocation includes the allocation of execution time, energy, memory space, bandwidth etc. Traditionally, these resources have been allocated independently. Integrated resource allocation is still not generally available. Memory allocation can be considered as a special case of resource allocation. Access times and energy consumption increase with the size of the memory. There is a growing gap between the speed of processors and the speeds of memories, even for larger on-chip memories of MPSoCs. Memory hierarchies are introduced to ease the problems resulting from this gap. Memory hierarchies are extremely important. Currently available memory hierarchies are typically designed to provide a good average-case performance. However, methods for increasing the average-case performance often deteriorate the worst-case performance and the timing predictability. Hence, timing predictability is becoming a key bottleneck for high-performance embedded systems and the memory system is a key source of unpredictability. Furthermore, memory hierarchies have not been designed for an efficient use of the available energy. In general, the link between memory architectures and compilation techniques is rather weak.
4. Software generation has evolved to a level where compilers are key components, but not the only components that are useful for generating executable code. New models of

computations such as data-flow based models aim at avoiding the well-known disadvantages of imperative programming styles. Software synthesizers generate imperative code from abstract specifications such as Matlab, or Kahn process networks. It can also be expected that the link between software engineering and embedded systems will become stronger. Hence, trends like the use of UML-based system models do have to be respected as well. For the above models, code is synthesized from specifications in non-imperative languages.

5. Many applications in the embedded systems domain are not only resource-restricted but also safety-critical. This in turn requires compilers for embedded processors to be both efficient and correct. One crucial phase in the compiler is the code generation. Due to its complexity, further increased by reason of parallel processing which needs substantial support, it is highly error prone. Hence, verification of code generation is necessary to ensure that transformations preserve the semantics during compilation.
6. Work on this activity is also linked to the ArtistDesign transversal clusters.

-- Changes wrt Y1 deliverable --

No changes with respect to Year 1.

1.6 Technical Description: Joint Research

In order to make the results available to as many designers as possible, tools will be based on pre-pass source-to-source optimization tools whenever feasible. This way, the mapping of applications to MPSoCs can be added to many existing, proven tool flows. Investments into compilers can be protected, the development effort can be reduced and the focus on new optimization techniques can be increased. The key advantage of pre-pass optimizers is their applicability in a large number of tool chains. Such tool chains do not require new compilers to be written. They may be using a compiler from a family of compilers (such as gcc) or specially designed compilers. Pre-pass optimizers can easily support a family of compilers without any modification and different compilers with only few modifications. Pre-pass optimizers do already exist for memory-architecture aware compilation and program parallelization. IMEC and partners at the Universities of Dortmund, Passau, and Edinburgh have significant experience with the design of pre-pass optimizers. They reflect the fact that the resources of a network of excellence are limited.

The following joint work with a focus on integration has been or will be performed in this activity:

1. *Compilation techniques for MPSoCs* cannot be developed from scratch since the problems to be solved are very challenging. The current project will certainly not provide enough resources to develop completely new techniques. Fortunately, we can build upon compilation techniques for high-performance computing. Using the limited resources, we established a link between the high-performance computing and the embedded system domain. Integration activities will comprise an in-depth analysis of the applicability of techniques designed in one domain to the other domain. For this purpose, it is very essential that the proposed project includes enough expertise in different areas of applications. Knowledge about hardware architectures would not be sufficient to really check the applicability of the techniques. The University of Passau is a link to the high-performance community. Cooperation with core partners and selected affiliates is used to check which of the existing techniques can be employed in embedded systems and which extensions are needed. Twelve months after the start of the network, a plan for integration of tools and for closing gaps was expected. After 24

months, the design of the integration work should be complete. Later, available automatic parallelization techniques will be integrated to close identified gaps in the tool support. After 36 months, the implementation of the integrated tools should be complete. After 48 months, an evaluation of the integration should be available. This area has not been tackled in the Artist2 network of excellence.

2. Reconciliation of compilers and timing analysis bridges the two activities of this cluster. The work in this area builds on top of the integration work performed in the Artist2 network of excellence. The existing integration of timing analysis and compilers will be used to explore the potential of this approach further. Additional information can be passed between compilers and timing analysis. The impact of optimizing for WCET has to be studied further. Additional hardware components have to be studied. The influence of context switches has to be analysed. Techniques for reducing the number of calls of timing analysers would be of interest. A detailed list of papers is included in sections 2.2. and 2.4.
3. The efficiency of designs is dealt with in ArtistDesign. It can be achieved with many different means. Research on specialized instructions and new optimizations can be expected. If feasible, such optimizations will be implemented as pre-pass optimizations so that they can be used with various compilers. Memory architectures will be considered in-depth, due to their potential for contributing toward an overall efficiency. Memory architectures are very important for the mapping to networked processors. Indeed, the mapping of applications to processing elements may be significantly affected by the connectivity of the memories. Hence, optimized mappings to memories are considered as well. Such techniques should provide optimization techniques taking several objectives into account. Work in this area builds on top of previous work in the Artist2 network.
4. Software synthesis will be a long-term goal. Software synthesis has not been considered in the compiler cluster of Artist2. As much as feasible, it is considered as well in ArtistDesign. The activity includes affiliate partners specializing on software synthesis. Also, other clusters of the network include prominent experts on software synthesis (Benveniste, Halbwachs). The potential resulting from this is being explored. However, the activity includes a very limited set of partners. Thus, we have to set priorities regarding the research areas to be covered and, unfortunately, software synthesis cannot receive a high priority.
5. In addition to topics 1 to 4, members of this activity will also extend the areas for which the correctness of compilers has been shown via formal verification, focussing on the crucial code generation phase during compilation. The work in this area builds on top of the work performed in the Artist2 network of excellence.
6. The members of this activity will also contribute to the thematic activities of the Transversal Integration work package, focussing on predictability and adaptivity issues. This area has not been tackled in the Artist2 network.

-- Changes wrt Y1 deliverable --

Goals have remained the same as for year 1. For year 2, we are seeing a tighter integration of tools and progress in their capabilities.

1.7 Work achieved in Year 1

The following work was performed for the different areas of the activity:

1. It was important to set up the required interaction of the partners regarding compilation for MPSoCs. The partners started with an intensive workshop in June, 2008. The workshop was held from June 16 to June 17, 2008 at Rheinfels Castle, St. Goar, Germany. Due to the complexity of the problem and the limited manpower of the network, we invited a number of European groups known to be working in relevant areas to the workshop, including members of the HIPEAC network of excellence and the ACOSTES project. This way, we tried to reach out far beyond the limited set of ArtistDesign partners, using these partners as the seed for a larger network of cooperating partners. A more detailed report is available in the Y1 deliverables as well as on the workshop web pages (see http://www.artist-embedded.org/artist/Mapping-of-Applications-to-MPSoCs.html). A summary from the workshop was presented at the CASA workshop held as part of the Embedded Systems Week in Atlanta on Oct. 19th, 2008.

   In addition, several smaller meetings took place. This work was performed in cooperation with the execution platforms cluster and involved teams outside the ArtistDesign network.

2. Regarding the reconciliation of compilers and timing analysis, significant work was performed as well. The key questions to be solved were: how much would a compiler benefit from a tight integration with timing analysis? How much different are the code generation results for an optimization of the average case and of the worst case? Will the average run time increase if we optimize for the worst case?

3. Regarding the work on design efficiency, the problem tackled concerned the integration of various tools from various partners (not just limited to this activity).

4. For software synthesis, the question was how to find a link to the work on mapping of applications to MPSoCs.

5. Concerning the support for verification of code generation, TU Berlin has continued its work on formalizing important parts of the semantics of the intermediate representation, of assembler and machine code and examples of transformation rules that describe the compilation between intermediate forms. In particular, we investigated the different kinds of number representations and the rules describing their compilation. Using the Isabelle/HOL theorem prover, we formalized various kinds of integer data types in assemblers. In one of the code generation rules of a compiler developed at TU Berlin (using the CoSy tool from ACE, Amsterdam), we found a mistake arising from a copy&paste bug when deriving one rule from a very similar, already existing rule.
   Besides the research on compiler verification, TU Berlin was also involved in research on compiler optimization. The work on compiler optimizations for parallel architectures has been continued. A demonstrator has been completed together with research on VLIW optimizations based on machine learning. Furthermore, current work deals with optimizations for MPSoCs.

6. For transversal integration, getting requirements from industry was a key goal

Resources of the network were used to support the cooperation. Research work was paid through other resources.

-- No changes wrt Y1 deliverable --

This section was already presented in the Y1 deliverable, in sections 1.7 and 3.1.

1.8 Problems Tackled in Year 2

1. Work on the mapping of applications to MPSoCs has been continued. First of all, the second workshop on mapping of applications to MPSOCs was held at Rheinfels Castle in June 2009. We managed to reach out far beyond the ArtistDesign partners by inviting prominent European, Asian and American researchers in the field. The road toward new integrated tools has been followed. The work on MAPS at Aachen continued in cooperation with other partners. TU Dortmund and ETH Zürich worked on an extension of the mapping and optimization framework DOL which was developed at Zürich. As a result DOL was extended by the integration of memory hierarchies in the mapping decision and design space exploration of the tool. Work on the integration of energy optimization is still ongoing.

2. Regarding the reconciliation of compilers and timing analysis: The impact of WCET minimization has been analyzed for additional optimizations, including optimizations for registers and scratch pad memories.

   Machine learning has shown its capabilities for an automatic generation of heuristics used by compiler optimizations. In Y2, supervised learning approaches are studied for the first time in the context of an automatic minimization of the WCET. Using a reconciling of a WCET-aware compiler and a machine learning tool, heuristics for a WCET-aware function inlining and loop invariant code motion have been developed. The model selection problem, i.e., selecting learning algorithms and their respective parameters, has been tackled by an evolutionary algorithm that automatically finds good solutions within the large search space.

3. Regarding the work on design efficiency; The MPARM simulator has been used by a numer of partners. In addition, TU Dortmund has ported IMEC's RTLib, thus allowing us to use MPARM together with IMEC's MPA tools.

   MPA parallelization assistant tool and MH static memory assignment tool by IMEC have been integrated more tightly. The main problems tackled were in respect with cleaning sequential source code in order to parallelize it more efficiently, parallelization exploration, FIFOs sizing and FIFOs access management.

   The MH static memory assignment tools by IMEC have been integrated tighter with the DMM dynamic memory assignment tools by NTUA. The main problem tackled was in respect with data interdependencies and sharing physical memory resources.

4. Going beyond the plan, software synthesis was not integrated into the second Rheinfels worksshop. Rather, we organized a separate workshop on this issue during the Embedded Systems Week at Grenoble. This approach required a bit more work, but turned out to be more useful, since we could maintain a clear focus for both workshops.

5. Concerning the support for verification of code generation, TU Berlin continued its cooperation and its work on formalizing important parts of the semantics of the intermediate representation.

6. Members of the cluster also contributed to work on predictability and industrial applications.

   Also, the educational workshop WESE was organized by the leader of this activity. The workshop attracted top researchers. For example, the keynote was given by Edward A. Lee (UC Berkeley). In order to improve the visibility of the results, WESE papers are now included in the ACM digital library.

   Another problem perpendicular to the cluster structure was tackled by the leader of the cluster: in order to extend the accessibility of results, the activity leader became editor for a special series of books on embedded systems published by Springer (see http://www.springer.com/series/8563).

   Several months of work was spent on improving available educational material: the bulk of the work on the next (extended) edition of the textbook "Embedded System Design" by P.

Marwedel was completed. It is being tested in a course held during the winter of 2009/2010. The second edition is scheduled to be published during the first quarter of 2010.

-- The above is new material, not present in the Y1 deliverable --

2. Summary of Activity Progress in Year 2

2.1 Technical Achievements

A high-level virtual platform for early MPSoC software development (RWTH Aachen, ACE)
In the context of MAPS project in RWTH Aachen, a high-level virtual platform technique for early MPSoC SW development has been proposed and developed, the MVP (MAPS Virtual Platform). The MVP provides a set of tools for abstract MPSoC simulation and the corresponding application programming support in order to enable the development of reusable C code at a high level. The tasks can be mapped to processing elements of a virtual prototype of the platform dynamically during the run-time (which uses System-C as parallel execution environment under the hood). Therefore functionality of the parallelized application and early performance measurement e.g. deadline misses can be checked. It uses source-level instrumentation technique to shield the user from System-C context so that they can program in the familiar C programming language. RWTH Aachen and ACE have co-operated on this and the CoSy framework has been used in the MVP. Two papers have been published on this research topic and a joint demo-booth from RWTH Aachen and ACE was held in this year's DAC.
http://www.iss.rwth-aachen.de

Integration RTLib and MPARM (TU Dortmund, IMEC)
To enable RTLib support under the MPARM platform TU Dortmund is developing R²G (RTEMS and RTLib Glued Together). R²G is an intermediate software layer between the real-time operating system (RTEMS) running on the MPARM and the run-time library (RTLib: initially provided by IMEC). This intermediate layer is necessary to eliminate the limitations of RTEMS and the simulator. Due to the POSIX like semantics of R²G, a first prototype portage of RTLib is already working.
http://ls12-www.cs.tu-dortmund.de/staff/heinig/research/projects/r2g/

CleanC, MPA parallelization assistant and MH static memory allocation for MPSoC (IMEC vzw)
IMEC has continued work on the CleanC, MPA and MH toolsuite for source code parallelization and static memory management for MPSoC. The tools are made more robust and the underlying exploration optimization methodologies were improved. By specifying the parallelization at a high abstraction level, and leaving the actual source code transformations to the tools, a designer can try out many parallelizations in a short time. A parallelization may use either functional or data-level splits, or a combination of both. Regarding memory optimizations the work in loop transformation methodologies has continued. Finally, it is worth noting the improvement in the IMEC CleanC Analysis tools, which analyze C code for a variety of coding patterns that make the C code hard to understand by humans and very difficult to analyze by tools. They are now fully integrated in the Eclipse development environment, and available as open source. For this effort IMEC's CleanC Tools has won the French electronic industry's annual Electron D'Or 2009 award in the category Software Tools.
http://www.imec.be/cleanc

Scheduling and data management using system scenarios (IMEC vzw, NTUA, TU/e)
System scenarios were deployed for execution scheduling and data (memory) management methodologies. This particular collaboration is relevant for both the SW Synthesis, Code Generation and Timing Analysis cluster and the Hardware Platforms and MPSoC cluster. More details can be found on the Hardware Platforms and MPSoC Design activity deliverable of Year 2.

Mapping of applications to HW/SW-platforms comprising FPGAs (University of Passau)
Progress on programming FPGAs (field programmable gate arrays) ease their usage and allow their integration in application scenarios. Primary applications show two benefits for the integration: (1) a significant increase in efficiency and (2) decrease in energy consumption could be achieved. Although, the usage of FPGAs is promising, their integration in applications is still tedious and error-prone. In ongoing work, we apply modern software engineering techniques to ease the integration of FPGAs. Furthermore, we will look at interactions between the programmable hardware and the ambient system.

Making the LooPo loop optimizer available in the embedded world (University of Passau, TU Dortmund)
The University of Passau presented their loop parallelization framework LooPo at the ArtistDesign working meeting in Düsseldorf in November 2008. In the resulting discussions, ideas about buffer management in the context of scratchpad memory and local memory on clients for automatic parallelization were exchanged. Specifically, we discussed our experience with the use of Ehrhart polynomials for target code generation. Furthermore, the presentation of the ICD-C compiler from Dortmund created interest in using ICD-C as a compiler interface for LooPo. Cooperation has been initiated, with a student from the Universität Passau working on investigating ways of adapting LooPo to the ICD-C interface. However, some further work has to be done on the recognition technique in ICD-C, especially in the context of determining whether structured (and possibly non-structured) loop code fits the restrictions of the polytope model.
https://www.infosun.fim.uni-passau.de/trac/LooPo/

Extending the polyhedron model for automatic loop parallelization to include non-linearities (University of Passau)

Armin Größlinger at the University of Passau defended his dissertation on “The Challenges of Non-linear Parameters and Variables in Automatic Loop Parallelisation” on 2 December 2009. It received special honours, praised as one of the most significant steps in polyhedral loop parallelisation in the last 15 years. One of the extensions to the model is aimed at automatic code generation for scratchpad memories in graphical processing units. This led to a paper in the conference CC 2009 (one of the ETAPS conferences).

-- The above is new material, not present in the Y1 deliverable --

2.2 Individual Publications Resulting from these Achievements

RWTH Aachen
Ceng, J., Sheng, W., Castrillon, J., Stulova, A., Leupers, R., Ascheid, G., and H. Meyr: A High-Level Virtual Platform for Early MPSoC Software Development, In: International Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS 2009), Grenoble, France, 2009.

Anastasia Stulova, Jianjiang Ceng, Weihua Sheng, Jeronimo Castrillon and Rainer Leupers: A Co-simulation Framework for MPSoC Run-Time Behavior Analysis in Early System Design, MCC 2009

TU Dortmund

Paul Lokuciejewski, Fatih Gedikli, Peter Marwedel, and Katharina Morik: Automatic WCET Reduction by Machine Learning Based Heuristics for Function Inlining, In: *Proceedings of the 3rd Workshop on Statistical and Machine Learning Approaches to Architectures and Compilation (SMART'09),*, pages 1-15, Paphos / Cyprus, January 2009.

Paul Lokuciejewski, Daniel Cordes, Heiko Falk, and Peter Marwedel: A Fast and Precise Static Loop Analysis based on Abstract Interpretation, Program Slicing and Polytope Models, In: *International Symposium on Code Generation and Optimization (CGO)*, pages 136-146, Seattle / USA, March 2009.

Heiko Falk (editor): Proceedings of the 12th International Workshop on Software & Compilers for Embedded Systems (SCOPES), April 2009. http://www.scopesconf.org/scopes-09.

Paul Lokuciejewski, Fatih Gedikli, and Peter Marwedel: Accelerating WCET-driven Optimizations by the Invariant Path - a Case Study of Loop Unswitching, In: *The 12th International Workshop on Software & Compilers for Embedded Systems (SCOPES)*, pages 11-20, Nice / France, April 2009.

G. Schünemann, P. Hartmann, D. Schirmer, P. Towalski, T. Weis, K. Wille, and P. Marwedel: An FPGA Based Data Acquisition System for a fast Orbit Feedback at DELTA, In: *9th European Workshop on Beam Diagnostics and Instrumentation for Particle Accelerators*, Basel / Switzerland, May 2009.

Sascha Plazar, Paul Lokuciejewski, and Peter Marwedel: WCET-aware Software Based Cache Partitioning for Multi-Task Real-Time Systems, In: *The 9th International Workshop on Worst-Case Execution Time Analysis (WCET)*, pages 78-88, Dublin / Ireland, June 2009.

Paul Lokuciejewski and Peter Marwedel: Combining Worst-Case Timing Models, Loop Unrolling, and Static Loop Analysis for WCET Minimization, In: *The 21st Euromicro Conference on Real-Time Systems (ECRTS)*, pages 35-44, Dublin / Ireland, July 2009.

Heiko Falk: WCET-aware Register Allocation based on Graph Coloring, In: *The 46th Design Automation Conference (DAC)*, pages 726-731, San Francisco / USA, July 2009.

Heiko Falk and Jan C. Kleinsorge: Optimal Static WCET-aware Scratchpad Allocation of Program Code, In: *The 46th Design Automation Conference (DAC)*, pages 732-737, San Francisco / USA, July 2009.

Peter Marwedel, Jeff Jackson, Kenneth Ricks (editors): Workshop on Embedded Systems Education, Proceedings, ACM Digital Library, ISBN: 978-1-60558-700-4

Paul Lokuciejewski, Timon Kelter, Peter Marwedel: Superblock-Based Source Code Optimizations for WCET Minimization, submitted to RTAS 2010

Paul Lokuciejewski, Marco Stolpe, Katharina Morik, Peter Marwedel: Automatic Selection of Machine Learning Models for Compiler Heuristic Generation, submitted to CGO 2010

IMEC

Baert, R.; Brockmeyer, E.; Wuytack, S. and Ashby, T.: Exploring parallelizations of applications for MPSoC platforms using MPA. In Design, Automation and Test in Europe, DATE 2009, Nice, France, April 20-24, 2009. IEEE 2009

Mignolet, J.; Baert, R.; Ashby, T.; Avasare, P.; Jang, H. and Son, J.: MPA: Parallelizing an application onto a multicore platform made easy. In IEEE Micro journal p.31-39, Vol.29, Issue 3, (2009)

Jean-Yves Mignolet, Roel Wuyts: Embedded Multiprocessor Systems-on-Chip Programming. In IEEE Software journal p.34-41, Vol.26, Issue 3, (2009)

Martin Palkovic, Francky Catthoor, Henk Corporaal: Trade-offs in loop transformations. ACM Trans. Design. Autom. Electr. Syst. TODAES journal, Vol.14, Issue 2, (2009)

Palkovic, M.; Corporaal, H. and Catthoor, F.: Dealing with data dependent conditions to enable general global source code transformations. International Journal of Embedded Systems p.27-31, Vol 4, Issue 1, (2009)

Universität Passau
Jörg Liebig, Sven Apel, Christian Lengauer, and Thomas Leich: RobbyDBMS: A Case Study on Hardware/Software Product Line Engineering, In: Proceedings of the International Workshop on Feature-Oriented Software Development (FOSD), pages 60-65. ACM Press, October 2009 (http://portal.acm.org/citation.cfm?doid=1629716.1629729).

Jörg Liebig, Sven Apel, Christian Lengauer, and Thomas Leich: RobbyDBMS: A Case Study on Hardware/Software Product Line Engineering, In: Proceedings of the International Workshop on Feature-Oriented Software Development (FOSD), pages 60-65. ACM Press, October 2009 (http://portal.acm.org/citation.cfm?doid=1629716.1629729).

TU Berlin
Lars Alvincz and Sabine Glesner: Breaking the Curse of Static Analyses: Making Compiler Intelligent via Machine Learning. 3rd Workshop on Statistical and Machine learning approaches to ARchitectures and compilaTion (SMART'09)

-- The above are new references, not present in the Y1 deliverable --

2.3 Interaction and Building Excellence between Partners

Main interaction between the partners was through the 2nd workshop on the mapping of applications to MPSoCs on June 29-30, 2009.

TU Dortmund is cooperating with ETH Zürich on exploring the idea of extending the design space exploration from ETZ Zürich with memory-aware techniques.

The partners from Dortmund (at ICD), Leuven (at IMEC) and Eindhoven (at TU Eindhoven, member in another ArtistDesign cluster) are jointly working on the MNEMEE project funded through the 7th framework (see http://www.mnemee.org). TU Eindhoven is actively using the compiler development framework ICD-C (see http://www.icd.de/es/index.html) into some of its tools. Members of the team at TU Dortmund have integrated the MPARM simulator from U. Bologna with IMEC's RTLib, thus allowing us to use MPARM together with IMEC's MPA tools.

IMEC is cooperating with TU/e and DUTH (affiliated partners in another ArtistDesign cluster) on system scenarios for MPSoC system level design optimizations (see http://www.es.ele.tue.nl/~vali/scenarios/).

Dortmund and Passau pursued the idea of using the ICD-C compiler from Dortmund as a frontend and/or backend for the loop parallelizer LooPo from Passau.

The partners from IMEC, DUTH and KTH are jointly working on the MOSART project funded through the 7th framework (see http://www.mosart-project.org).

The partners from RWTH Aachen and TU Dortmund are jointly teaching a course in retargetable compilation (including memory-architecture aware compilation) at the Advanced Learning and Research Institute (ALARI) in Lugano, Switzerland (see http://www.alari.ch).

The partners from Dortmund and members of other ArtistDesign activities (Bologna, Pisa, Saarbrücken, Zürich) are jointly working on the PREDATOR project funded through the 7th framework (see http://www.predator-project.eu).

RWTH Aachen is also a member of the HIPEAC Network of Excellence where they lead the research cluster on Design Methodology and Tools. Within this NoE and carrying the ARTIST banner they have interacted with the top level academic and industrial partners. On 1st June, 2009, a joint seminar was held in at FORTH, Greece with the group of Manolis Katevenis

RWTH Aachen is participating in a large scale project funded by the German government, the excellence cluster “Ultra high-speed Mobile Information and Communication” (UMIC) where they lead the sub-area “RF Subsystems and SoC Design”. In the “Nucleus” project of UMIC, Aachen has been looking into the research topics on designing and mapping SDR (software-defined radio) applications onto heterogeneous MPSoC platforms.

RWTH Aachen and Compaan are co-operating on mapping Kahn Process Networks applications onto a real-life TI OMAP platform through a master thesis work.

RWTH Aachen and ACE are co-operating on a technique to generate C-code from a high-level intermediate representation of C compiler during a master thesis work.

RWTH Aachen and ACE are collaborating on the MAPS project - CoSy was used in the MAPS Virtual Platform for high level exploration and profiling of embedded MPSoC software. A joint demonstration booth of RWTH Aachen and ACE highlighting the capabilities of CoSy in terms of providing efficient support for C code instrumentation and high-level code optimization was held in this year’s DAC in San Francisco.

On Feb 11, 2009, the team from Edinburgh University (Dr. Bjoern Franke) visited Aachen to hold a joint seminar workshop in the UMIC research centre. The seminar topics included computer architecture, design tools and simulation.

RWTH Aachen invites ACE to give a guest lecture every year in the course of “Compiler Construction” for Master-level students. On June 17, 2009, Dr. Marcel Beemster from ACE visited Aachen to give the guest lecture for this year. The topics covered the compiler backend techniques and new trends towards MPSoC compilation.

TU Berlin and ACE extended their cooperation concerning the development of optimizing compiler transformations as well as verifying transformations.

Sander Stuijk of TU Eindhoven visited TU Dortmund from March 9th to May 28th. TU Dortmund and TU Eindhoven are cooperating to develop a novel solution for mapping applications cost-efficiently to the memory hierarchy of any MP-SoC platform. Both groups have in the past developed their own approach. The objective of the visit is to align both approaches in order to develop a mapping flow that combines best practices of both approaches. A common mapping flow has been defined during the visit. Both groups have continued to work on this flow after the visit ended. Also, Sander Stuijk provided comments on a pre-release of the forthcoming second edition of the textbook “Embedded System Design” by P. Marwedel. These have been taken into account.

Christos Baloukas of the Institute of Communication and Computer Systems (ICCS, associated to the National Technical University of Athens) visited TU Dortmund from Sept 8th to Oct. 5th. The reason for the visit was to get acquainted with the MACC framework used at Dortmund for the integration of memory-architecture aware pre-pass optimization tools, both at TU Dortmund and its spin-off ICD, including work in the MNEMEE-project. ICCS tools were successfully integrated into the MACC framework.

Ioannis Iosifidis of the Institute of Communication and Computer Systems (ICCS, associated to the National Technical University of Athens) visited IMEC from 15.09.09 to 15.11.2009.
The reason for the visit was to integrate exploration methodologies for static and dynamic memory assignment and data management methodologies, including work in the MNEMEE-project. The ICCS' tools were successfully integrated into MPA/MH framework.

Aurore Junier (ENS Rennes) visited Dortmund from June 1 to July 6 to work on WCET-aware register allocation. An experimental version of a WCET-oriented register allocator was developed and tested.

-- Changes wrt Y1 deliverable --

Further integration of tools was achieved for all partners.

2.4 Joint Publications Resulting from these Achievements

RWTH Aachen, NXP, UC Irvine
R. Leupers, S. Ha, A. Vajda, R. Doemer, M. Bekooij and A. Nohl: Programming MPSoC Platforms: Road Works Ahead, DATE 2009

TU Dortmund, ETH Zürich
Paul Lokuciejewski, Heiko Falk, Sascha Plazar, Peter Marwedel, Lothar Thiele: Multi-Objective Exploration of Compiler Optimizations for Real-Time Systems, submitted to ISORC 2010

IMEC vzw., TU/e

S.V. Gheorghita, M. Palkovic, J. Hamers, A. Vandecappelle, S. Mamagkakis, T. Basten, L. Eeckhout, H. Corporaal, F. Catthoor, F. Vandeputte, K. De Bosschere: *A System Scenario based Approach to Dynamic Embedded Systems*, ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 14, Number 1, (2009)

IMEC vzw., NTUA

Baloukas, C.; Temmerman, M.; Keller, A.; Mamagkakis, S.; Catthoor, F.; Soudris, D. and Demeyer, S.: Abstract and concrete data type optimizations at the UML and C/C++ level for dynamic embedded software. In Book Chapter of Behavioral Modelling for Embedded Systems and Technologies: Applications for Design and Implementation, p.55-84, (2009)

-- The above are new references, not present in the Y1 deliverable --

2.5 Keynotes, Workshops, Tutorials

Tutorial: S. Mamagkakis and P. R. Panda 'Memory Architectures and Software Transformations for System Level Design', ASP-DAC 2009

Yokohama, Japan, – January, 2009

In this tutorial a memory-aware system level design flow was presented that can address strict power and performance budgeting problems by customizing both the underlying memory architectures/organizations, as well as by transforming the system-level source code to generate an input for system-level design that is better tuned to the memory architectures and organizations. Such a "memory-aware" system level design flow can result in LSI designs exhibiting superior performance, power and memory footprint characteristics.

http://www.aspdac.com/aspdac2009/tutorial/

Course: Peter Marwedel, Rainer Leupers: Retargetable Compilation

Lugano, Switzerland, Feb. 16-19 & Feb 23-25, 2009

The course consisted of two parts: the first part (by Peter Marwedel) focused on memory-architecture aware compilation. The second part (by Rainer Leupers, RWTH Aachen) focused on processor retargetability. The course was supported by ALARI.

http://www.alari.ch

Invited talk: From Embedded Systems to Cyber-Physical Systems: Does the Name Change Matter? – Inauguration of the Uppsala Programming for Multicore Architectures Research Center (UPMARC)

Uppsala, Sweden, March 26, 2009

Objectives: Providing an overview over Embedded Systems Research at Dortmund
Speaker: Peter Marwedel (TU Dortmund)
http://www.it.uu.se/research/upmarc/inauguration

SPECIAL SESSION – Programming MPSoC Platforms: Roadworks Ahead! (Multicore Applications Special Day) DATE 2009

Nice, France, – April 23, 2009

This panel session was organized by R. Leupers (RWTH Aachen) and moderated by M. de Lange (ACE). The goal of this session was to consolidate today's different MPSoC programming approaches, and to provide focus for future R&D activities. M. Bekooij from NXP also participated in this special session.

http://www.date-conference.com/date09/conference/date09-session-12-1

Workshop: Software & Compilers for Embedded Systems (SCOPES) 2009

Nice, France – April 23-24, 2009

SCOPES focuses on the software generation process for modern embedded systems. Topics of interest include all aspects of the compilation process, starting with suitable modelling and specification techniques and programming languages for embedded systems. The emphasis of the workshop lies on code generation techniques for embedded processors. The exploitation of specialized instruction set characteristics is as important as the development of new optimizations for embedded application domains. Cost criteria for the entire code generation and optimization process include run time, timing predictability, energy dissipation, code size and others. Since today's embedded devices frequently consist of a multi-processor system-on-chip, the scope of this workshop is not limited to single-processor systems but particularly covers compilation techniques for MPSoC architectures.

In addition, this workshop puts a spotlight on the interactions between compilers and other components in the embedded system design process. This includes compiler support for e.g. architecture exploration during HW/SW codesign or interactions between operating systems and compilation techniques. Finally, techniques for compiler aided profiling, measurement, debugging and validation of embedded software were also covered by this workshop, because stability of embedded software is mandatory.

SCOPES 2009 was the 12th workshop in a series of workshops initially called "International Workshop on Code Generation for Embedded Processors". The name SCOPES has been used since the 4th workshop. The scope of the workshop remains software for embedded systems with emphasis on code generation (compilers) for embedded processors.

SCOPES 2009 was organized by Heiko Falk from TU Dortmund and was held as DATE Friday Workshop. There were many discussions between cluster members at SCOPES (starting already on the eve before the sessions), at DATE, making the entire week the key joint event in spring.

http://www.scopesconf.org/scopes-09

Meeting: 2nd Workshop on Mapping Applications to MPSoCs, 2009

St. Goar*, Germany – June 29-30, 2009*

This is the flagship workshop of this cluster. For the second edition, it was possible to attract researchers from all over the world as presenters. For example, Soonhoi Ha of Seoul National University presented his work on the HOPES system. Also, Jürgen Teich from the University of Erlangen-Nürnberg presented his work on the SystemCoDesigner. New presenters also included Tajana Simunic (UCSD) and Qiang Xu from the Hong Kong City University. This way, we managed to establish links to key researchers outside the network and potential new affiliate members. A discussion on benchmarks was started. The workshop is now a key forum for discussions in this area. Attendees expressed their strong interest to continue this series of informal workshops as a platform for discussions.

http://www.artist-embedded.org/artist/-map2mpsoc-2009-.html

Keynote: S. Mamagkakis 'Emerging multicore hardware platforms and their software support challenges', ECRTS 2009

Dublin, Ireland, – July, 2009

In this keynote talk, the latest developments and future directions of hardware MPSoC platforms for nomadic embedded applications were presented. Next to the hardware perspective, the software related challenges of these emerging MPSoC platforms were discussed and some of the proposed parallelization and memory hierarchy management solutions were evaluated. This keynote is also relevant for the Scheduling and Resource Management activity.

http://ecrts09.dsg.cs.tcd.ie/keynote-speaker.php

Special Series of presentations: P. Marwedel: Overview of work from Dortmund

Seoul (Korea), Fukuoka (Japan), Singapore, Delhi (India), – Aug. 3-14, 2009

In a special sequence of presentations, P. Marwedel provided a survey of research work from Dortmund, including work in the ArtistDesign context, at Samsung (Seoul, Korea), Seoul National University (Korea), Kyushu University (Fukuoka, Japan), NTU and NSU Universities (Singapore) and IIT Delhi (India).

Invited Talk: P. Marwedel: 7th IEEE East-West Design & Test Symposium – EWDTS'09

Moscov, Russia, - Sept. 19.2009

This talk provided an overview over research activities in the "Design Automation for Embedded Systems" group at TU Dortmund.

http://www.ewdtest.com/conf/

Workshop: 5th Workshop on Embedded Systems Education, 2009

Grenoble, France, – October 15, 2009

Embedded system education is still a very young area and frequently restricted to teaching the details of microcontroller programming. A long-term objective of this workshop is to improve the visibility of work in the area and to stimulate the introduction of broader curricula. In 2009, P. Marwedel was the main organizer of the workshop. Visibility was improved by the inclusion of the proceedings in the ACM digital library. Presenters included top researchers from the US and Asia. Attendees were extremely satisfied with the quality of the presentations.

http://www.artist-embedded.org/artist/-WESE-09-.html

Workshop: 1st Workshop on Software Synthesis, 2009

Grenoble, France, – October 16, 2009

An increasing amount of software is not written manually any more. Rather, software is synthesized from abstract models of the required functionality. Software synthesis has been implemented in various disperse communities. The workshop aimed at bringing these communities together. Presenters at this workshop presented industrial as well as academic results. Attendees agreed on the necessity of more work in this area. The workshop was organized by P. Marwedel and A. Sangiovanni-Vincentelli.

http://www.artist-embedded.org/artist/-WSS-09-.html

Invited Talk: C. Lengauer on the proposal "Manycore" for a DFG National Research Intiative, Yearly Meeting: GI Working Group for Software Engineering for Parallel Systems (SEPARS)

Saarbrücken, Germany, -- November 6, 2009

The talk stressed the necessity for a national research initiative on the topic of Manycore software technology. It also sketched a number of new opportunities that manycore platforms offer. At the meeting, Lengauer was elected onto the Board of SEPARS.

Invited Talk: P. Marwedel: IP – Embedded Systems Conference

Grenoble, France, - Dec. 3, 2009

This talk provides an overview over results presented at the first two Rheinfels workshops on mapping applications to MPSoCs.

http://www.design-reuse.com/ipesc09/program/

-- The above is new material, not present in the Y1 deliverable --

3. Milestones, and Future Evolution

3.1 Problem to be Tackled over the next 12 months (Jan 2010 – Dec 2010)

1. In order to improve the cooperation on solving the problem of mapping applications to MPSoCs, we will continue to run the Rheinfels series of workshops. The third workshop is scheduled to take place on June 28-29, 2010 (see http://www.artist-embedded.org/artist/-map2mpsoc-2010-.html). The SCOPES workshop, recently held as a DATE Friday workshop, will be moved to Rheinfels Castle as well and will be held on June 29-30, 2010 (see http://www.artist-embedded.org/artist/-SCOPES-2010-.html) . Also, work on actual mapping tools will continue. The MAPS tool will be extended in cooperation with other partners. Cooperation between ETH Zürich and TU Dortmund will be continuing.
2. Work on code optimizations taking the WCET into account will be extended toward multi-objective optimization, multi-cores and links with operating systems.
3. Work on memory-architecture-aware compilation tools will be continued. The focus will be on pre-pass compilation tools and on the support of multi-processor systems.
4. Work on compiler verification will be continued. It is planned to investigate if semantics of intermediate and assembler/machine code can be formalized such that it can also be executed. Also the transformation between intermediate and assembler/machine code shall be given such that the compiler can be generated using the code generator of the Isabelle/HOL theorem prover.
5. We will be continuing to contribution to the state of the art in Embedded Systems Education. The next edition of the text book “Embedded System Design” by P. Marwedel will be published in the spring of 2010. P. Marwedel will also continue to work on the publication of a series of books on Embedded Systems to be published by Springer (see http://www.springer.com/series/8563). Also, the network will be involved in the organization of the next WESE workshop, scheduled for Oct. 28th, 2010.
6. We are planning to organize a second workshop on software synthesis during the Embedded Systems Week at Scottsdale, Arizona, on Oct 29, 2010
7. The partners will also contribute to other activities, such as the transversal activities

-- Changes wrt Y1 deliverable --

Initially, we planned to cover software synthesis at the Rheinfels workshop on the mapping of applications to MPSoCs. We assume that we will continue organizing an independent workshop on this topic.

3.2 Current and Future Milestones

The following list of current and future milestones used the same enumeration which was used in sections 1.5 to 1.7.

1. Mapping of applications to MPSoCs

- The identification of the needs and possible approaches was the focus of the first year. The goal was to come up with ideas for the design of mapping tools and to see how existing tools could be integrated into a flow meeting the requirements. *This goal has been achieved. The results from the Rheinfels workshop ((*see http://www.artist-embedded.org/artist/Mapping-of-Applications-to-MPSoCs.html) *together with the results from the working meeting at Düsseldorf provide sufficient input (see* http://www.artist-embedded.org/artist/map2mpsoc-08-fall-meeting.html).
- The design of an integrated tool flow will be the goal for the second year. This design will comprise the key decisions regarding interfaces and implementations. It will not include a full implementation. *Work on mapping tools is actually ahead of schedule. A prototype of the MAPS tool suite is available. A first demo of the Mnemee tools was performed in June at Rheinfels castle.*
- The **completion of mapping tools** will be the goal for the third year. This implementation will be based on the design to be available at the end of the second year.
- The evaluation of an integrated tool flow will be the goal for the fourth year.

2. Reconciliation of timing analysis and compilers

- The impact of WCET-aware compilation on the resulting code should be analyzed. *This goal has been achieved. Several WCET-aware optimizations have been designed and their impact on the code quality has been published.*
- The analysis of the impact of WCET-aware compilation on the resulting code should be continued in the second year, since many of the standard optimizations have not been considered yet. *Several additional optimizations have been considered, as can be seen from the list of publications*.
- **For year 3, we plan extending the work toward multi-objective optimization, integration with the operating system and beyond the current focus one target architecture.**
- A critical evaluation of advantages and limitations of WCET-aware compilation should be performed.

3. Resource-aware compilation

- Support for predicated execution should be available. Support for extended modelling of memory architectures in the MPARM simulator should be available. An interface for driving simulators and optimizers from the same architectural description should be designed. *These goals have been achieved. A paper on exploiting predicated execution has been published by RWTH Aachen. The extended version of MPARM has been submitted to Bologna by TU Dortmund. The MACC framework for architecture-aware compilation has been designed.*
- MPARM should be used as a key simulation tool by an extended set of partners. *The link to IMEC's MPA tools has been created, even though this was not among the initial targets.* Additional support for special features of embedded

processors should be available. *Support for scratchpad memories has been extended.* Areas 2 and 3 should be linked by exploiting memory hierarchies in WCET-aware compilers. This work should be performed in year 2 of the network. *WCET-aware scratchpad allocation was published at DAC.*

- **Results from the integration in year 2 should be available in year 3.**
- At least one source-to-source transformation tool exploiting memory hierarchies should be made publicly available in year 4.

4. Software synthesis

- The impact of software synthesis should be analysed. *This goal has been only partially achieved. NXP and Compaan presented their results at the Rheinfels workshop. However, due to the limited number of partners in this cluster, many of the specialists in this area could not be involved.*
- Due to the increasing importance of non-standard models of computation, software synthesis will be continued as a sidetrack. *A special workshop was held during the embedded systems week.*
- **The new workshop will be held during the embedded systems week 2010 as well.**

5. Development and Verification of compiler transformations

- The goal here is to facilitate compilers to generate efficient and correct code. *This goal has been achieved. Papers on verifying code transformation during compilation and on interprocedural speculative optimization techniques have been published by TU Berlin.*
- Improving the support of compilers towards efficient and correct code generation will be the goal for the second year. Additional transformations will be considered in the verification effort. *This goal has been achieved.*
- **Verification of compiler transformations** will remain a goal for the third year.

6. Transversal cluster

- The activity maintains a link to the transversal cluster. *This goal has been achieved. The activity leader participated in the meeting at Rome on Nov. 12th and 13th.*
- *Contributions in the area of timing predictability have been made in year 2. The workshop on software synthesis provided a strong interface to industrial applications and was jointly organized in cooperation with the corresponding transversal cluster.*
- The activity will maintain a **link to the transversal** cluster in the coming years. Cooperation will be on a partner by partner basis.

3.3 Main Funding

The ArtistDesign NoE funds integration and building excellence with the partners, and with the European research landscape as a whole. Beyond this “glue” for integration and excellence, during Year2 this activity has benefited from direct funding from:

- **RWTH Aachen**
  The ISS institute at RWTH Aachen University also receives funds from

- Deutsche Forschungsgemeinsschaft (DFG), e.g. via the new Excellence Cluster UMIC (Ultra High Speed Mobile Information and Communication), a large scale next-generation mobile internet research program.
- EU FP6 and FP7 projects like SHAPES, HiPEAC, and NEWCOM.
- Industrial partners like Siemens, Nokia, Infineon, CoWare, and Tokyo Electron.

- **TU Dortmund**
  The group works on several projects, including
  - the MORE project aiming at middleware design for group communication http://www.ist-more.org
  - the PREDATOR project targeting predictable designs http://www.predator-project.eu
  - the MNEMEE project, which is performed at Dortmund's technology transfer center ICD. MNEMEE focuses on the exploitation of the memory hierarchy. http://www.mnemee.org
  - University funding
- **IMEC, Leuven**
  IMEC works on many projects, including
  - **MOSART IST-215244 Project:**
    Mapping Optimization for Scalable multi-core ARchiTecture. ArtistDesign partners involved: Interuniversitair Micro-Elektronica Centrum (IMEC) vzw., Democritus Uni. Thrace (DUTH) and Kungliga Tekniska Hagskolan (KTH) http://www.mosart-project.org/
  - **MNEMEE IST-216224 Project:**
    Memory maNagEMEnt technology for adaptive and efficient design of Embedded systems. ArtistDesign partners involved: Interuniversitair Micro-Elektronica Centrum (IMEC) vzw., Democritus Uni. Thrace (DUTH) and Technische Universiteit Eindhoven (TU/e) http://www.mnemee.org/
  - **IMEC Apollo research program:**
    Disruptive technologies needed to realize nomadic embedded systems for 2012 and beyond. These are technology aware architectures, multiprocessor system-on-chip technology, and reliable design methodologies for sub-45nm unreliable components. For the Apollo research, IMEC cooperates with industrial partners, such as integrated device manufacturers, fabless and fablite IC solution providers, and system integrators.
    http://www2.imec.be/imec_sites/objects/80acd42f851591023f893a7d96fd96bf/annualreport.pdf (page 36)
- **University of Passau**
  The group works on several projects, including
  - the CompSpread project supported by the Deutsche Forschungsgemeinschaft (DFG)
  - the FeatureFoundation project supported by the Deutsche Forschungsgemeinschaft (DFG). This project related to aspect-oriented programming is expected to find applications for embedded system programming.
  - University funds

- **TU Berlin**
  - The group for Software Engineering for Embedded Systems at TU Berlin currently also receives funding from the Deutsche Forschungsgemeinschaft (DFG) for two projects: DFG project VATES (Verification and Transformation of Embedded Systems).
  - DFG project “Optimization and Verification during the Compilation of Higher Programming Languages”, funded within the Emmy Noether excellence program of the DFG.
  - University funding

-- Changes wrt Y1 deliverable --

There is no major change in the funding situation.

4. Internal Reviewers for this Deliverable

- **Andreas Heinig** (TU Dortmund, Informatik 12)
- **Prof. Dr. Olaf Spinczyk** (TU Dortmund, Informatik 12)