Year 2 Review
Brussels, February 12th, 2010

Scientific Management

Achievements and Perspectives

ArtistDesign Network of Excellence

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VERIMAG Laboratory

Reviewers' Recommendations

from the Y1 Review Report

Reviewer's Recommendations (1/3)

Recommendation 1:

ArtistDesign worldwide impact could be accelerated by establishing a more direct link with ACM SIGBED. For example, with a minimum effort, links between the SIGBED and ARTISTDESIGN websites could be established. ArtistDesign could also supply information for the SIGBED review (information about and summary of meetings, initiatives, etc.) http://www.sigbed.org/

DONE

Direct links with SIGBED

- Links to SIGBED on the NoE home page (http://www.artist-embedded.org/)
- APRES 2009 (an ARTIST workshop) published:
  SIGBED Review, Volume 6, Number 3, October 2009
  Special Issue on the 2nd International Workshop on Adaptive and Reconfigurable Embedded Systems (APRES'09)
- SCOPES (an ARTIST workshop) in cooperation with ACM SIGBED

Reviewer's Recommendations (2/3)

Recommendation 2:

The Common Technical Baseline initiative is extremely promising. In fact, it would be useful considering extending its goal and scope and creating an international activity patterned after the UMLS (Unified Medical Language System) in the medical field. (http://www.nlm.nih.gov/research/umls/). It could be an interesting topic for the EU-US collaborative activities, and very beneficial for the educational organizations.

DONE

Common Technical Baseline development is being pursued

Discussions initiated on a collaboration with Vanderbilt

Reviewer's Recommendations (3/3)

Recommendation 3:

Concerning technical deliverables for Year 2 reporting period onwards and in order to avoid redundancy, we would like to propose the possibility of having just incremental documents containing only what is new for that reporting period and referring to previous year's documents for the unchanged sections.

DONE

We have indicated in each deliverable, for each section, whether the text is unchanged, partially updated, or entirely new.

Overview of the NoE

Concepts and Objectives – Main Ideas

Main Idea 1

- *Embedded systems are essential to ensuring a leading position for Europe in key industrial sectors services.*
  This is well-recognized in the ICT FP7 priorities, and through the ARTEMIS ETP.

Main Idea 2

- *Embedded systems design is an emerging scientific discipline, mobilizing a large international community, around a set of fundamental challenging and multi-disciplinary problems.*
- *For this discipline to emerge, a considerable focused research effort by the best teams is needed.*

Objectives

Reinforce and strengthen scientific and technological excellence in Embedded Systems Design:

- The NoE acts as a Virtual Center of Excellence
- **Two levels** of integration
  to create critical mass from selected European teams
  - **Strong integration** within selected topics
    by assembling the best European teams,
    to advance the state of the art in the topic.
  - Integration **between** topics
    to achieve the multi-disciplinary excellence and skills required for the development of future embedded technologies.
- Integration is around a Joint Programme of Activities

Core Participants (1/2)

N°	Beneficiary name	Beneficiary short name	Country
1	UJF FILIALE	FLORALIS	France
2	UNIVERSITE JOSEPH FOURIER GRENOBLE 1	UJF/VERIMAG	France
3	AACHEN	AACHEN	Germany
4	AALBORG UNIVERSITET	AALBORG	Denmark
~~5~~	~~UNIVERSIDADE DE AVEIRO~~ *replaced by UnivPorto*	~~AVEIRO~~	~~Portugal~~
6	ALMA MATER STUDORIUM - UNIVERSITA DI BOLOGNA	BOLOGNA	Italy
7	TECHNISCHE UNIVERSITAET BRAUNSCHWEIG	TUBS	Germany
8	UNIVERSIDAD DE CANTABRIA	CANTABRIA	Spain
9	COMMISSARIAT À L'ENERGIE ATOMIQUE	CEA	France
10	DANMARKS TEKNISKE UNIVERSITET	DTU	Denmark
11	UNIVERSITAET DORTMUND	DORTMUND	Germany
12	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	EPFL	Switzerland
13	EMBEDDED SYSTEMS INSTITUTE	ESI	Netherlands
14	EIDGENOESSISCHE TECHNISCHE HOCHSCHULE ZUERICH	ETH Zurich	Switzerland
15	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	Belgium
16	INRIA	INRIA	France
17	TECHNISCHE UNIVERSITAET KAISERSLAUTERN	TUKL	Germany
18	KUNGLIGA TEKNIKA HOGSKOLAN	KTH	Sweden

Core Participants (2/2)

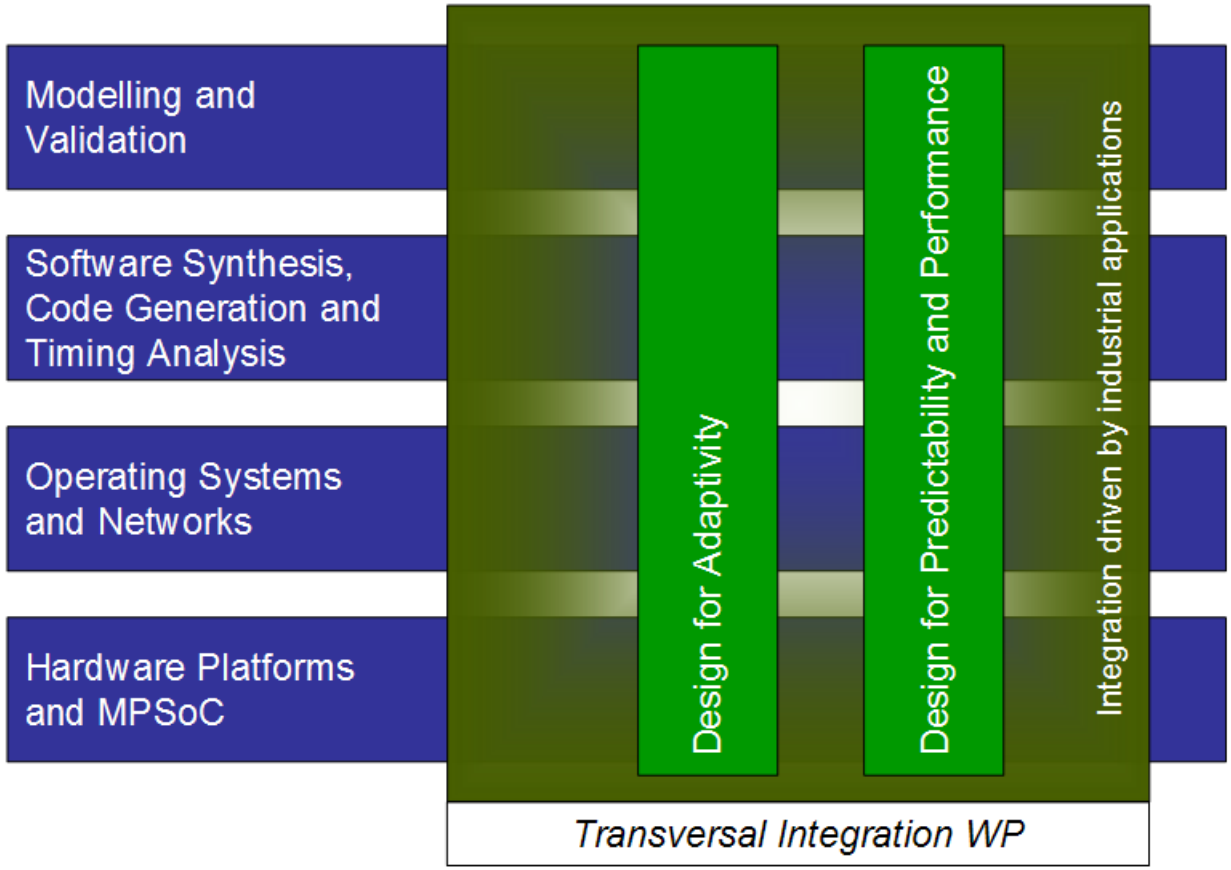
N°	Beneficiary name	Beneficiary short name	Country
19	LINKÖPINGS UNIVERSITET	LINKOPING	Sweden
20	LUNDS UNIVERSITET	ULUND	Sweden
21	MAELARDALENS HOEGSKOLA	MDH	Sweden
22	OFFIS E.V.	OFFIS	Germany
23	PROJECT FOR ADVANCED RESEARCH OF ARCHITECTURE AND DESIGN OF ELECTRONIC SYSTEMS *replaced by Trento*	PARADES	Italy
24	UNIVERSITAET PASSAU	PASSAU	Germany
25	SCUOLA SUPERIORE DI STUDI UNIVERSITARI E DI PERFEZIONAMENTO SANT'ANNA	SSSA-PISA	Italy
26	INSTITUTO SUPERIOR DE ENGENHARIA DO PORTO	PORTO	Portugal
27	UNIVERSITAET DES SAARLANDES	SAARLAND	Germany
28	UNIVERSITAET SALZBURG	PLU-SALZBURG	Austria
29	UPPSALA UNIVERSITET	UPPSALA	Sweden
30	TECHNISCHE UNIVERSITAET WIEN	VIENNA	Austria
31	UNIVERSITY OF YORK	YORK	UK
32	IST-Austria	IST-Austria	Austria
33	UNIVERSITY OF PORTO	UnivPorto	Portugal
34	UNIVERSITY OF TRENTO	TRENTO	Italy

Jointly-executed Programme of Research Activities (JPRA)

Clusters are autonomous entities, with specific objectives, teams, leaders, and a dedicated yearly budget.

The set of Thematic Clusters cover all the main topics in Embedded Systems Design. The thematic activities in the Transversal Integration workpackage focus on Design methodologies, with specific objectives (Predictability, Adaptivity).

Each cluster may have one or several Activities, as appropriate.



Theory, Methods and Tools for ES Design

Design flow involves topics leading from initial requirements to a final implementation satisfying them. The objective is to study specific needs for these design activities, as well the possibility of integrating them in a coherent design flow.

We distinguish four essential topics, for which existing techniques should be adapted and extended :

- **Modelling and Validation**: We need formal modelling techniques that take into account the characteristics of a system's external and execution environments. These techniques should support component-based construction for heterogeneous components to be applicable throughout the design process. For embedded systems, validation focuses on testing and verification of non functional properties, including performance and dependability.
- **Software Synthesis, Code Generation and Timing Analysis**: Strong integration should be sought for these interrelated topics. The aim is to study and implement resource-aware synthesis and code generation techniques. These techniques allow the generation of an implementation meeting given user requirements from a functional description of an application (e.g. application software) and a model of a target platform.
- **Real-Time Operating Systems Scheduling and Networks**: The aim is to develop theory methods and tools for new real-time software infrastructures, for the execution and communication between embedded applications. The main problems include adaptive resource management and dependability techniques, in particular to improve robustness to deviations from nominal conditions.
- **Platforms and MPSoC Design**: The aim is implementation of complex applications on multi-core HW platforms. It raises a number of problems for ensuring predictability and efficiency. These include adaptive techniques for resource management, and the study of reliable programming models for multi-core architectures.

Long Term Integration

Embedded systems design is a multidisciplinary area requiring competences from hardware engineering, operating systems and networks, programming and compilation, modelling and software engineering, control engineering. The ArtistDesign NoE gathers together leading European teams from all these areas.

ArtistDesign continues and extends these activities, both quantitatively and qualitatively. In setting up the consortium, we have the right balance between critical mass, excellence, and commitment from the core partners.

- **Critical Mass**
  We have a sufficient number of partners, to achieve a fair coverage of the main topics in the area, as well as the capacity to impact the European research landscape. Nonetheless, to ensure efficiency, we have limited the number of core partners, based on previous experience. At the same time, our impact is amplified through the large number of affiliated academic, SME, industrial, and international collaboration partners.
- **Excellence**
  The ArtistDesign core partners include the main European leading teams, as attested by their leadership in their respective areas, as well as their strong involvement in national and European projects and initiatives.
- **Commitment**
  The majority of the ArtistDesign core partners were already involved as core partners in the Artist2 NoE. They have demonstrated a high degree of investment to achieve the workprogramme objectives, by committing the resources needed, which are an order of magnitude larger than those provided by the NoE financing. We estimate that the effort for implementing the JPA is roughly 10 times the financial contribution for integration.

Joint Programme of Activities

•ArtistDesign acts as a Virtual Centre of Excellence, composed of a set of virtual teams, called clusters. Each cluster gathers together selected teams from partners, to create the critical mass and expertise in one of the essential topics for embedded systems design.

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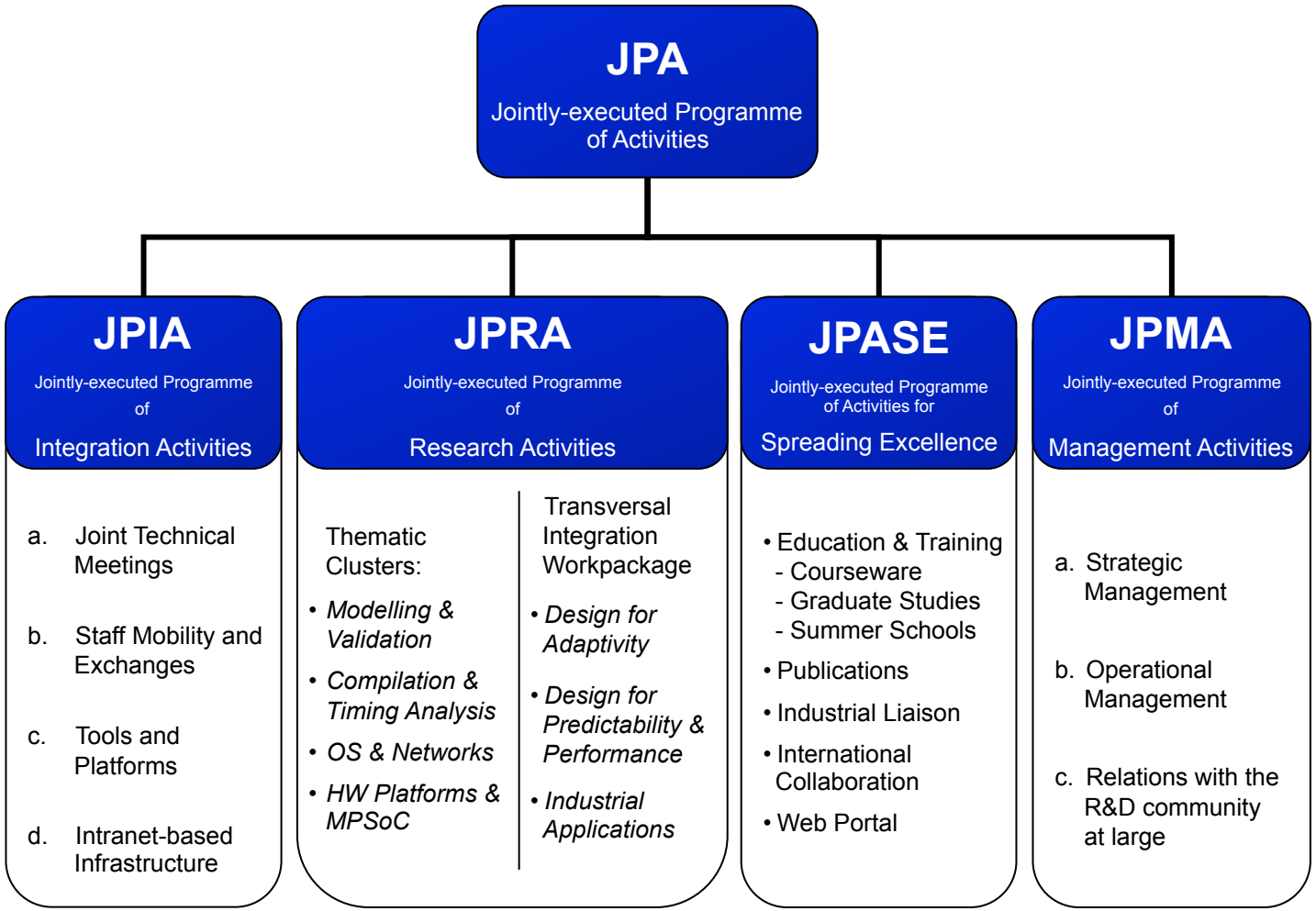


Jointly-executed Programme of Management Activities (JPMA)

In order to ensure correct integration and coordination of activities, and coordination between the partners, the Consortium carries out a Joint Programme of Management Activities (JPMA). It includes:

- **Strategic Management**
  The Strategic Management Board (SMB) plays a key role in ensuring ongoing integration at 3 levels: I) within the cluster; II) between clusters; III) with the larger European Embedded Systems Design community.

- **Operational Management**
  is ensured by the ArtistDesign Office, and the Executive Management Board (composed of the Cluster Leaders). The ArtistDesign Office ensures that all aspects of the NoE are running smoothly, and that progress is made towards the overall NoE objectives. It is composed of the Scientific Coordinator, the Technical Coordinator, the Financial and Administrative Coordinator from Floralis.

- **Relations with the R&D community at large**
  The NoE has a very strong presence within the embedded systems design community, at all levels. High-level interaction with the main institutions and bodies such as ARTEMIS/ ARTEMISIA, professional organisations such as ACM TECS, NSF, DARPA, large conferences, are ensured and supported by various members of the Strategic Management Board, and the Scientific and Technical Coordinators.

Jointly-executed Programme of Integrating Activities (JPIA)

•Each ArtistDesign research activity has work within both the JPIA and the JPRA workpackages. Funds for staff mobility are allocated by taking into account the needs for research.

- **Joint Technical Meetings**
  Present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

- **Staff Mobility and Exchanges**
  Mobility is justified by and refer to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

- **Tools and Platforms**
  Research platforms lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. Some of these have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

Joint Programme of Activities for Spreading Excellence (JPASE)

These NoE-level activities serve as a relay between the NoE and the international embedded systems design community at large.

- **Education and Training**
  These actions serve as incubators for developing integrated curricula and materials, and to disseminate results and spread excellence well beyond the partners and affiliated partners of ArtistDesign.

- **Publications in Conferences and Journals**
  Implemented through publication in the main conferences on Embedded Systems Design of the area, as well as the active participation for the organization and management of these events.

- **Industrial Liaison**
  This consists of actions oriented towards affiliated industrial partners, to transfer results follow and get feedback on the research and integration activities in the JPA (JPRA, JPIA).

- **International Collaboration**
  These activities play a dual role: showcase the participants' results, and reinforce the NoE's leadership role worldwide. They will also collect relevant information about evolution of the state of the art outside Europe.

- **Web Portal**
  This plays a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large, and be an essential mechanism for achieving integration and recognition.

Workpackages

WP0	Jointly-executed Programme of **Management** Activities (JPMA)	MGT	Floralis
WP1	Jointly-executed Programme of **Integration Activities** (JPIA)	RTD	VERIMAG
WP2	Joint Programme of Activities for **Spreading Excellence** (JPASE)	OTHER	VERIMAG
WP3	Thematic Cluster: **Modeling and Validation** (JPRA) • *Activity: Modelling* • *Activity: Validation*	RTD	Aalborg + VERIMAG
WP4	Thematic Cluster: **Software Synthesis, Code Generation and Timing Analysis** (JPRA) • *Activity: Software Synthesis, Code Generation* • *Activity: Timing Analysis*	RTD	Dortmund
WP5	Thematic Cluster: **Operating Systems and Networks** (JPRA) • *Activity: Resource-Aware OS* • *Activity: Scheduling & Resource Mgt* • *Activity: Embedded RT Networking*	RTD	Pisa
WP6	Thematic Cluster: **Hardware Platforms and MPSoC** (JPRA) • *Activity: Platform and MPSoC Design* • *Activity: Platform and MPSoC Analysis*	RTD	DTU
WP7	**Transversal Integration** (JPRA) • *Activity: Design for Adaptivity* • *Activity: Design for Predictability and Performance* • *Activity: Integration Driven by Industrial Applications*	RTD	~~PARADES~~ TRENTO

Thematic Cluster: Modeling and Validation

cluster leaders: Kim Larsen (Aalborg) + Susanne Graf (Verimag)

JPRA Activity: "Modeling"

Suzanne Graf (Verimag - France)

Develop model- and component-based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. Simultaneously address software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based.

JPRA Activity: "Validation"

Kim Larsen (Aalborg - Denmark)

Designing scalable techniques allowing for efficient and accurate analysis of performance and dependability issues with respect to the various types of (quantitative) models considered, covering a range of model-based validation techniques ranging from simulation, testing, model-checking, compositional techniques, refinement and abstract interpretation.

Thematic Cluster:

Software Synthesis, Code Generation and Timing Analysis

cluster leader:
Peter Marwedel (Dortmund)

JPRA Activity: "Software Synthesis, Code Generation "

Peter Marwedel (Dortmund - Germany)

Software generation has evolved to a level where compilers are key components, but not the only components that are useful for generating executable code. New models of computations such as data-flow based models aim at avoiding the well-known disadvantages of imperative programming styles. It can also be expected that the link between software engineering and embedded systems will become stronger.

JPRA Activity: "Timing Analysis"

Björn Lisper (Mälardalen - Sweden)

Timing analysis of MPSoC systems is a new scientific field, and is very timely from an application perspective as MPSoC and Multicore architectures rapidly are becoming mainstream. A research effort in this area will thus establish European dominance in a field that rapidly is becoming very important.

Thematic Cluster: # Operating Systems and Networks

cluster leader:
Giorgio Buttazzo (Pisa - Italy)

JPRA Activity: "Resource-Aware Operating Systems" *Giorgio Buttazzo (Pisa - Italy)*

Investigate how RTOS have to be extended or modified to support emerging RT embedded systems (high complexity, highly variable resource requirements and parallel processing). Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, while guaranteeing isolation properties.

JPRA Activity: "Scheduling and Resource Management" *Alan Burns (York - UK)*

Provision of models of embedded platform resources and policies, and the necessary analysis for undertaking the run-time scheduling of these resources and policies. A key scientific challenge is to link this resource-centred analysis with models of the application (and their resource usage policies) and the performance profiles of the hardware platform itself.

JPRA Activity: "Real-Time Networks" *Luis Almeida (U. Aveiro – Portugal)*

This activity addresses numerous research challenges in the frameworks of Networked Embedded Systems (NESs), Wireless Sensor Networks (WSNs) and Mobile Ad-hoc Networks (MANETs).

Thematic Cluster: # Hardware Platforms and MPSoC

cluster leader:
Jan Madsen (DTU - Denmark)

JPRA Activity: "Platform and MPSoC Design"

Luca Benini (U. Bologna - Italy)

The main scientific challenges addressed in this activity are focused on how to map complex applications onto multi-core hardware platforms. This includes addressing allocation and scheduling issues like: scalability, flexibility, composability, predictability, design-time reduction and increased dynamism. The problem is complex and multi-faceted. On one hand, we have static (design/compile time) approaches, where applications are analyzed and optimal mapping decisions are taken before the platform is deployed in the field. On the other hand, we have dynamic, runt-time approaches where mapping decisions are taken online, and they are triggered by environmental and workload variations.

JPRA Activity: "Platform and MPSoC Analysis"

Jan Madsen (DTU - Denmark)

Establish a set of models and analysis methods that scales to massively parallel and heterogeneous multiprocessor architectures, is applicable to distributed embedded systems as well, allows for the analysis of global predictability and efficiency system properties and takes the available hardware resources and the corresponding sharing strategies into account.

Transversal Integration

WP leader:
Alberto Sangiovanni (Trento - Italy)

JPRA Activity: "Design for Adaptivity"

Karl-Erik Årzén (Lund University – Sweden)

An embedded hardware-software system is adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is required both off-line at design-time and on-line at run-time. Off-line adaptivity is required to handle changing system specifications and to support platform-based or product-family based development.

JPRA Activity: "Design for Predictability and Performance"

Bengt Jonsson (Uppsala - Sweden)

The technical achievements contribute to a suite of techniques across the abstraction levels of embedded system design, including application modelling and analysis, scheduling support, compilers, and platform design techniques. The achievements will also entail interfacing of existing tools for design of embedded systems.

JPRA Activity: "Integration Driven by Industrial Applications"

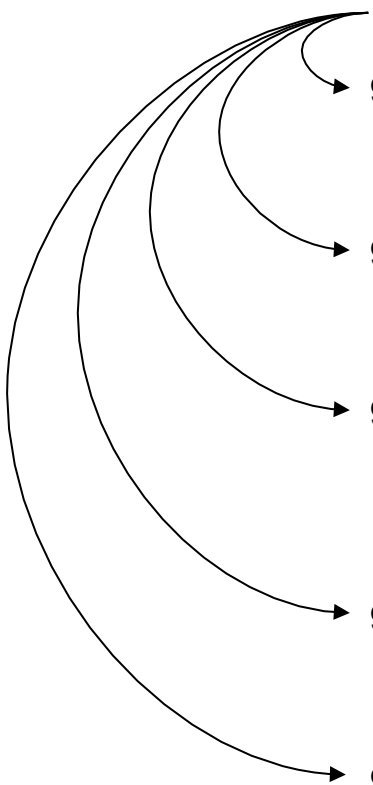
Alberto Sangiovanni (~~PARADES~~->Trento – Italy)

The ultimate goal of this activity is to provide the "meta rules" according to which the design transformations are carried out and interfaces are built and hence to provide strong guidance to the clusters to make their results more relevant and applicable.

Budget

7% **WP0: Jointly-executed Programme of Management Activities (JPMA)**

36% **WP1: Jointly-executed Programme of Integration Activities (JPIA)**
- 12% Transversal Integration
- 6% Each Thematic Cluster



12% **WP2: Joint Programme of Activities for Spreading Excellence (JPASE)**

9% **WP3: JPRA/Thematic Cluster: Modeling and Validation**
- Activity: Modelling
- Activity: Validation

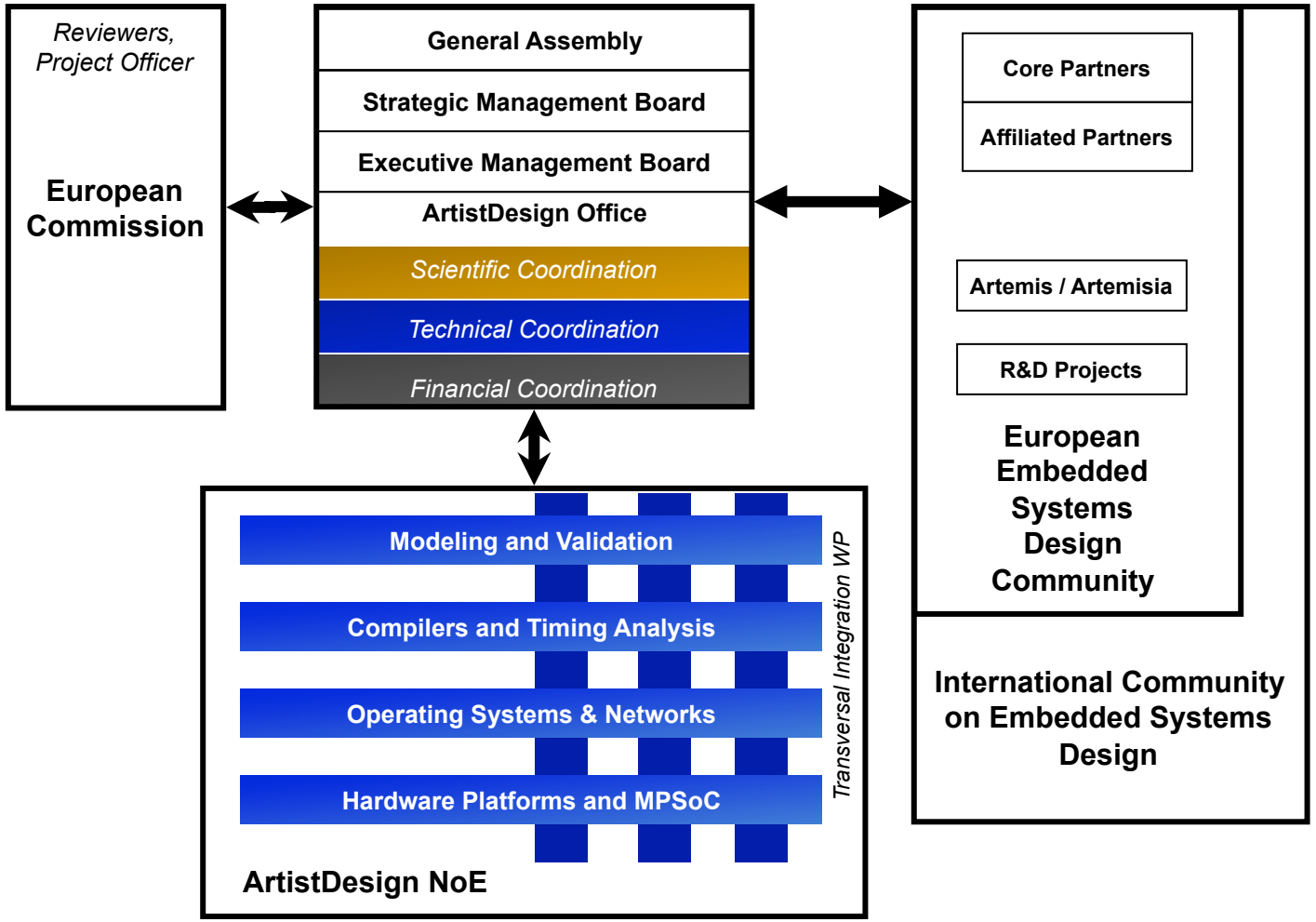
9% **WP4: JPRA/Thematic Cluster: Compilers and Timing Analysis**
- Activity: Software Synthesis and Code Generation for Embedded Systems
- Activity: Timing Analysis

9% **WP5: JPRA/Thematic Cluster: Operating Systems and Networks**
- Activity: Real-Time Operating Systems
- Activity: Scheduling and Resource Management
- Activity: Embedded Real-Time Networking

9% **WP6: JPRA/Thematic Cluster: Hardware Platforms and MPSoC**
- Activity: Execution Platform and MPSoC Analysis
- Activity: Platform and MPSoC Design

9% **WP7: Transversal Integration Activities**
- Activity: Design for Predictability
- Activity: Design for Adaptivity
- Industrial Integration

Management Structure



Summary of Main Achievements

Cluster: Modeling and Validation

(1/2)

Modeling

- foundations of a contract-based theory for components
  + theory for relational interfaces (compositional verification)
- development of modeling languages such as MARTE and Y-charts, application to non-trivial case studies.
- model-based design methodologies for:
  - flight control systems
  - complex systems ranging from automobiles, buildings, and airplanes,
  - multi-core systems.
- development of resource modelling techniques based on languages and models that explicitly represent different resource types, such as processors, memories and energy.
- study a sound semantic basis for quantitative modelling, including:
  - performance models
  - quantitative generalisation of classical languages
  - synthesis of optimal controllers from quantitative high-level specifications.

Cluster: Modeling and Validation

(2/2)

Validation

- compositional validation techniques:
  - compositional verification of deadlock freedom,
  - modular analysis for timed systems,
  - compositional safety analysis,
  - compositional verification of probabilistic systems.
- development of quantitative validation techniques, including:
  - analysis of energy-related properties of sensor-networks
  - verification of hybrid systems
  - study of multi-processor scheduling techniques and cache policies for ensuring timing predictability,
  - study of quantitative models and their associated verification techniques, such as timed automata, and stochastic automata,
  - verification of transactional memories, by model checking.
- development of techniques for cross-layer validation, such as:
  - control under partial observation,
  - adapting abstraction techniques to black-box analysis and learning,
  - test-case generation techniques, under partial observability.

Cluster: SW Synthesis, Code Gen and TA

Timing Analysis

- model identification and learning techniques for estimating WCET
- theory for ensuring timing predictability, and timing composability
- common annotation language for WCET analysis
- integration of Timing Analysis and Compilation
  => WCET-aware compilation
- integration of Timing Analysis and Schedulability

Software Synthesis and Code Generation

- techniques for mapping applications to MPSoCs, to meet a given set of non-functional properties
- code optimization techniques, taking into account WCET
- Techniques for verifying code generation methods

Cluster: Operating Systems and Networks (1/2)

Scheduling and Resource Management

- resource management, including:
  - development of a taxonomy of resource management as a wiki
  - memory resource management techniques
  - adaptive resource management
- scheduling, including:
  - hierarchical scheduling
  - scheduling and placement algorithms for multi-processor systems
  - multi-resource contract-based scheduling
  - data-flow scheduling, using constraint programming
- sporadic event-based control

Cluster: Operating Systems and Networks (2/2)

Real-Time Networks

- timeliness in wireless sensor networks,
- mobility issues in ad-hoc real-time wireless communication
- robust communication with star topologies,
- real-time support to middleware and composability,
- applications of wireless networks in industrial environments, in intelligent transportation systems, and in health applications.

Cluster: HW Platform and MPSoC Design (1/2)

Platform and MPSoC Design

- MPSoC design and programming
  - modelling concepts, methods and tools
    => cost-efficient applications mapping
  - run-time resource management techniques
  - architectures on chip communication, in future many-core processors
  - MPSoC mapping tools, for multi-media and wireless applications
  - MPSoC architecture exploration
- design of fault-tolerant distributed embedded systems
- resource-aware, system-level optimisation
  - power optimisation
  - performance optimisation in energy harvesting systems
  - optimisation-centric MPSoC design

Cluster: HW Platform and MPSoC Design (2/2)

Platform and MPSoC Analysis

- modelling and analysis techniques for performance evaluation
  - performance estimation of distributed real-time systems, for control applications
  - unifying approaches for hierarchical scheduling
  - modelling of shared resources in multi-processor systems
  - modelling and analysis of adaptive systems
  - contract-based architecture dimensioning
- timed automata and analytic performance evaluation techniques
- modelling and analysis of fault-tolerant distributed systems
- verification of design properties of hardware architectures

Transversal Integration: Design for Adaptivity

Design for Adaptivity

- analysis techniques for adaptive systems
  - dynamic changes in real-time parameters
  - assignment of real-time parameters to control tasks
  - timing analysis and sampling mechanisms, for event-driven control systems.
- adaptive design techniques
  - algorithms for QoS-aware, cooperative systems
  - adaptive topology management, to combine energy efficiency and QoS
  - in-system self-optimization for real-time systems
  - reconfigurable self-organizing and self-healing hardware platforms
  - adaptive energy management.
- modeling and analysis of adaptive systems,
- support for Adaptivity in distributed systems.

Design for Predictability and Performance (1/2)

Intersection with: **Modeling and Validation of component –based systems**

- continued the study of predictability in relation with robustness
- identified two major challenges in embedded systems design
  => rethinking the conventional, purely discrete + functional foundation of computing
- worked on methodologies for designing component-based systems, participated in the standardisation of the MARTE-UML profile

Intersection with: **Timing Analysis and Compiler Techniques**

- relations between Timing Analysis and Timing Predictability
  - identified heuristics to derive operating mode candidates from source code
  - procedure to exploit mode information to arrive at mode-specific WCET bounds
  - started to explore strategies for eliminating timing anomalies
- investigated WCET analysis techniques in the presence of context switches
- integrated Timing Analysis and Compilation techniques for optimizing code generation.

Design for Predictability and Performance (2/2)

Intersection with: **OS / MW / Networks**

- integrating scheduling analysis techniques + model checking
- partitioning shared caches on multi-core processors for timing predictability
  - developed a sufficient schedulability test for non-preemptive fixed priority scheduling for multi-cores, with shared L2 cache, encoded as a linear programming problem
  - compared several scheduling models for multi-processor systems

Intersection with: **Architecture and System Design**

- predictability for fault-tolerant embedded systems
- studied techniques allowing predictability for multi-processor MPSoC architectures
  => developed power prediction algorithms for an energy harvester.
- developed a new bus model for MPSoC system bus analysis and optimisation.
- developed the Precision Timed (PRET) language,
  => allows determinism and time predictability

Transversal Integration:

Industrial Integration

Industrial *interactions* and *collaborations* with ArtistDesign teams.

- long-term goal is to understand industrial design methodologies
- identify the research results that could be applied in these methodologies
- The work this year has consisted in :
  - organising a few high-profile meetings with industry (eg: SEEC ’09, WESH ‘09,) as well as joint workshops and technical meetings. SEEC in particular was extremely successful, with a high international visibility far beyond European borders.
  - a wide array of collaborations with industrial partners and ArtistDesign partners, including general frameworks for system-level design, automotive applications, applications for chip design, smart energy-efficient buildings, and wireless communication.

Spreading Excellence

ARTIST Summer School in Europe 2009 - 5th edition

- high quality technical programme, excellent feedback from participants
- 85 participants (out of 150 applicants) and 16 invited speakers.

International ARTIST Summer School in China 2009 – 4th edition

International ARTIST Summer School in South America 2009 – 3rd edition

New international summer school in Rabat, Morocco

Graduate Schools:

- ARTIST Graduate Course: Automated Formal Methods for Embedded Systems
- ARTIST Graduate Course on Embedded Control Systems
- New ARTIST Graduate school on Quantitative Model Checking in 2010

Conferences support for CPS Week, ES Week, FORMATS, MEMOCODE, DATE (including a booth)

Embedded Systems Seminar for the Embedded Systems Unit in June 2009

ARTIST Workshops

UML&FM, WESH , CRTS , WSS'09 ,WESE'09 , RePP , WFCD , APRES', SEEC'09 , IRTAW-14 , ACESMB ,VVPS ,WCET , OSPERT , Mapping Applications to MPSoCs , Runtime Verification, DySCAS

ARTIST web portal

Changes to the DoW

Changes to the DoW

- PARADES switched to Trento
- Aveiro switched to University of Porto
- EPFL team moved to IST Austria
  - *but EPFL retained : Giovanni De Micheli*
  - *leadership for the Modelling activity switched to Susanne Graf (Verimag)*
- Ed Brinksma (Embedded Systems Institute)
  replaced by Boudewijn Haverkort :
  organised WESH 2009 *(ArtistDesign WS on Embedded Systems in Healthcare)*
- Budget updated to reflect :
  - *Changes above*
  - *Distribution of funds for events organised in WP2: Spreading Excellence*

To be completed

Deliverables

Deliverables (1/2)

WP0: Joint Programme of Management Activities (JPMA)

Floralis	D1-(0.1)-Y2	**Periodic Report**
	D2-(0.2)-Y2	Project Activity Report
UJF/Verimag	D2-(0.2a)-Y2	*ch. 1* - **Executive Summary and Overview**
Aalborg	D2-(0.2b)-Y2	*ch. 2* - **Modelling and Validation**
Dortmund	D2-(0.2c)-Y2	*ch. 3* - **SW Synthesis, Code Generation and Timing Analysis**
Pisa	D2-(0.2d)-Y2	*ch. 4* - **Operating Systems and Networks**
DTU	D2-(0.2e)-Y2	*ch. 5* - **Hardware Platforms and MPSoC Design**

WP1: Joint Programme of Integration Activities (JPIA)

UJF/Verimag	D3-(1.0)-Y2	**Integration Activities Report**

WP2: Joint Programme of Activities for Spreading Excellence (JPASE)

UJF/Verimag	D4-(2.0)-Y2	**Spreading Excellence Report**

WP3: Modeling and Validation (JPRA)

UJF/Verimag	D5-(3.1)-Y2	**Modelling**
Aalborg	D6-(3.2)-Y2	**Validation**

Deliverables (2/2)

WP4: Software Synthesis, Code Generation and Timing Analysis (JPRA)

Dortmund	D7-(4.1)-Y2	**Software Synthesis, Code Generation**
Saarland	D8-(4.2)-Y2	**Timing Analysis**

WP5: Operating Systems and Networks (JPRA)

Pisa	D9-(5.1)-Y2	**Resource-aware Operating Systems**
York	D10-(5.2)-Y2	**Scheduling and Resource Management**
UnivPorto	D11-(5.3)-Y2	**Embedded Real-Time Networking**

WP6: Hardware Platforms and MPSoC (JPRA)

Bologna	D12-(6.1)-Y2	**Platform and MPSoC Design**
DTU	D13-(6.2)-Y2	**Platform and MPSoC Analysis**

WP7: Transversal Integration (JPRA)

Lund	D14-(7.1)-Y2	**Design for Adaptivity**
Uppsala	D15-(7.2)-Y2	**Design for Predictability**
Trento	D16-(7.3)-Y2	**Integration Driven by Industrial Applications**

THANK YOU