Year 2 Review
Brussels, February 12th, 2010

Cluster

Achievements and Perspectives :

Software Synthesis, Code Generation and Timing Analysis

leader : Peter Marwedel

TU Dortmund, Germany

High-Level Objectives

- Limitations of increasing clock speeds any further
  ☞ focus on using MP platforms, in particular MPSoCs
  (increased importance since the proposal writing)
- Different from multi-core situation: Multiple applications, heterogeneous processors, and multiple objectives
- MP platforms pose threats to timing predictability;
  - make MPSoC architects aware of hazards; develop MP/MPSoC design principles for maximal predictability
  - develop models/methods for timing analysis of parallel software
- Efficient design + software synthesis also in the scope
  (see deliverables; coordination with other projects)
- Partners contribution to transversal clusters
  (e.g. for predictability: WCC)

State of the Integration in Europe

- Mapping to MP platforms generally seen as one of the largest challenges of current and future technology
- Interaction with Execution Platform Cluster
- Incorporating work from outside the cluster:
  - DAEDALUS (Leiden), SystemCoDesigner (Erlangen), HOPES (Seoul),
  - hipeac, CoreGrid, KDUbiq, … NoEs,
  - Predator, Mnemee, EmBounded, … projects
  - Companies (AbsInt, ACE, CoWare, ICD, Infineon, NXP, Rapita, ST)
- Goal: Contributions to state of the art in multi-core based design
- Aiming at providing a focused forum for comparing approaches, and for coping with the challenge

Building Excellence

- NoE provides the required size of research teams, necessary to handle the complexity of technology.
- Rheinfels workshop, St. Goar, June 2009
  Incorporating external experts
- TA meetings
- Tutorials, summer schools, teaching at ALARI,
- WESE, Software Synthesis Workshop (NEW!), …

Overall Assessment and Vision at Y0+2

What went well:

- Abundant amount of results on resource-efficiency
- Results from mapping tools
- Extension of well-visible workshop
- Agreement to cooperate on benchmarks
- While ArtistDesign partners acted as a core, the involvement of researchers went far beyond ArtistDesign

Challenge:

- Do timing analysis concerns affect MPSoC architectures?

2nd Rheinfels Workshop on Mapping of Applications to MPSoCs

- June 29-30, 2009

Highlights

- Reaching out beyond Europe:
  - T. Simunic (UCSD),
  - Soonhoi Ha (Seoul National University),
  - Qiang Xu (Chinese University of Hong Kong)
- 1st Session on Benchmarks
- Increased attendance for Software Synthesis & Code Generation activity
- Difference between approaches is now better understood
- Call for special issue of IEEE “Industrial Informatics“ aiming at journal versions of presentations is out.

Integration at TU Dortmund

- ERIKA operating system from Pisa ported to TriCore
  This enables its use in research on timing predictability.
- Cooperation with AbsInt/USaar on the integration of the aiT timing analyzer into Dortmund‘s worst case execution time aware compiler WCC continued,
  now the focus is on results.
- MPARM from Bologna integrated into MACC tools and used.
- DOL-tools from ETH extended by memory aware mapping.
- New R^2G (RTEMS and RTLib Glued together) links RTEMS with IMEC‘s RTLib; placed in public domain.

Integration at Aachen

- Design of a high-level virtual platform MVP for MAPS
- MAPS design in cooperation with ACE, using CoSy.
- Cooperation with Edinburgh on Code Optimization
- Contribution to education at ALARI
- Continuing cooperation with Bologna and Dortmund

IMEC

NTUA (ICCS)
DDTR + DMM tools

↔

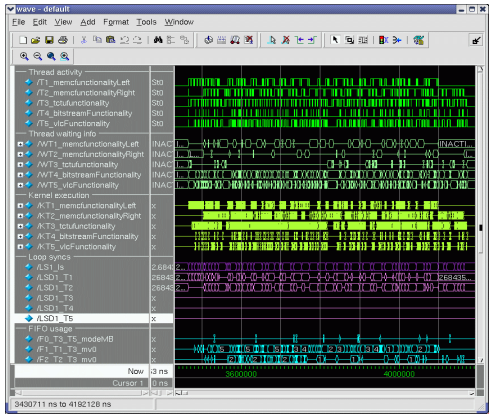
IMEC
MPA + MH tools

↔

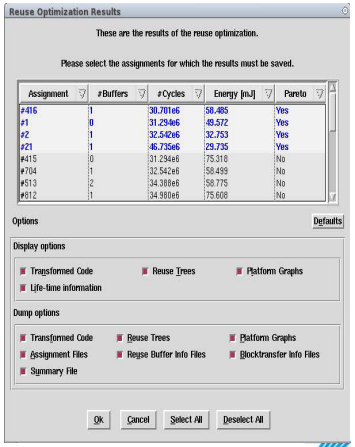
TU Dortmund / ICD
MACC + R²G

- **IMEC** provides the prototype versions of MPSoC Parallelization Assistant (MPA) and Memory Hierarchy (MH) tools.
- **IMEC** did the integration as a single MP-MH tool.
- **NTUA (ICCS)** is integrating the dynamic data type and dynamic memory management tools and design flows with the IMEC MPSoC mapping tool flows.
- **TU Dortmund/ICD** is integrating its pre-pass-compiler and compiler framework to the static MH tool of IMEC.

MPA tool



MH tool



*In collaboration with MNEMEE FP7

Integration at Passau

- Connection of loop parallelizer LooPo and Dortmund's ICD-C compiler:
- Extending IMEC's and Dortmund's work on scratchpads and applying it to GPUs:
  Precise determination of which values to load into the scratchpad and when to copy values back to main memory for loop programs with affine loop bounds and array indices [CC 2009, Dissertation Größlinger 2009].
- Parallelization using the polyhedron model
- Feature-oriented development of software product lines
  Proposal for a German (DFG) Research Priority Programme "Manycore":
  The programme would be for six years of national research on making manycores better programmable, starting in 2011.

Workshop on Software Synthesis (WSS)

- Joint organization with industrial activity @ ESWEEK
- Discussion on software synthesis started
- Slides from 2 companies (Mathworks, dSPACE)
- Need to pay increased attention to synthesis from model in academic emphasized.
- Slides and results of discussion on-line
- Call for special issue of IEEE “Industrial Informatics“ aiming at journal versions of presentations is out (in cooperation with MPSoC workshop).
- Follow-up workshop scheduled for 2010

Workshop on Embedded System Education (WESE)

- Mainly organized by this cluster
- Excellent keynote (Edward Lee, Berkeley)
- Focused morning: different approaches for ES education
- Focused afternoon: special courses
- Improved visibility by publication through ACM digital library
- Target: Keep improved visibility for WESE'10 (Scottsdale)
- Complements preparation of the second edition of the textbook "Embedded System Design" by P. Marwedel

Plans for Y3

- Extending cooperation
- Working Meeting: DATE 2010
- 3rd Workshop on Mapping of Applications to MPSoCs
  - To be held June 29-30, 2010, at Rheinfels Castle
  - Information: http://www.artist-embedded.org/artist/-map2mpsoc-2010-.html
  - Followed by Mnemee & Madness meetings
- WESE 2010
- WSS 2010

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Achievements and Perspectives :

Timing Analysis

Activity leader: Björn Lisper

Mälardalen University

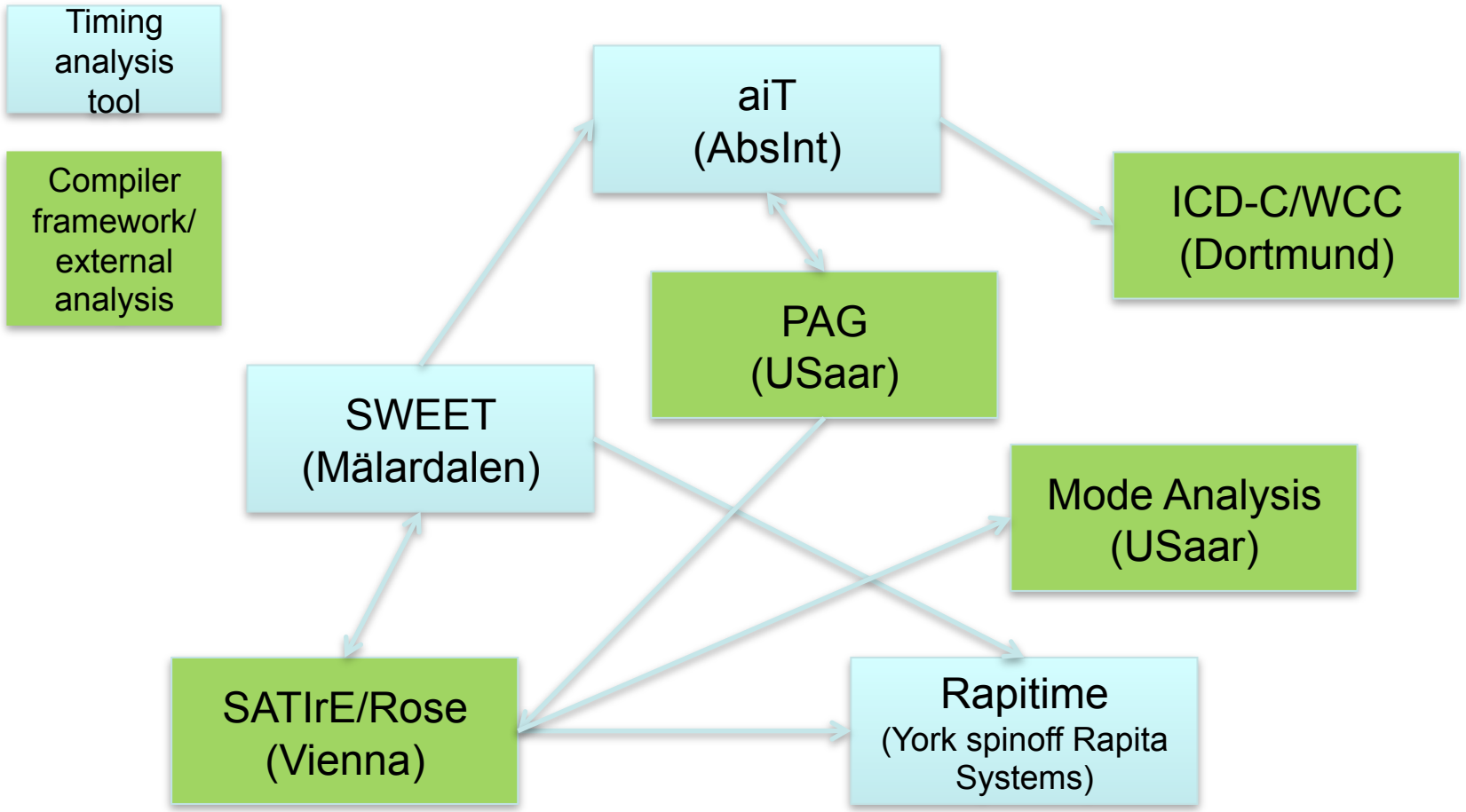
High-Level Objectives

- Timing analysis of MPSoC/Multicore systems
- Novel area, initiate research
- Implications for system design
  - Software
  - Hardware
- Influence how MPSoC/Multicore systems are built for time-critical applications

State of the Integration in Europe

- ArtistDesign integration extends heritage from ARTIST2
- Some joint projects:
  - ALL-TIMES (FP7 STREP)
  - PREDATOR (FP7 STREP)
  - TIMMO-2-USE (ITEA2, starting 2010, TA partners participating)
- Extensive tool integration (see next slide)

Timing Analysis Tool Integration Map



Building Excellence

- WCET Workshop, main TA community event
  - Keynote speech by Petru Eles, HW/MPSoC Design Cluster
- RePP Workshop, cross-cluster organization
- Two joint technical meetings with the HW/ MPSoC Design Cluster:
  - At DATE, April -09
  - At ESWEEK, Oct -09

Selected Technical Achievements Y2

Three strands:

- Design principles for timing-predictable parallel architectures
  - Timing composability
- Static analysis for timing predictability
  - context switches, microarchitectural analysis, analysis of shared caches
- Pragmatic (unsafe) timing analysis
  - machine learning, model identification, test-case generation

Plans for Y3

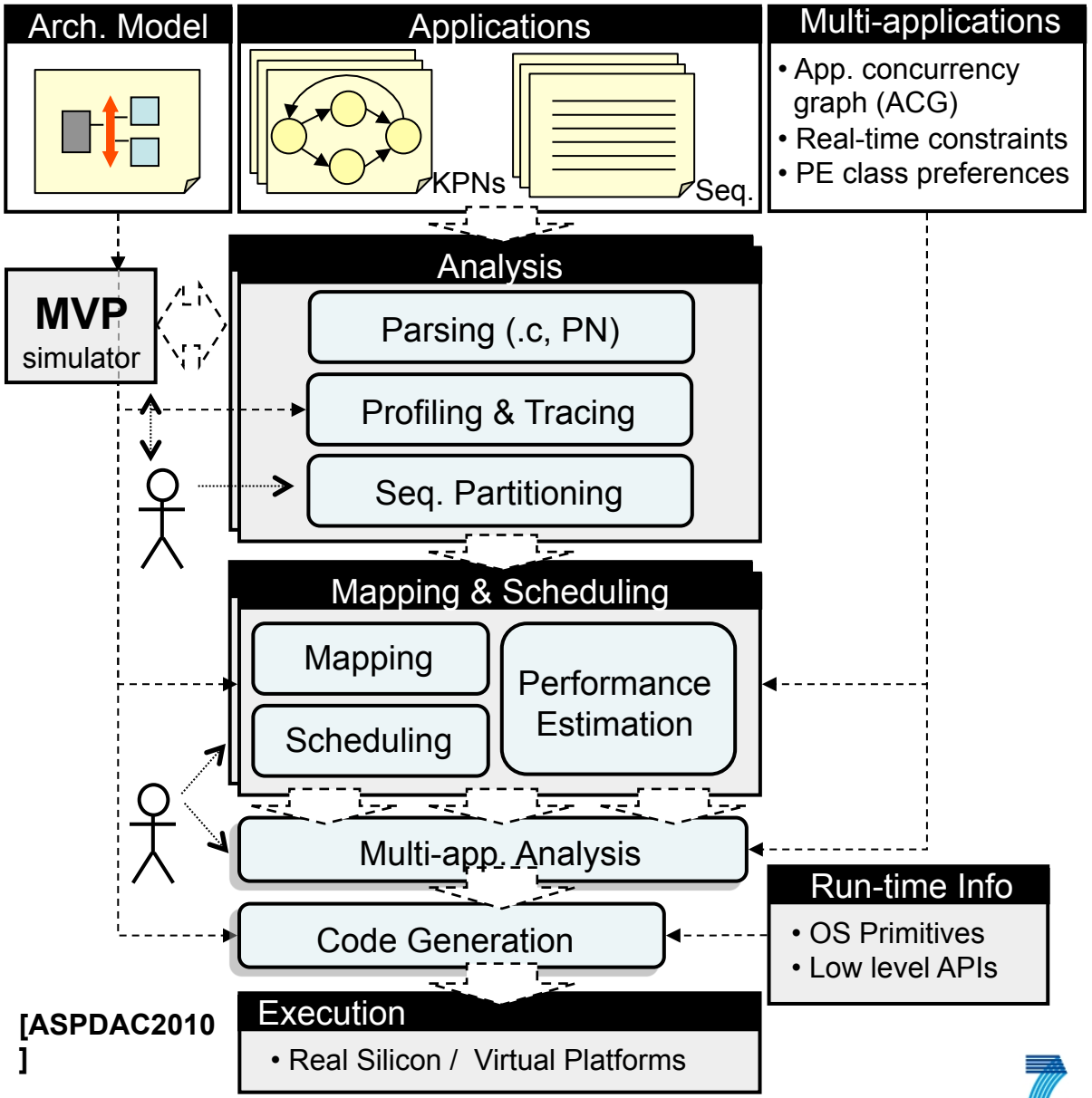
- Timing analysis of shared resources in multi-cores
- Design of predictable multi-core architecture
- Extending timing-composable designs to systems with hierarchical memory architectures
- Improved test-case generation
- WCET Workshop 2010
- Special issue of Journal of Systems Architecture on WCET analysis
- Special issue of Real-Time Systems on predictability vs. performance

Additional information

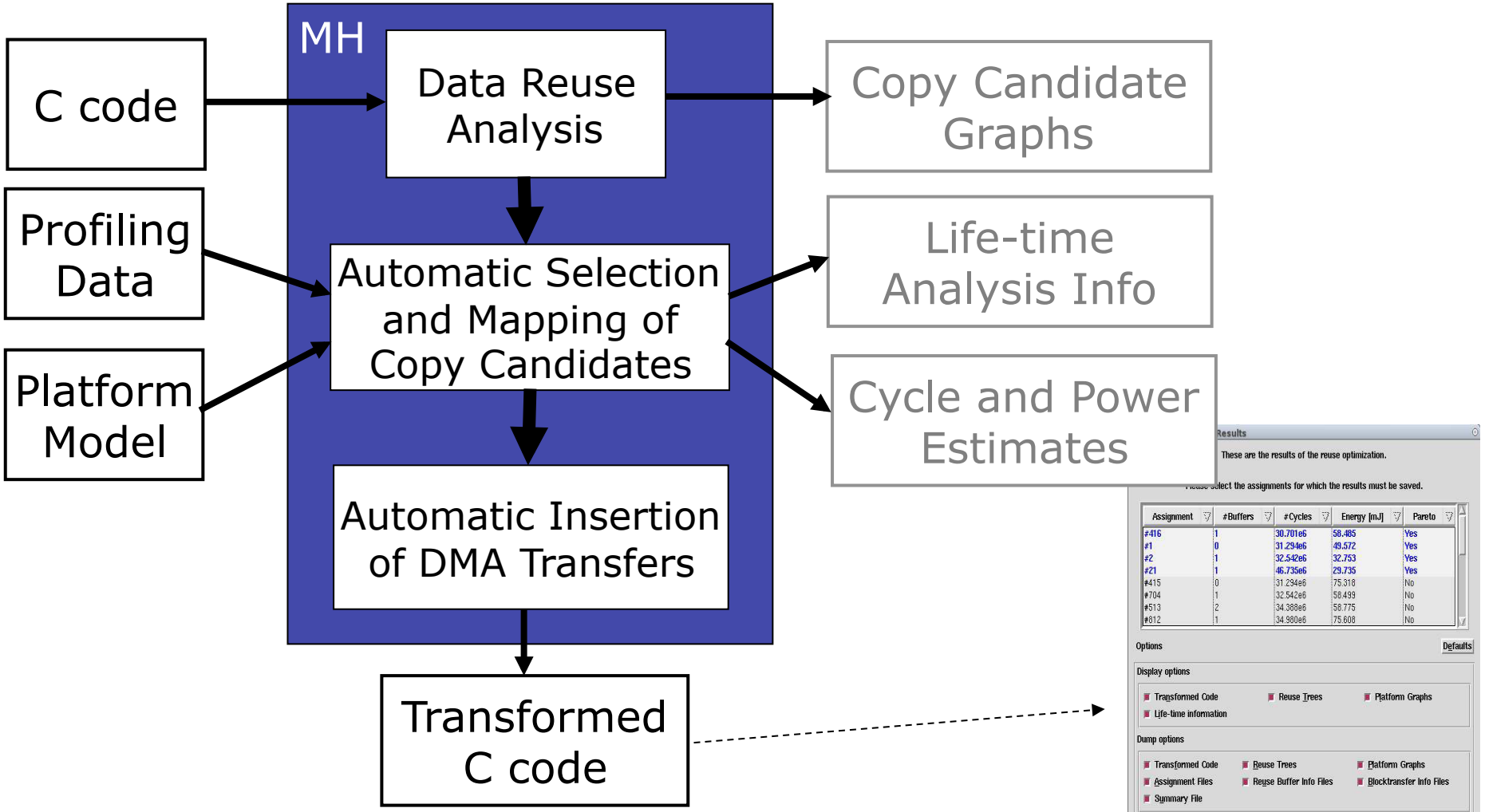
Specific information about work performed at the different sites

MAPS Project @ RWTH Aachen

- MVP
  - [CODES+ISSS 2009]
  - [MCC09]
- Multi-KPN Composability Analysis
  - [DATE2010]
- Run-time task management
  - [ICCAD2009]
- Work-in-progress
  - C-extension for Process Networks Applications



Scientific Highlights – Memory Hierarchy (MH)*



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University of Edinburgh

- Extraction of Parallelism from Sequential Codes
  - Hybrid static analyses and profiling
  - Hierarchical levels of parallelism
- Mapping of Parallel Applications
  - Retargetable mapping approach
  - Use of machine learning to derive new mapping strategies for new platforms
  - Combined deterministic and speculative execution models
- High Performance
  - Within 5% of performance levels of manually parallelised codes

Compiler Verification & Optimization at TU Berlin

(Sabine Glesner, Lars Alvincz, Elke Salecker)

- **Research goal:**
  investigate compiler verification and optimization in a unified setting
- **Results on the verification side:**
  - continued work on the formalization of the semantics of intermediate representation, Intel Itanium assembler and transformation between both,
    within the Isabelle/HOL theorem prover
  - special focus on number representations and BEG code generation rules
- **Results on the optimization side:**
  - complete compiler for the Intel Itanium
  - optimizations for memory accesses by machine learning
- **Interconnection between verification and optimization:**
  - detected an error in the Itanium code generation specification, which resulted due to a copy & paste bug