

Year 2 Review  
Brussels, February 12th, 2010

*Cluster*

*Achievements and Perspectives :*

# Hardware Platforms and MPSoC Design

leader : Jan Madsen

Technical University of Denmark (DTU)

## Cluster Participants

- **Jan Madsen** (DTU – Denmark)
- **Luca Benini** (UNIBO – Italy)
- Lothar Thiele (ETHZ – Switzerland)
- Rolf Ernst (TUBS – Germany)
- Petru Eles (LiU – Sweden)
- Stylianos Mamagkakis (IMEC – Belgium)
- Axel Jantsch (KTH – Sweden)
- **Raphaël David** (CEA/LIST – France)
- **Giovanni de Micheli** (EPFL – Switzerland)
- Volvo –Sweden
- SymTAVision – Germany
- Robert Bosch – Germany
- Intel – Germany
- Prevas – Denmark
- Bang & Olufsen ICEpower – Denmark
- Telecom Italia Lab – Italy
- NTUA – Greece
- EPFL – Switzerland
- NTNU - Norway
- Duke University - USA
- Virginia Tech - USA

# High-Level Objectives

- Focus on **Design** and **Analysis**
- Hardware architecture and software components in their **interaction**
- Tools for accurate estimation
- Growing importance of **resource awareness** in embedded systems
- Design methodology
  - Scales to **massively parallel** and **heterogeneous** multiprocessor architectures
  - Allows for **predictable** system properties
  - Uses the available hardware **resources** in an efficient manner
- **Adaptivity**
  - Robustness
  - Life-time management
  - Resilience

## State of the Integration in Europe

- Distributed, communication-centric embedded systems
  - Multi- and Many-core System-on-Chip (MPSoC)
  - Networked embedded systems
  - Emerging platform technologies
- Hardware platforms for embedded applications will continue to be multi-core
- Programming models, design-time and run-time application environments are less clear
- Growing maturity of scalable performance analysis algorithms and tools
- New challenges, platform robustness and adaptivity

# State of the Integration in Europe

- National
  - Influencing curriculum for Embedded Systems
  - Networks on Embedded Systems bringing industry and academia together
    - InfinIT, DaNES, ...
- European
  - Strengthen long-term research through FP7 projects
    - COMBEST, COMPOSE, PREDATOR, PRO3D, EURETILE, ...
  - Strengthen short-term research through ARTEMIS JU projects
    - SYSMODEL, RECOMP, SMECY, ASAM, SCALOPE, ...
- World
  - Collaboration with US, Asia and South America
    - Research
    - Graduate education: Summer school in China

# Building Excellence

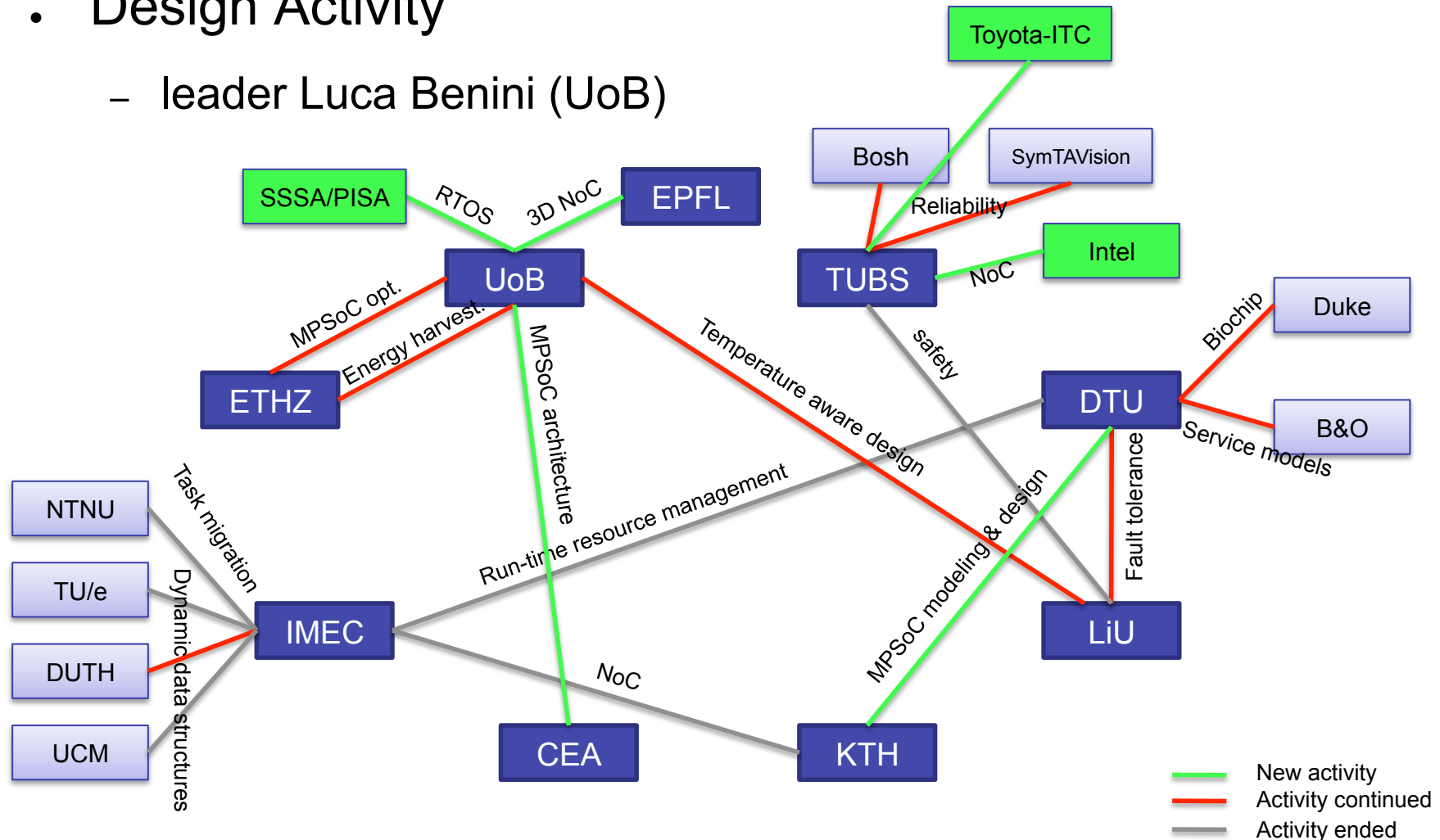
- High interaction among partners in the cluster
  - “new” partners fully integrated
- Increased interaction with other ArtistDesign partners
- Joint publications in 2009
  - 25 out of 77
- Strong impact on international conferences
  - DATE, CODES+ISSS, EMSOFT, CASES, ASP-DAC, MPSoC, ...
- Joint organization of workshops, tutorials, and special sessions

# Building Excellence

- Joint participation in European projects
- ARTEMIS JU:
  - **RECOMP** [DTU, TUBS, AAU, ...]
  - **SMECY** [CEA, TUBS, DTU, VERIMAG, ...]
  - **ASAM** [DTU, TUBS, ...]
  - SYSMODEL [DTU, KTH, ...]
  - SCALOPES [IMEC, UoB, CEA, ...]
- FP7:
  - PREDATOR [ETHZ, UoB, SSSA, Saarland, Dortmund, ...]
  - COMBEST [ETHZ, TUBS, VERIMAG, OFFIS, ...]
  - **PRO3D** [ETHZ, EPFL, VERIMAG, UoB, CEA, ...]
  - **EURETILE** [ETHZ, Aachen, ...]

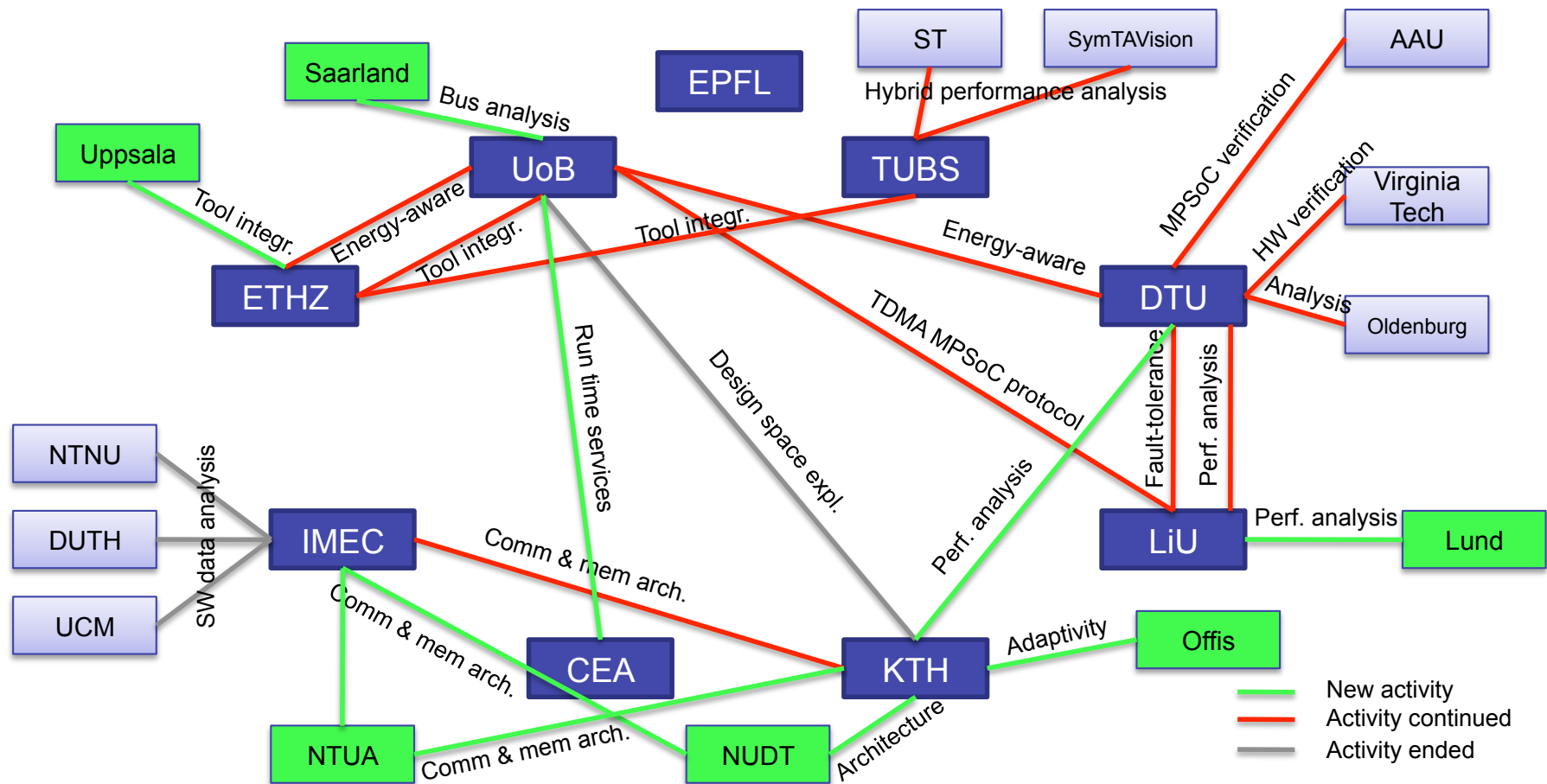
# Building Excellence

- Design Activity
  - leader Luca Benini (UoB)



# Building Excellence

- Analysis Activity
  - leader Jan Madsen (DTU)



# Building Excellence

## Tools:

- SymTA/S [TUBS, Symtavision, ETHZ, AbsInt]
- Analysis and optimisation framework for fault tolerant distributed embedded systems [LiU, DTU]
- MPA + MH MPSoC [IMEC, KTH, DUTH, Tue, TU Dortmund]
- MoVES [DTU, AAU]
- MPA [ETHZ, TUBS]
- DOL [ETHZ, UoB]

# Building Excellence

MPSoC cluster got all 3 **best paper awards** at ESWeek 2009

- EMSOFT best paper award 2009
  - Kai Lampka, Simon Perathoner, **Lothar Thiele**: Analytic Real-Time Analysis and Timed Automata: A **Hybrid Method for Analyzing** Embedded Real-Time Systems In the 8th ACM & IEEE International conference on Embedded software, EMSOFT 2009, Grenoble, France, October, 2009, pp. 107-116.
- CODES+ISSS best paper award 2009
  - Alireza Ejlali, Bashir Al-Hashimi, **Petru Eles**: A Standby-Spacing Technique with **Low Energy-Overhead for Fault-Tolerant** Hard Real-Time Systems. In Proceedings of the International Conference on Hardware-Software Co-Design and System Synthesis (CODES +ISSS), Grenoble, France, October 11-16, 2009, pp. 193-202.
- CASES best paper award 2009
  - Elena Maftai, Paul Pop, **Jan Madsen**: Tabu Search-Based Synthesis of **Dynamically Reconfigurable Digital Microfluidic Biochips**, in Proceedings of the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, Grenoble, France, October, 2009, pp. 195-204.

## Overall Assessment and Vision at Y0+2

- Strong research collaboration within cluster
  - 25 joint publications, 3 best paper awards at ESWeek 2009
  - 6 tools (3 added in 2009)
- Increased research collaboration with other clusters
- Joint participation in many European projects
  - FP7, ARTEMIS, ...
- Explored approaches for upcoming embedded systems
  - to increase predictability and adaptability for multi-core platforms
  - energy-aware embedded systems
  - fault-tolerance in distributed embedded systems
  - Programming models for multi- and many-core platforms
  - new technologies – e.g. biochips, 3D NoC

# Scientific Highlights

1. Multiprocessor systems with **shared resources**
2. **Hybrid** approach to performance analysis
3. **Fault tolerance** optimization with hardened processors
4. **Energy harvesting**
5. Scalable and predictable **3D platforms**

# Methods and Tools for MPSoC

$$R_i = C_i + \sum_{j \in hp(i)} \eta_j(R_i) \cdot C_j + S(R_i)$$

Related projects  
(Artist2, Combest, ...)

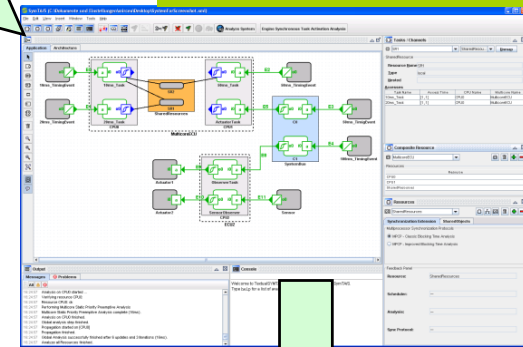
**ArtistDesign  
Universities**

TUBS  
ETHZ  
Linköping  
DTU  
...

Research on  
Multiprocessor  
Performance  
Analysis

**Formal Methods**

**Tool support**

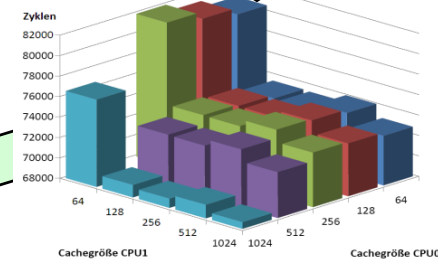


**Industry**  
Symtavision  
GM  
Bosch  
EADS  
...

- Use-cases
- architecture constraints

Tool support enables:

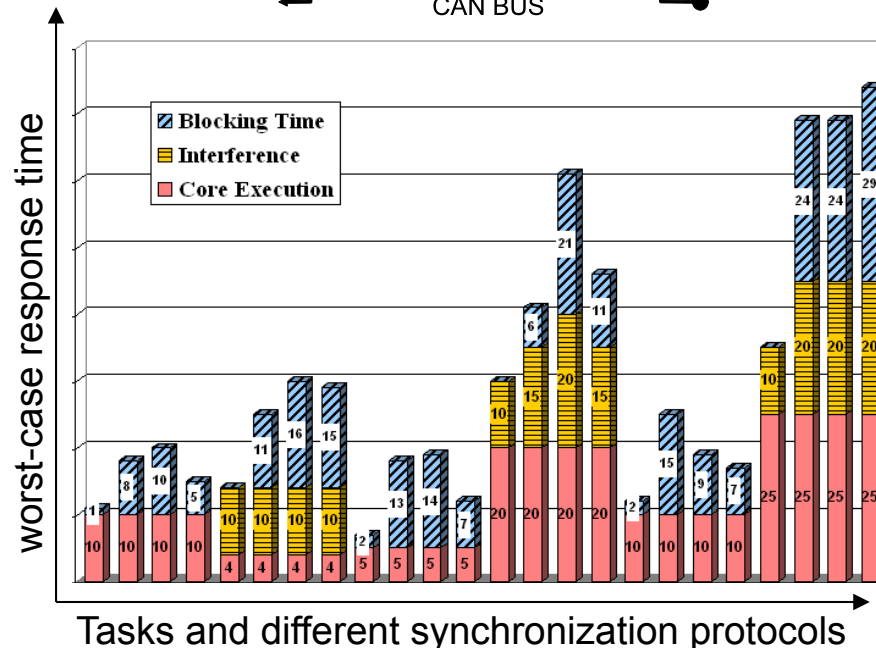
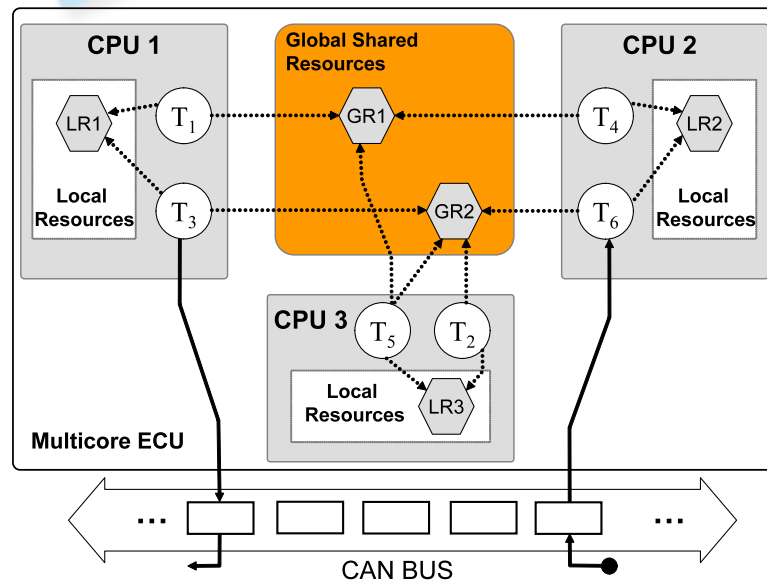
- Architecture evaluation
- Support for protocol standardization (e.g. AutoSar)
- Identification of research directions



Quantitative / Qualitative  
Evaluation of architecture options

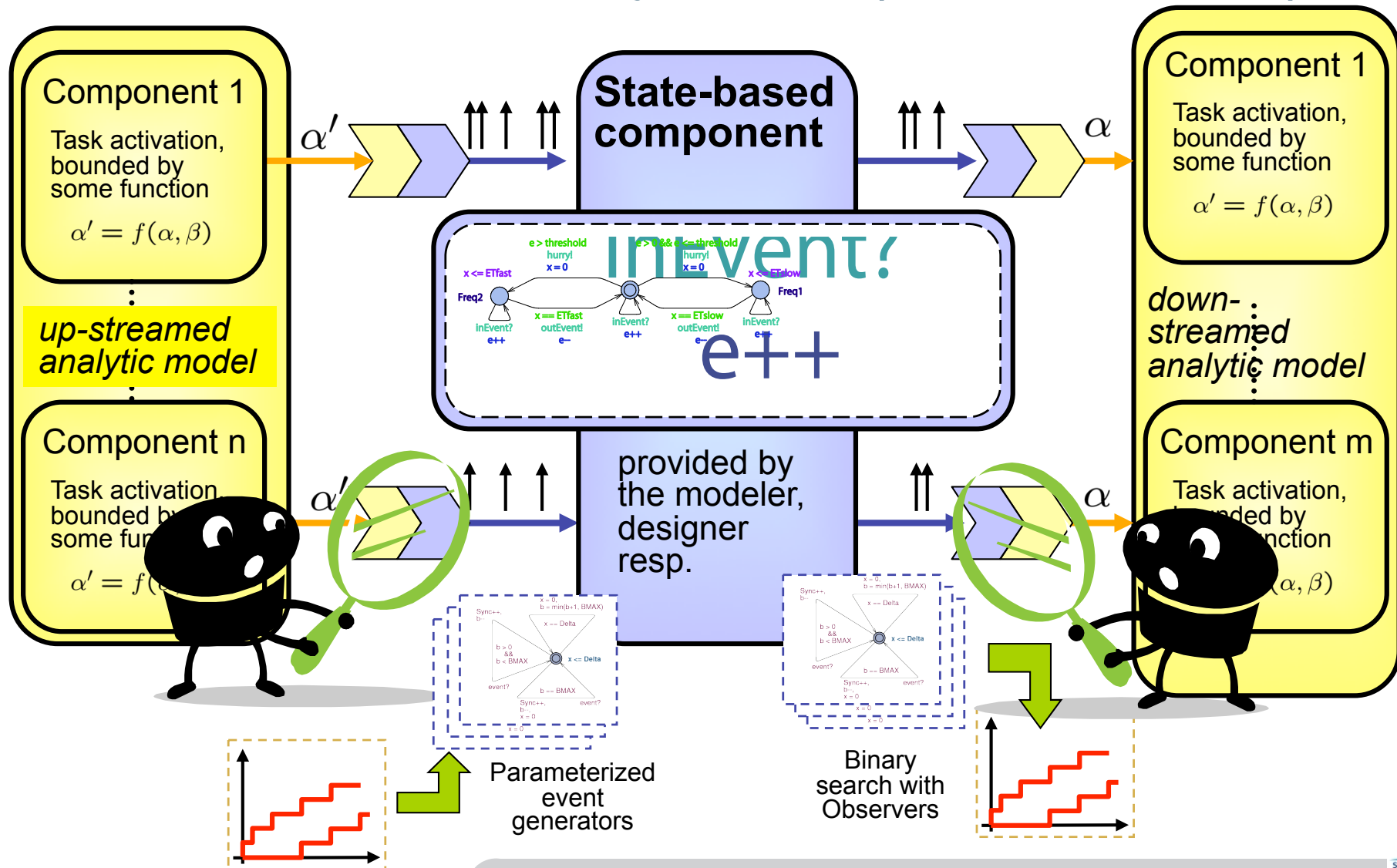


# Exploration of Different Synchronization Strategies

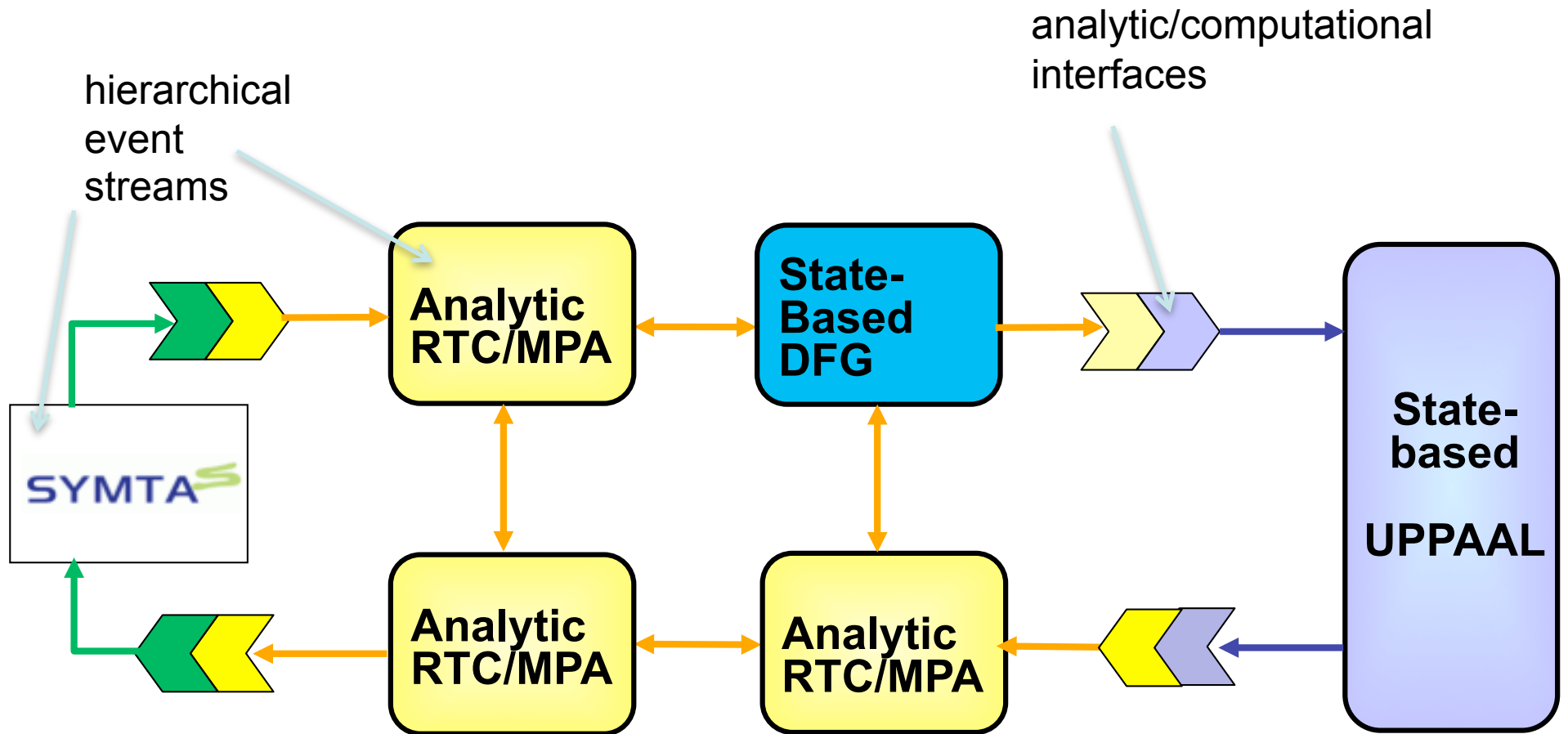


- Use Case: Automotive industry moving towards multicore (drivers of use case in ArtistDesign: Bosch, GM)
  - Increased performance
  - Functional clustering (reduce number of ECUs)
  - Reliability
- Challenge: Tasks on different cores share resources (such as data or coprocessors)
  - inter-core timing dependencies previously unknown in automotive development
- Solution: use deterministic strategy to arbitrate shared resources
  - explore different synchronization strategies + formal analysis
  - Q1: how to arbitrate shared resources?
  - Q2: how to treat blocked task locally?

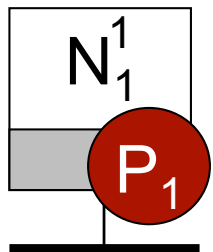
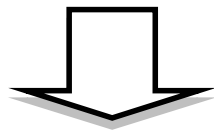
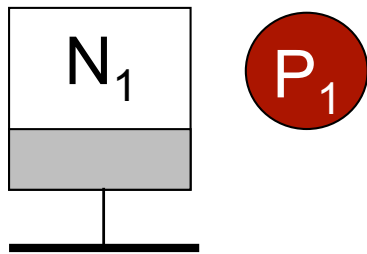
# Hybrid approach to performance evaluation of embedded RT-systems (TUBS, ETHZ)



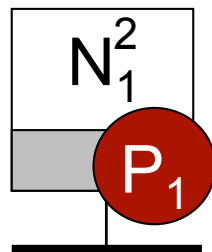
# Global Picture



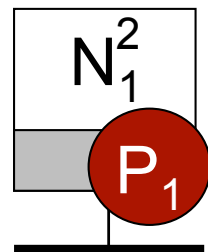
# Fault tolerance optimization with harden processors (LiU, DTU)



Cost=10



Cost=20

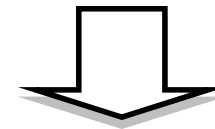


Cost=40

**Several hardening versions:**

Increase in reliability /

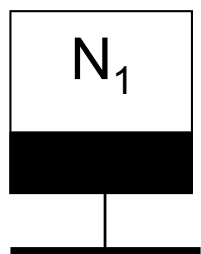
Decrease in process failure probabilities



Increased execution time of processes

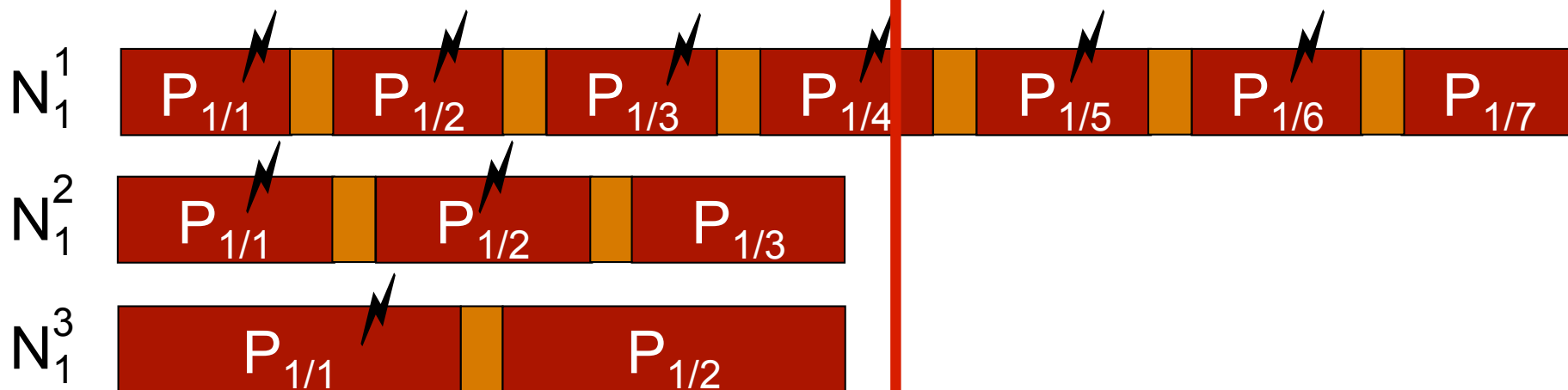
**Increased hardware cost**

# Application Example



$\rho = 1 - 10^{-5}$   
 $\mu = 20 \text{ ms}$   
 $D = 360 \text{ ms}$

$N_1$	$h = 1$		$h = 2$		$h = 3$	
	t	p	t	p	t	p
$P_1$	80	$4 \cdot 10^{-2}$	100	$4 \cdot 10^{-4}$	160	$4 \cdot 10^{-6}$
Cost	10		20		40	



# Selected Experimental Results

**MAX** – hardening-only optimization

**MIN** – software-level-only optimization

**OPT** – combined architecture

## Accepted architecture:

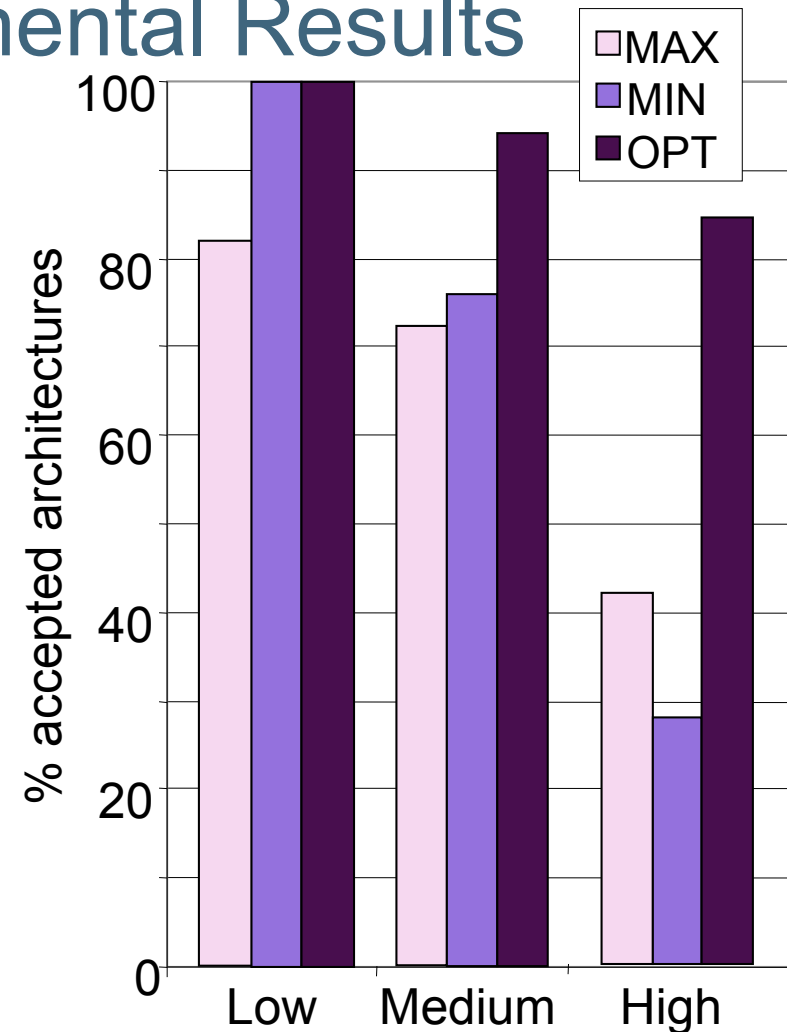
- Cost constraint
- Time constraints
- Reliability goal

## Hardening performance

**degradation (HPD) 5%**

Performance difference between the least hardened and the most hardened versions

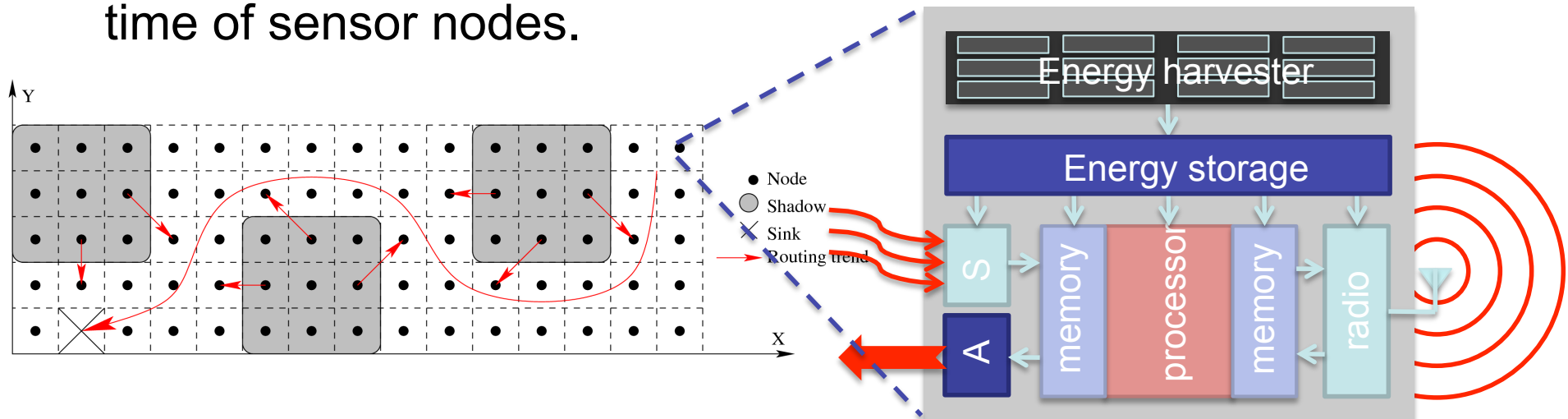
**Maximum cost 20**



% accepted architectures in relation to different technologies (fault rates)

# Energy Harvesting Aware Routing with Scheduling optimization (DTU, UoB, ETHZ)

Energy harvesting aware routing protocols and task scheduler in a combined approach to extend the life-time of sensor nodes.



## Benefits from combination

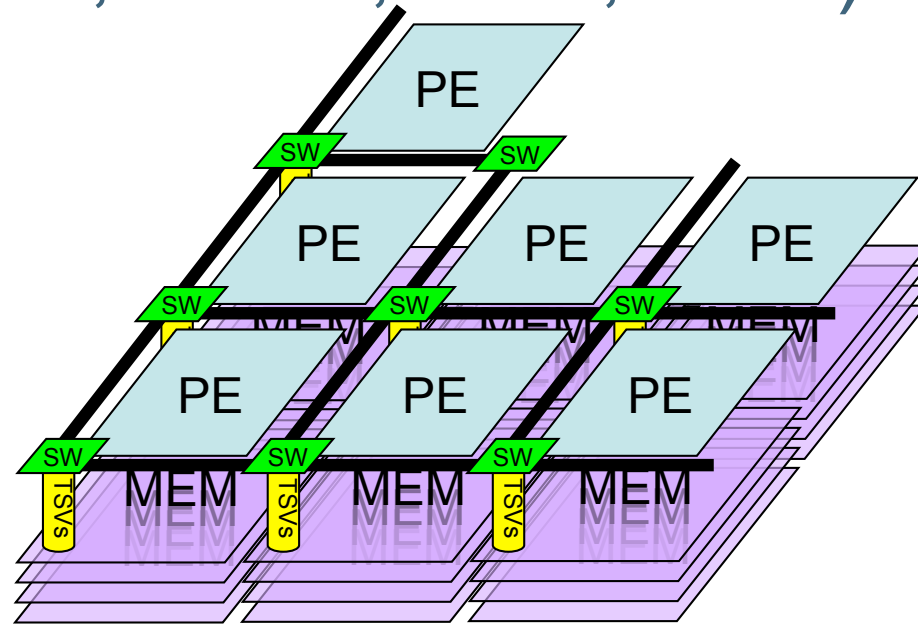
Conservative estimate of hops, by using complete height map

Yields larger time share (local deadline) for weak nodes

# Scalable & predictable 3D-platform (UoB, IMEC, EPFL, ETHZ, CEA, STM)

## 3D-Network on-chip

- Packet-based communication with **QoS support** (TDMA/priorities/regulated traffic)
- **Architecturally scalable**: more nodes, more bandwidth
- **Physically scalable**: segmented P2P links

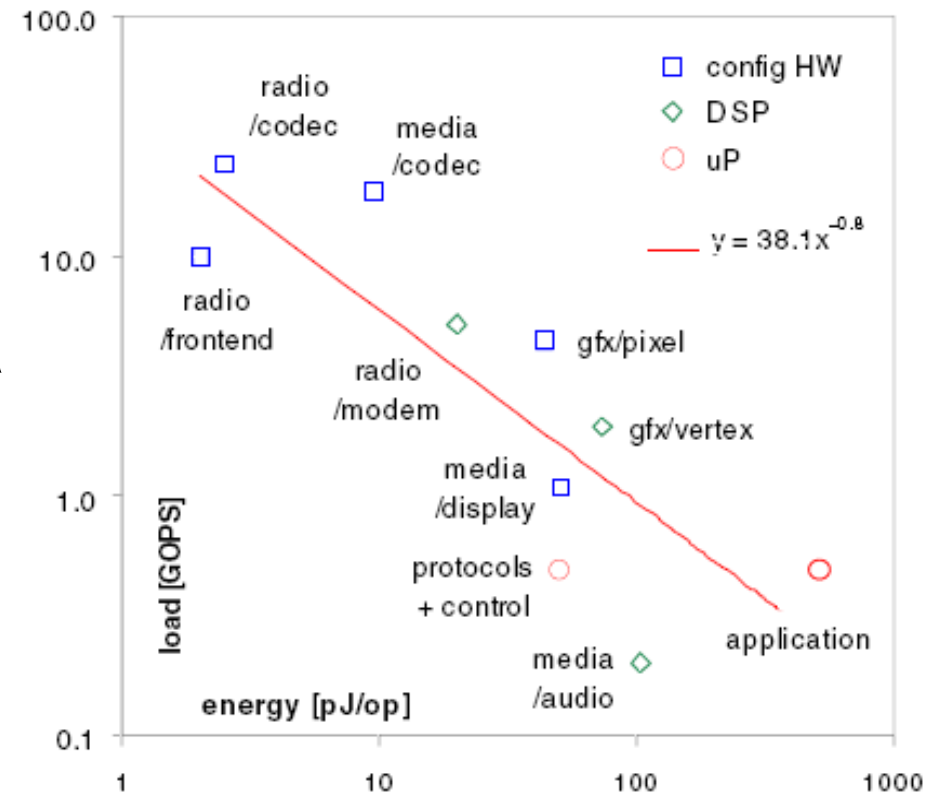


## Vertically Integrated main memory (not only DRAM!)

- TSV main-memory communication from 10pJ/bit to 10fJ/bit
- $10^5$  interconnect density increase
- Priority/Bandwidth reservation (mainly for low-latency memory neighborhood)

# Scalable & predictable 3D-platform

- Homogeneous processor fabrics are conceptually appealing, but most likely not an industry-viable answer
  - heterogeneous IOs
  - heterogeneous applications
  - ...**and** cost !!!
- GOPS/W & GOPS/mm<sup>2</sup> are a hard reality
- We don't need homogeneity, we need modularity!
- The real challenge is how to design a scalable modular heterogeneous many-core system



[NXP09]

## Plans for Y3

- Continue the ongoing joint research
- Focus on:
  - Hybrid approaches to performance analysis (simulation and analytical)
  - Interaction with run-time and application layers (predictability)
  - Communication (3D NoC)
  - Resource awareness and management (energy, adaptivity)
  - Fault tolerance (biochips)
- Tools:
  - Refinement and dissemination