ARTIST Summer School in Europe 2010

Autrans, France

September 5-10, 2010

Nanosystems:

Devices, circuits, architectures and applications

Invited Speaker: Giovanni De Micheli

EPFL

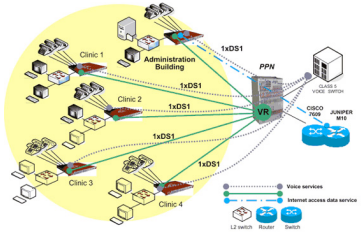
SEVENTH FRAMEWORK PROGRAMME

http://www.artist-embedded.org/

Emerging societal & economic problems

Main issues on the *global agenda*

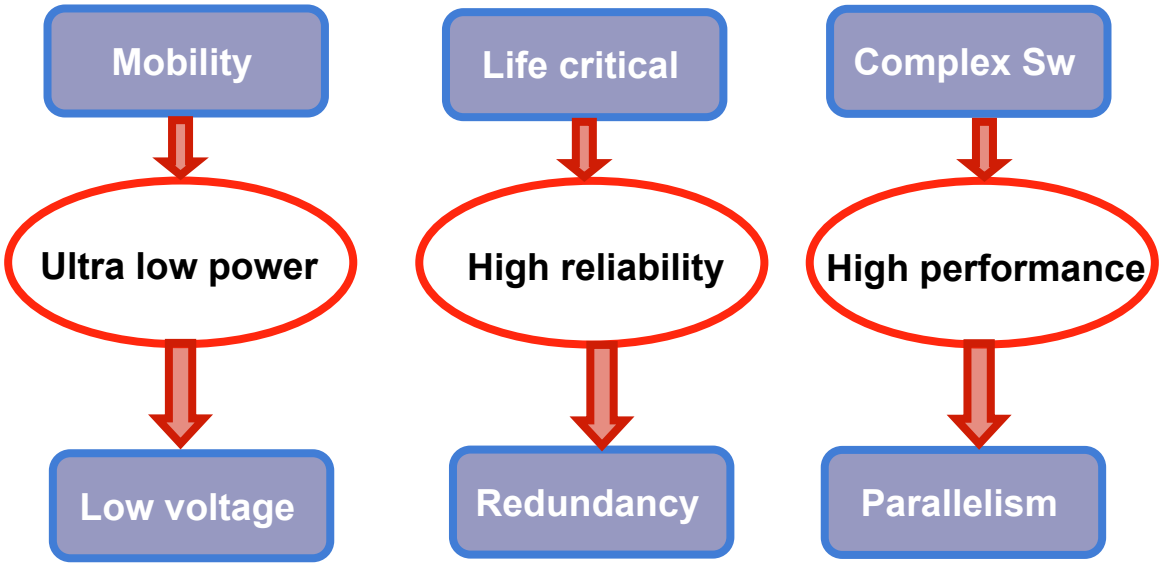
- Ensuring sustainability
  - Smart energy production and distribution
  - Intelligent water management
- Strengthening welfare
  - Better, affordable health care and wellness
  - Dealing with ageing and young population
- Mitigating risks
  - Preventing catastrophes and pandemics
  - Monitoring the environment
- Enhancing security
  - Future of the internet
  - Preventing cyber and physical attacks

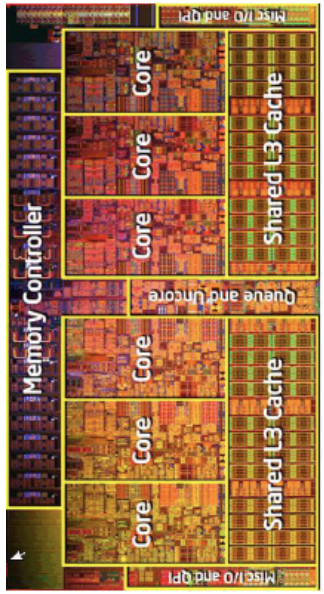


The technology

Requirements for integrated systems

- Unprecedented computing and storage capability
- Ubiquitous high-bandwidth communication
- Mobility, reliability, ease of use





- From processors to multi-processors
- How far can standard CMOS support the needs?

Nano-systems

Nano

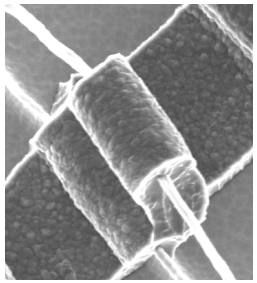
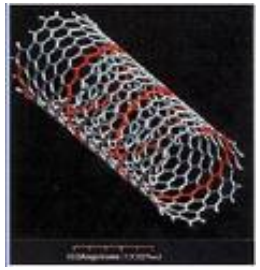
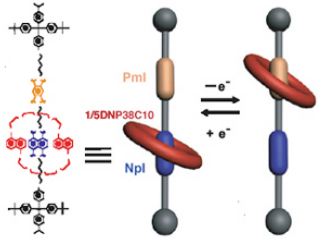
- Nanoelectronics:
  - CMOS < 32nm node
  - Silicon nanowires
  - Carbon nanotubes
- Nano-bio-sensing:
  - Size compatibility
  - Electro-chemistry

Systems

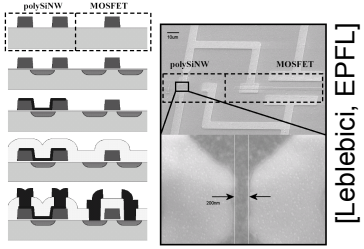
- Tera-scale systems:
  - Heterogeneity
  - Sensing, Processing, Communication, SW Transducers
- Complexity:
  - Design
  - Management

Beyond CMOS

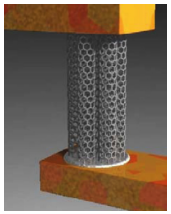
- Nano-technology provides us with new devices

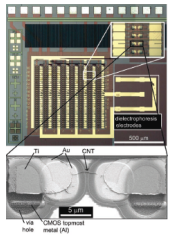




- Can they mix and match with standard CMOS technology ?



[Leblebici, EPFL]

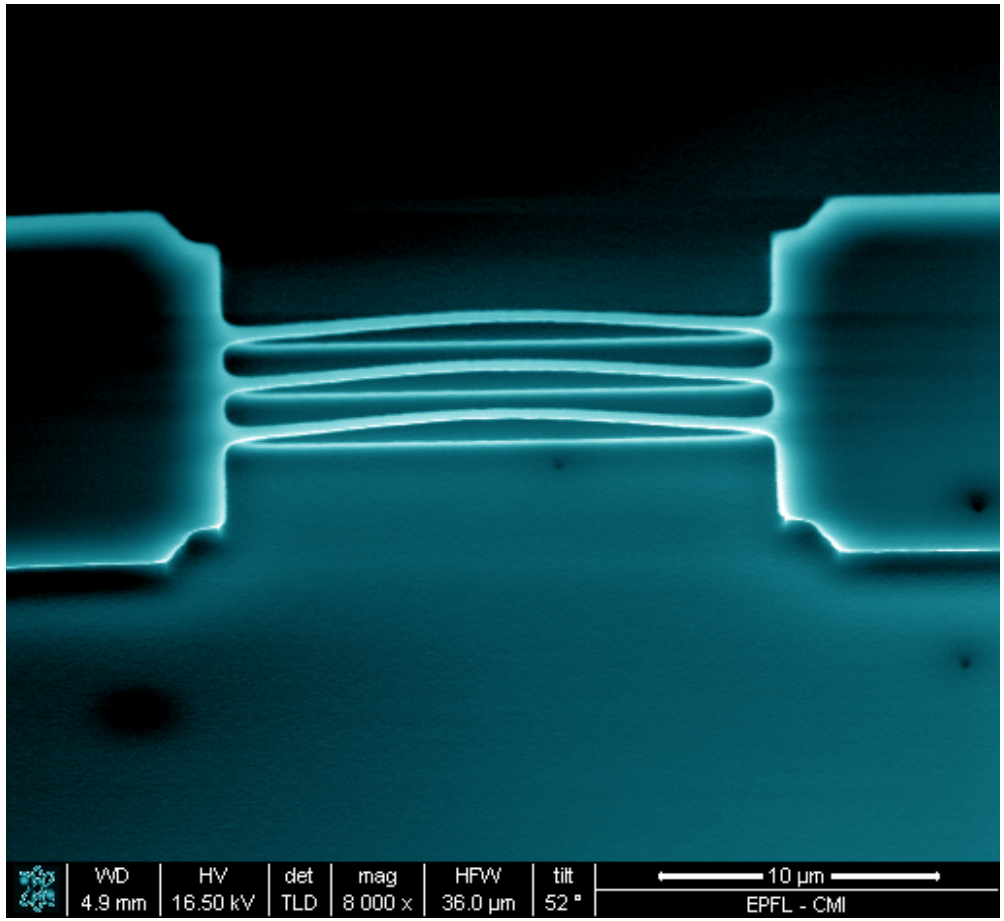

[Infineon]


[Close, Stanford]

- What is the added value?

- What are the drawbacks of these technologies?

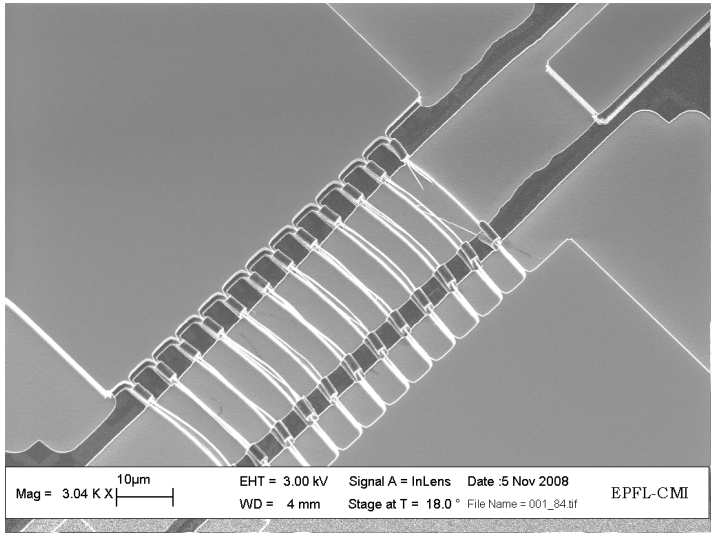
Nano-devices



Devices

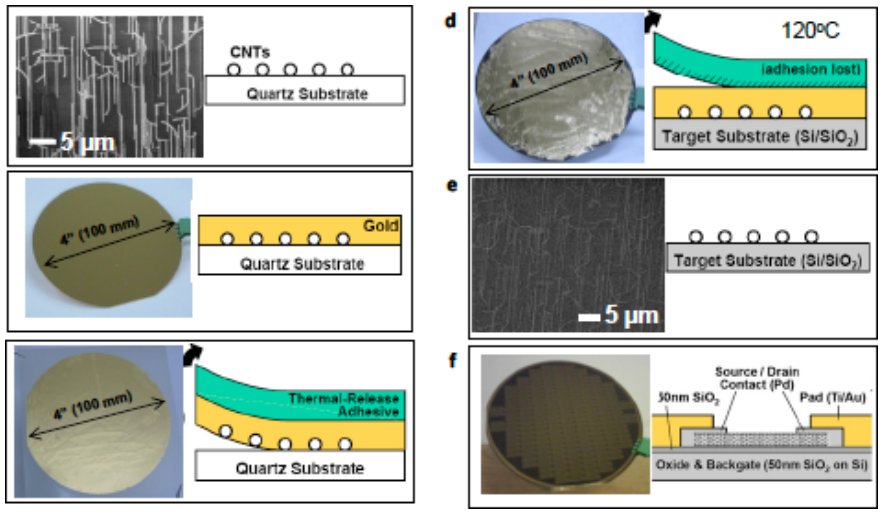
Silicon nanowires

- Silicon process
- CMOS compatible
- Top-down design

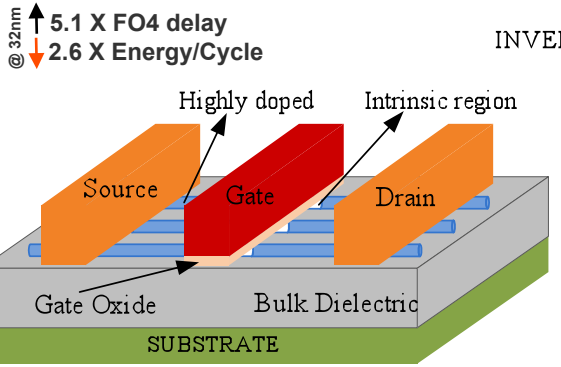


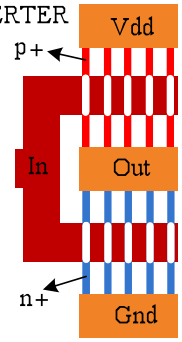
Carbon nanotubes

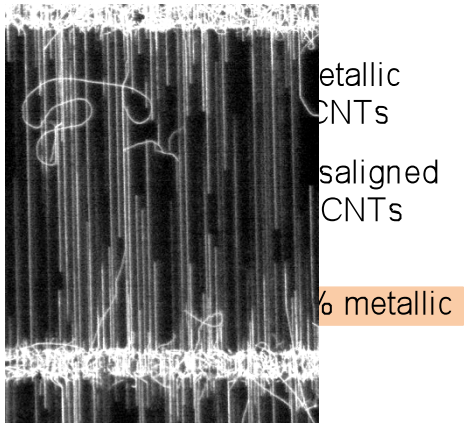
- Deposition or growth
- CMOS compatible
- Top-down patterning

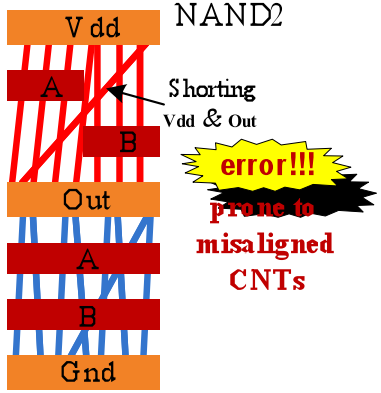


Imperfection-Immune Carbon Nanotube Circuits





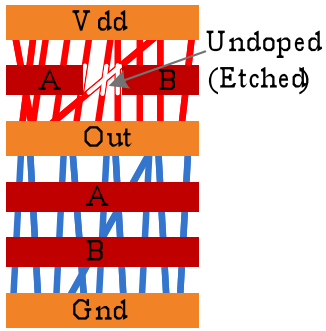




In Reality

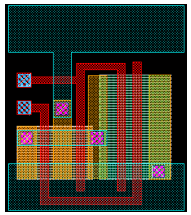
Layout level strategies to tackle misaligned CNTs
"Misaligned-Immune layouts"

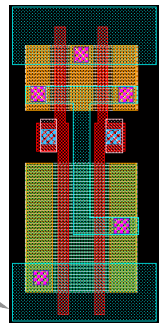
Misaligned-Immune Layouts



Scheme 1

Scheme 2

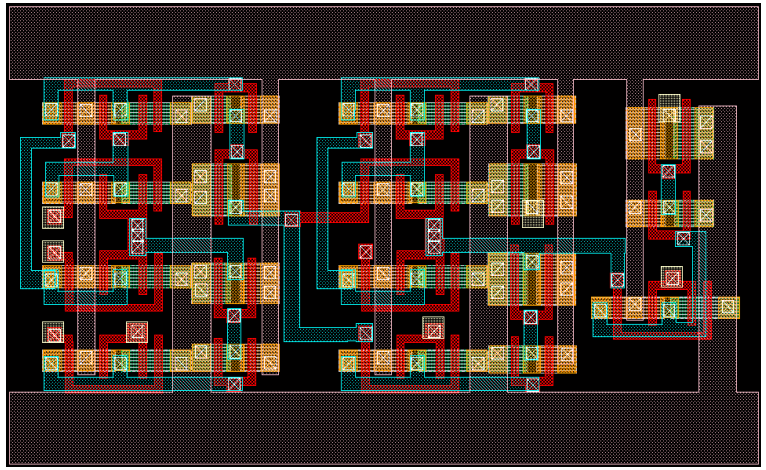




Area Optimization

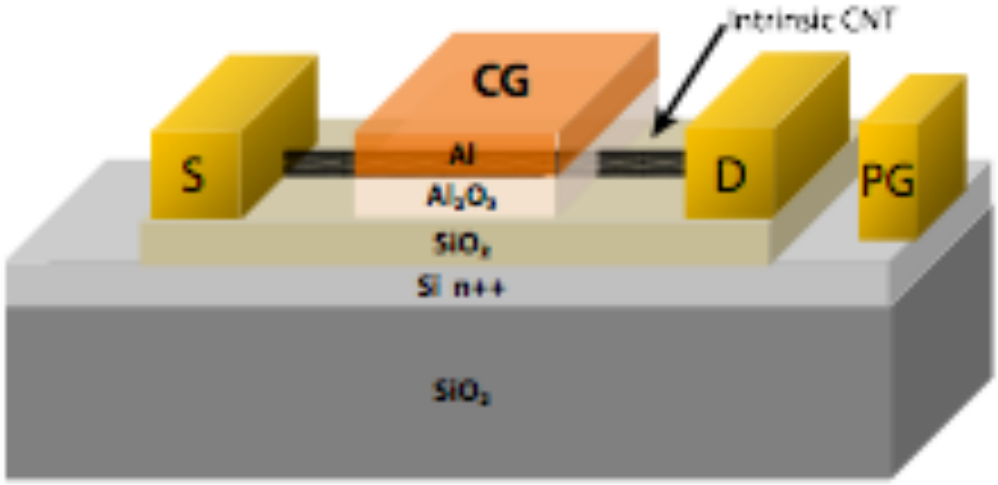
Standardization

CNFET DesignKit

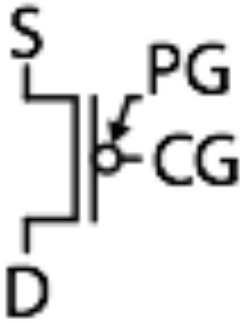


CNFET based Full Adder

Double-gate ambipolar CNFET



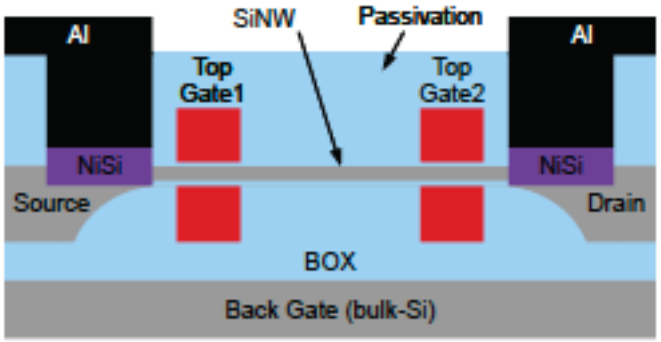
- Device structure

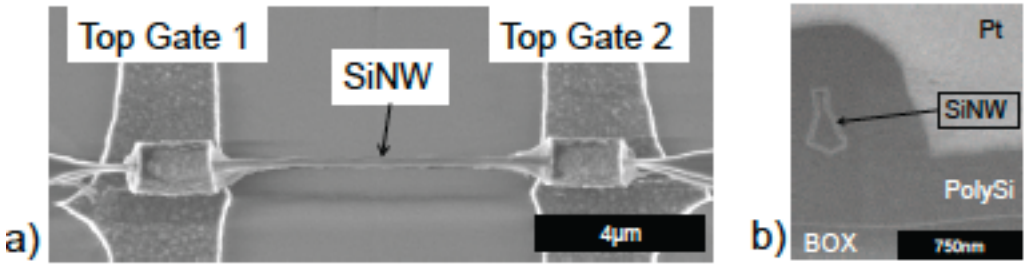


- Circuit symbol

Silicon Nanowires

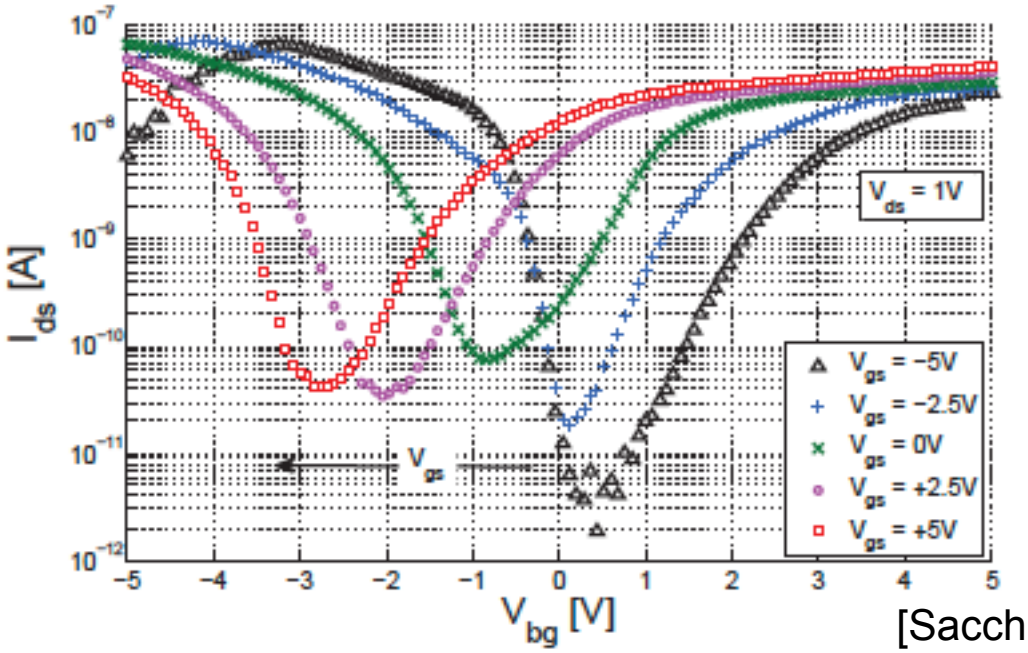
- *Silicon on Insulator* (SoI) wafer
- Deep reactive ion etching (DRIE)
- Gate all around transistors





Ambipolarity

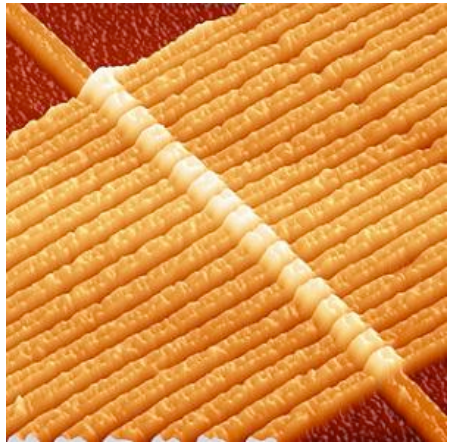
- Device characteristics controlled by backgate voltage
  - Four-terminal devices
  - Back gate determines type: *p* or *n*
  - Applicable to both CNT and SiNW FETs

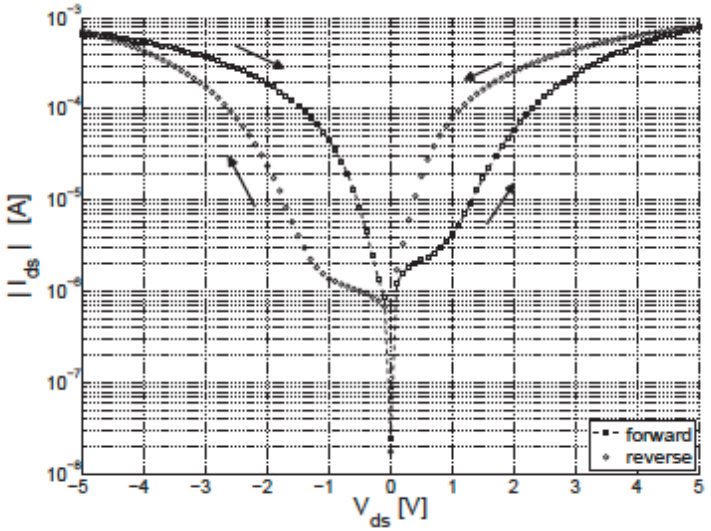


[Sacchetto – SiNW]

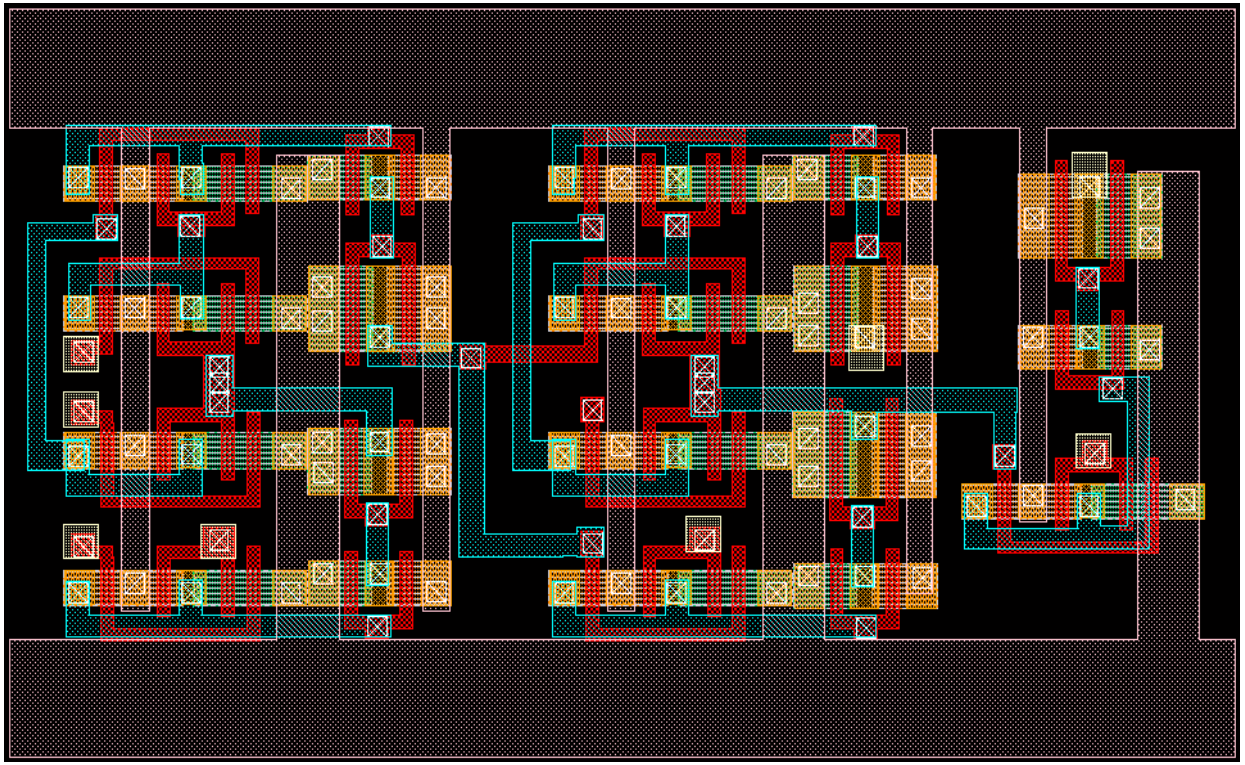
Memristive effects

- Memristor devices:
  - TiO_2 devices [Williams, HP]
  - SiNW Schottky junctions [EPFL]
- Applications:
  - Resistive RAMs (RRAMs)
  - Digital components
  - Neural networks



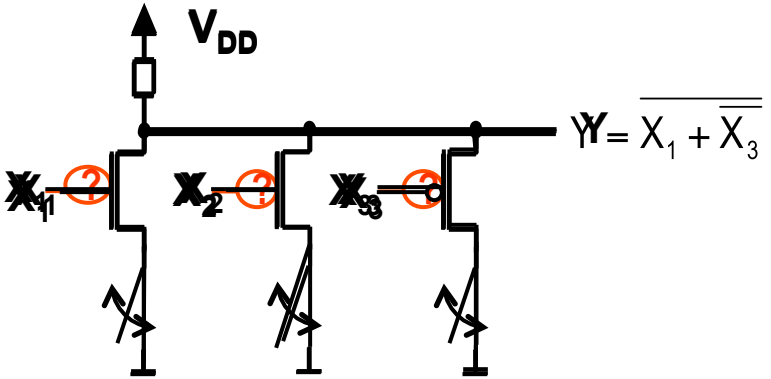


Nano-circuits

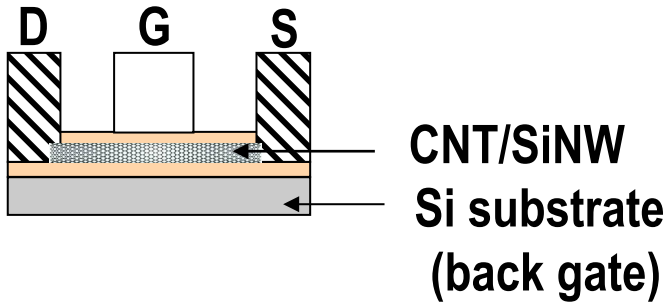


Logic abstraction of ambipolar devices

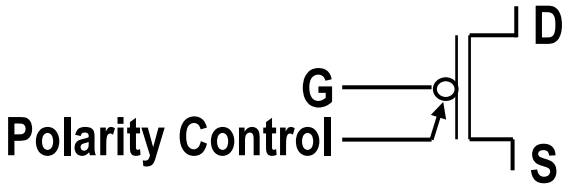
- Online polarity control:
  - On-line control: *p* or *n* device
  - Expressive power in realizing circuit function

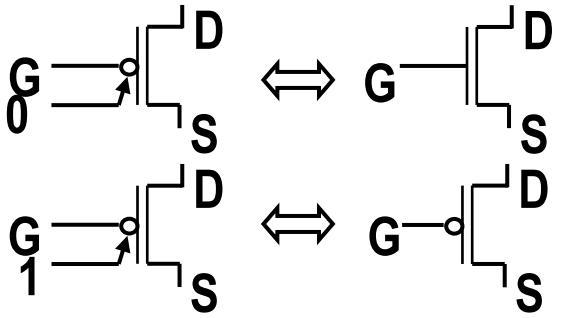


- Fabrication technology: double gate CNT/SiNW FET



- Device symbol and operation:

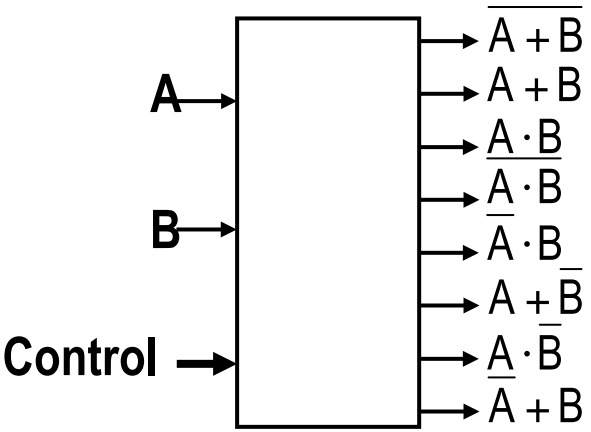




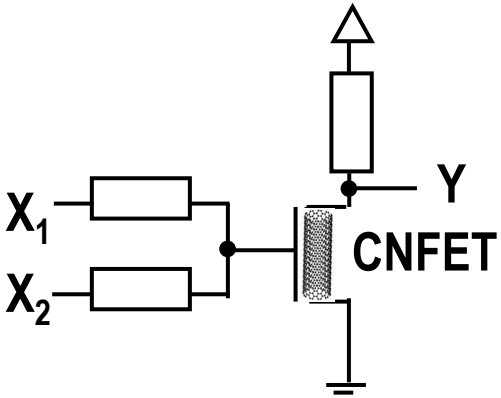
Previous work with with ambipolar CNTFETs

- Use of ambipolar CNTFET in logic circuits:
  - Pseudo logic XOR gate
  - Dynamic 8-function gate
  - Dynamic GNOR gate:

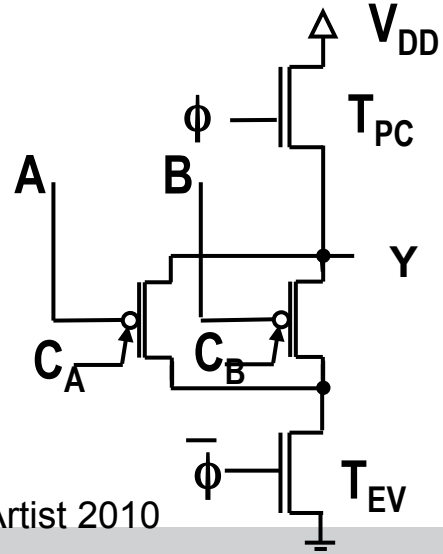
$$Y = \overline{A \oplus C_A + B \oplus C_B}$$



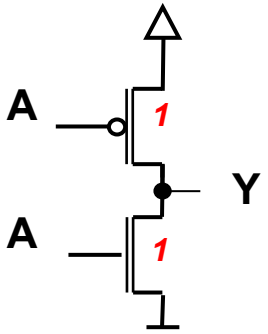
[O'Connor et al., IEEE TCS'07]



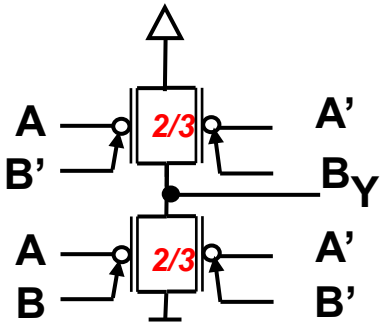
[Sordan et al., Appl. Phys. Lett.'06]



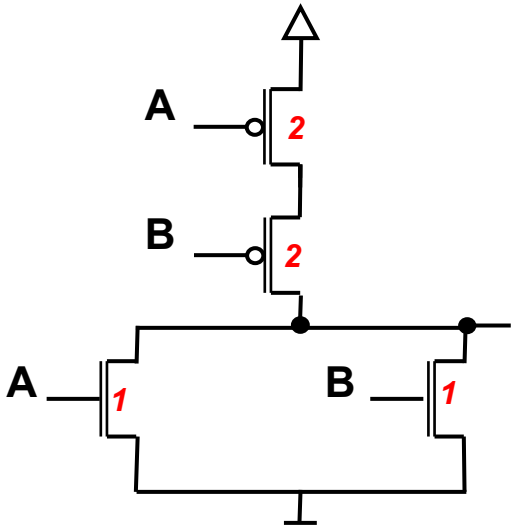
Static logic family



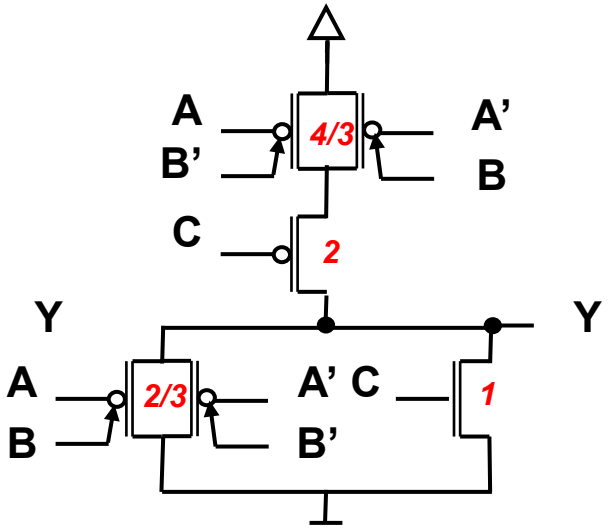
$Y=\overline{A}$



$Y=\overline{A \oplus B}$

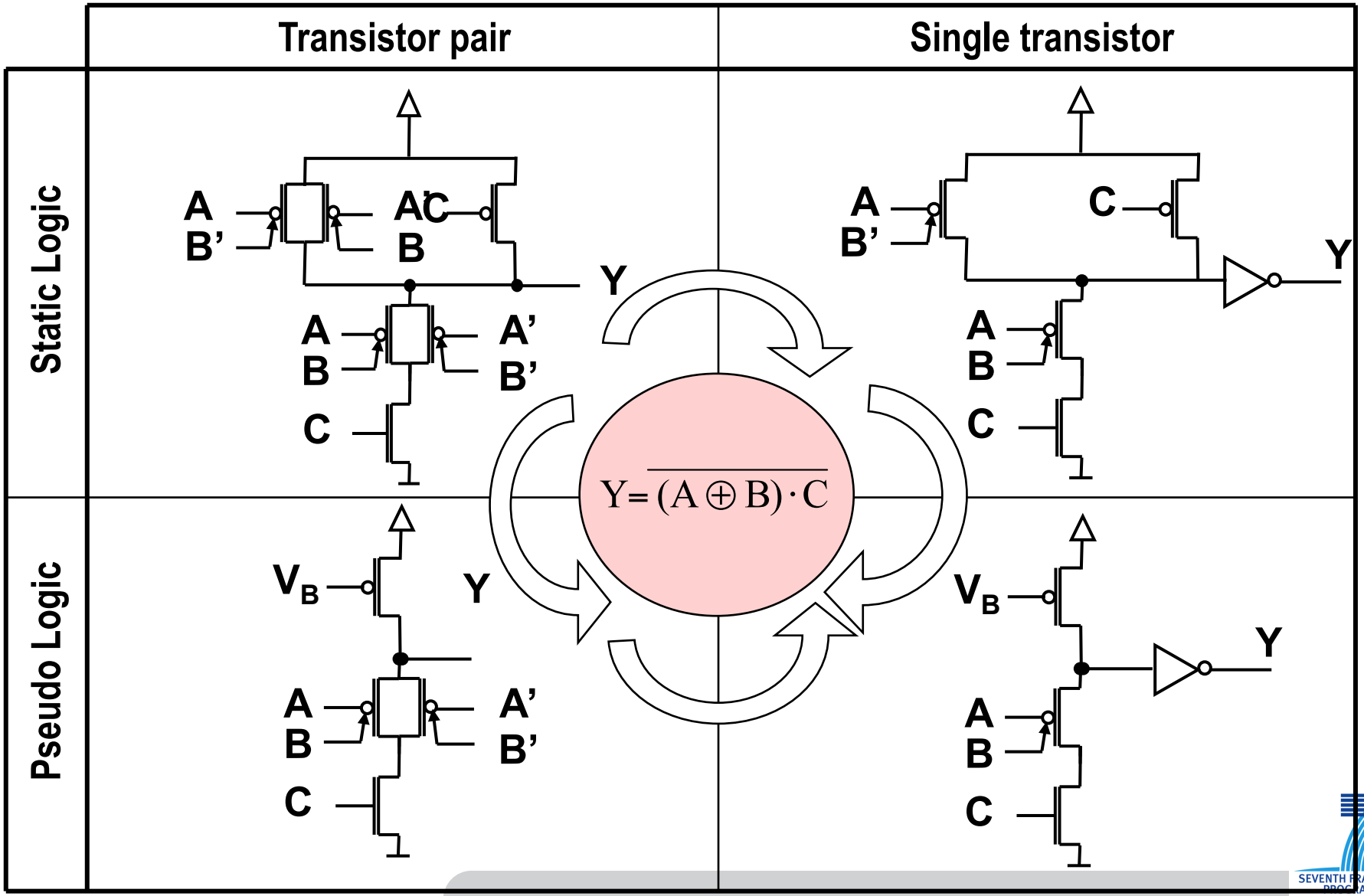


$Y=\overline{A+B}$



$Y=\overline{(A \oplus B)+C}$

Alternative logic families



Library characterization

- AMBI vs MOSFET:
  - Larger T count, but lower A
  - Static TP AMBI: equal normalized FO4 to MOS
- AMBI CNTFET families
  - TP pseudo vs TP static: 31% smaller, 33% slower
  - TP pseudo vs. ST pseudo: faster!

	CNT FET Technology									MOS FET Techno.		
	TP Static τ_1 ~0.6 ps			TP Pseudo τ_1 ~0.6 ps			ST Pseudo τ_1 ~0.6 ps			Static τ_2 ~3 ps		
	T	A	FO4/τ_1	T	A	FO4/τ_1	T	A	FO4/τ_1	T	A	FO4/τ_2
Avg.	9.1	12.3	9	5.6	8.5	12	3.7	11.5	24.1	4.9	12.7	9

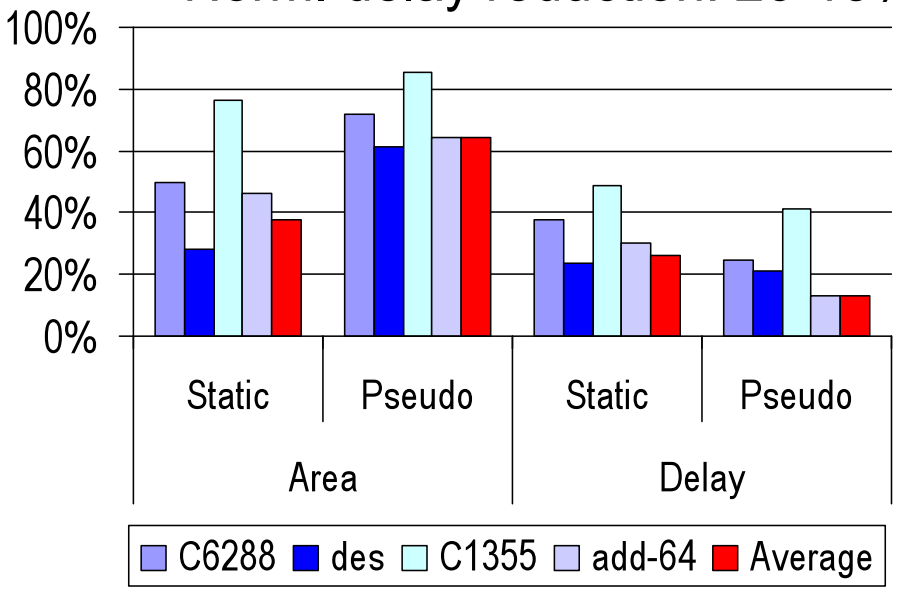
T = Average transistor count

A = Average gate area

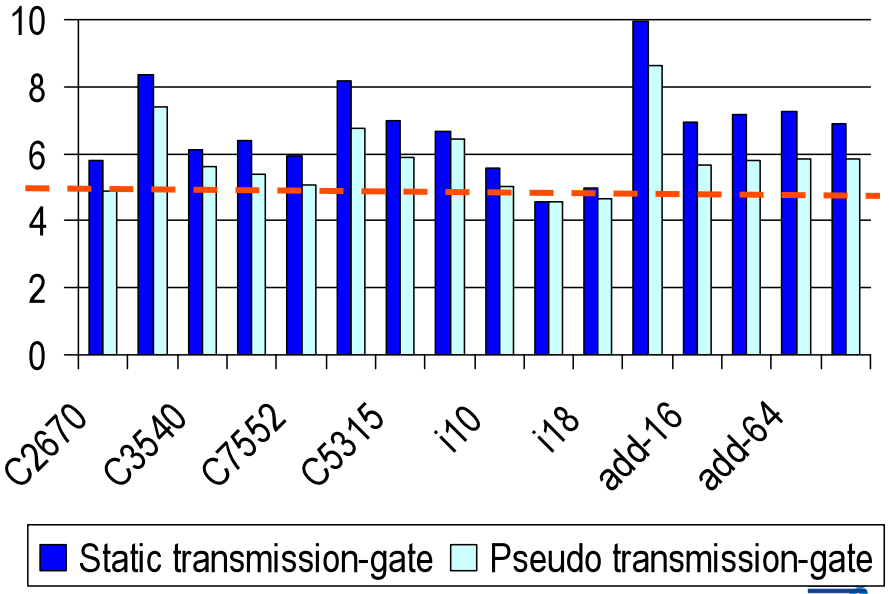
τ = Technology-dependent intrinsic delay

Multi-level logic synthesis results

- AMBI implementation needs fewer physical resources:
  - 38% fewer gates
  - 40% less logic levels
- Area saving: 38-65%
- Norm. delay reduction: 26-13%



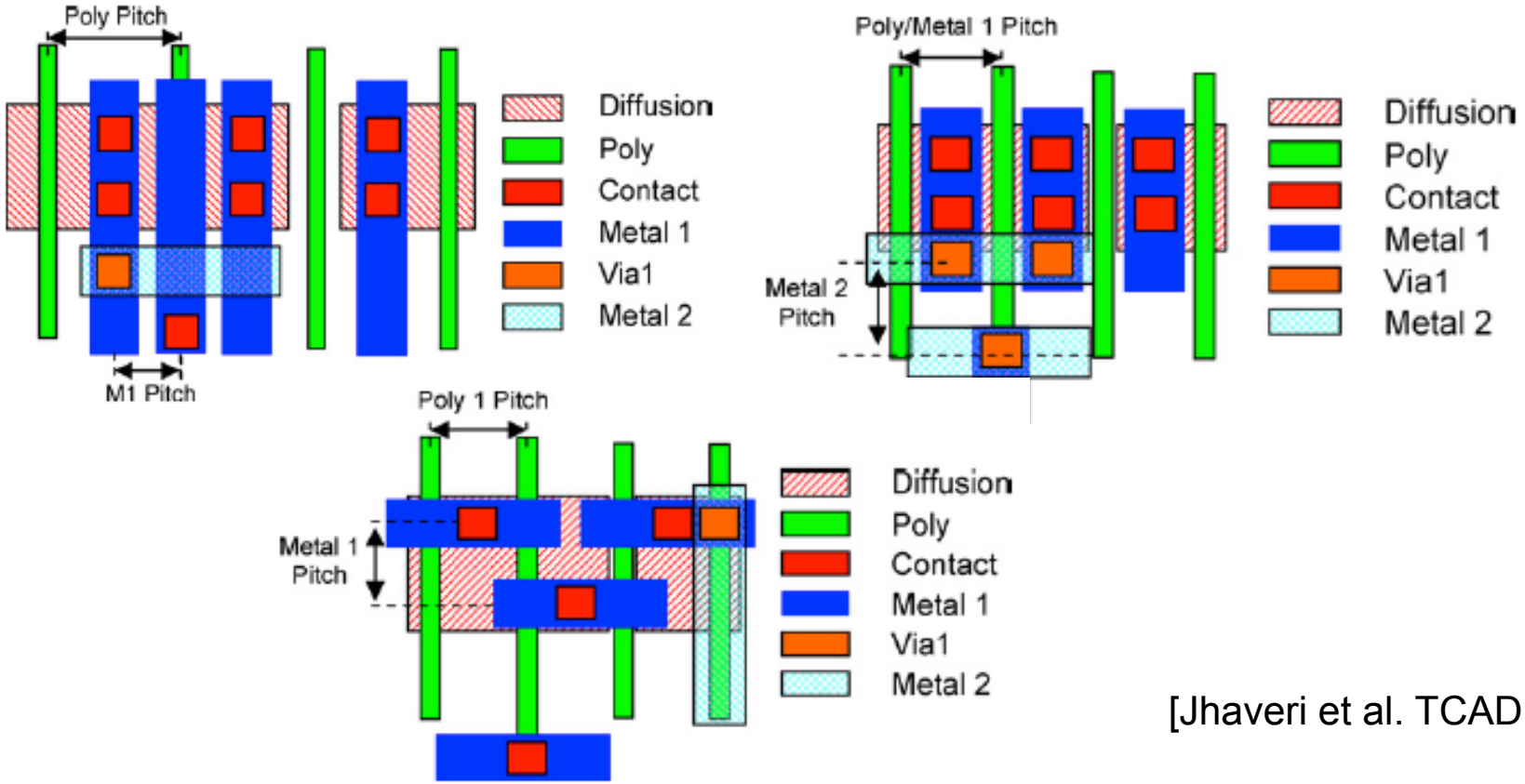
- AMBI's τ is ~5× lower.
- Absolute speed-up:
  - 6.9x for TP static AMBI
  - 5.8x for ST static AMBI



Nano-architectures

Regular fabrics

- Manhattan geometries
- Constraints on directions in each layer

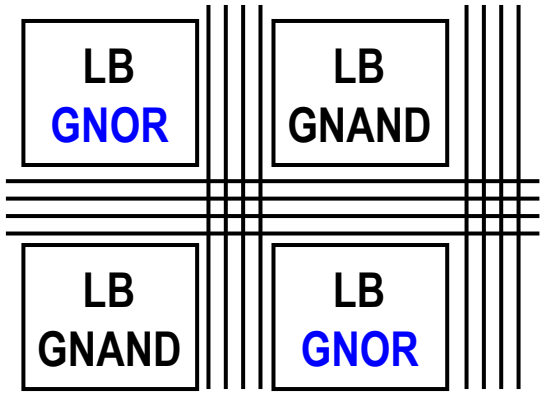


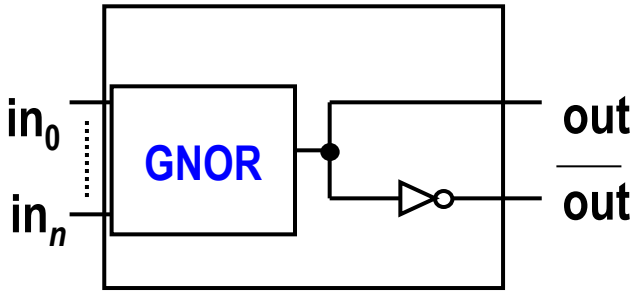
[Jhaveri et al. TCAD10]

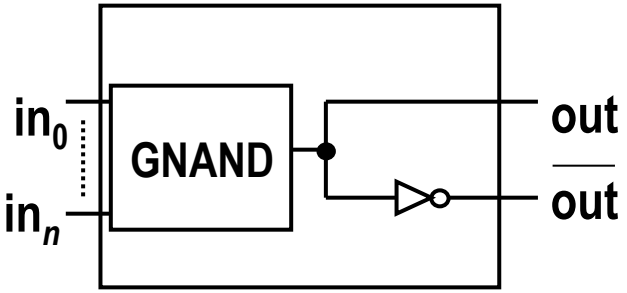
Regular fabrics

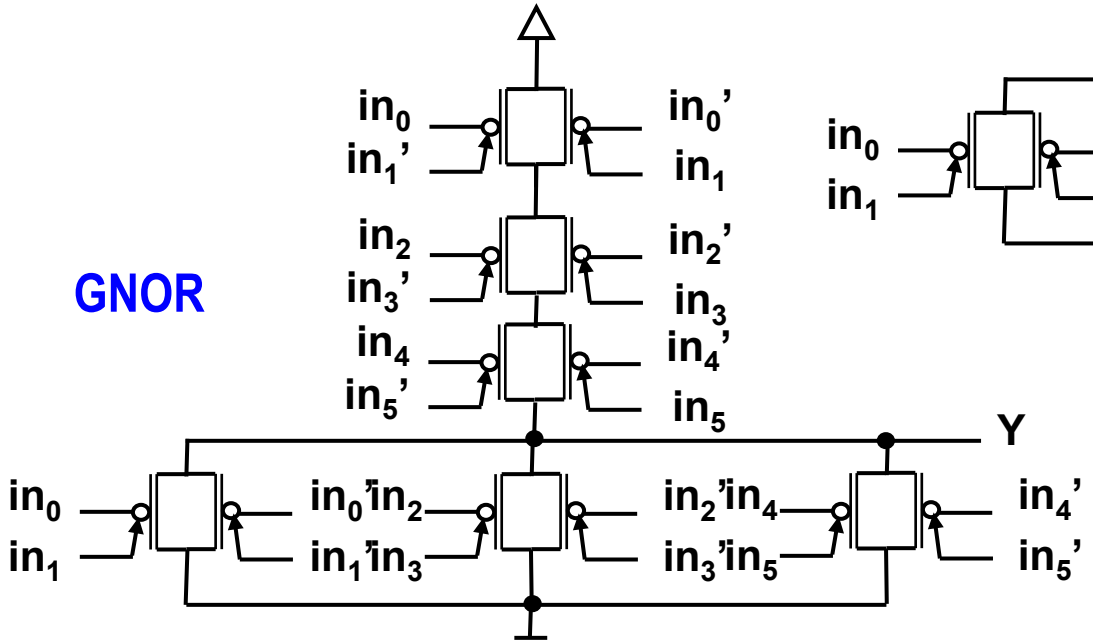
- Ambipolar cells are very regular
  - Tile arrangement of GNOR and GNAND cells
  - Application to FPGAs
- Ambipolar cells support PLA design
  - Dynamic operation
- Cells themselves are highly regular
  - Hierarchical construction
  - 3-Dimensional construction

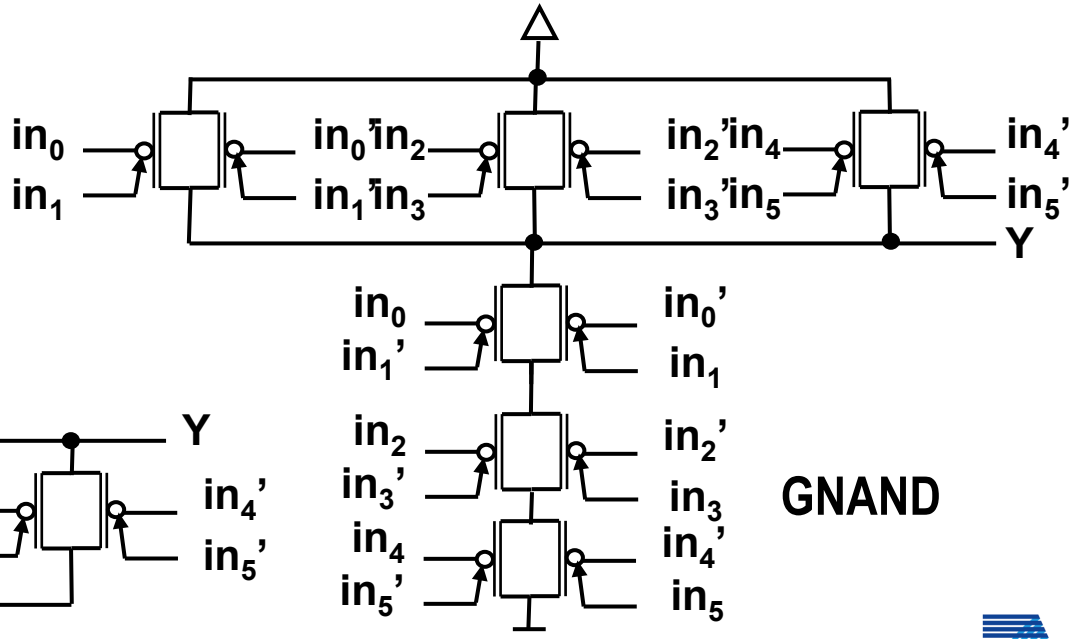
Static regular fabrics











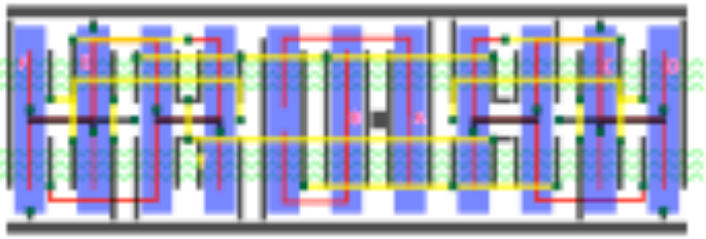
New FPGA Design

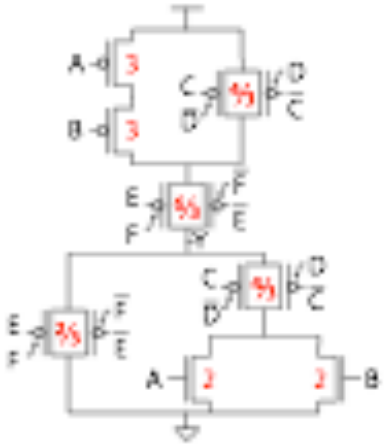
- An ambipolar cell can be made programmable:
  - By connecting one/more input/s to Vdd or Gnd
  - By bridging two inputs
- Programming can be made after manufacturing
  - Various physical means to achieve programming
- Many derived cells, because of intrinsic expressive richness
  - Mix of unate and binate functions
  - Good for data path and control logic

Number of programmed functions

Name	Function	N_i	N_f		
			Single	Dual	NPN
F14	$\overline{(A \oplus B) + C + D}$	4	12	20	6
F17	$\overline{((A \oplus B) + C) \cdot D}$	4	16	20	6
F21	$\overline{(C + D) \cdot (A \oplus B)}$	4	15	24	7
F30	$\overline{(A \oplus B) + (C \oplus D) + E}$	5	28	52	10
F33	$\overline{((A \oplus B) + E) \cdot (C \oplus D)}$	5	48	84	13
F42	$\overline{(A \oplus B) + (C \oplus D) + (E \oplus F)}$	6	47	90	13
G4	$((A \cdot B) + (C \oplus D)) \cdot (E \oplus F)$	6	105	186	27
ACT1	Actel ACT1 block	8	702		175
LUT4	4-input Look-Up Table	4	65536		221

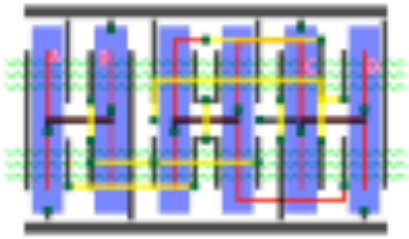
Example of layout

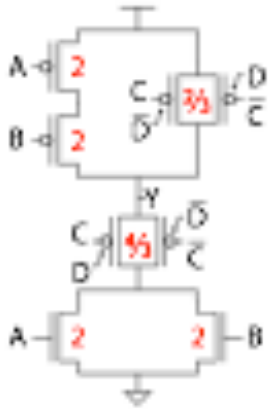




Implemented Function

$$G4 = \overline{((A \cdot B) + (C \oplus D)) \cdot (E \oplus F)}$$

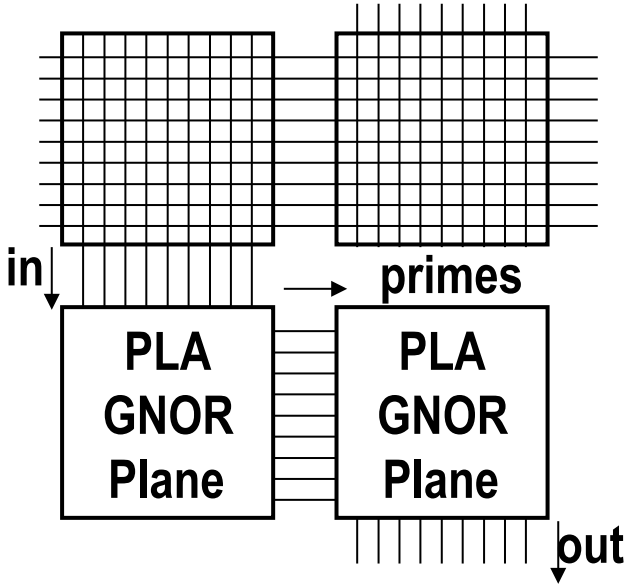


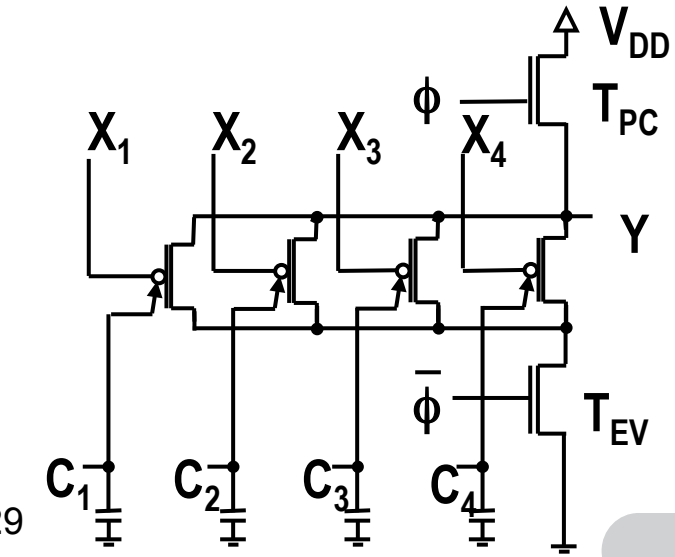


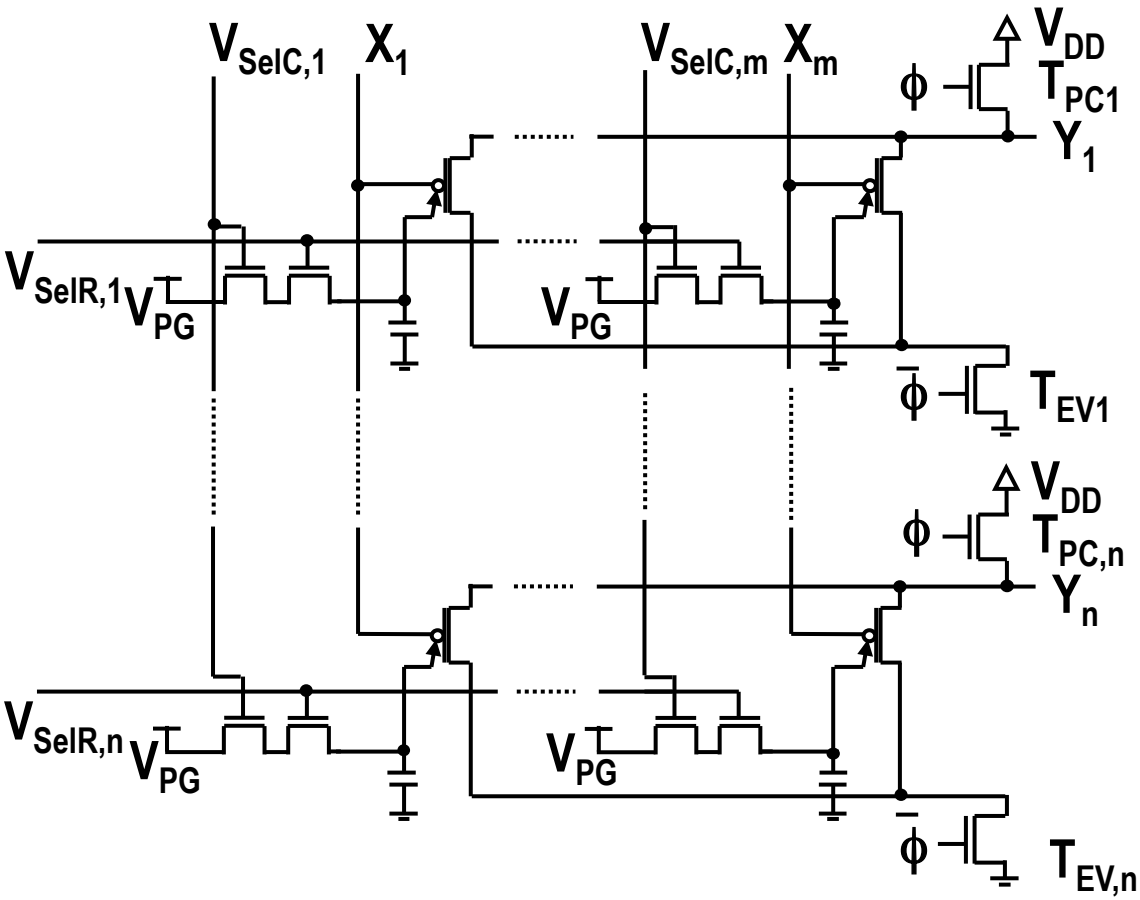
Implemented Function

$$F21 = \overline{(A + B) \cdot (C \oplus D)}$$

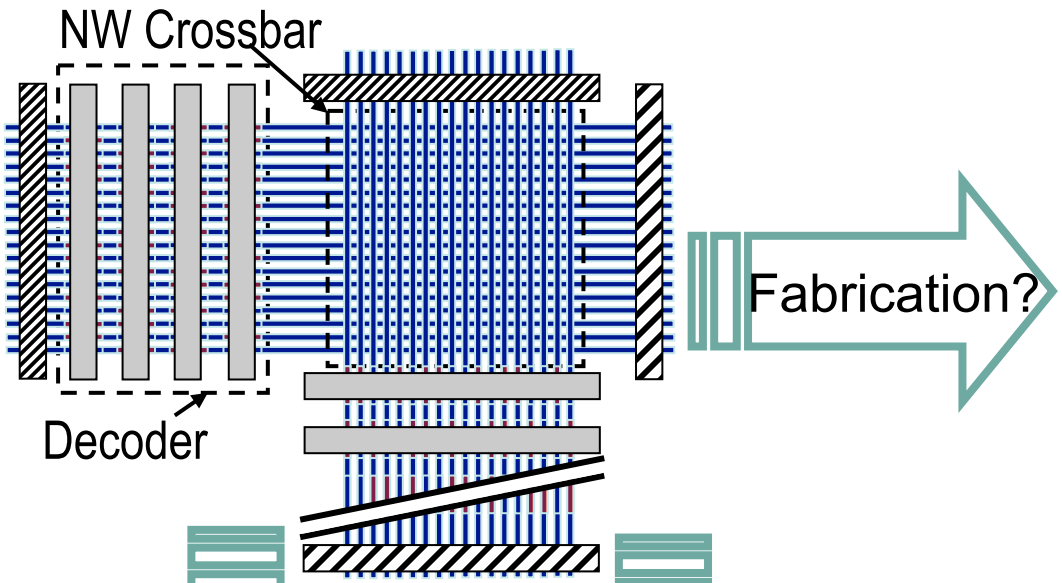
Dynamic regular fabrics



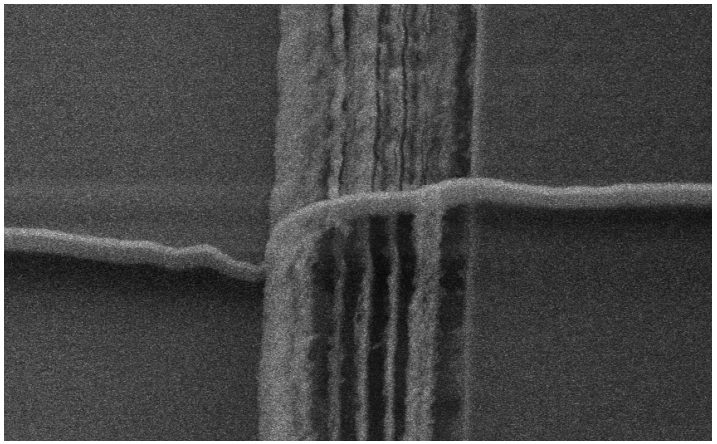




Nano-array design issues

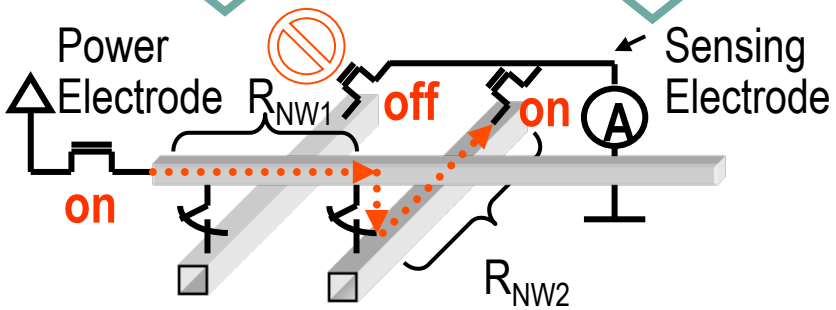


Fabrication?



Design?

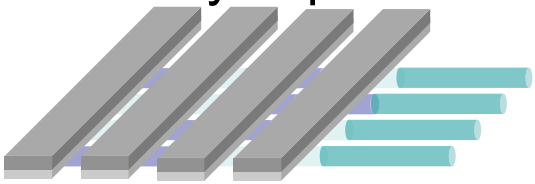
Test?



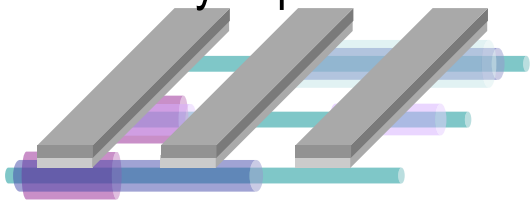
- Connecting array to meso-wires
- Easing test and self-test
- Support redundancy

Decoder Technologies

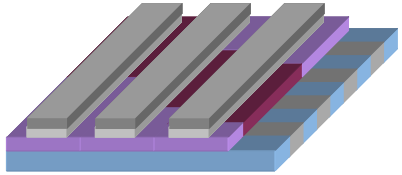
- Axial decoder [*DeHon et al. 03]*: differently doped NW regions



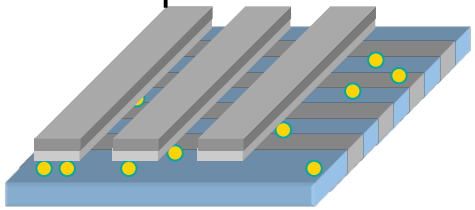
- Radial decoder [*Savage et al. 06]:* differently doped NW shells



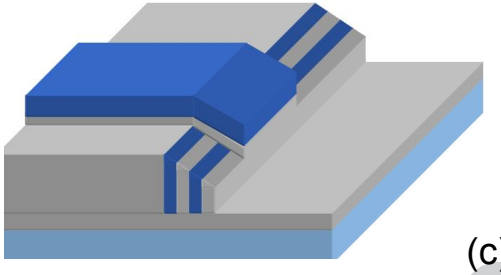
- Mask-based [*Beckman et al. 05]:* low- and hign-k dielectric



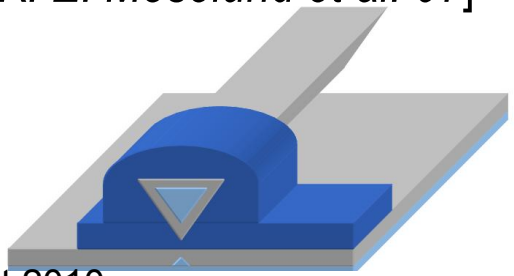
- Random contact [*Williams & Kuekes 01*]: random impurities



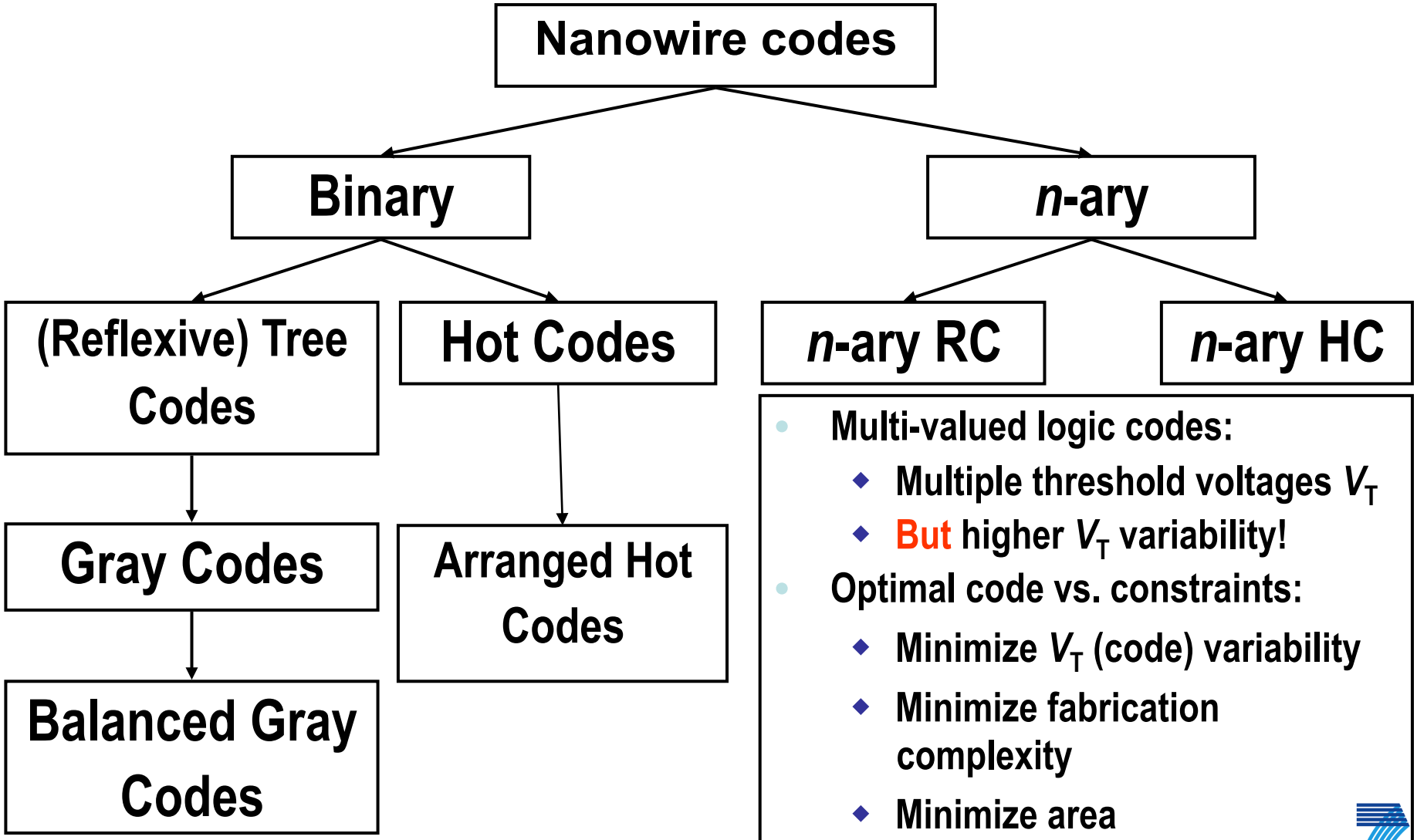
- Multi-spacer patterning technique [*G. Cerofolini 07*]



- Gate-All-Around decoder [*K. E. Moselund et al. 07*]

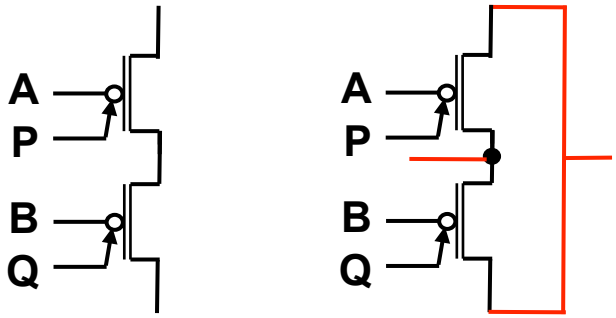


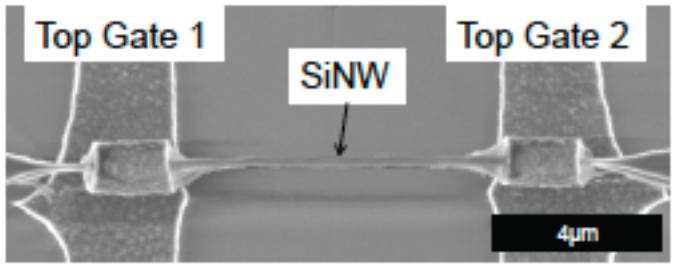
Nanowire encoding schemes



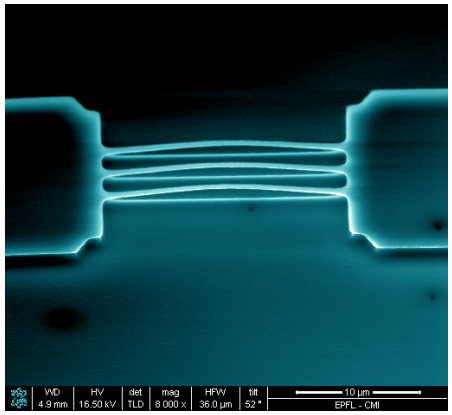
Physical design

- Basic building blocks:



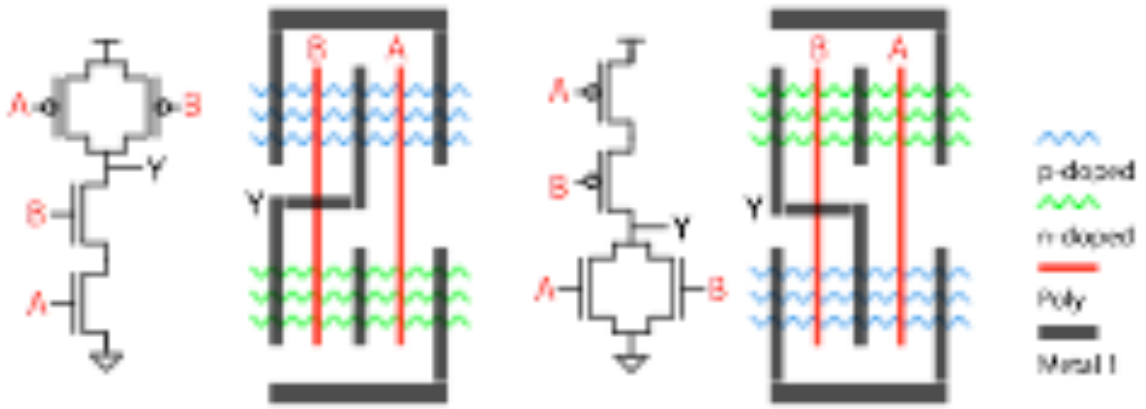


- Bottom-up construction
- Vertical stacking
  - 3D structure



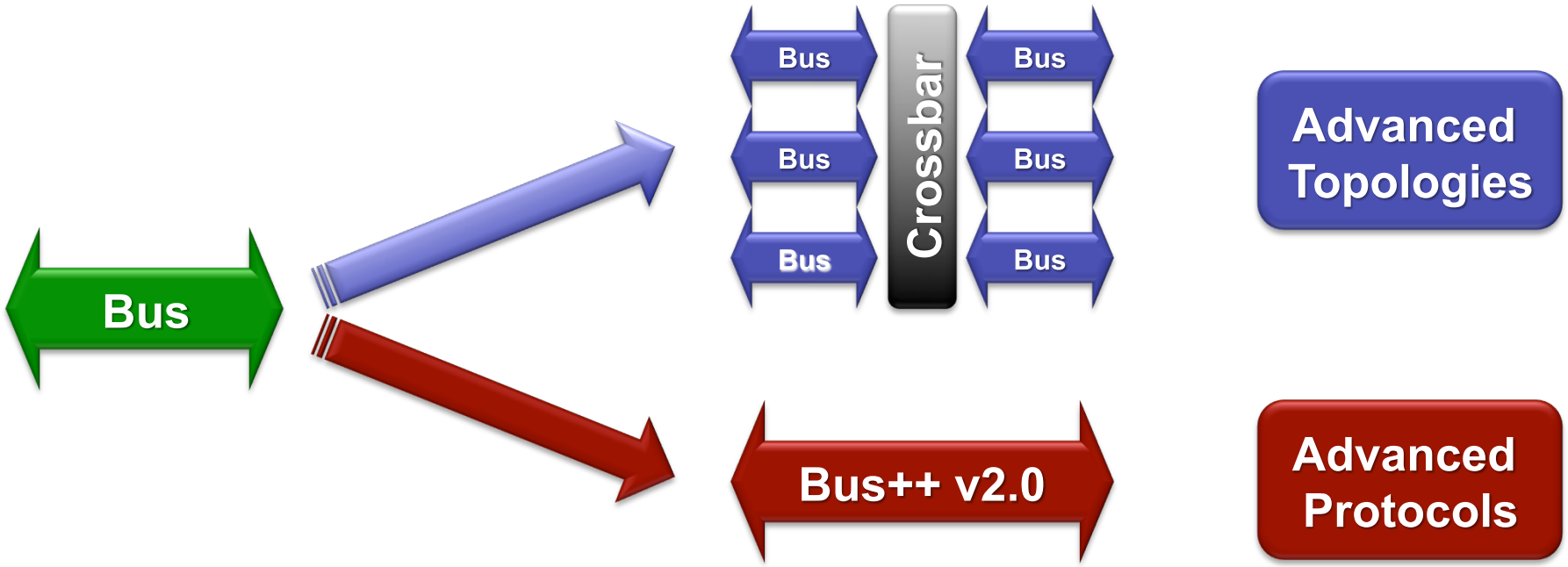
Physical layout

- Symmetric cells
  - Dual gates obtained by mirroring
- No wells



Nanosystems: communication

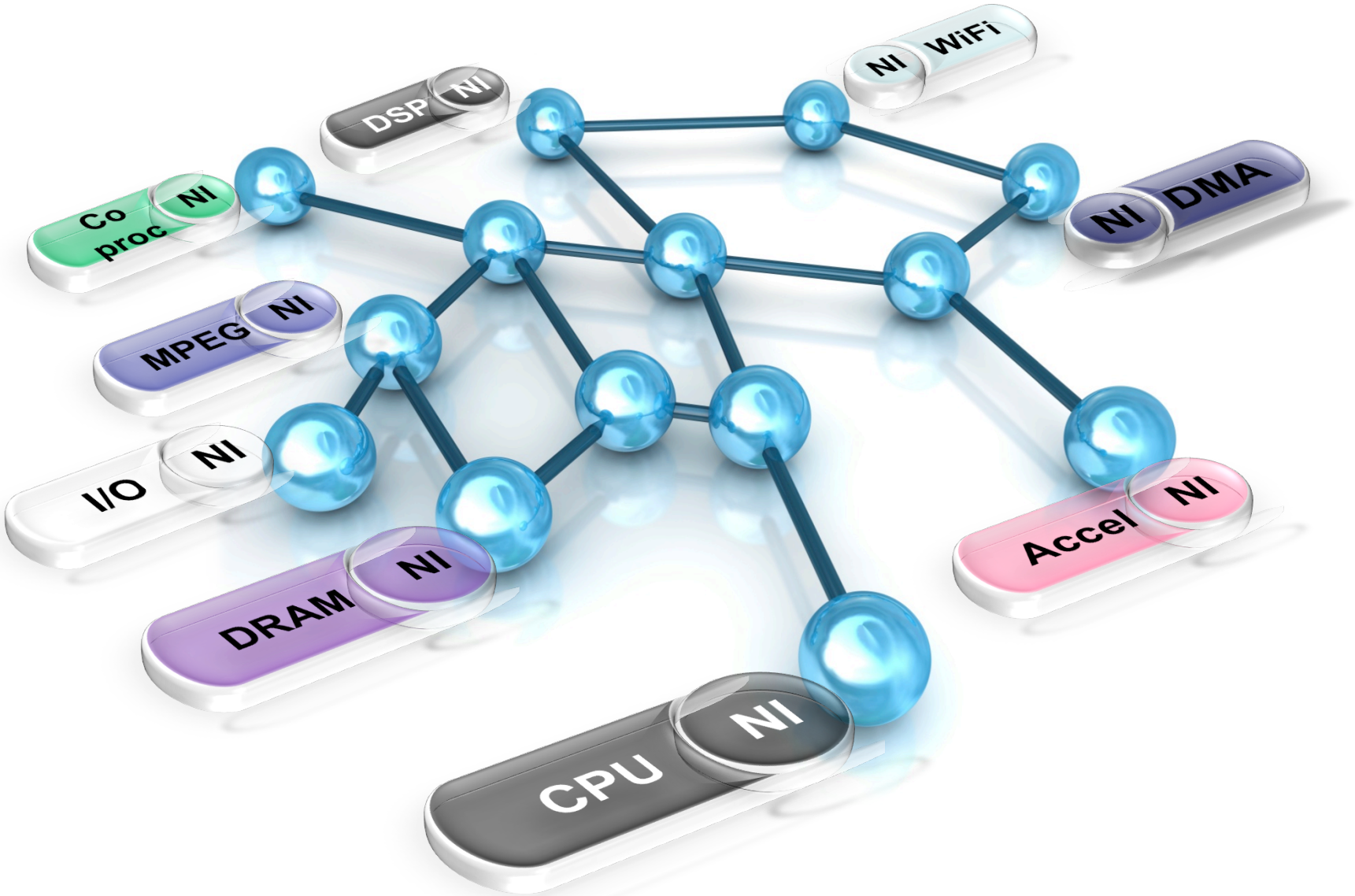
Coping with increased on-chip parallelism



- Evolution to more bandwidth, more usable bandwidth
- Natural evolutionary trajectory

Interconnection issues today

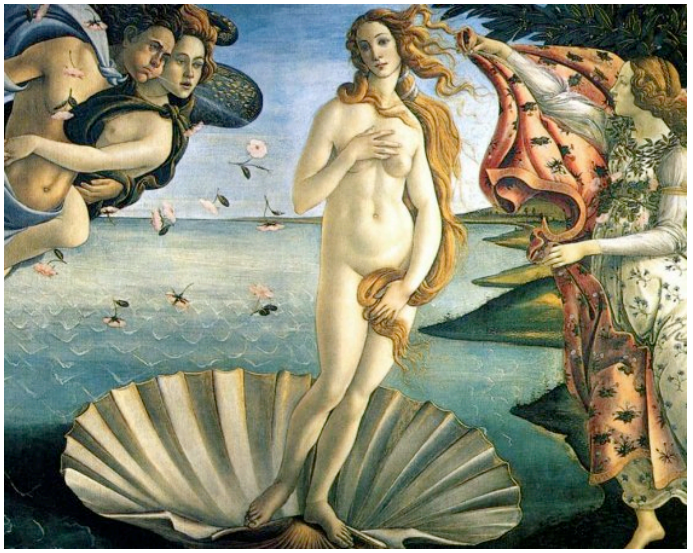
Evolving to Network-on-Chips (NoCs)



Why NoCs?

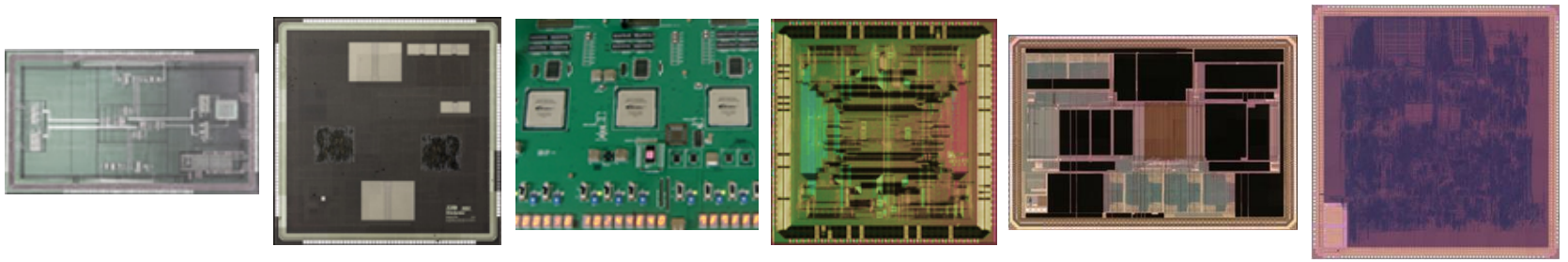
- Next step in on-going evolution
- Advantages as seen in large-area networks:
  - Scalable to many actors
  - Scalable to comparatively long distances
  - Suitable for homogeneous and heterogeneous systems
  - Well-understood theory and implementation
- Key principles:
  - Separate computation and communication concerns
  - Packet-based communication
  - Adjusted to on-chip medium peculiarities (area, power, bandwidth, latency)

The Birth of the NoC Idea

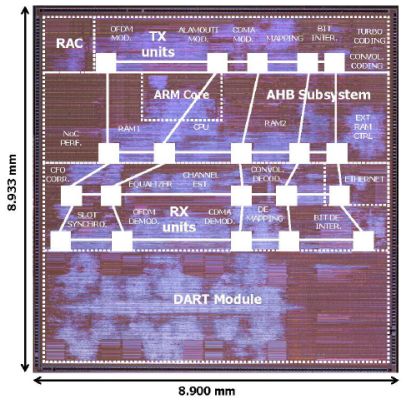


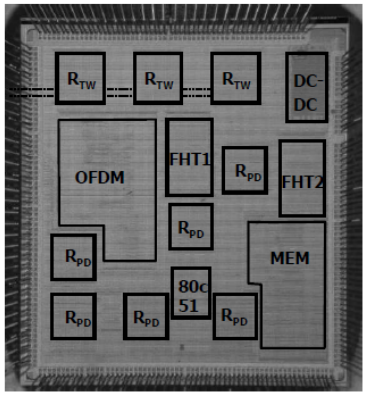
- Architecture:
  - Dally et al.
    - Parallel computing and wormhole routing
  - Greiner et al.
    - SPIN, the first NoC realization
  - Agarwal et al.
    - RAW architecture
- Design Automation:
  - Benini et al.
    - The NoC Manifesto and the first NoC synthesis tool
  - Carloni et al.
    - Separating computation and communication with latency-insensitive design
  - Goossens et al.
    - Æthereal: Support of QoS in NoCs

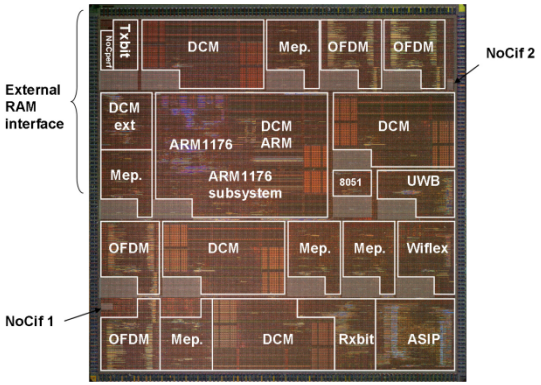
NoC-Based Chip Implementations



KAIST 03-08



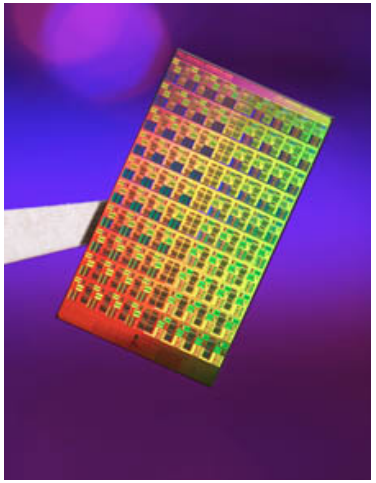




CEA-LETI 07-10

SEVENTH FRAMEWORK PROGRAMME

From Research to Products



Intel Polaris

2007, 80-core

8x10 mesh NoC, ~365 GB/s aggr. @ 5.7 GHz

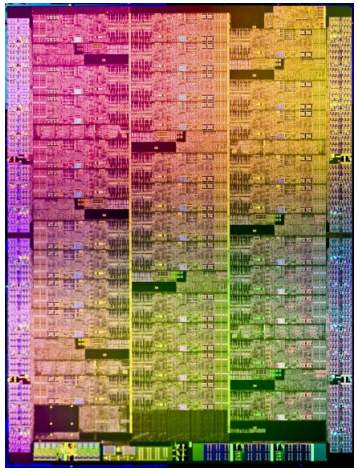
RESEARCH

Intel Single-Chip Cloud Computer

2009, 48-core, x86

6x4 mesh NoC, 256 GB/s bisection

RESEARCH

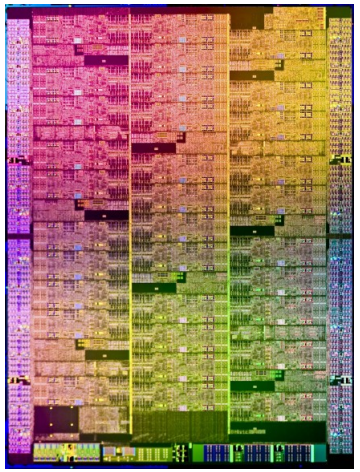


Intel "Knights Corner"

2011, 50-core, x86

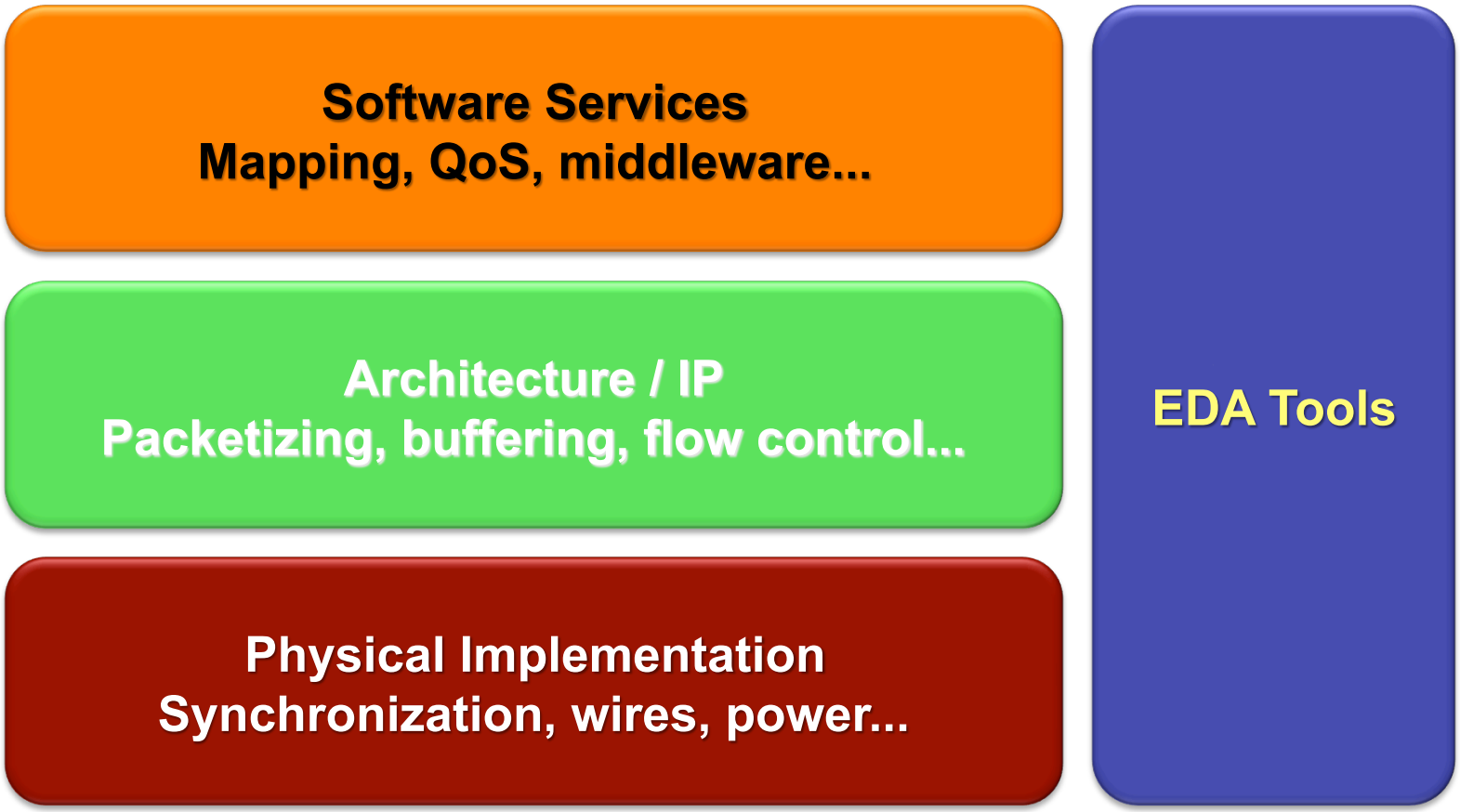
PRODUCT

Industry Traction



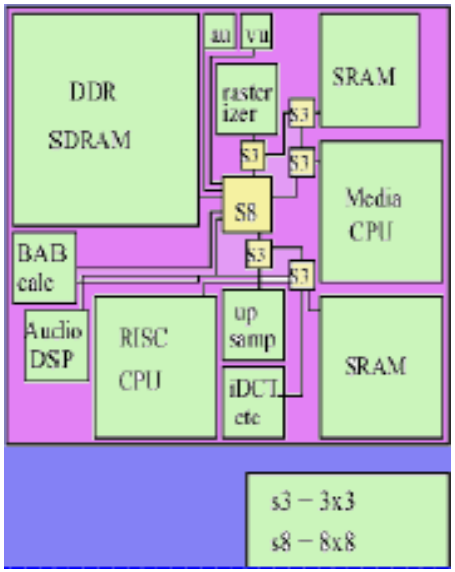
- Large semiconductor vendors
  - Intel: multicore x86
  - STMicro: STNoC for SoCs
  - NXP: Æthereal (now w/Virage/Synopsys)
  - Research efforts by many other players
- IP vendors
  - ARM's AMBA 3 and 4
  - Sonics
  - Arteris
  - Silistix
  - NoCs in use today in products by TI, Toshiba, …
- Specialized product vendors
  - Tilera, Recore, …

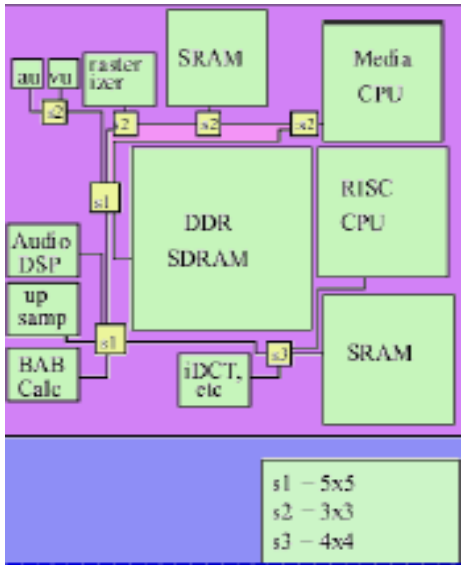
The NoC Framework

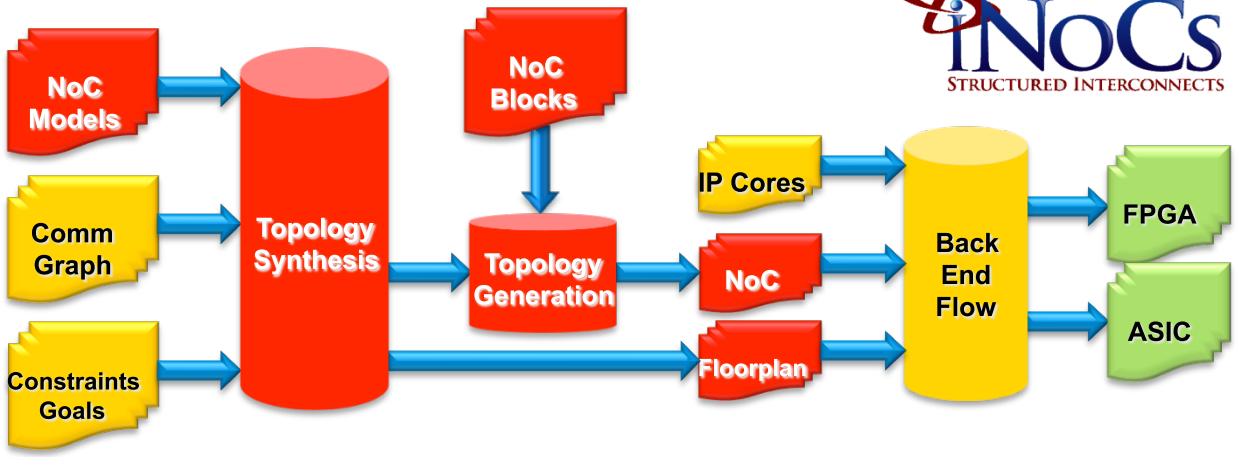


Design automation for NoCs

- Large design space
  - What topology
  - Which mapping
  - Which routes to use
- Optimize parameters
  - Link width, buffer sizes
- Simulate, verify, test







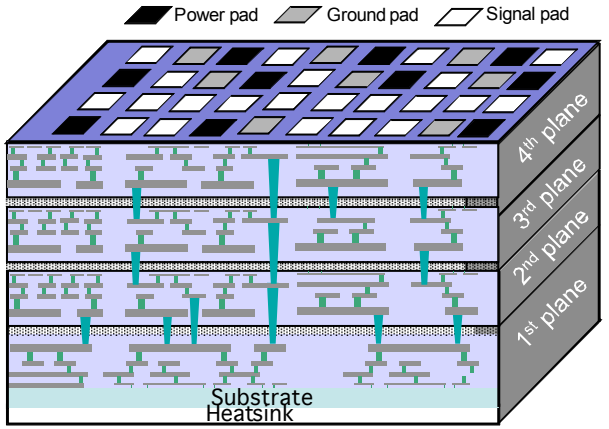
iNoCs
STRUCTURED INTERCONNECTS

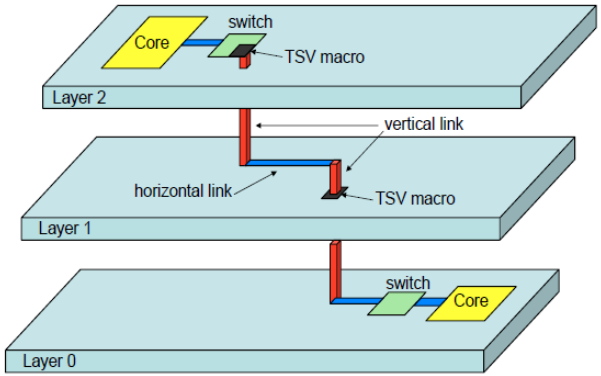
SEVENTH FRAMEWORK PROGRAMME

The vertical dimension

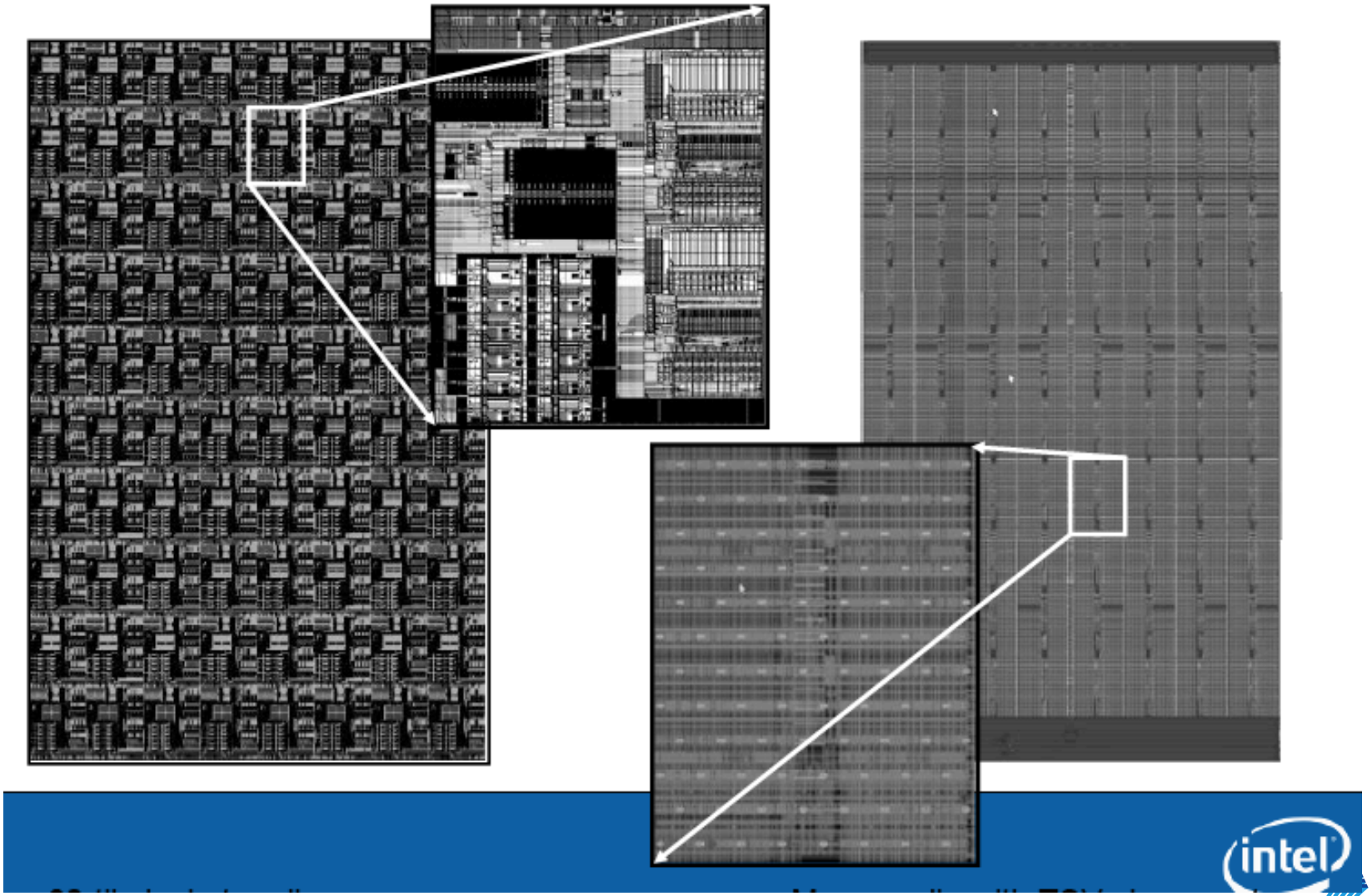
3-Dimensional integration

- Denser computational structures
  - Exploit *through silicon vias*
  - Shorter connections and access time
- Easier heterogeneous integration
  - Digital, analog, RF
- Strong thermal requirements
  - Heat generation, propagation and remova
- Novel design challenges
  - Routing, signal integrity, power distributio
- Reconfigurability
    - 3D networks on chip



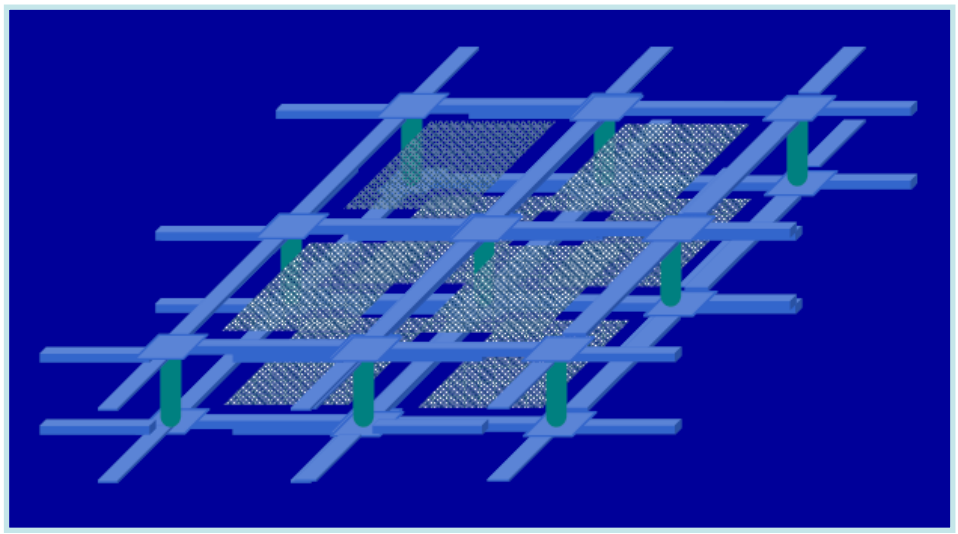


Processor and memory 3D integration



3D NoCs

- Which topology, switches, layers and floorplan locations?
- Meet application constraints
  - Bandwidth, latency
- Meet 3D technology constraints
  - Maximum available TSV constraints
  - Communication between adjacent layers



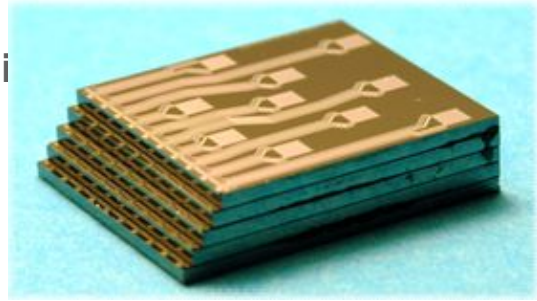
Thermal management

- Large power generation
  - Extract heat
  - Reduce temperature *gradients* in space and time
- Control *policies* for temperature management
  - Control clock and Vdd – heat generation
  - Control cooling flow – heat extraction
- *Holistic* approach to run-time control
  - Temperature, reliability, power dissipation

CMOSAIC

3D stacked architectures with interlayer cooling

John Thome (EPFL)



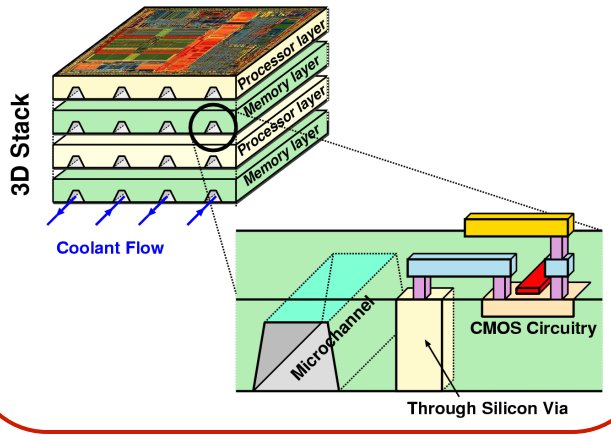
- 3D stacks of computer chips allow a huge functionality per uni
- Recent progress in the fabrication of through silicon vias

→ new ways for high density array interconnects between stacked processor & memory chips

BUT heat needs to be removed ! [each layer dissipates 100-150 W/cm^2]

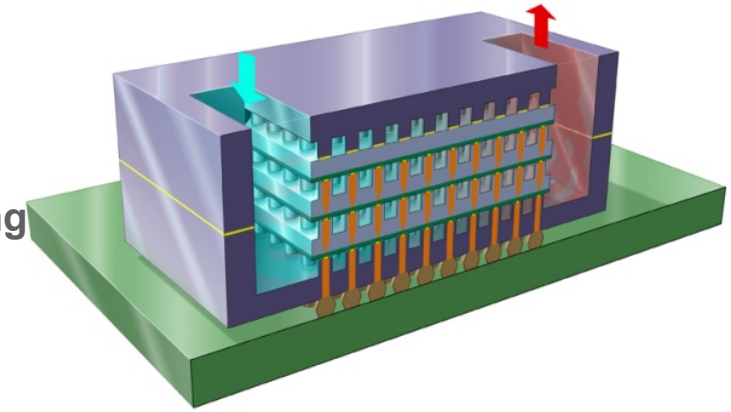
These 3D integrated circuits need novel electro-thermal co-design

Microchannels etched on back side of chips to circulate liquid coolant



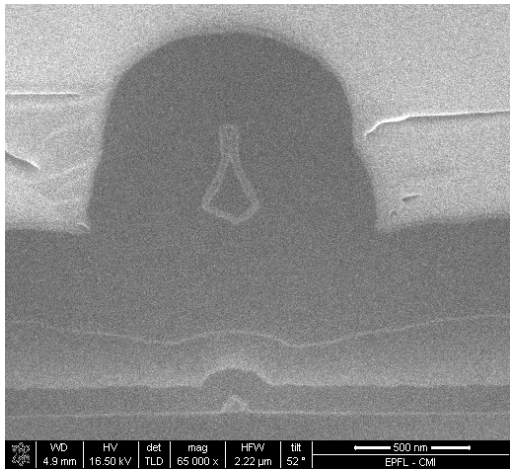
Interdisciplinary problem approached at various levels:

- architecture
- microfabrication
- liquid cooling
- two-phase cooling
- nano-fluids

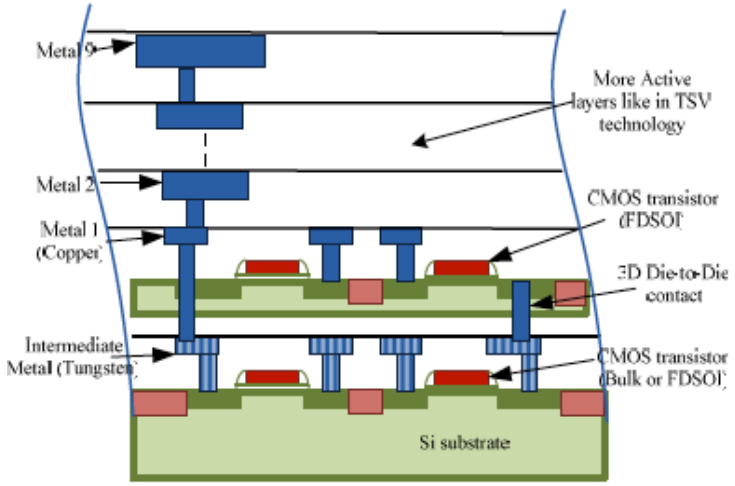


3D nano-devices

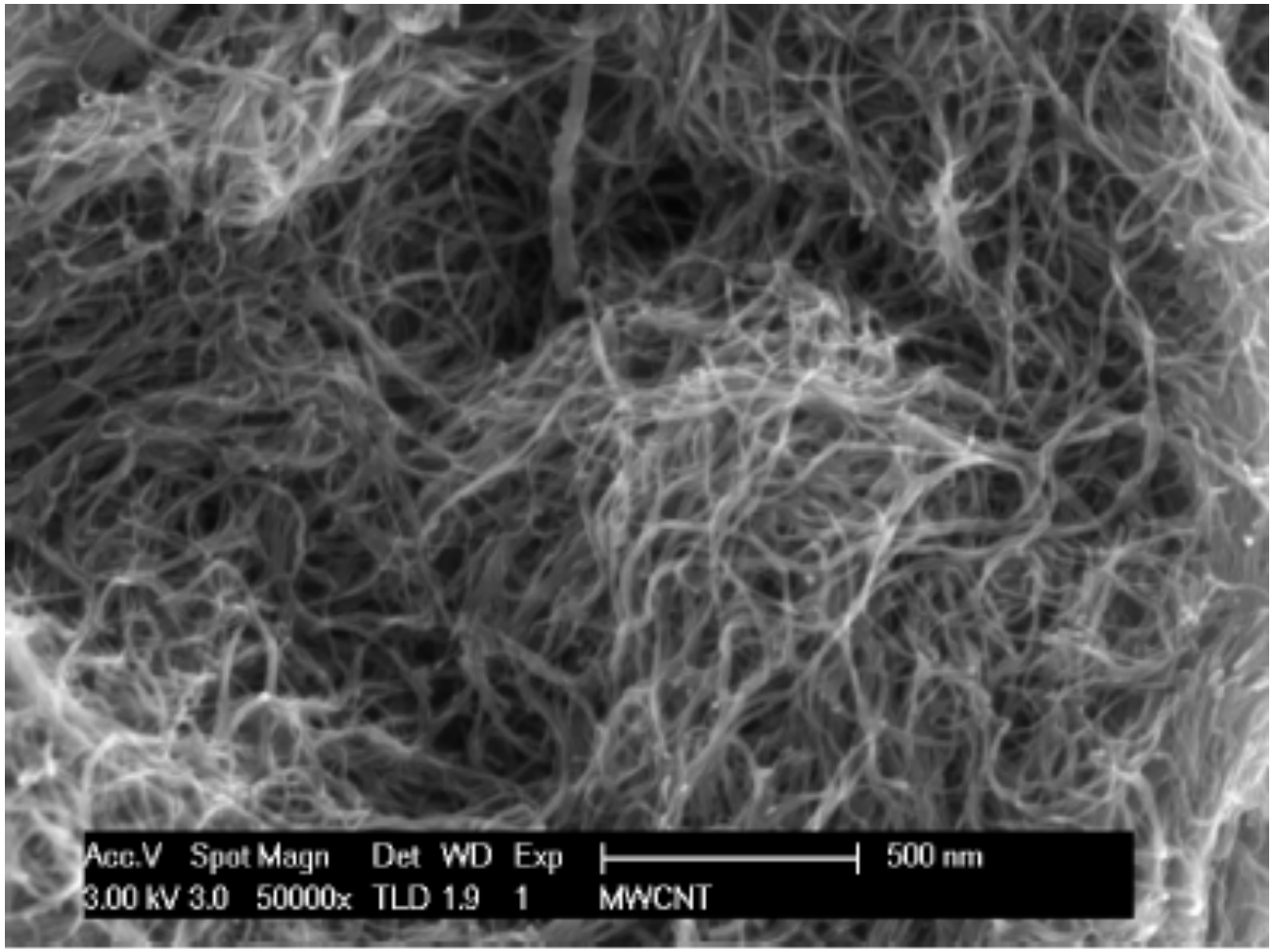
- Vertical stacking of SiNW
  - 3D cells with superimposed transistors



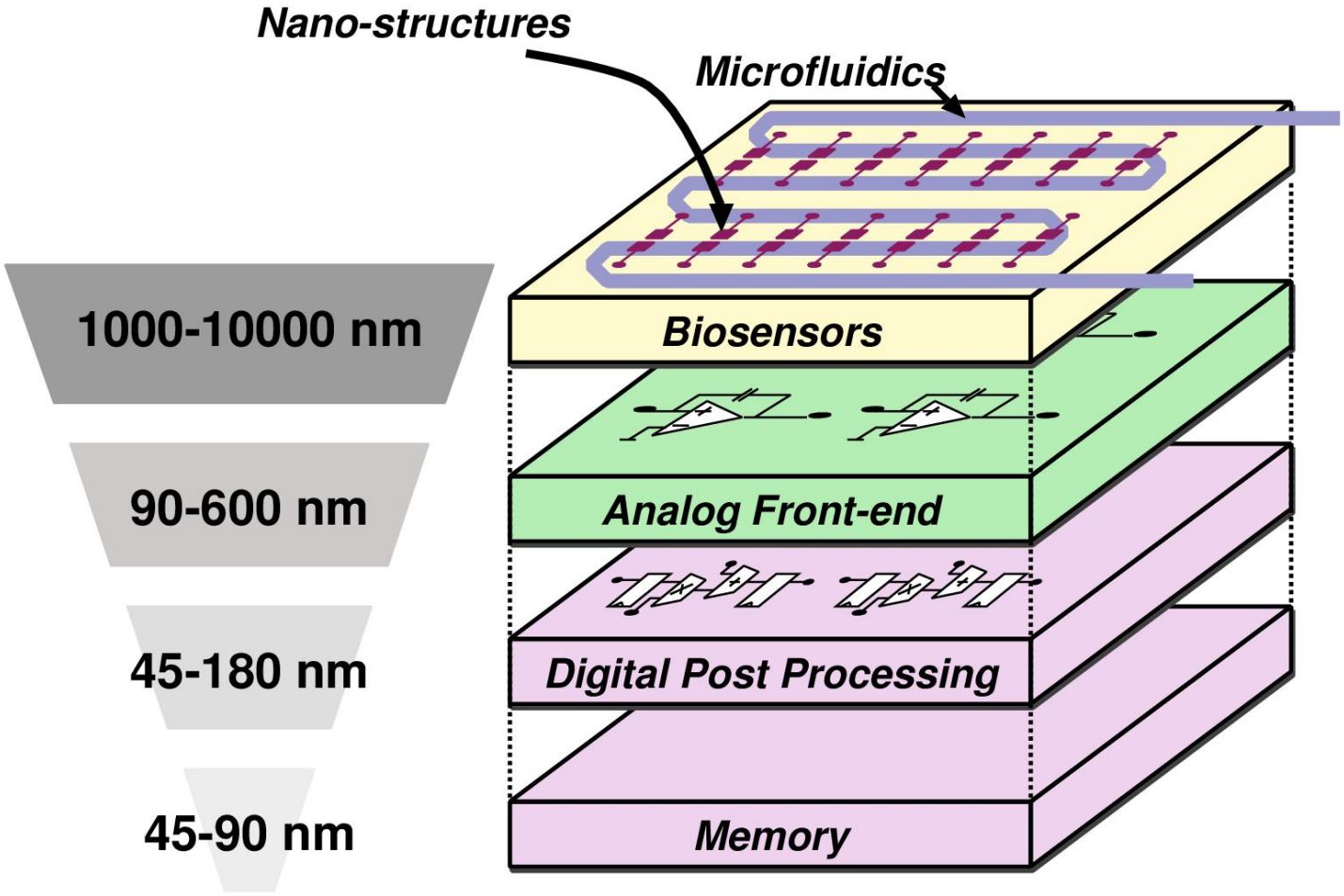
- Superposition of 2 CMOS layers [LETI]
  - 3D cells split on two layers

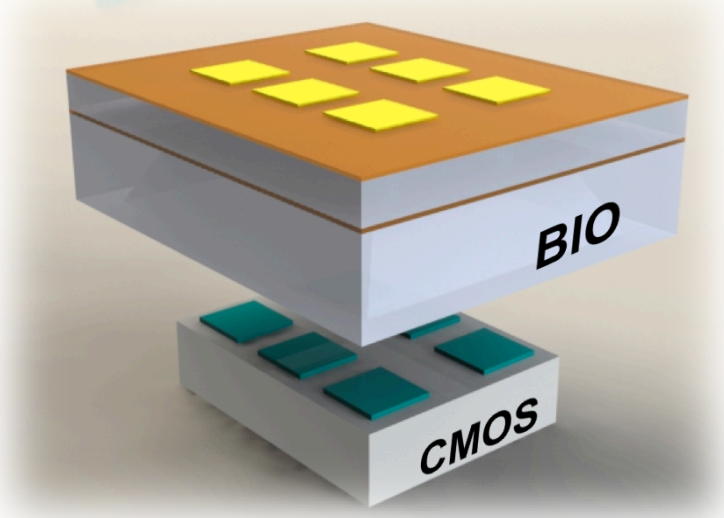


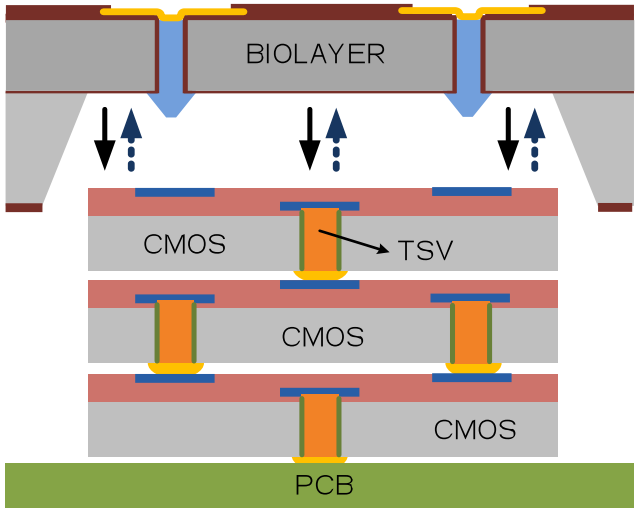
Nano-bio-systems

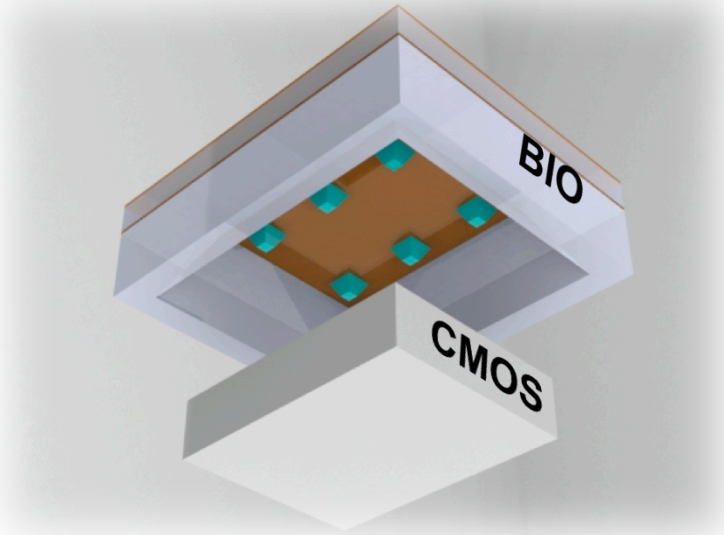


Nanosystems: the bio-layer









◆ No need for cleaning. Bio-layer is disposed after each measurement and CMOS layers are used repeatedly.

◆ Increased sensitivity and array density due to vertical interconnections from the bio-layer to the readout electronics.

◆ Sophisticated algorithms for highly-specific target identification run on-chip DSP and memory.

[C. Guiducci 2010]

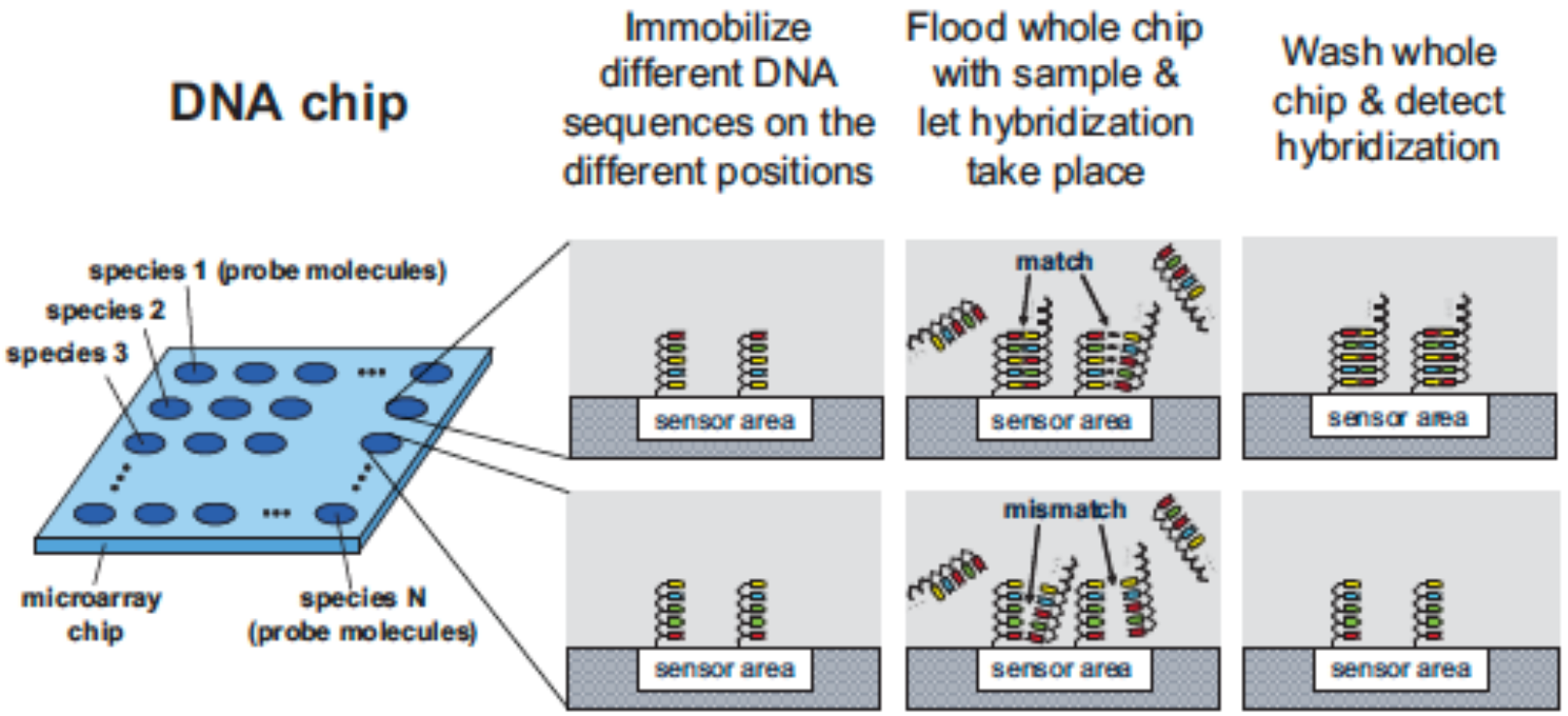
Electro-bio-systems

- Electronic processing of biological information
  - Autonomous (no human intervention)
  - Real-time
- Applications
  - Diagnostics
  - Environmental monitoring
- Targets
  - DNA, viruses, proteins, non-organic compounds

DNA microarray chips

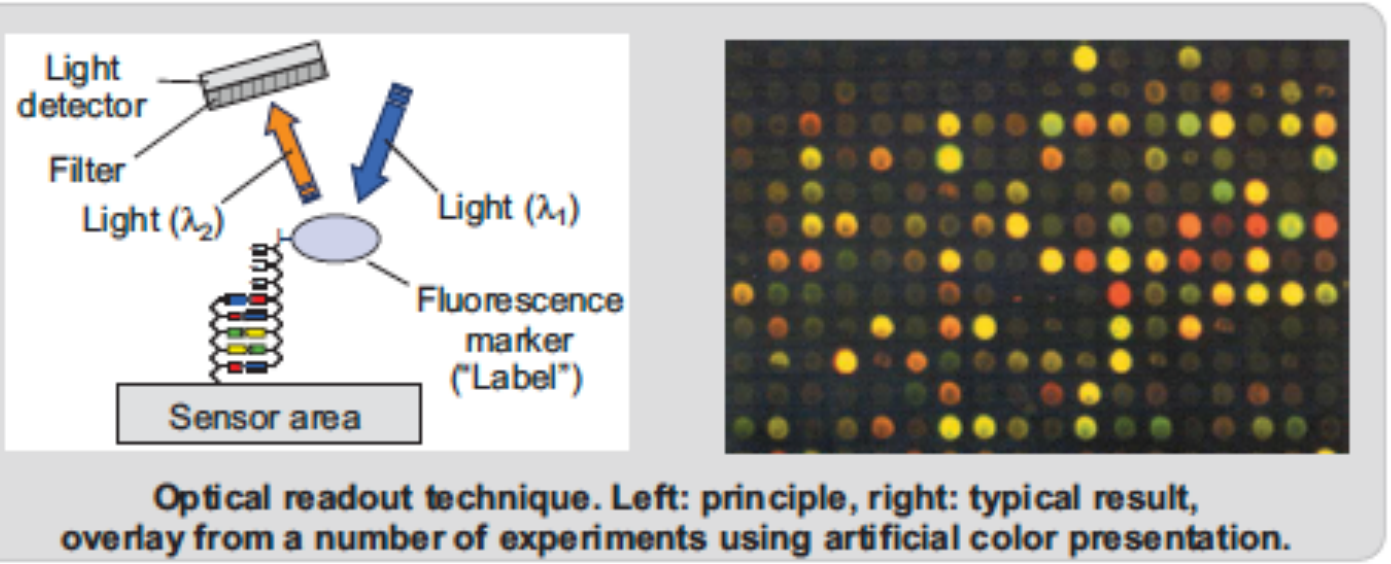
- Purpose:
  - Parallel detection of presence/absence of specific DNA sequences in a sample
  - Different from sequencing
  - High-throughput biology
- Various approaches
  - Optical reading
  - Labeled samples
  - Non-labeled samples
- Quantitative parameters
  - Size
  - Sensitivity
  - Specificity

Basic operating principles



[R. Thewes]

Basic operating principles

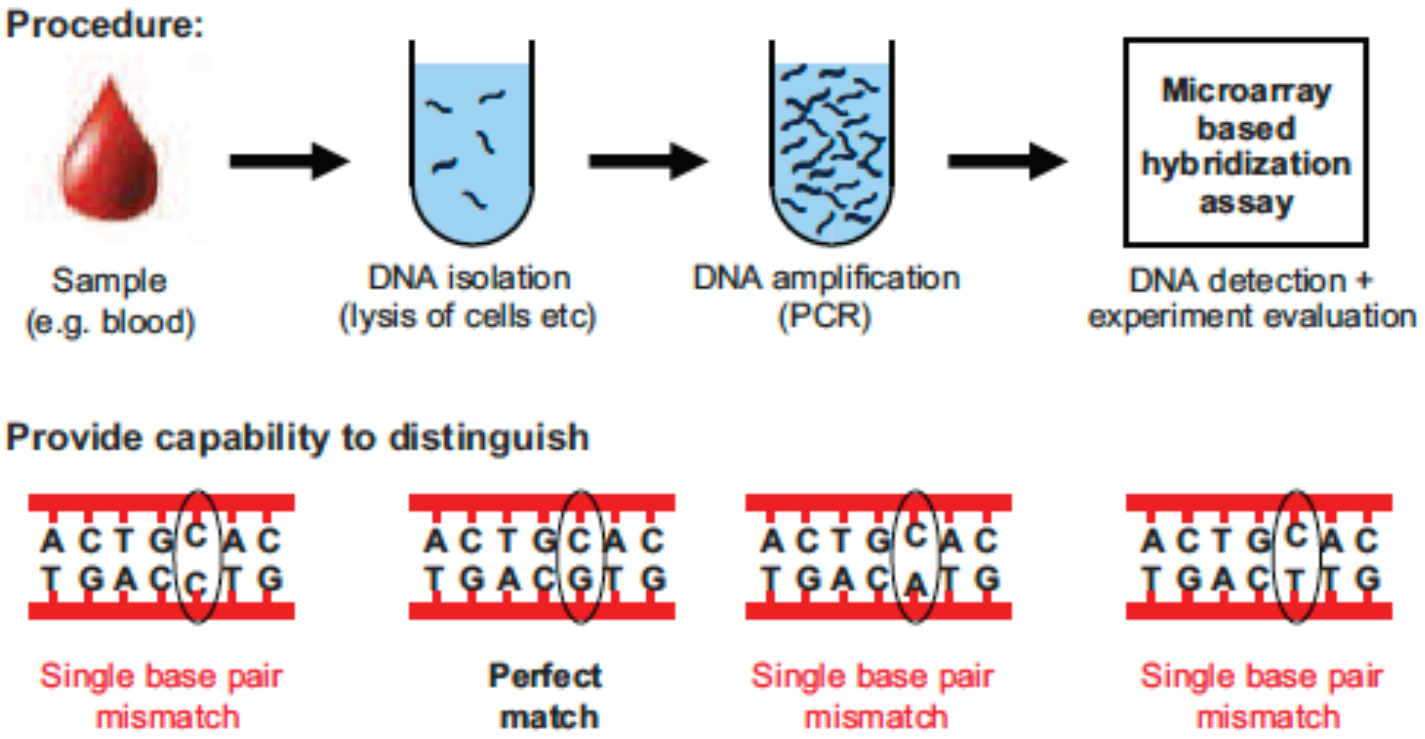


Optical readout technique. Left: principle, right: typical result, overlay from a number of experiments using artificial color presentation.

- Principle:
  - target strands are labeled with fluorescence marker molecules
  - chip is illuminated with light of wavelength λ_1
  - entire chip is scanned by a camera system and fluorescence light (λ_2) is detected
- Most commercially available systems are based on this detection method
- Alternative optical technique: chemiluminescence

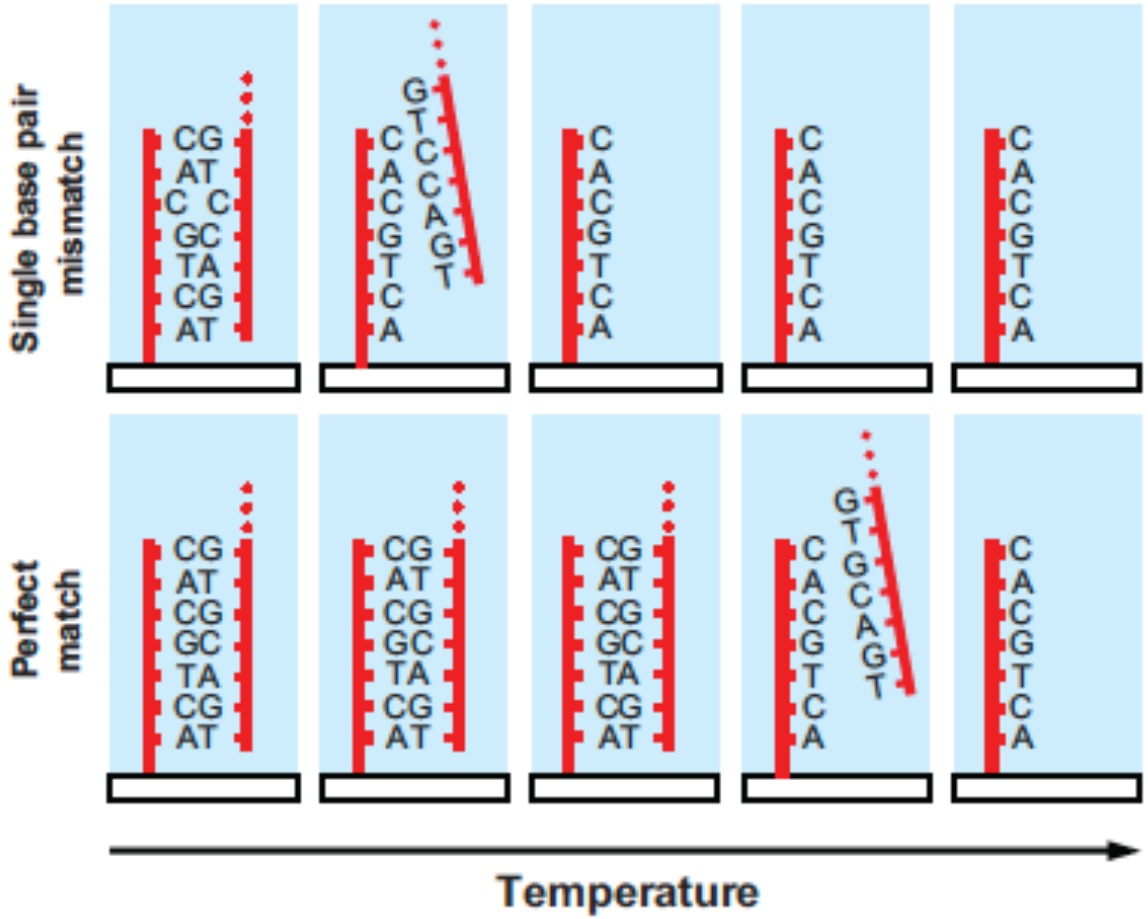
[R. Thewes]

Microarray



[R. Thewes]

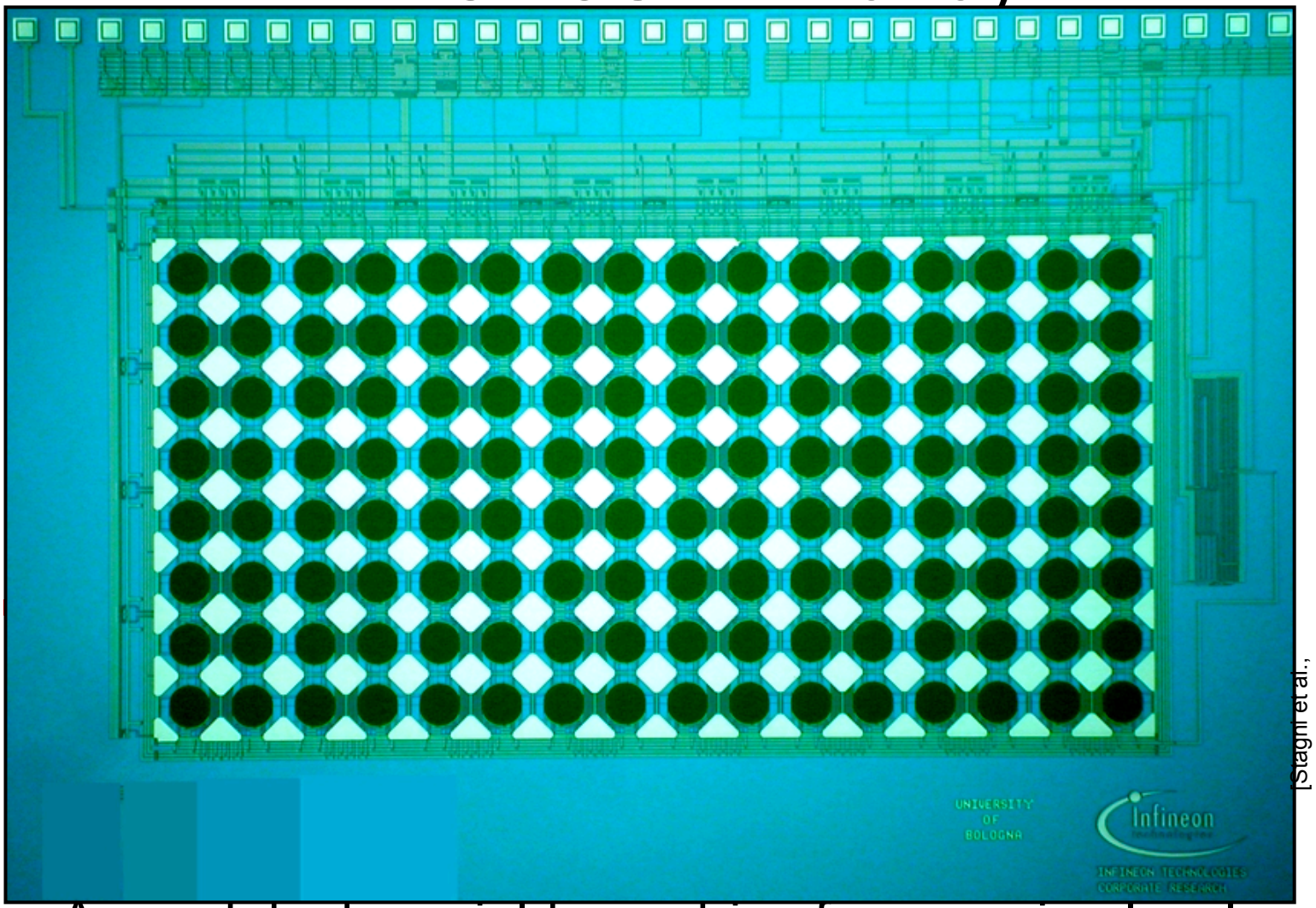
Specificity



High specificity is achieved by subsequent measurements under increasingly unfavorable binding conditions, e.g. at increasing temperature.

[R. Thewes]

CMOS DNA array

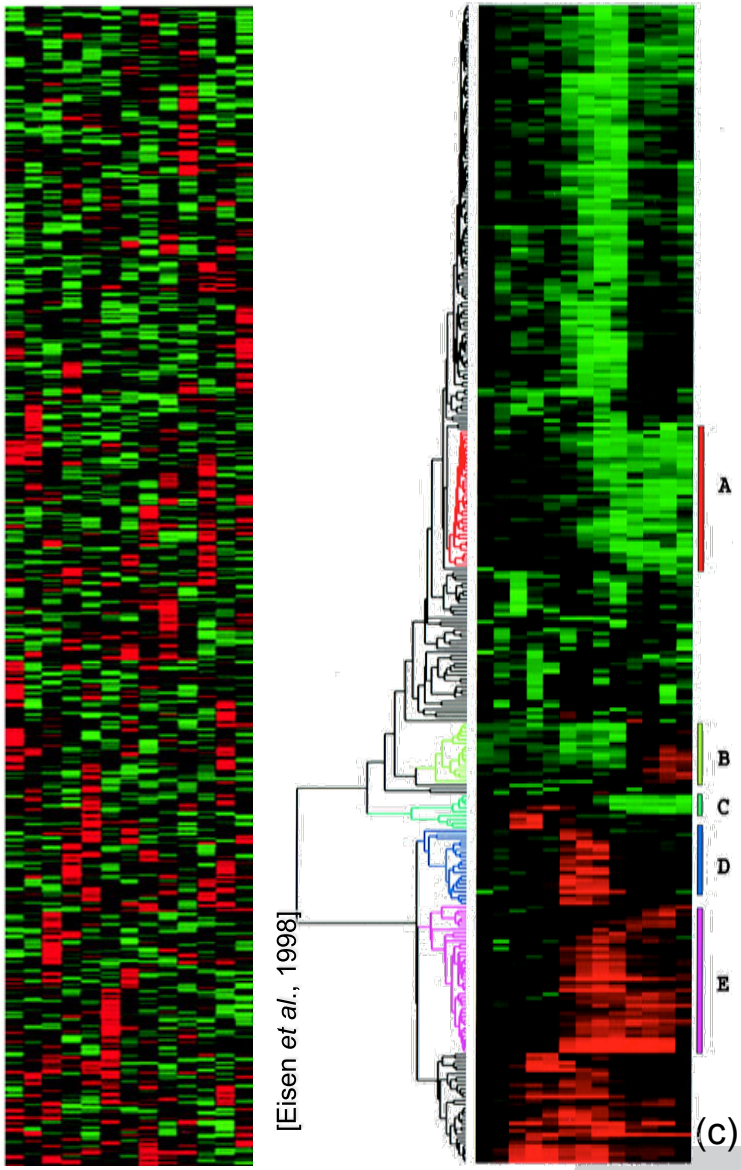


[Stagni et al., ISSCC]

- Array detectors yield a matrix of expression levels

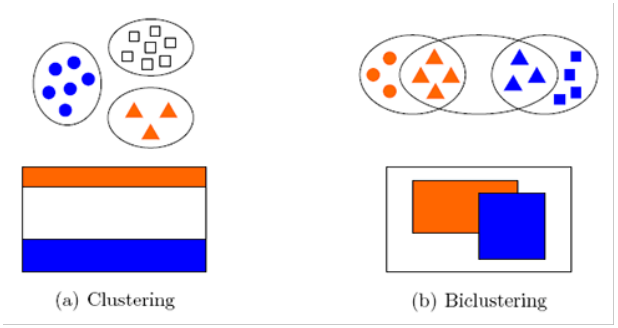
Data mining and interpretation

Data interpretation and clustering



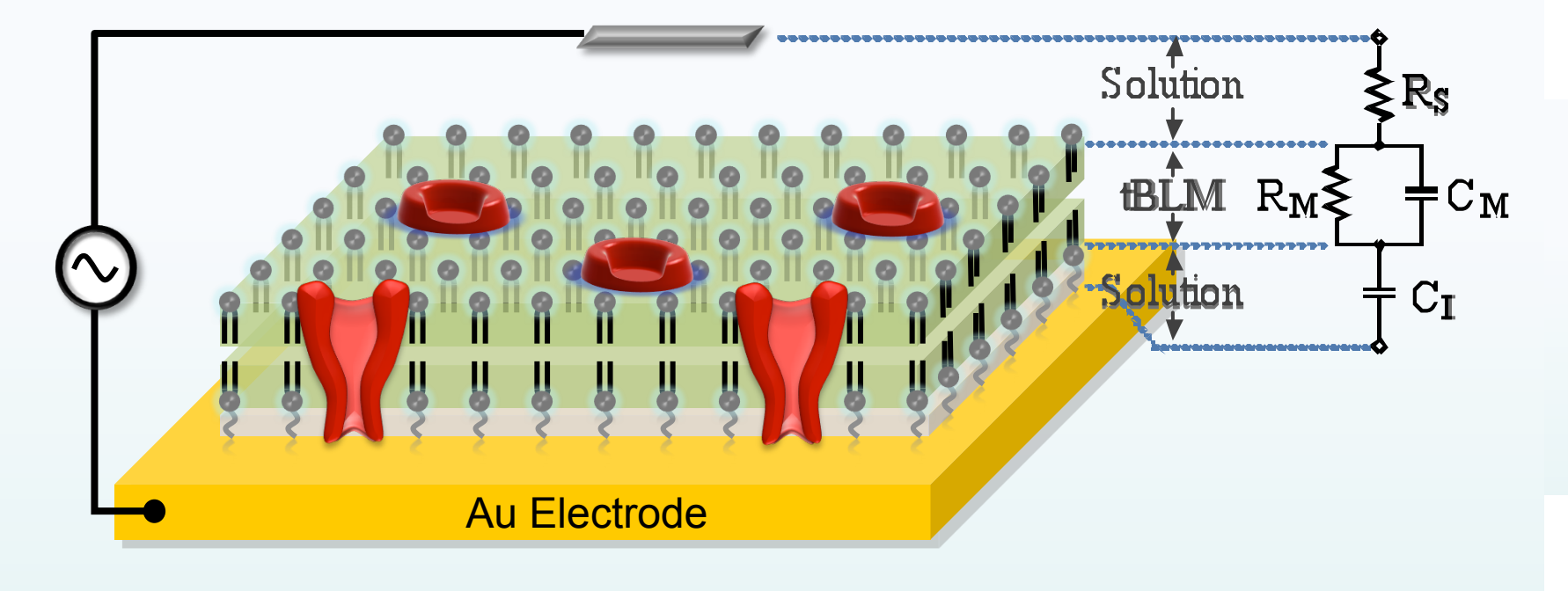
[Eisen *et al.*, 1998]

- Grouping similar objects together
  - Detecting gene variations consistent with the sample choice
  - Inference of specific conditions
- Bi-clustering on large data sets
  - Simultaneous cluster of subsets of rows and columns
    - Gene and samples



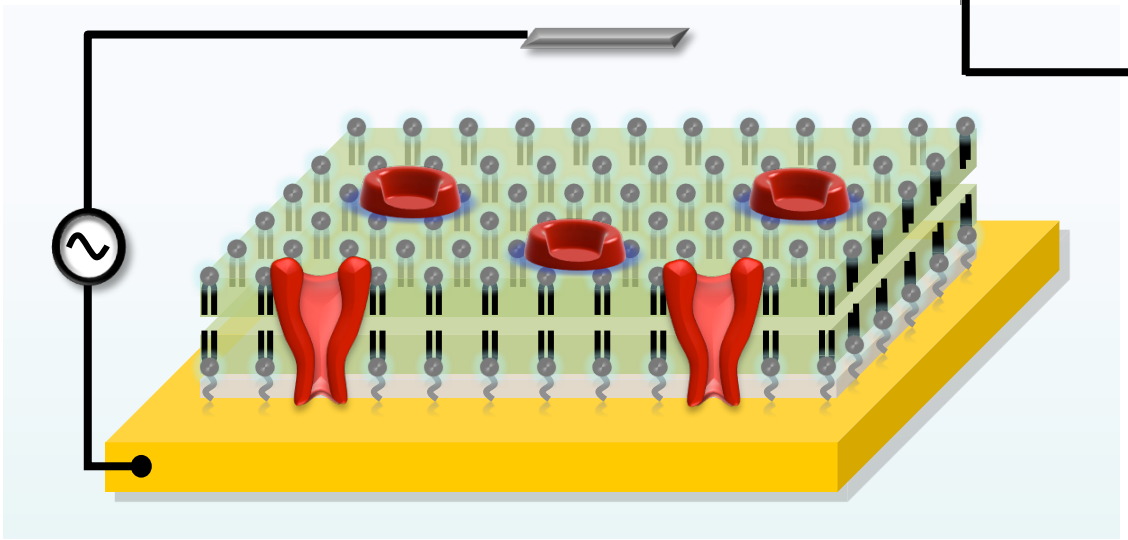
- Problem solved with ZDD technology
  - Fast and complete data interpretation

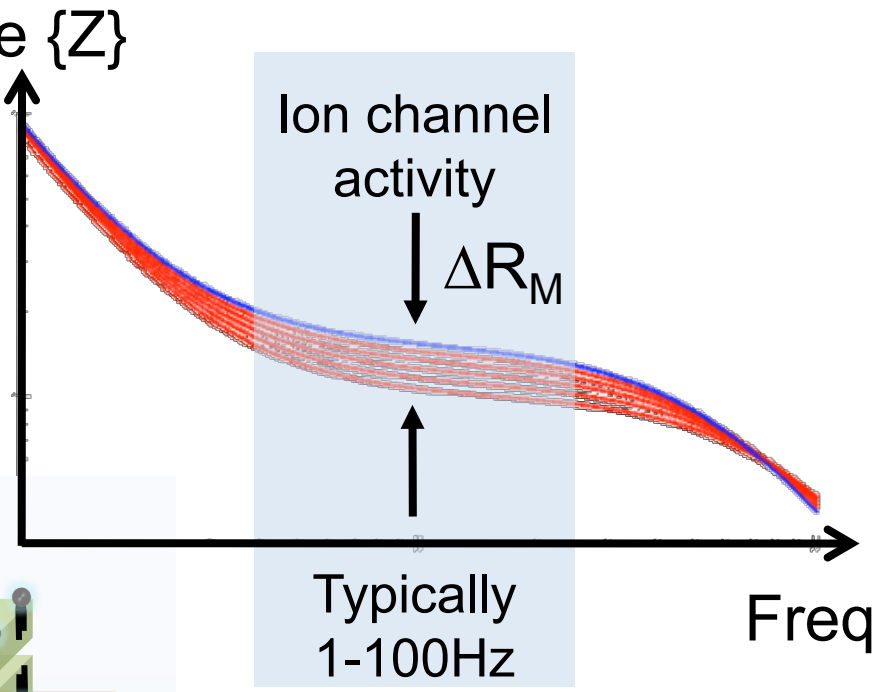
Advanced integrated sensors



Modulation of membrane resistance

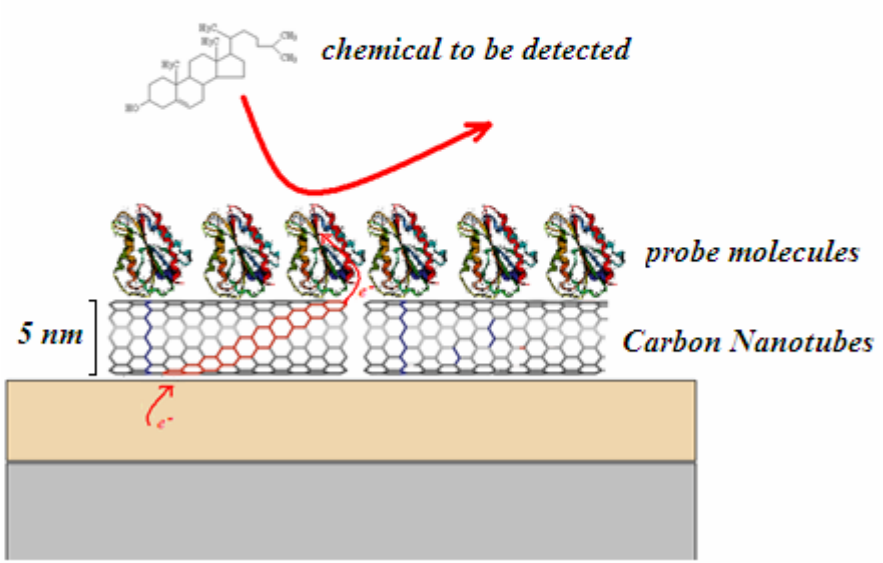
Modulation of the membrane resistance (R_M) is used to detect or quantify the ligand binding to an ion channel.

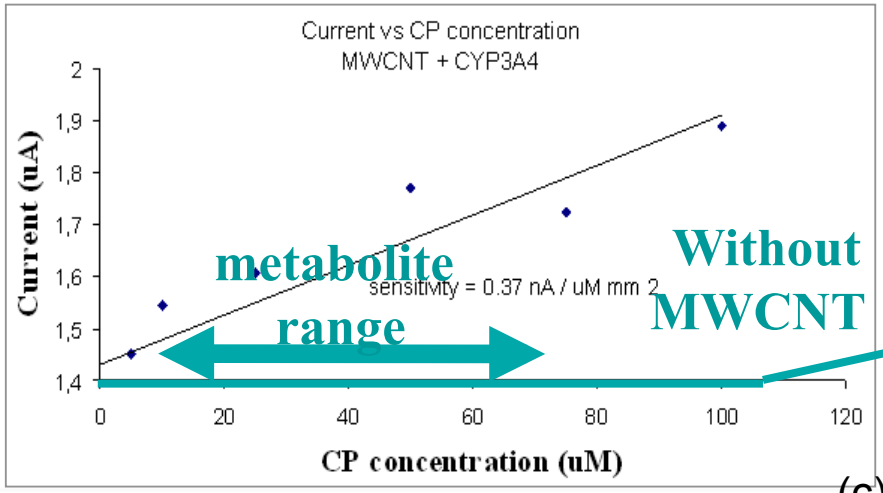


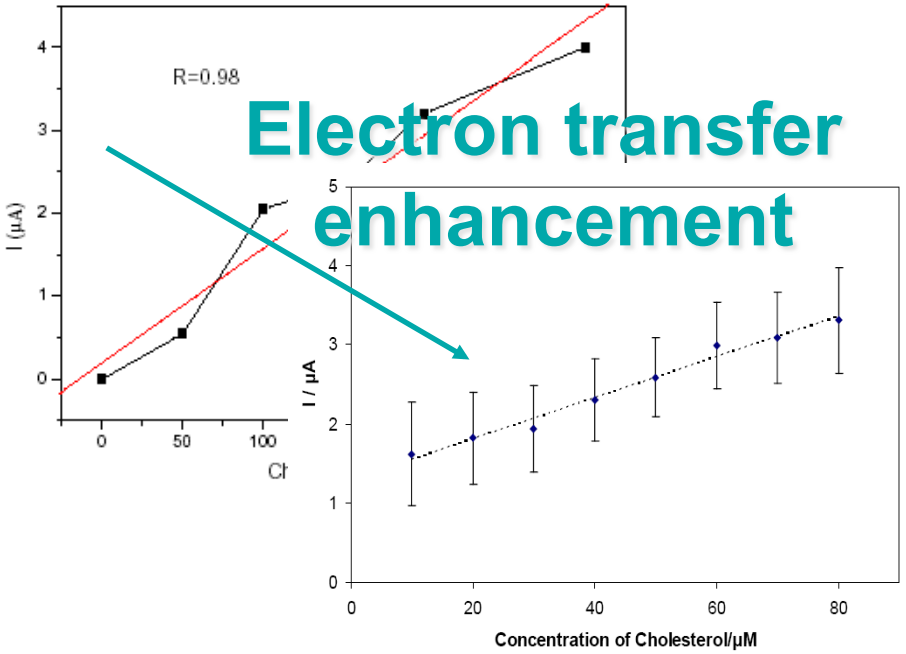


Increase of **Re(Z)** as a function of concentration is seen at mid-frequencies

CNT nanostructured sensors

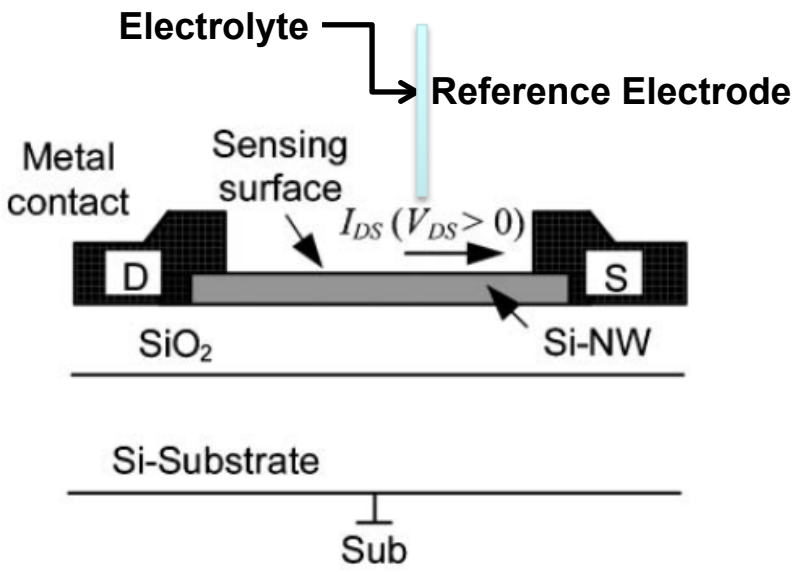






Cyclophosphamide detection - *S.Carrara*

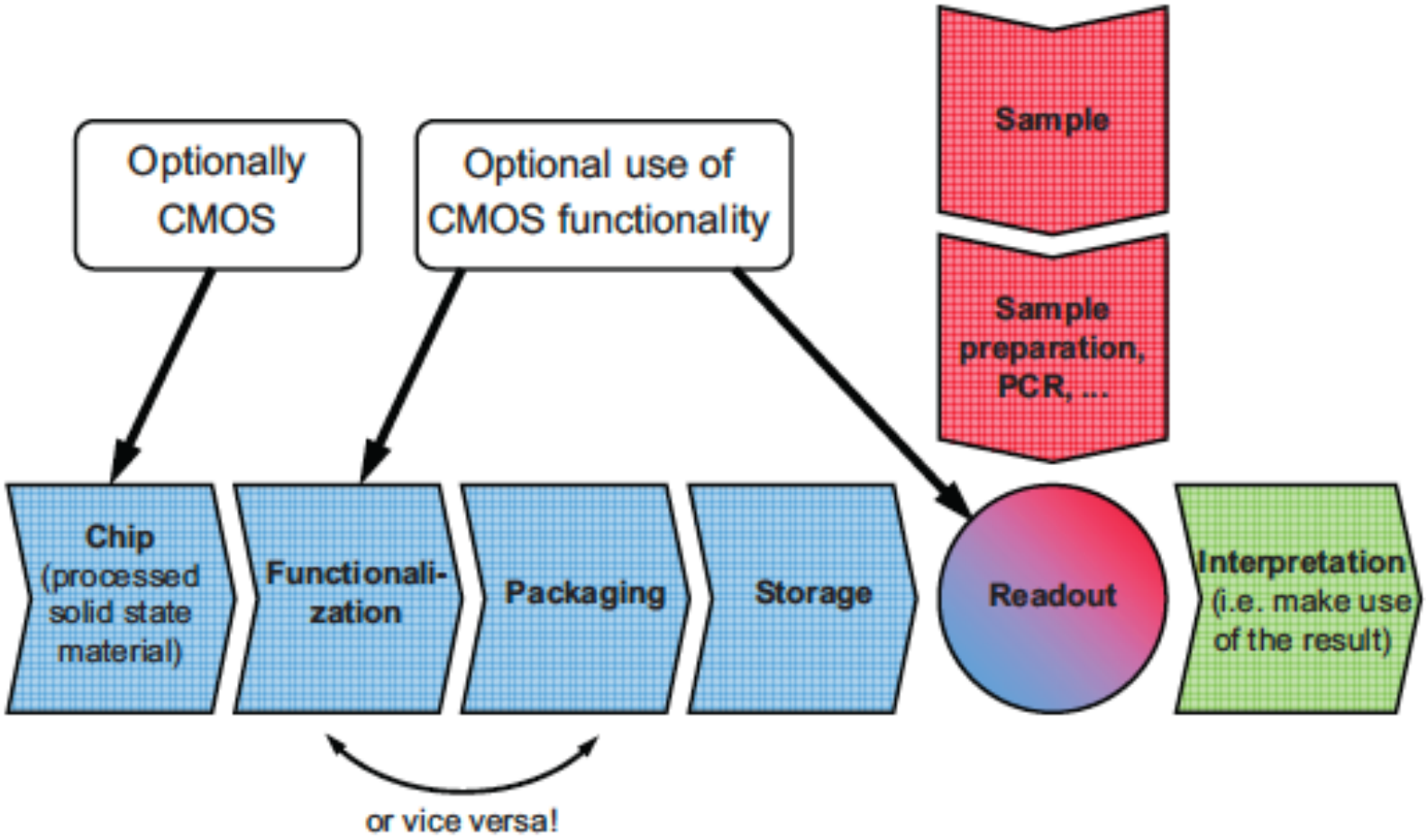
Silicon NanoWire sensors



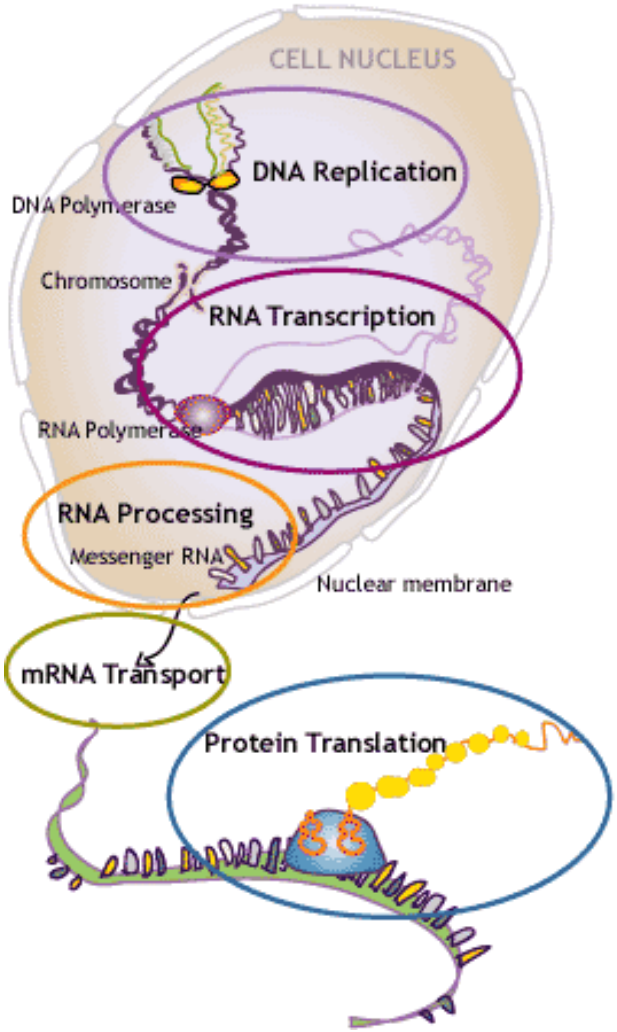
- High label-free detection sensitivities in aqueous phase
- Suitability for large-scale high density integration
- Scaling width from 200 nm to 50nm would result in a 20× increased sensitivity

[E.T. Carlen and A. van den Berg, Lab-on-a-chip 2007]

Entire chain

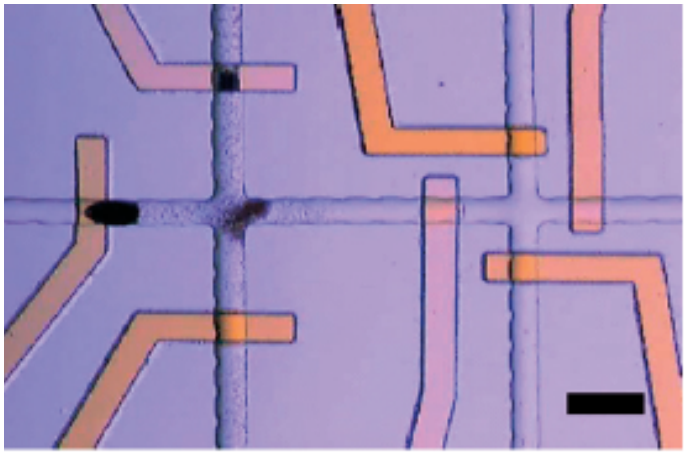


Advanced technological platforms for sample pre-treatment



Extraction of DNA from 28 cells

2004, Caltech

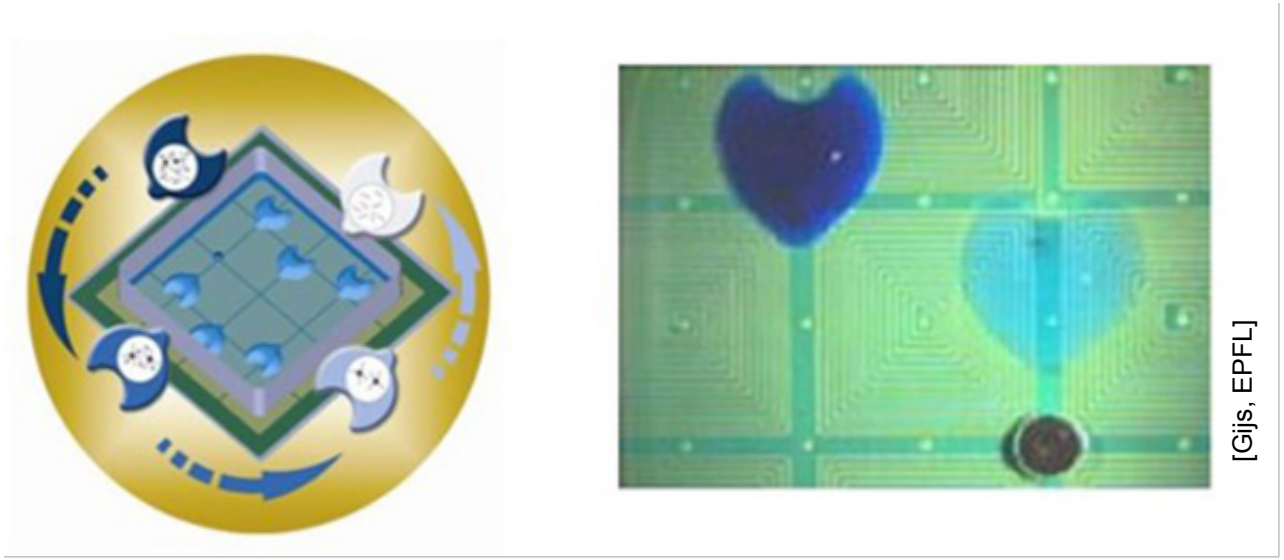


RTPCR
STMicroeletronics

Multiplying the DNA sample on a chips

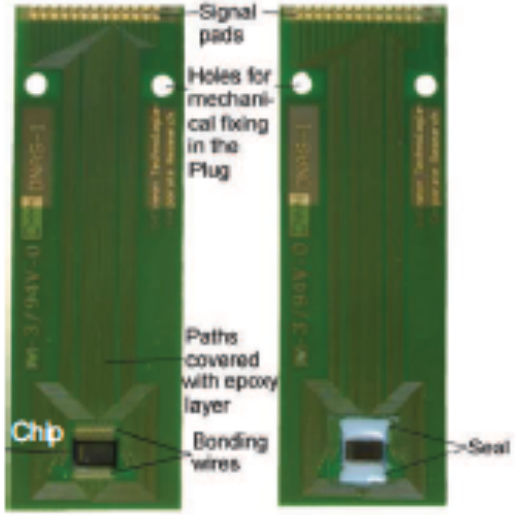
[C. Guiducci 2010]

Sample transport



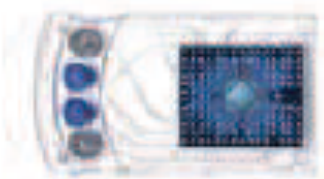
- Cell or sample transport, split and merge
  - On a 2-dimensional array
- Parallel scheduling and routing of multiple samples

Systems

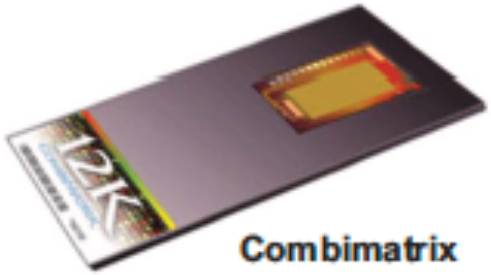


Infineon (until 2005)

- "open system"
- simple fluidic interface
- PCB-based electrical interface



Nanogen



Combimatrix

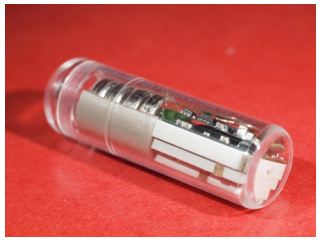
- fluidic interface with in-package microfluidics
- electrical interface with in-card electrical interconnects

Siemens (under development)

- fluidic + electric interface with in-package microfluidics and in-card el. interconnects
- in-card stored bio-chemical compounds

Complexity

Nano-systems: applications

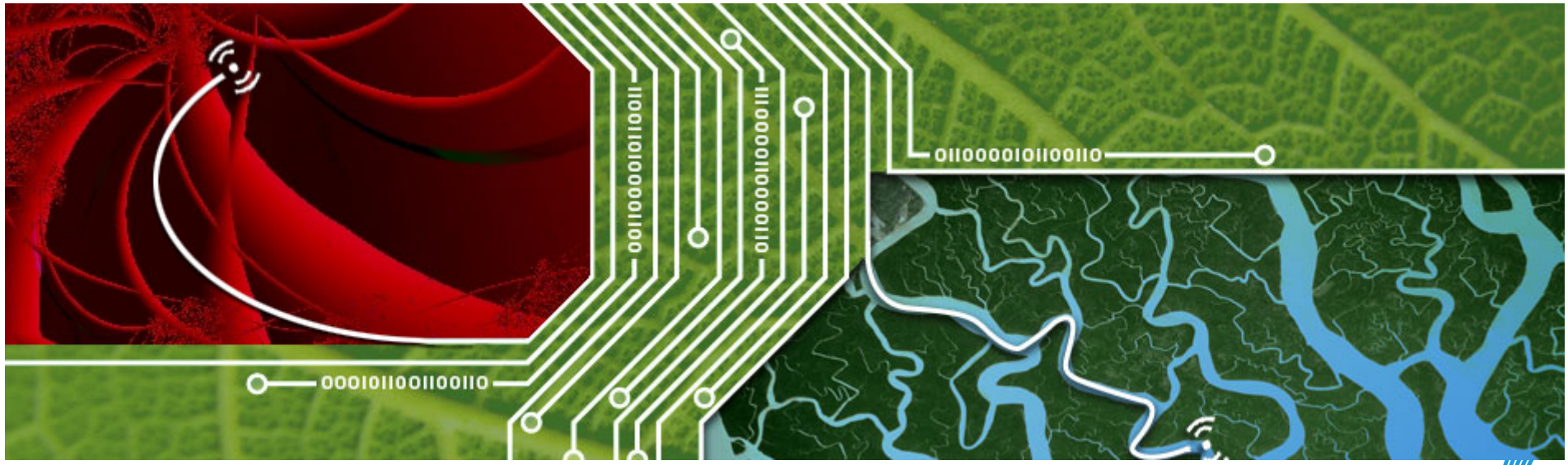


Nanosystems applications

- Health:
  - High-throughput biology, real-time medical monitoring
- Environmental monitoring:
  - Weather, pollution, seismic analysis
- Security:
  - Cryptography, secure communication
- Computing, communication, control
  - Scientific and consumer applications
- Defense:
  - Design of command and control systems

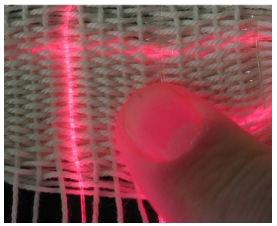
Nano-Tera.ch

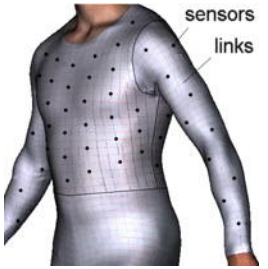
- Health:
  - High-throughput biology, real-time medical monitoring
- Environmental monitoring:
  - Weather, pollution, seismic analysis
- Security:
  - Cryptography, secure communication

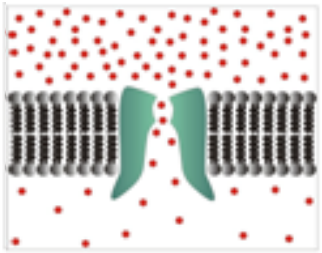


Electronic health

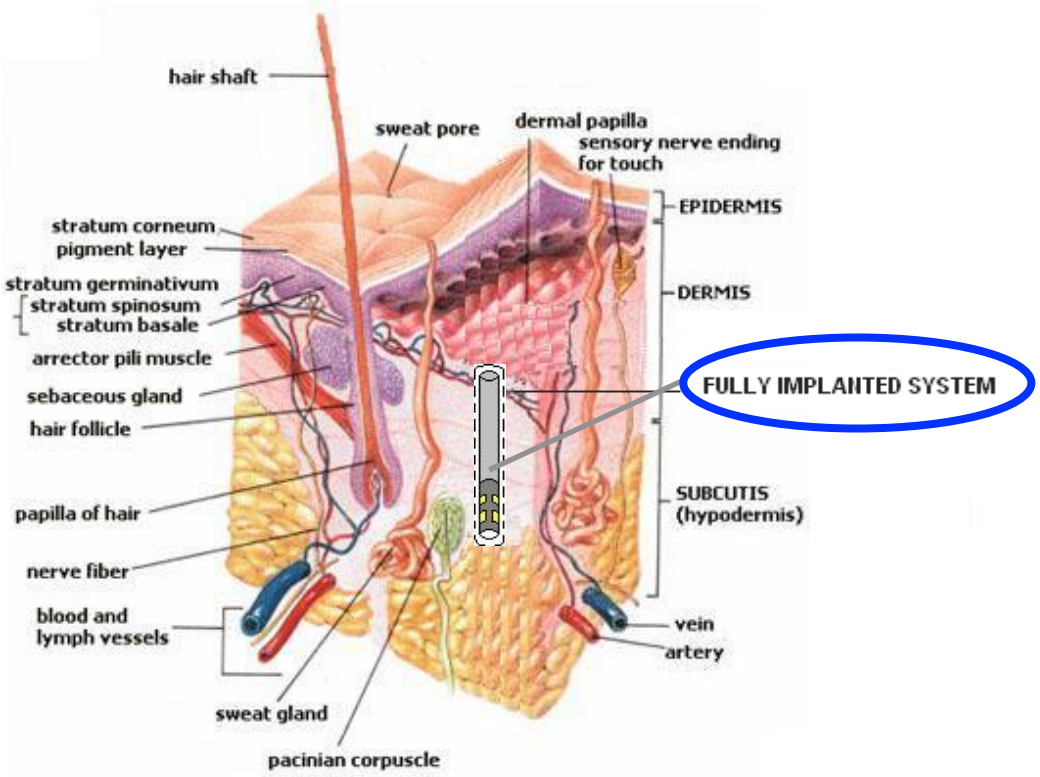
- Body monitoring
  - Biosensors
  - Body area networks
  - Smart textiles
- Clinical support
  - Remote diagnosis
  - Drug delivery
- Prevention
  - Monitoring nutrition
- *Challenges:*
  - *Non-invasiveness*
  - *Safety and security*

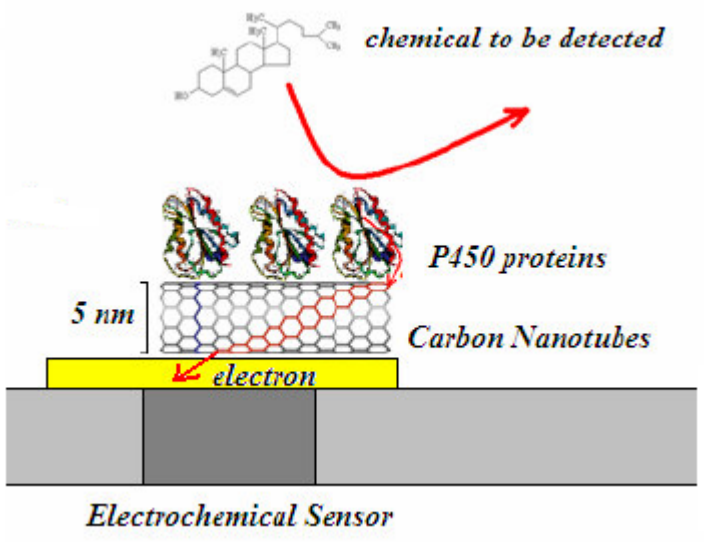


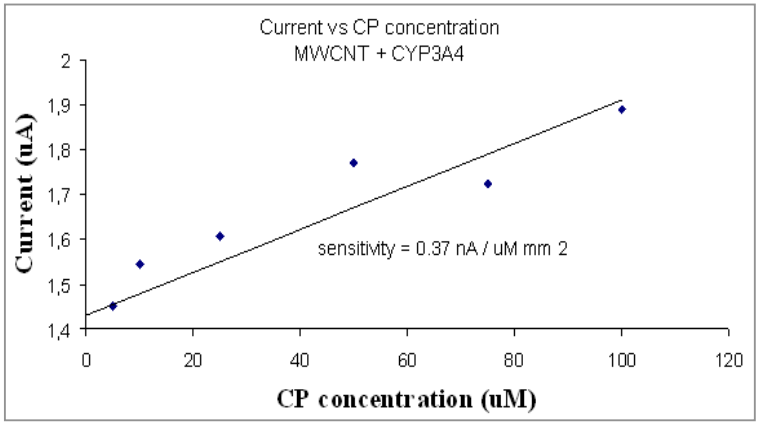




Example: smart implants







Environment

- Monitoring heat, wind, vibration
  - Earthquake, flood prediction
  - Movement of glaciers
- Controlling pollution
  - Water, air purity
  - Bio-contamination
- Emergency relief control
  - Real time support for reaction
- *Challenges:*
  - *Seamless presence and biodegradability*
  - *Autonomous and adaptive operation*

Example: water purity

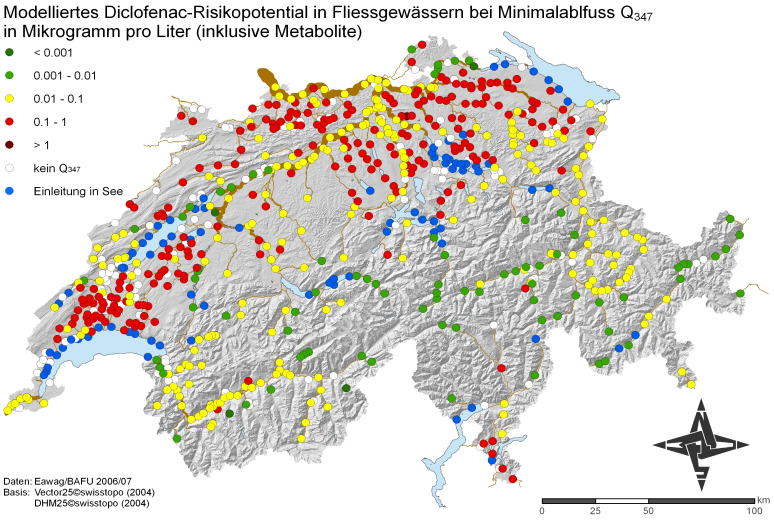
antenna

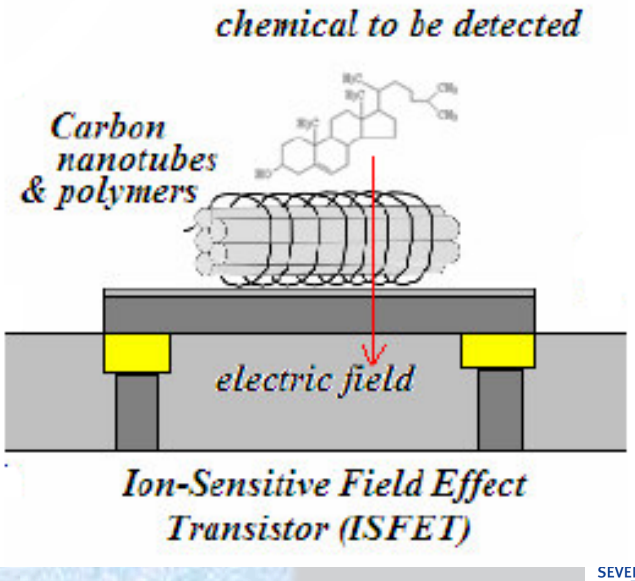
solar cells

sensors and electronics

water flow

pico-turbine





SEVENTH FRAMEWORK PROGRAMME

Human enhancement

- Deep interaction of nanosystems with humans
  - Deep brain stimulation
  - Prosthetics, artificial organs
- Correcting deficiencies, extending capabilities
  - Vision, audition, memory
  - Ethical and legal limitations

Conclusions

- Nano-systems exploit new technologies and devices:
  - *Silicon nanowire* and *carbon nanotube* devices
  - *Ambipolarity* can be efficiently used in logic design
  - *Memristive* effects can be effectively used for memory design
- New nano-architectures and design styles:
  - *Regularity* of the fabric is key to robustness
  - 3-Dimensional integration gives an extra degree of freedom
- Hybridization of new technologies opens new frontiers
  - Nano-bio-systems to probe and interact with living matter
  - Profound impact on health, environment and human evolution

Thank you