imec

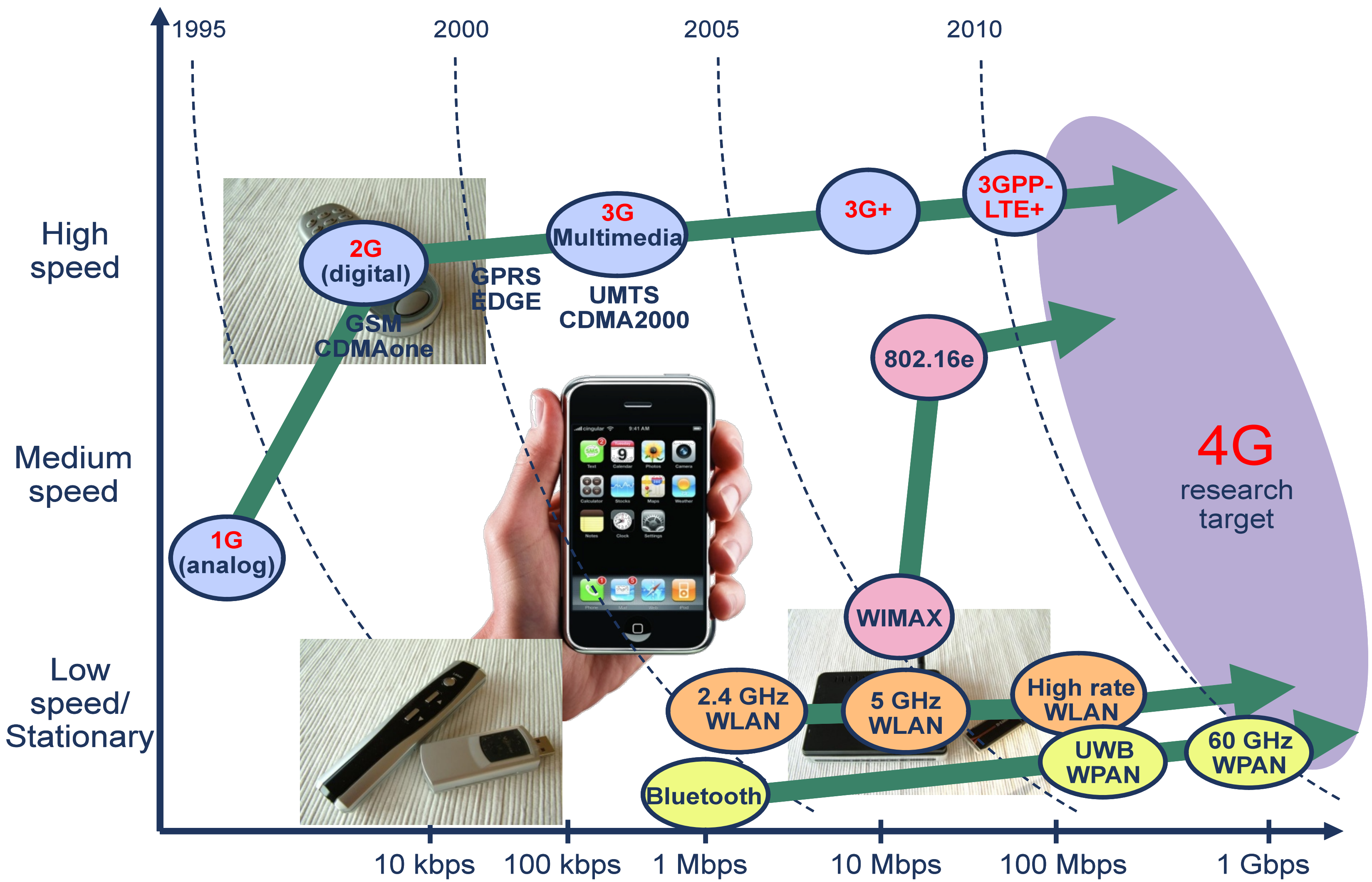
PARALLELIZATION STRATEGIES FOR WIRELESS BASEBAND

MARTIN PALKOVIC

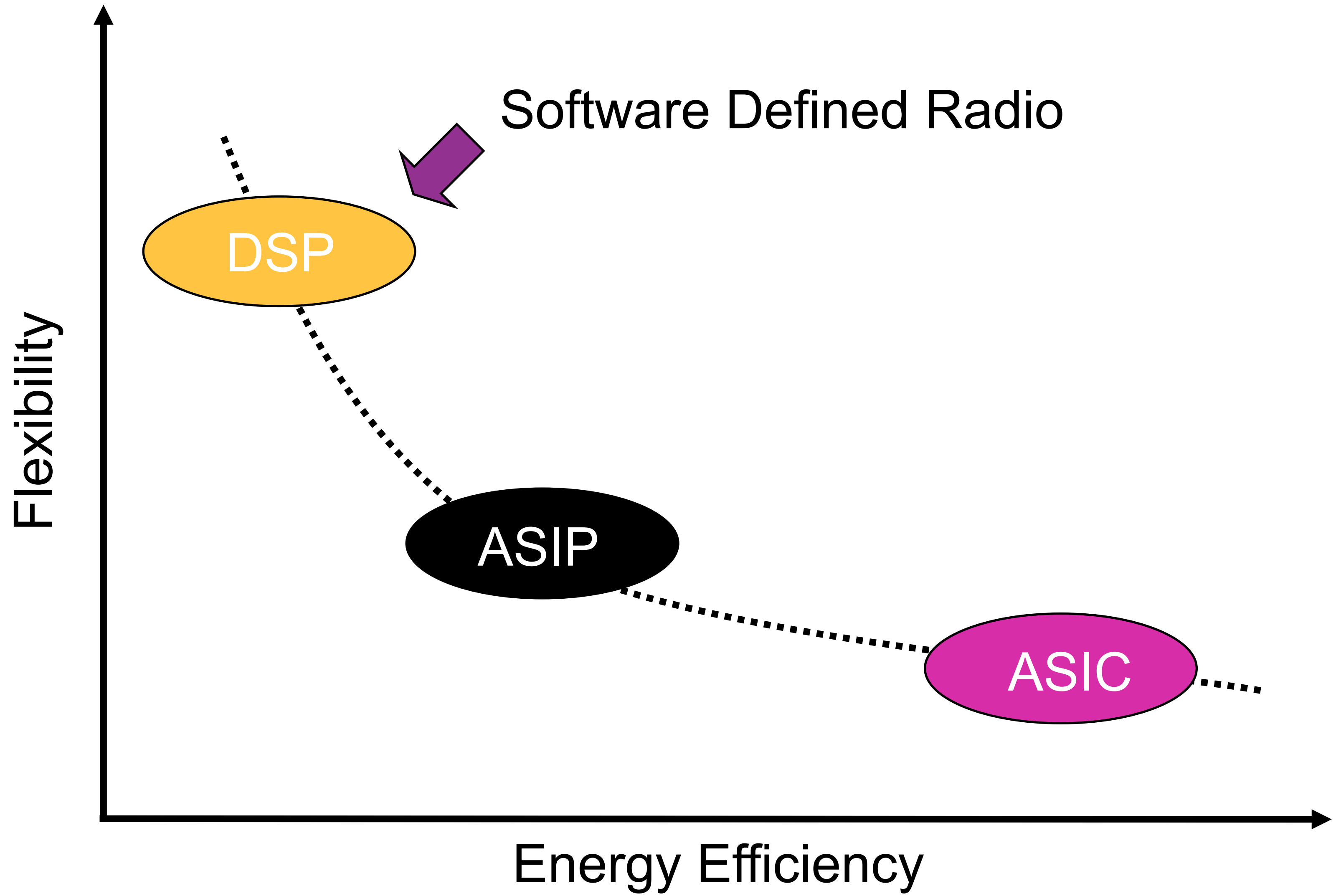
ARTISTDESIGN MPSOC CLUSTER MEETING

7TH JULY 2010

WIRELESS DOMAIN CONTAINS "SEA" OF STANDARDS; AND CUSTOMERS WANT TO HAVE THEM ALL IN ONE DEVICE



FOR MULTI-MODE >100MBPS WIRELESS COMMUNICATION SOFTWARE DEFINED RADIO (SDR) SOLUTIONS ARE CRUCIAL



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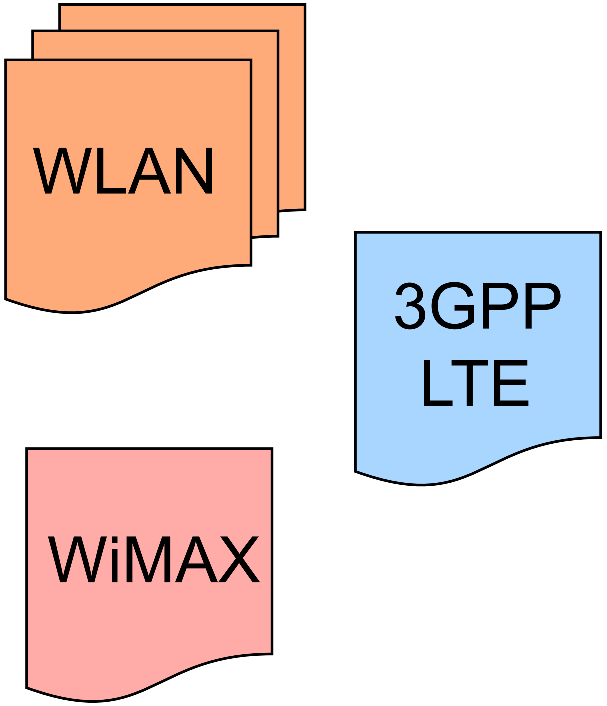
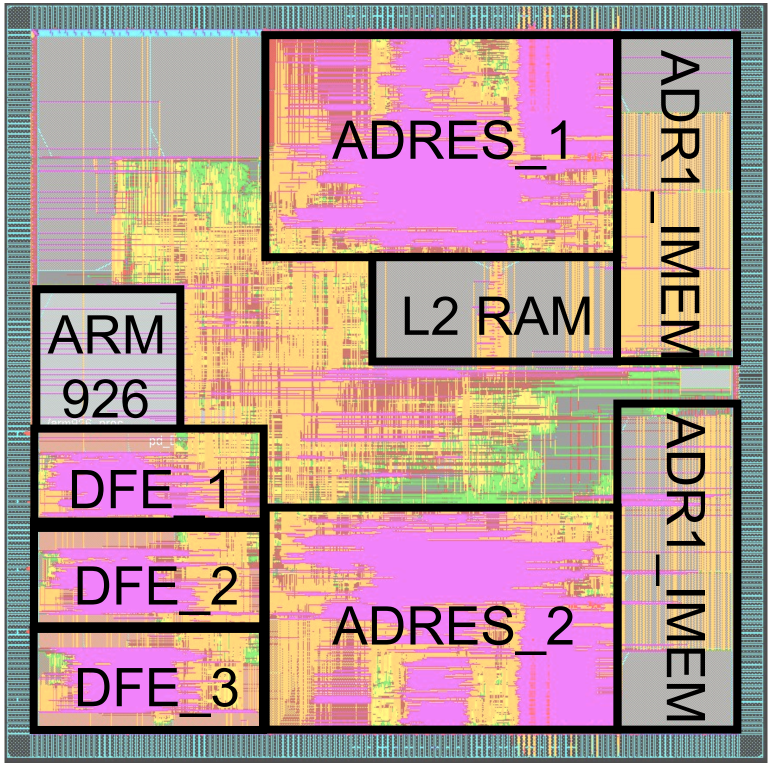
THERE IS A LONG WAY TILL STANDARD SPECIFICATION IS MAPPED ON THE SDR PLATFORM

Standard specification

SDR platform





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OUTLINE

IMEC SDR BEAR platform

Baseband SW mapping flow

- Sequential MATLAB code

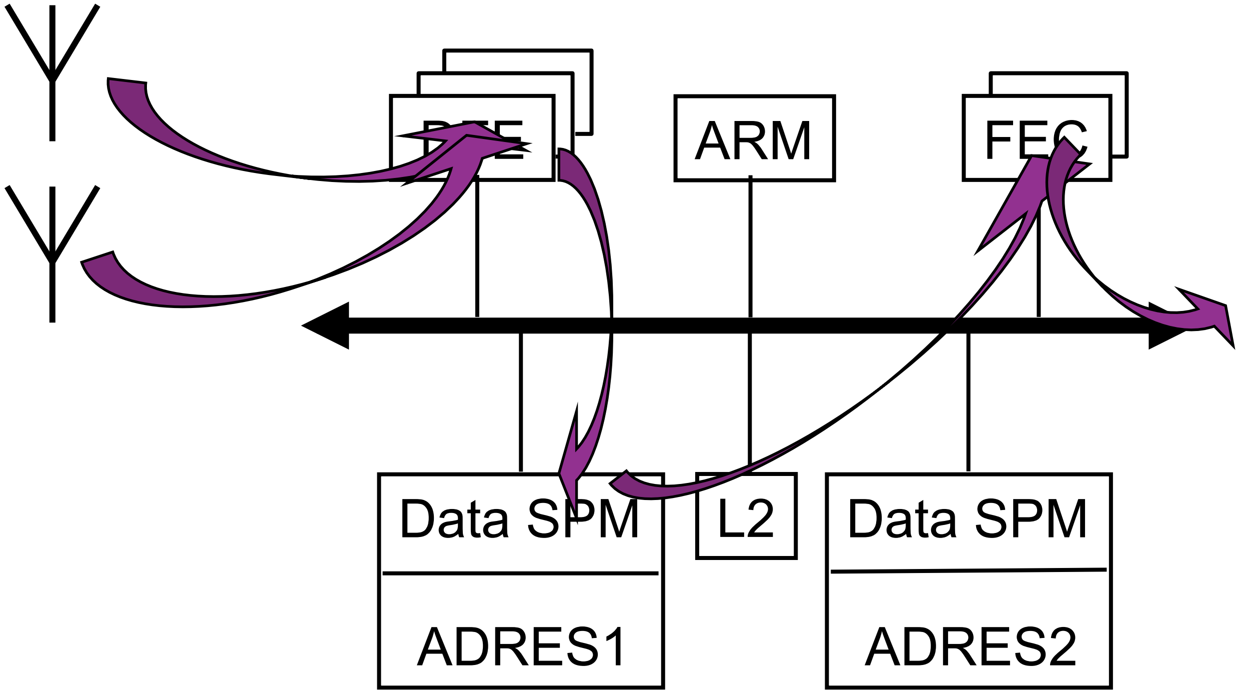
- Sequential C code

- Parallel C code

IMEC SDR COBRA platform

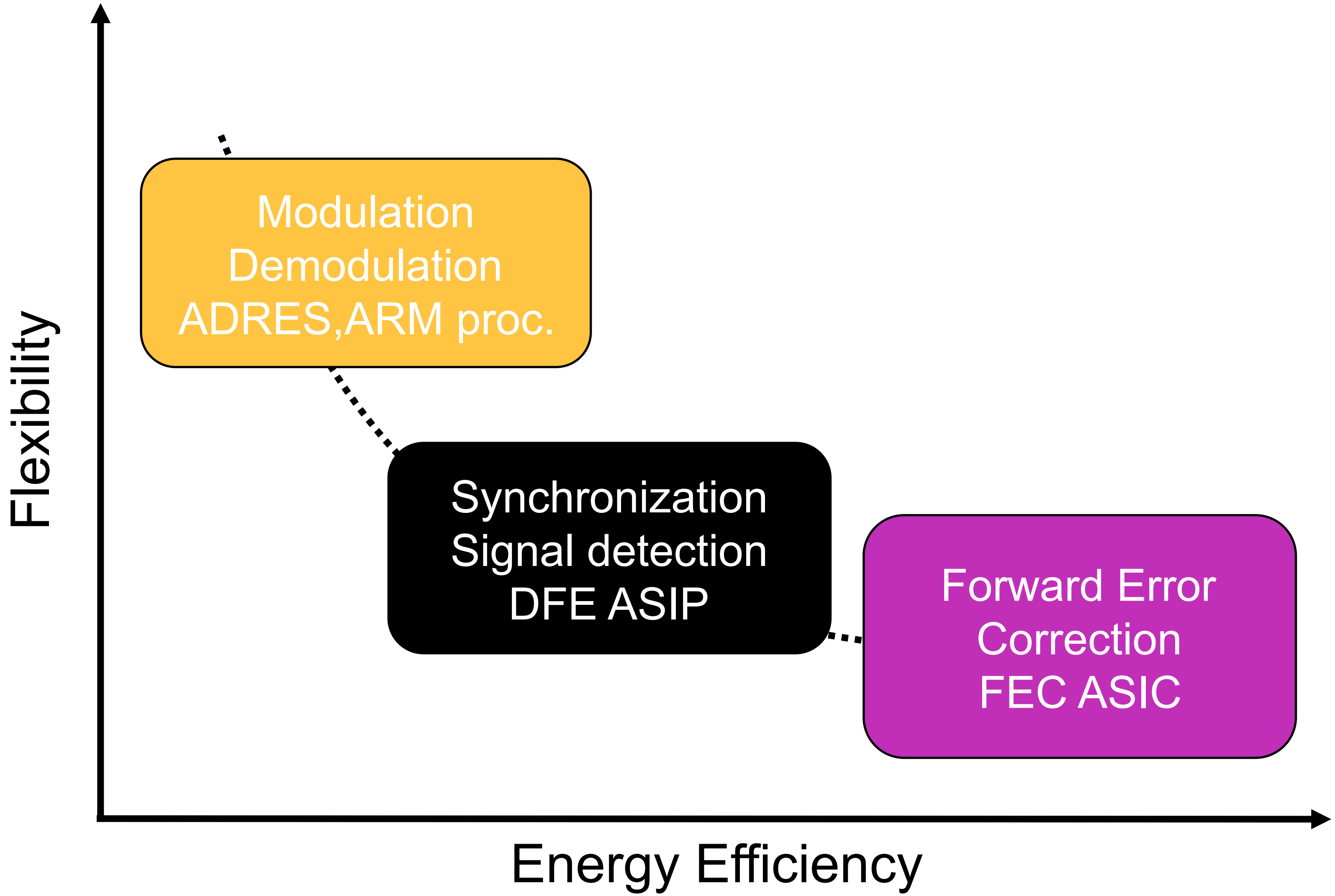
Conclusions

OUR PLATFORM DEALS WITH THE STREAM FROM THE ANTENNA RECEIVER TILL THE FORWARD ERROR CORRECTION ENGINE

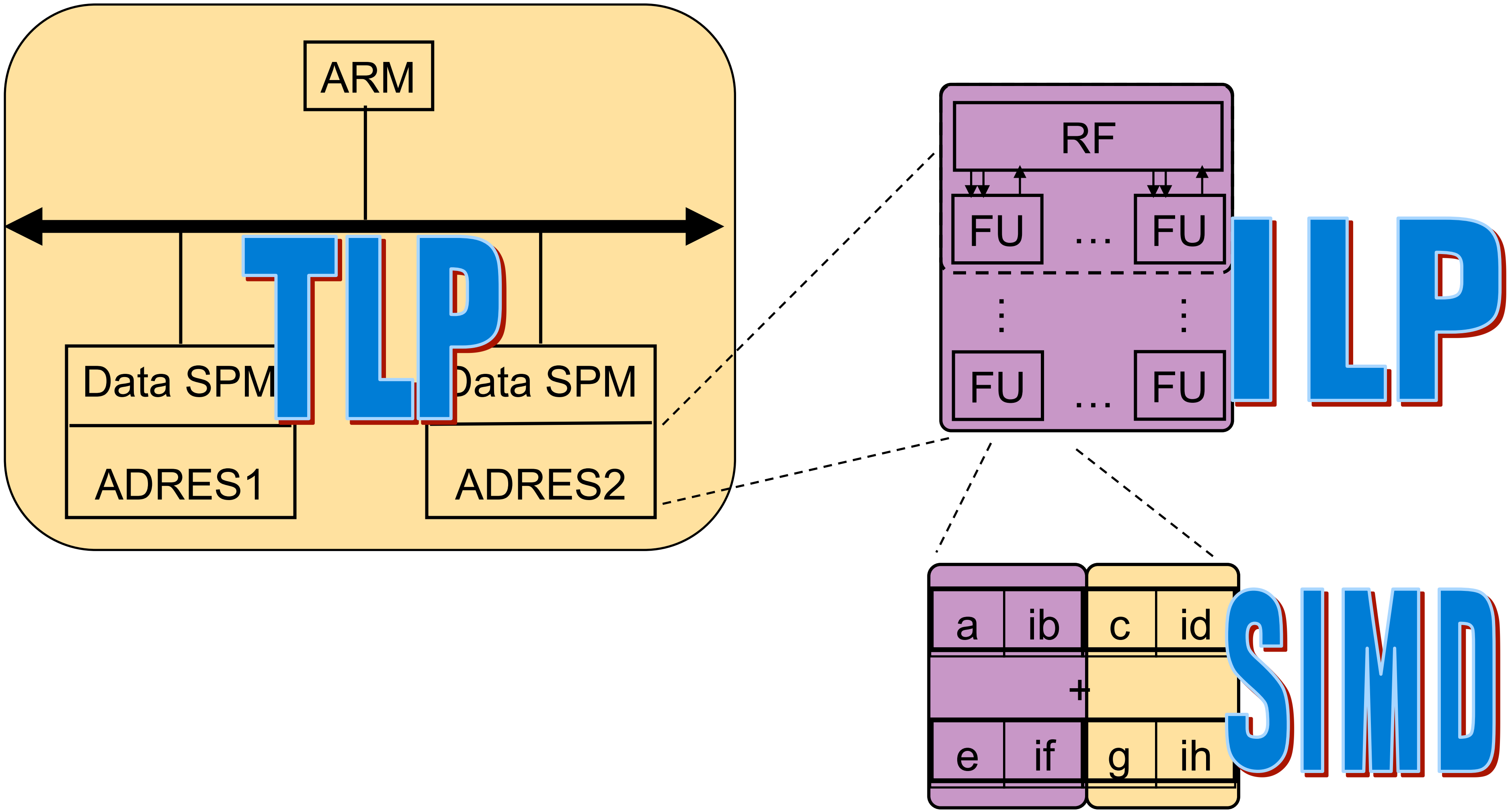


DFE	= Digital Front-End	SPM	= Scratch-Pad Memory
ARM	= ARM processor	L2	= Layer 2 memory
FEC	= Forward Error Correction	ADRES	= ADRES processor

TO OBTAIN ENERGY EFFICIENCY ON THE PLATFORM, COMBINATION OF DSP, ASIP AND ASIC IS USED



THE BASEBAND PART OF OUR SDR PLATFORM, WE WILL FOCUS ON, FEATURES ALL DIFFERENT LEVELS OF PARALLELISM



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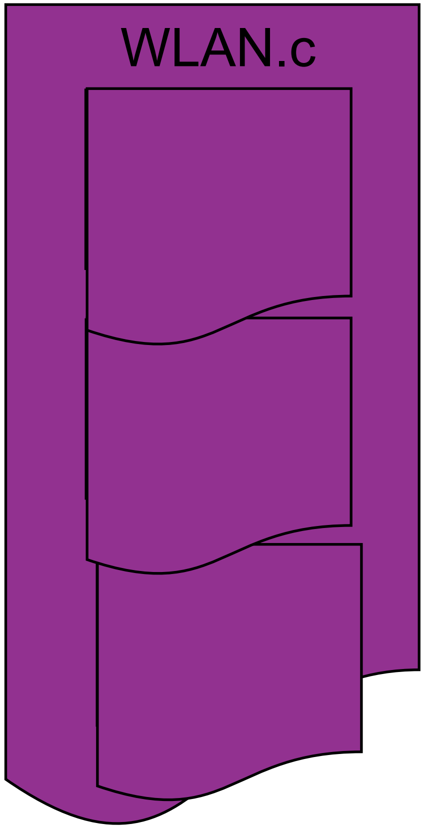
KERNEL SELECTION FROM THE CODE GENERATED BY MATLAB2C CONVERSION TOOL



fft.c

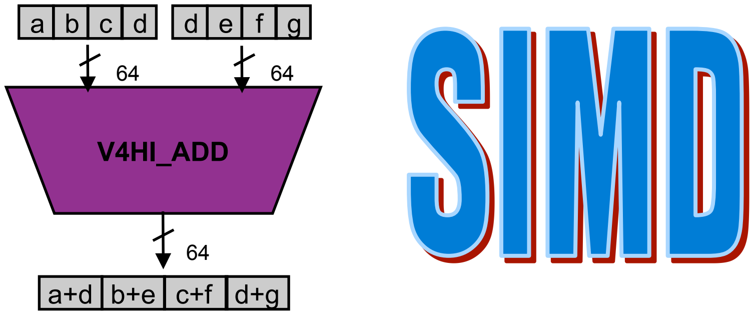
chan_comp.c

demap.c

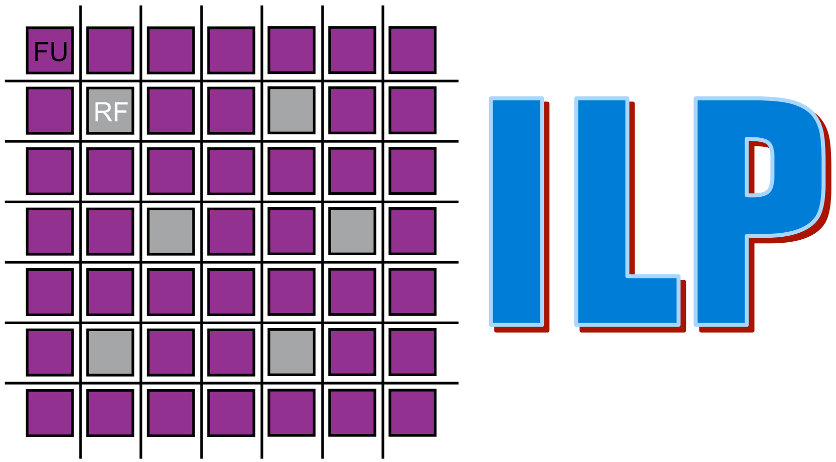
DATA LEVEL PARALLELISM (DLP) AND INSTRUCTION LEVEL PARALLELISM (ILP) ARE EXPLOITED IN THE KERNEL CODE

DLP

- Intrinsics



ADRES



ILP

- DRESC Compiler

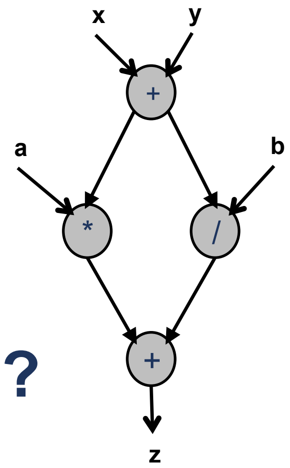
OUR MODULO SCHEDULING ALGORITHM IN THE DRESC COMPILER IS THE KEY TO EFFICIENT ILP EXPLOITATION

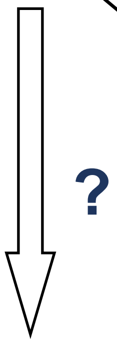
Loop body:

```
for (i=0;i<n;i++)
  z = (x+y)*a + (x+y)/b;
```

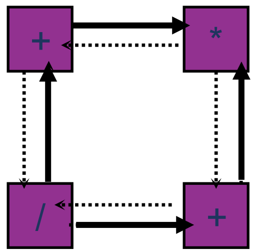
Where to place an operation? (**placement**)
When to schedule an operation? (**scheduling**)
How to connect operations? (**routing**)

DFG

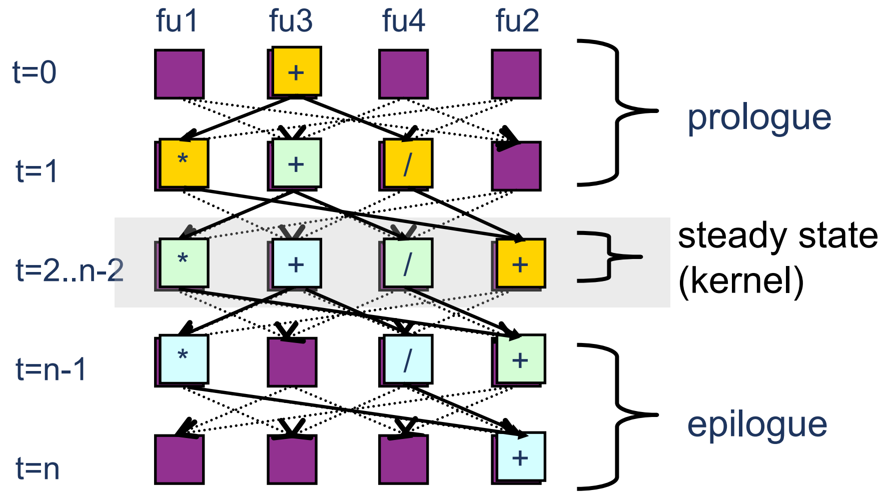




Matrix



Modulo-Scheduling *(Space-time representation)*

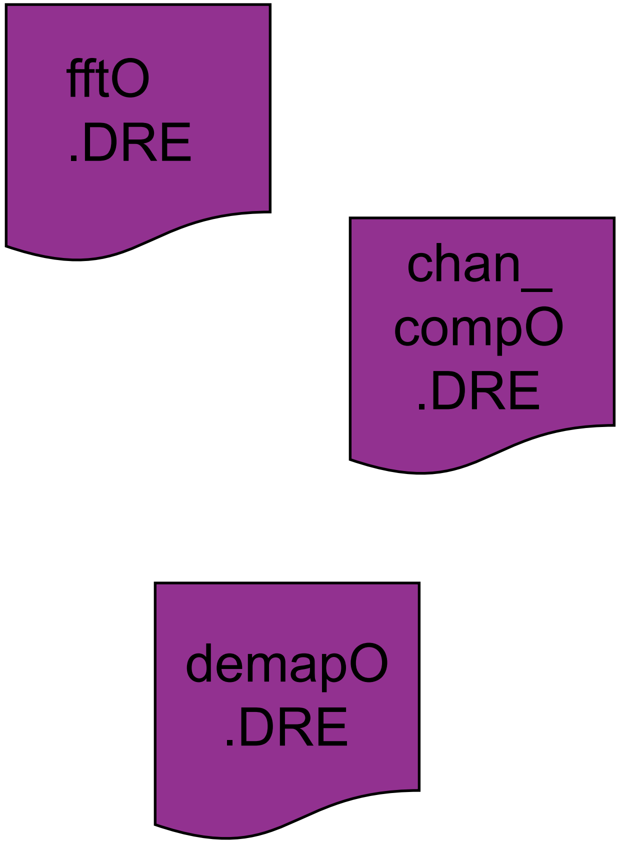


Initiation Interval (II) = 1

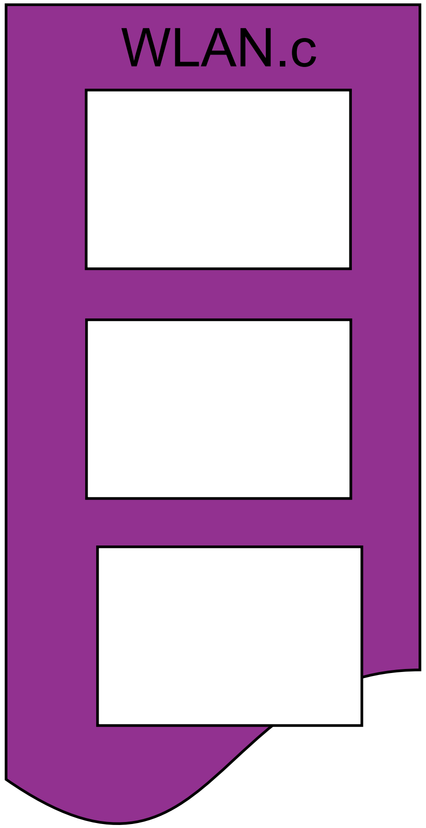
Pipeline stages = 3

4 operations/cycle for kernel

OPTIMIZED KERNELS ARE USED IN THE SKELETON CODE WHICH WAS OBTAINED BY MATLAB2C CONVERSION TOOL



Optimized kernel library



Skeleton code

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STILL, WLAN 40 MHZ MIMO NOT REAL-TIME FOR 1 ADRES. TASK LEVEL PARALLELISM (TLP) IS NOT EXPLOITED YET!

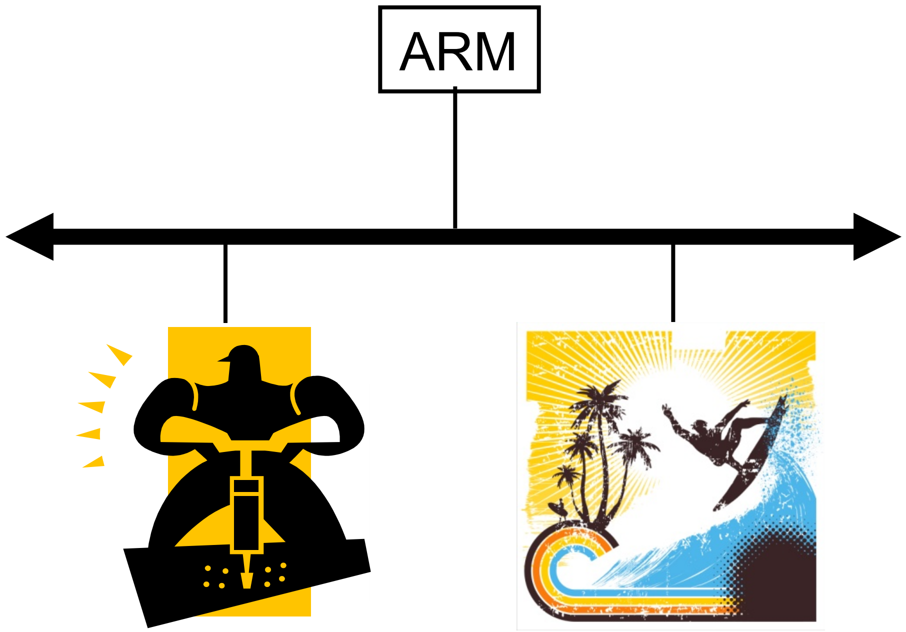
Input stream:

Preamble	Symb1	Symb2	Symb3	Symb4	…
12µs	4µs	4µs			

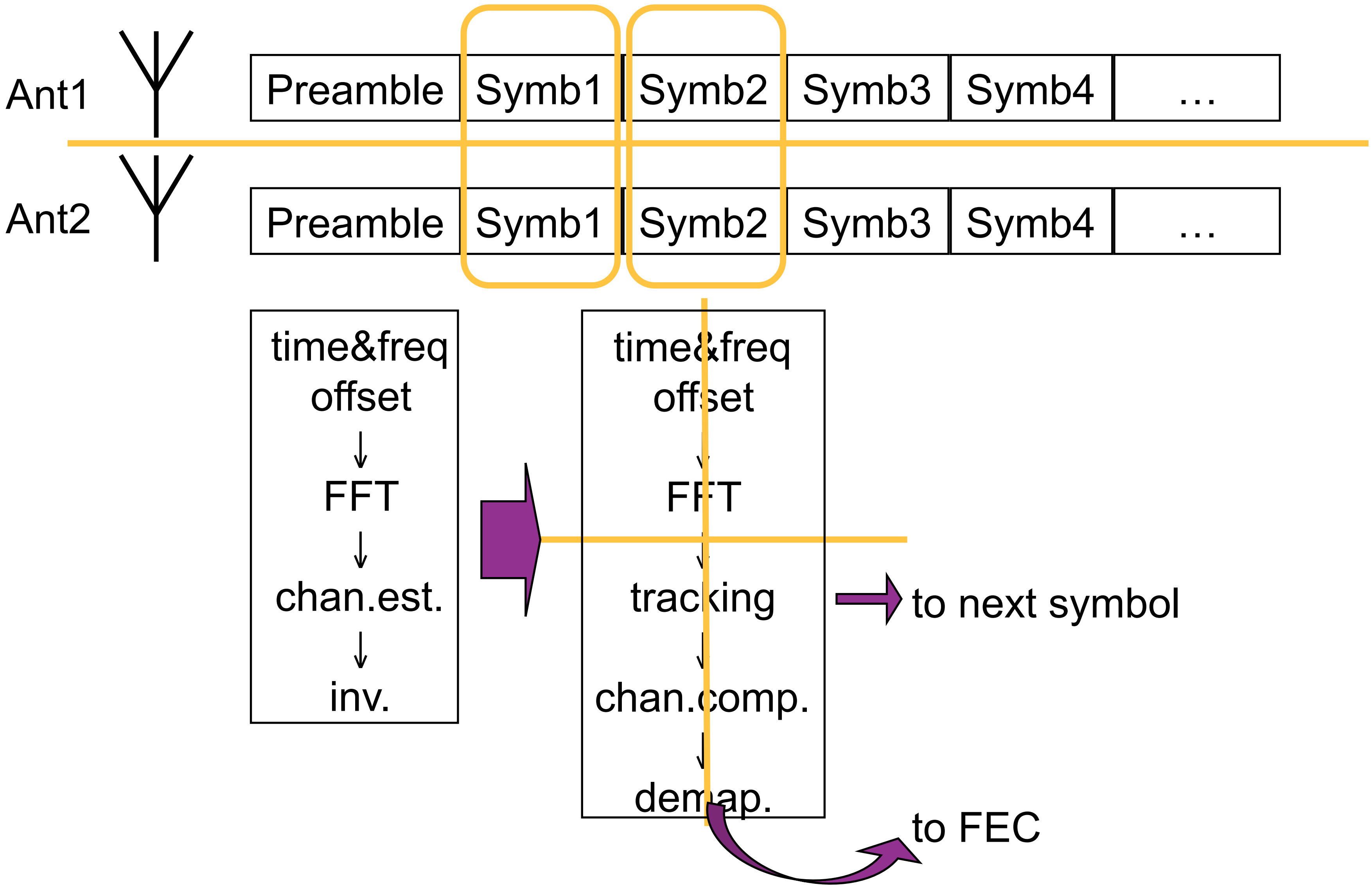
Decoding time:

5.8µs

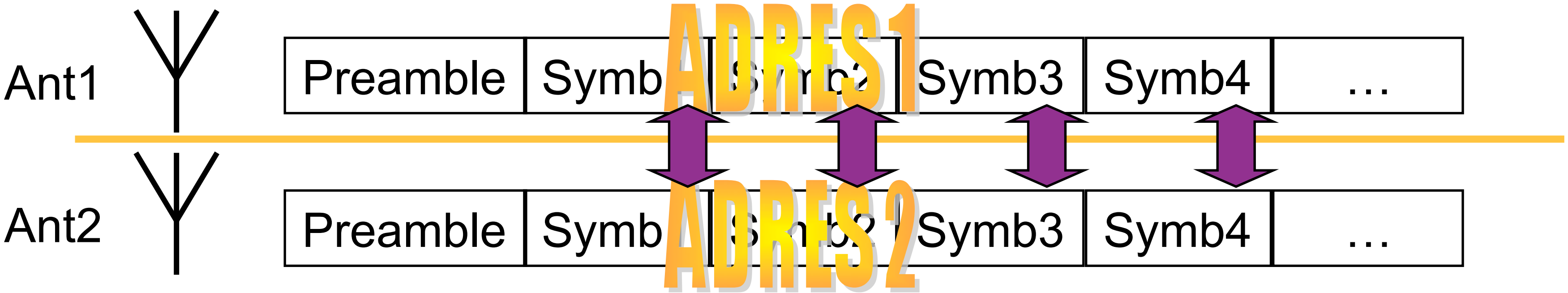
TLP



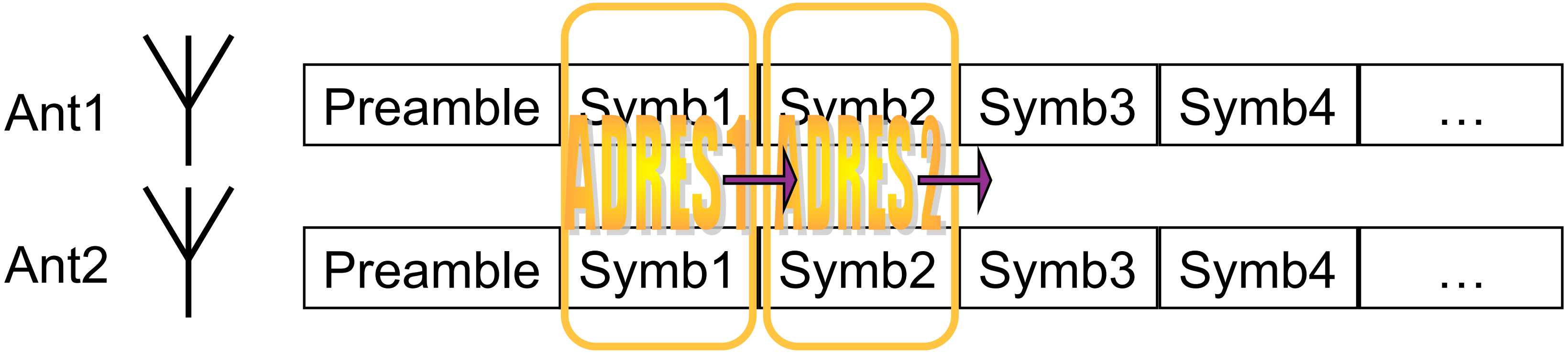
THE APPLICATION OFFERS MULTIPLE WAYS FOR PARALLELIZATION. WHICH ONE TO CHOOSE?



ANALYZING THE COMMUNICATION FOR POTENTIAL SPLITS IS ALWAYS A GOOD THING TO DO!

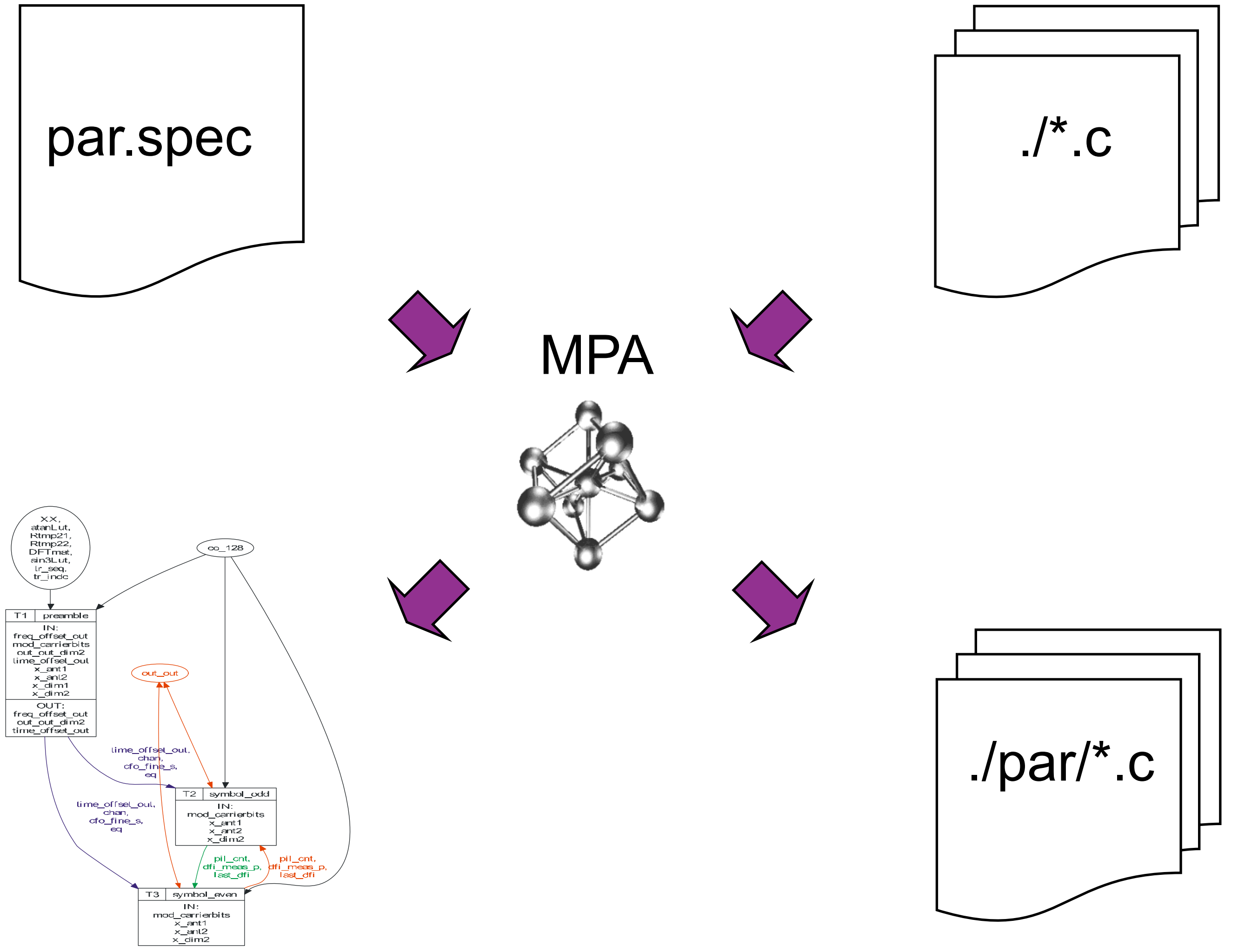


Per antenna split 100MB/s (1/3 bus)

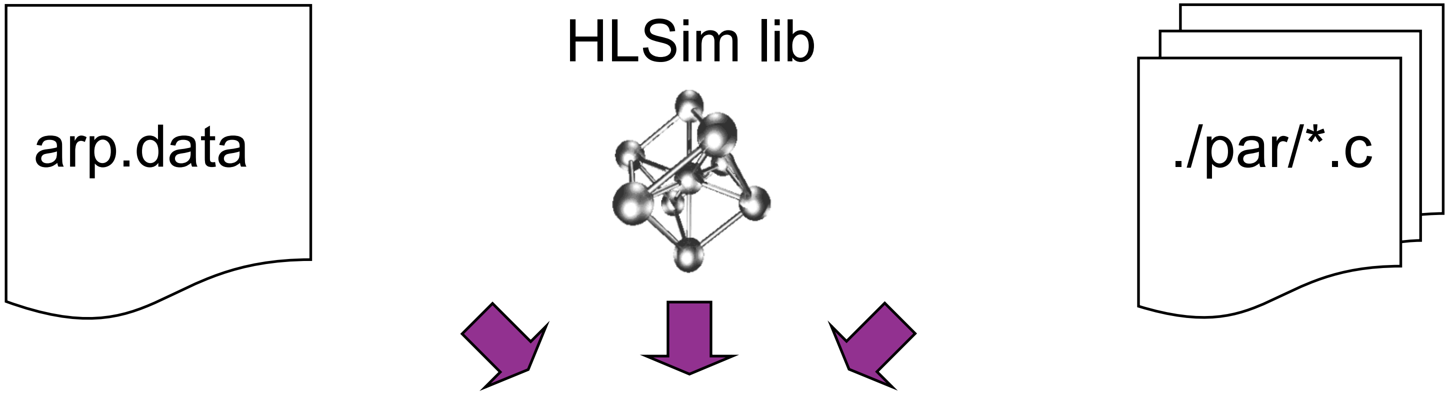


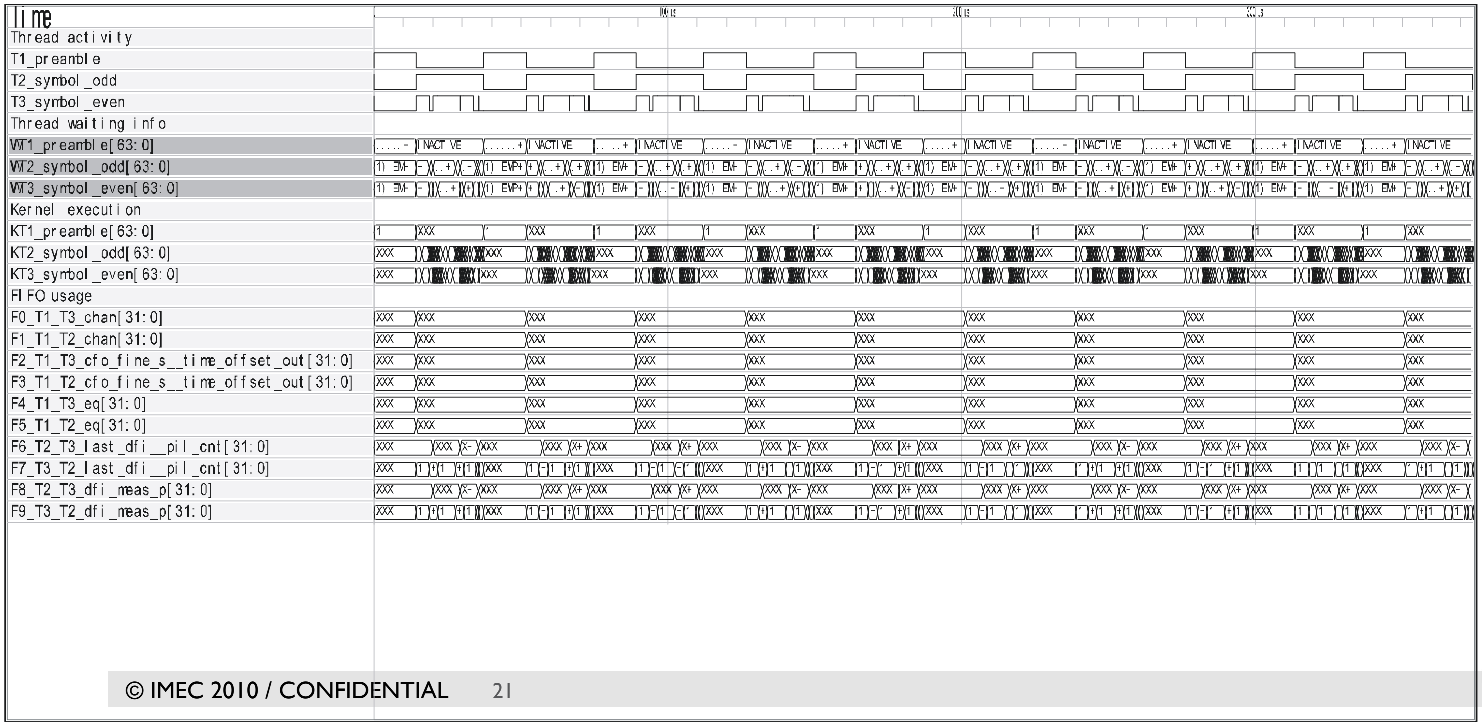
Odd-even symbol split 2.5MB/s (<1%)

CREATION OF THE PARALLEL CODE AND FAST EVALUATION ARE HARD THINGS FOR THE DESIGNER – TOOL SUPPORT NEEDED!

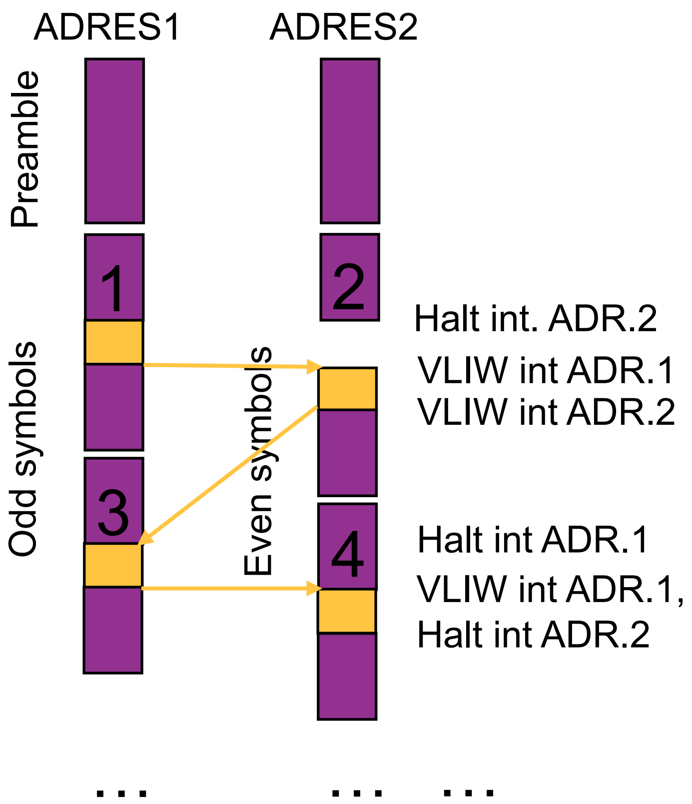


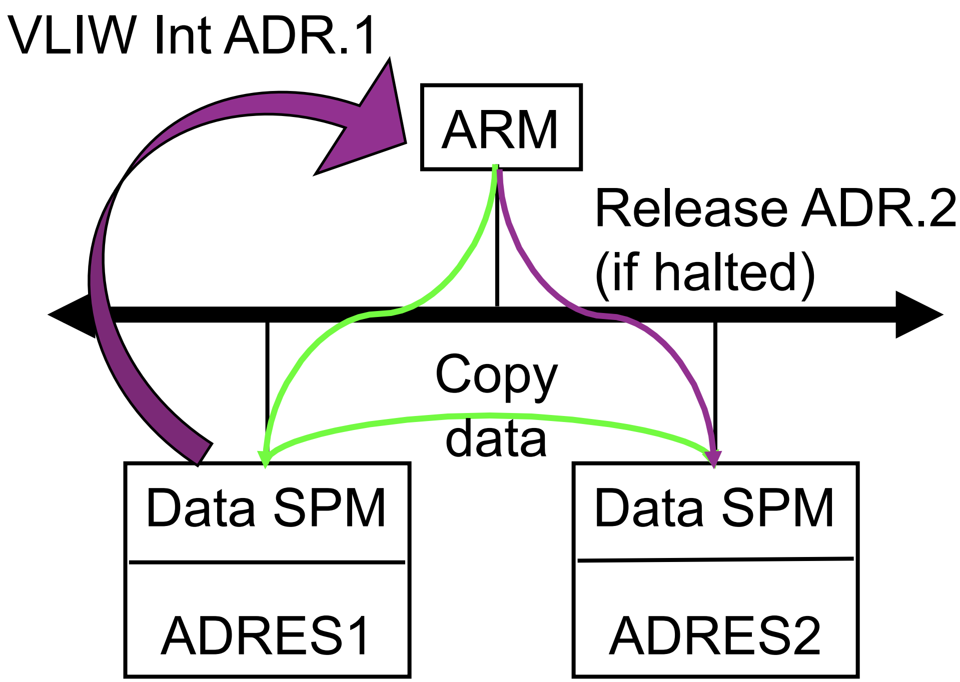
HIGH-LEVEL SIMULATOR PROVIDES FAST INFORMATION ABOUT THE QUALITY OF OUR PARALLELIZATION





WE IMPLEMENTED THE FIFO COMMUNICATION VIA THE VLIW AND HALT INTERRUPTS OF ADRES ENGINES





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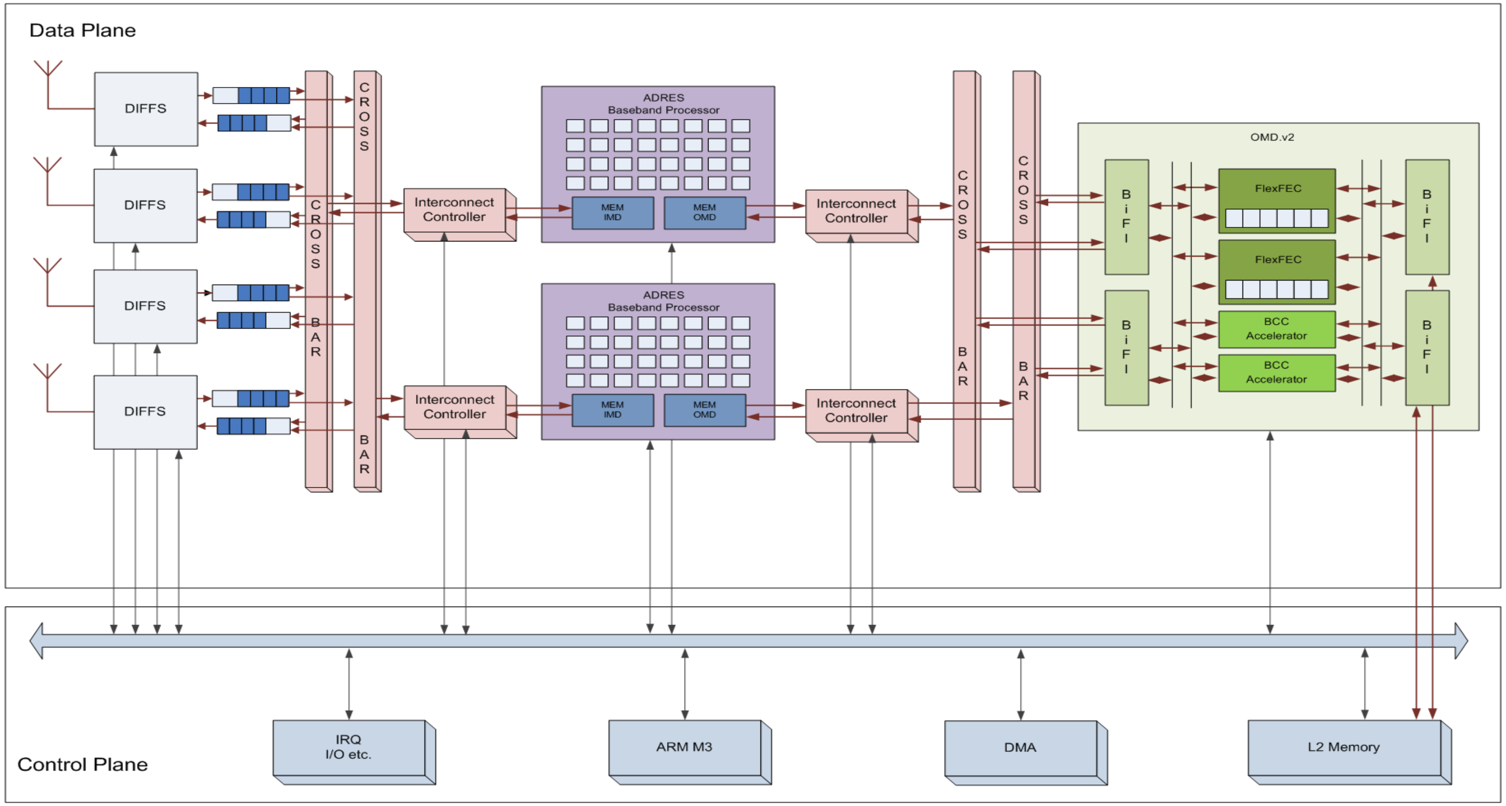
COBRA PLATFORM LEARNED FROM THE DRAWBACKS OF BEAR



CONCLUSIONS

Multi-mode >100Mbps wireless communication requires multi-processor software-defined radio (SDR) solutions

Parallelization for SDR should be exploited on each level – SIMD (DLP), ILP and TLP

Odd-even symbol group split seems to be the right choice for TLP for 40 MHz MIMO SDM OFDM

ILP was explored by our robust C DRESC compiler and TLP split was supported by our MPA parallelization tool

With combination of DLP, ILP and TLP we achieved real-throughput behavior of 40 MHz MIMO SDM OFDM

Cobra platform is the natural evolution of Bear to >500Mbps, multistream and run-time reconfiguration

IMEC SMART SYSTEMS
Building a flexible interactive world