Research in 3-D Integration .....a Year Later

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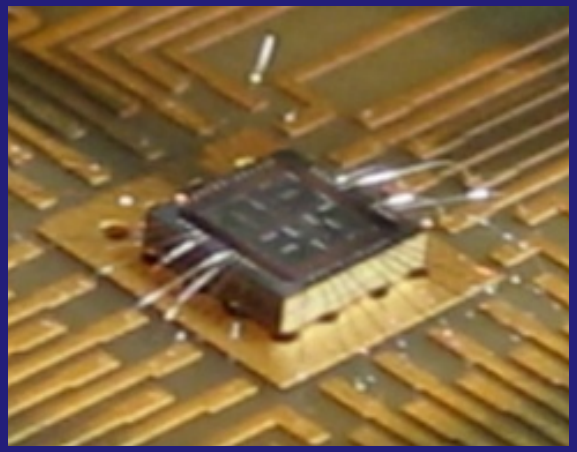
Presentation Outline

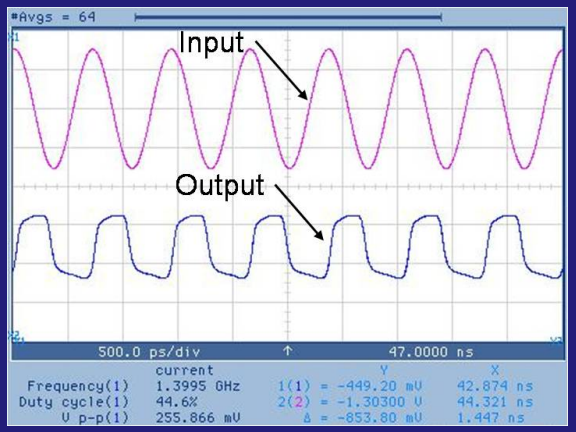
- 3-D Integration: Where are we Standing Today?
- Variability Issues in Synchronization Schemes
- Power Integrity Challenges
- Thermal TSV Modeling
- Summary

Most Recent 3-D Circuits

Academia

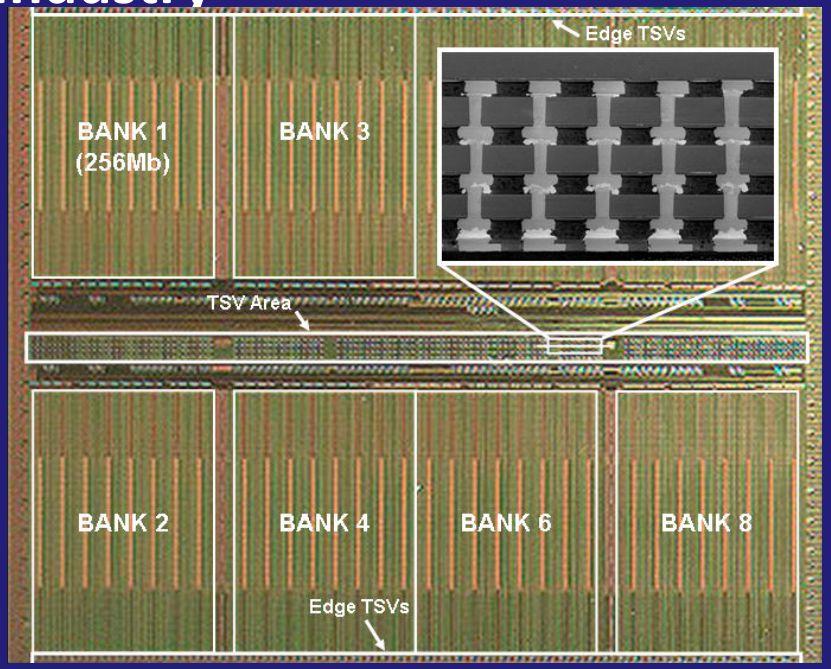


- Clock frequency - 1.4 GHz



V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks for 3-D ICs," *Proceedings of the IEEE International Custom Integrated Circuits Conference,* pp. 651-654, September 2008

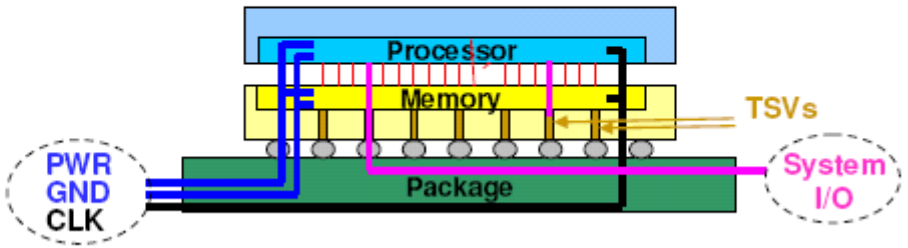
Industry



- Samsung 8-Gb 3-D DDR3 DRAM
  - Four planes
  - TSV located in the periphery

U. Kang *et al.,* "8-Gb 3-D DDR3 DRAM Using Through-Silicon-Via Technology," *IEEE Journal of Solid State Circuits,* Vol. 45, No. 1, pp. 111-119, January 2010

What does 3D fundamentally change



- Major design components are fundamentally different than 2D
  - Power and clock distribution, chip IO and thermal conduction are significantly altered
  - Memory level is riveted with TSVs for power distribution and level to level communication
  - Macros on the memory level need to be redesigned to tile around the power distribution

Ruchir Puri, IBM Thomas Watson Research Center
Yorktown Heights, NY, USA
D43D Workshop, May 2010, EPFL, Lausanne, Switzerland

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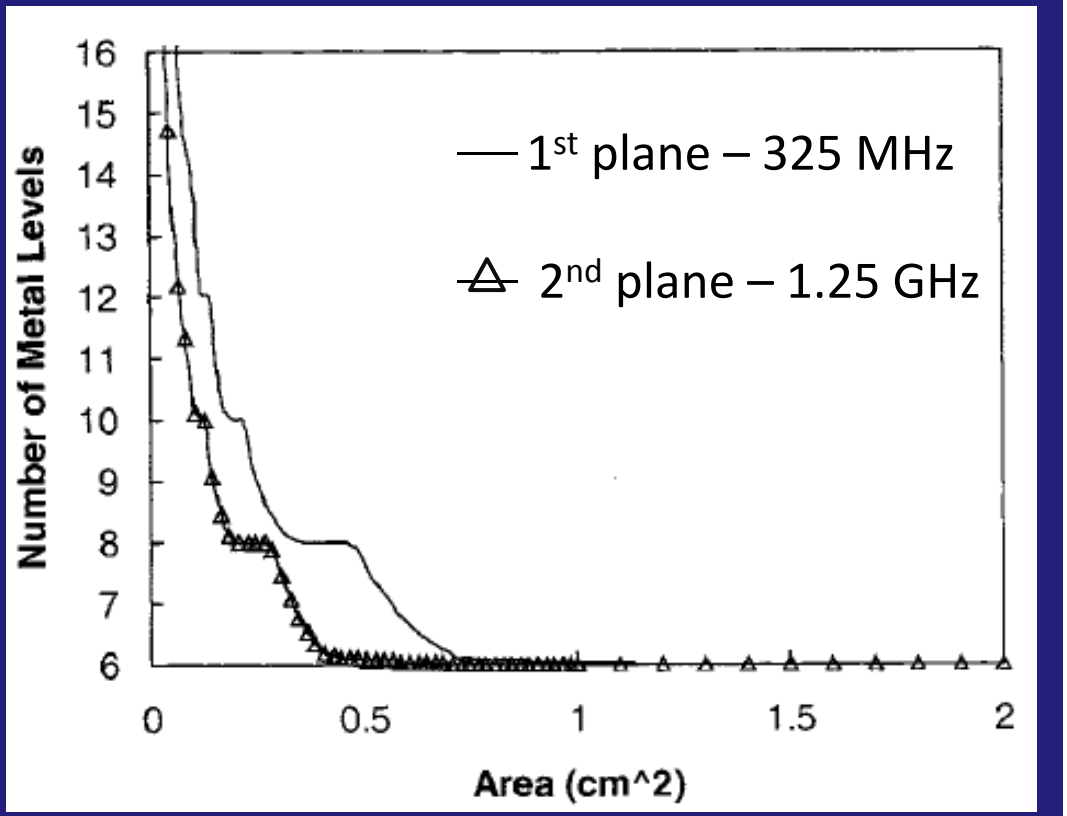
Key Advantage of 3-D Integration

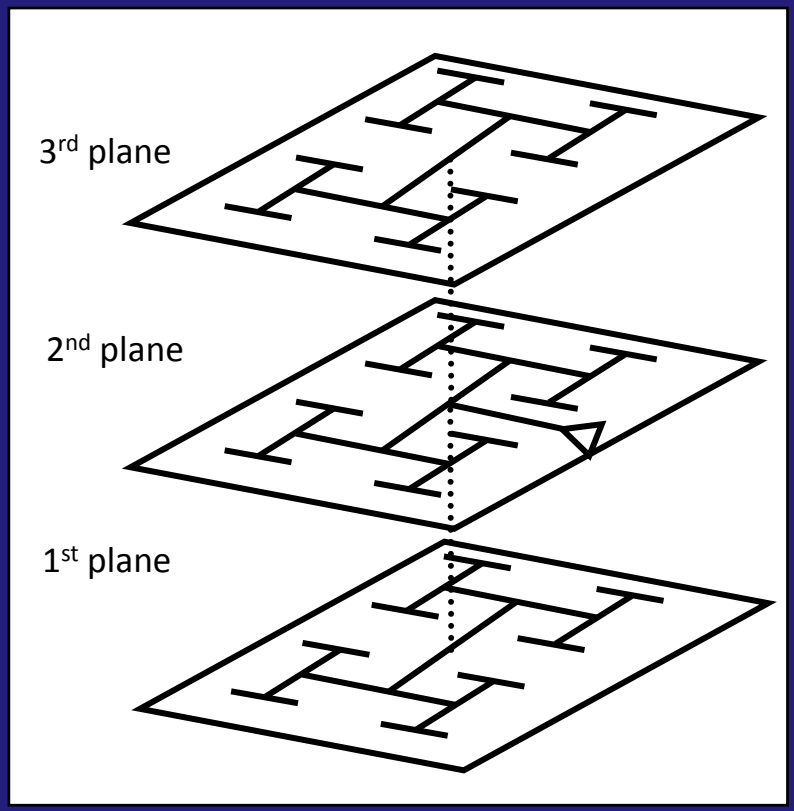
- Higher performance
  - Speed and power
- Area reduction
  - For wire-limited circuits
    - Fixed clock frequency
- Decrease in interconnect resources
  - Number of metal layers
    - For specific speed and area



*J. Joyner *et al.*, "Impact of Three-Dimensional Architectures on Interconnects in Gigascale Integration," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* Vol. 9, No. 6, pp. 922-927, December 2001

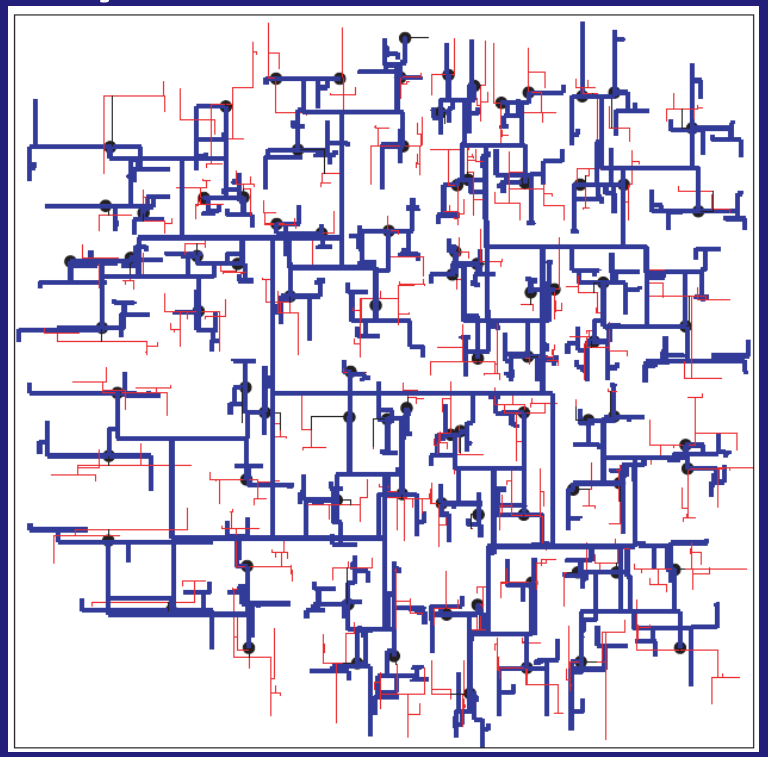
Clock Signal Distribution for 3-D ICs

- Multiplane system
  - Process variations
- Different forms of 3-D integration
  - System-in-Package (SiP)
  - 3-D ICs (high density vias)
- Clock signal distribution under pronounced thermal effects



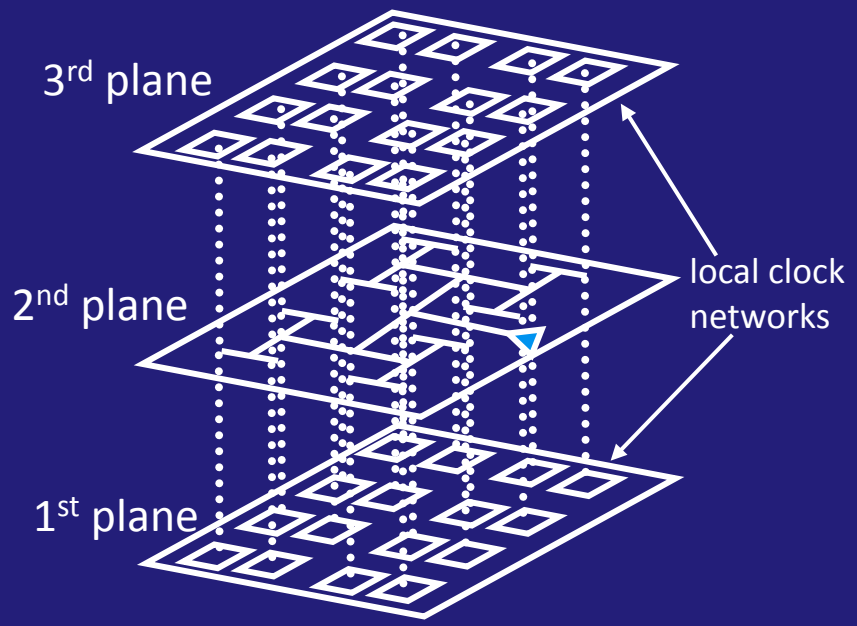
3-D Clock Distribution Networks

- **Synthesized 3-D clock tree**



- A synthesized 3-D clock tree with 87 TSVs [1]

- **Symmetric 3-D clock tree**

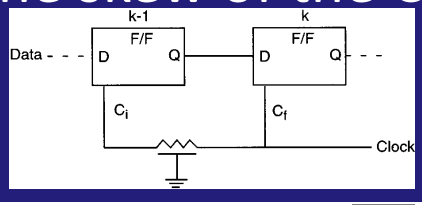


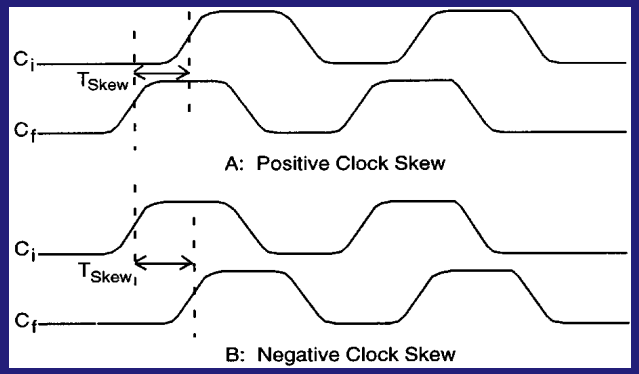
- 3-D global H-trees spanning multiple planes [2]

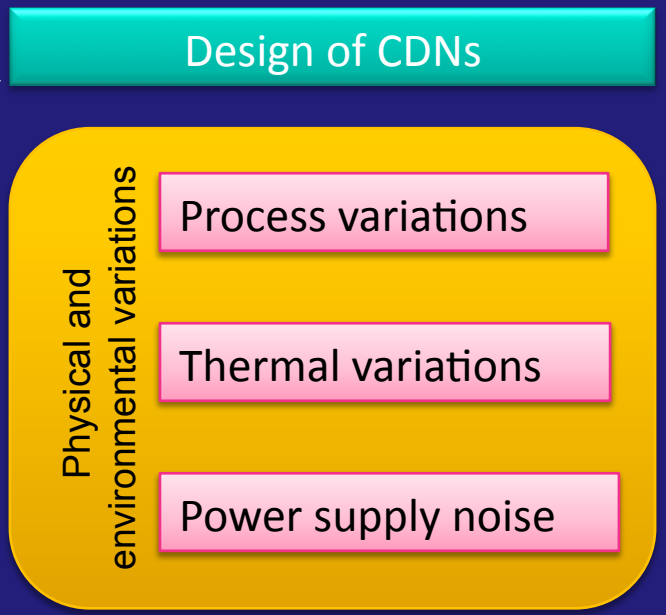
[1] J. Minz *et al.*, "Buffered Clock Tree Synthesis for 3D ICs Under Thermal Variations," *Proc. of ASPDAC*, January 2008.
[2] V. F. Pavlidis *et al.*, "Clock Distribution Networks for 3-D Integrated Circuits," *Proc. of IEEE CICC,* September 2008.

Skew Sources in Clock Distribution Networks

- Clock skew is the difference between the delay from the clock source to various clock sinks
  - Pair wise skew – the skew between each pair of sinks (data-related sinks)
  - Global skew – the skew between the minimum and maximum path delay
- The highest operating frequency of a circuit can be constrained by the skew of the CDN

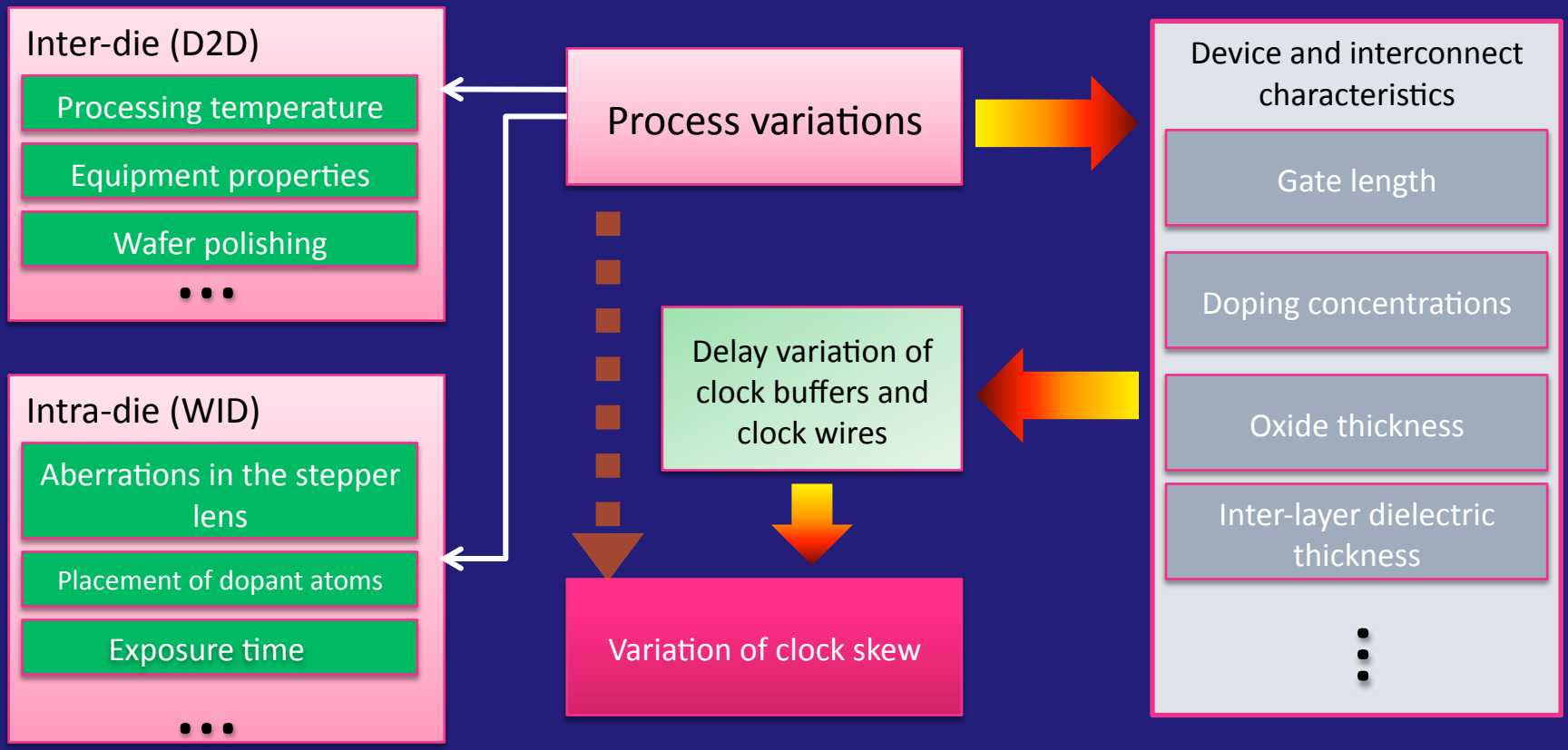






* E. G. Friedman, "Clock Distribution Networks in Synchronous Digital Integrated Circuits," *Proceedings of the IEEE*, Vol. 89, No. 5, pp. 665-692, May 2001.

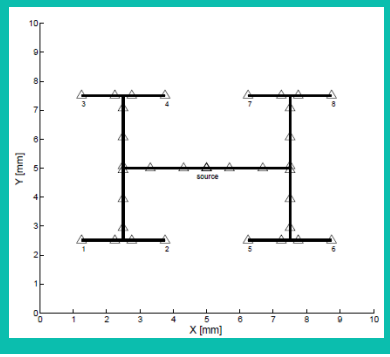
Sources of Process Variations

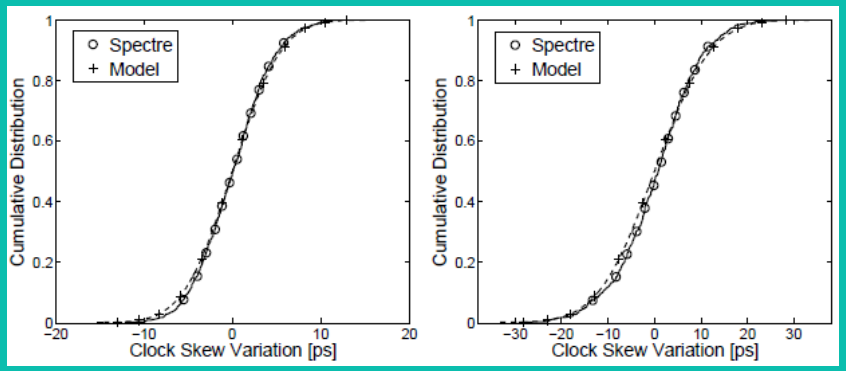


* K. Bowman *et al.*, "Impact of Die-to-Die and Within-Die Parameter Fluctuations on the Maximum Clock Frequency Distribution for Gigascale Integration," *IEEE Journal of Solid-State Circuits*, Vol. 37, No. 2, pp. 183-190, February 2002.

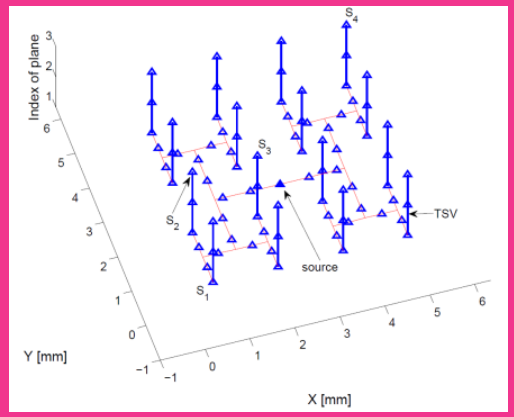
Analytic Skew Variation Model

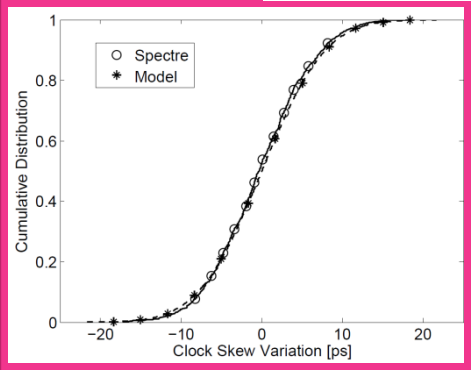
- 2-D CDNs
  - UMC 90 nm CMOS technology
  - Buffers are inserted under the same constraint of slew rate
  - The error compared with Monte-Carlo simulations is below 10%

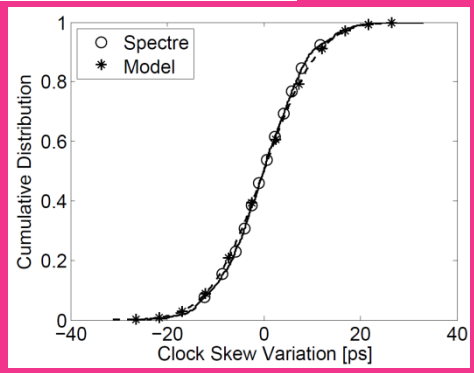




- 3-D CDNs
  - UMC 90 nm CMOS technology
  - Three planes, 48 sinks in total
  - The error is < 10%

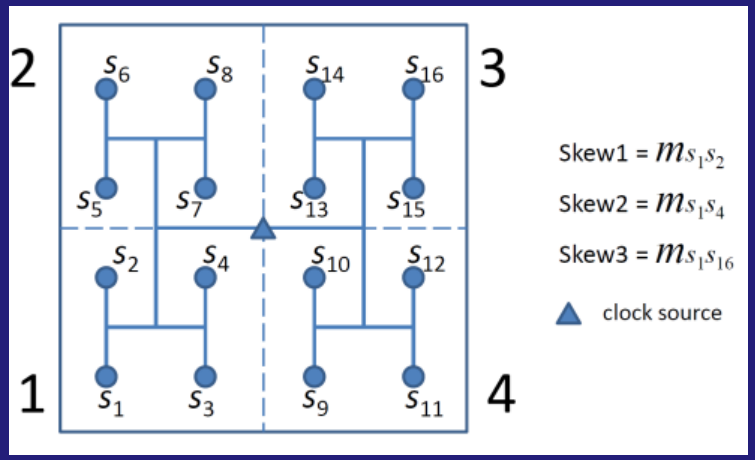


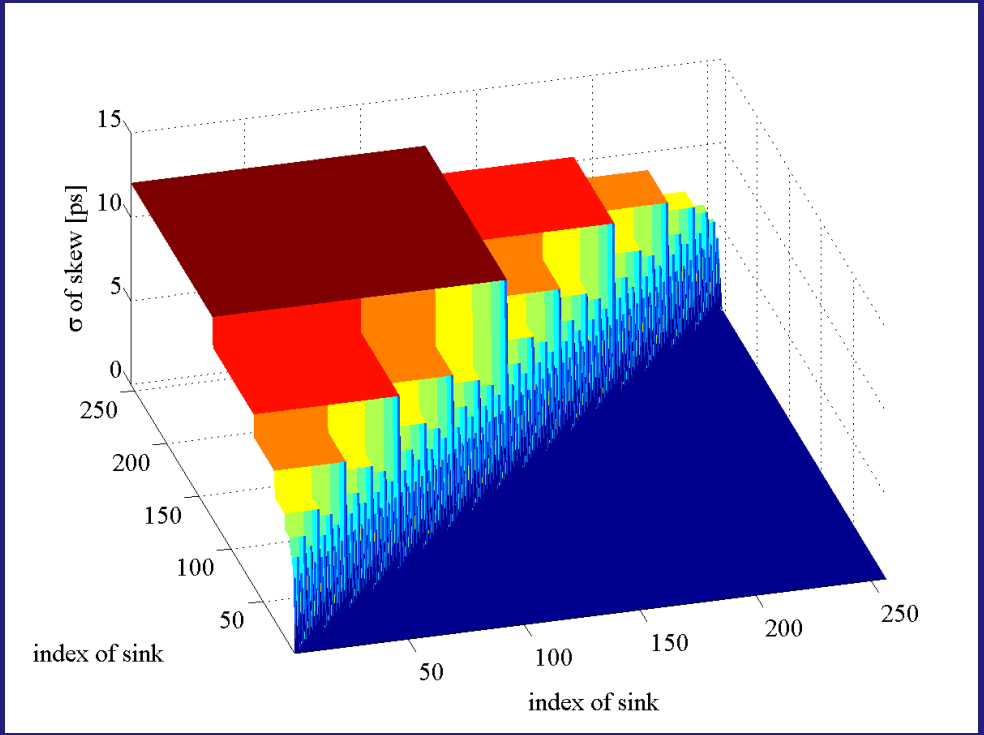




Skew Variation in Scaled 2-D ICs

- A global clock H-tree with 256 sinks
  - The characteristics of buffers is obtained from ITRS for 90 nm
  - The max. σ of skew variation is about 11 ps

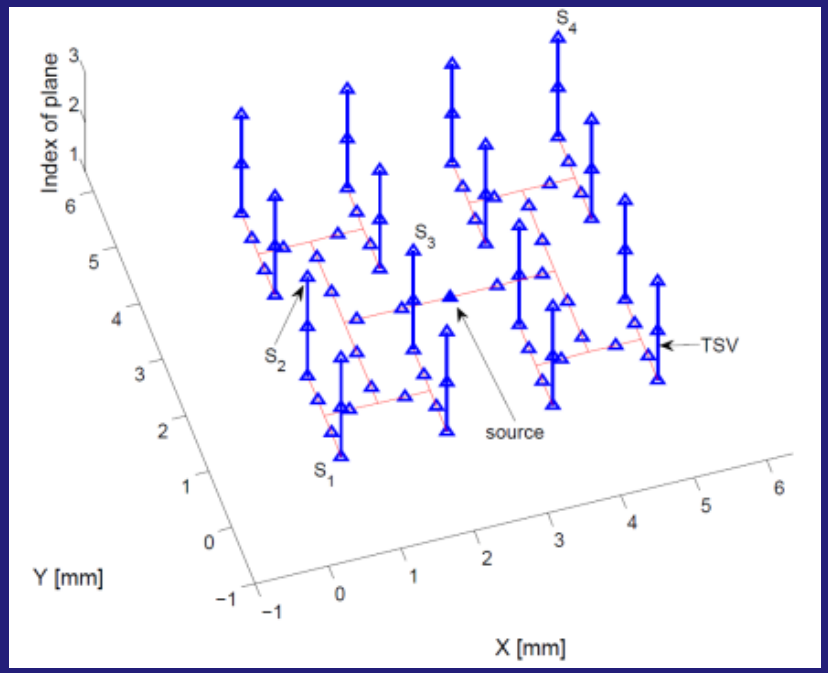




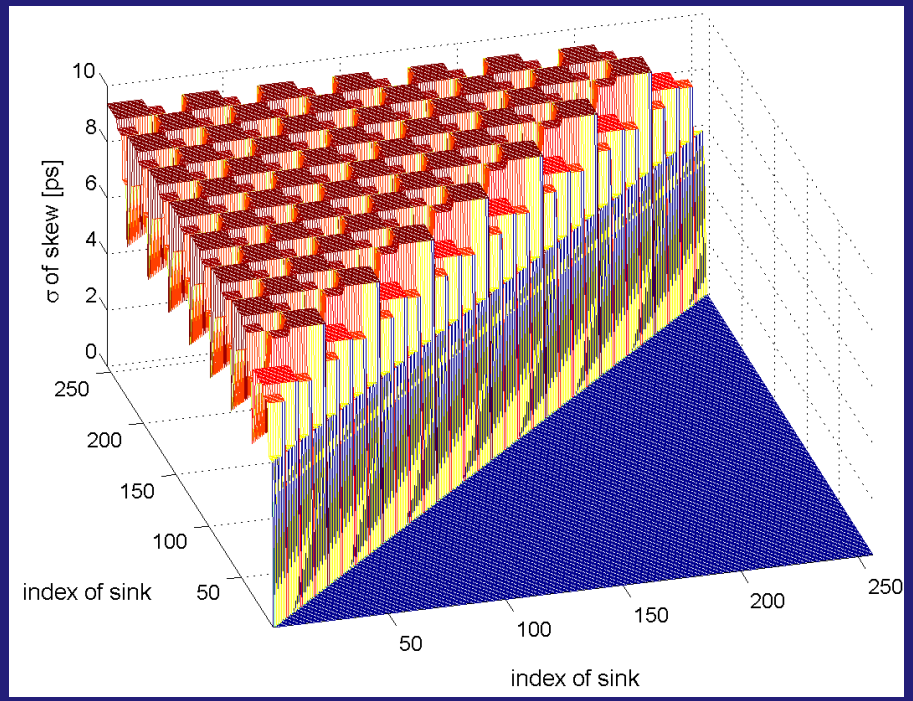
H. Xu, V. F. Pavlidis, and G. De Micheli, "Process-Induced Skew Variation for Scaled 2-D and 3-D ICs," *Proceedings of the ACM System Level Interconnect Prediction Workshop,* pp. 17-20, June 2010.

Skew Variation in Scaled 3-D ICs

- A global clock H-tree with 256 sinks
  - The parameters are similar to the 2-D CDN at 90 nm
  - The σ of skew between the bottom and topmost planes is the largest



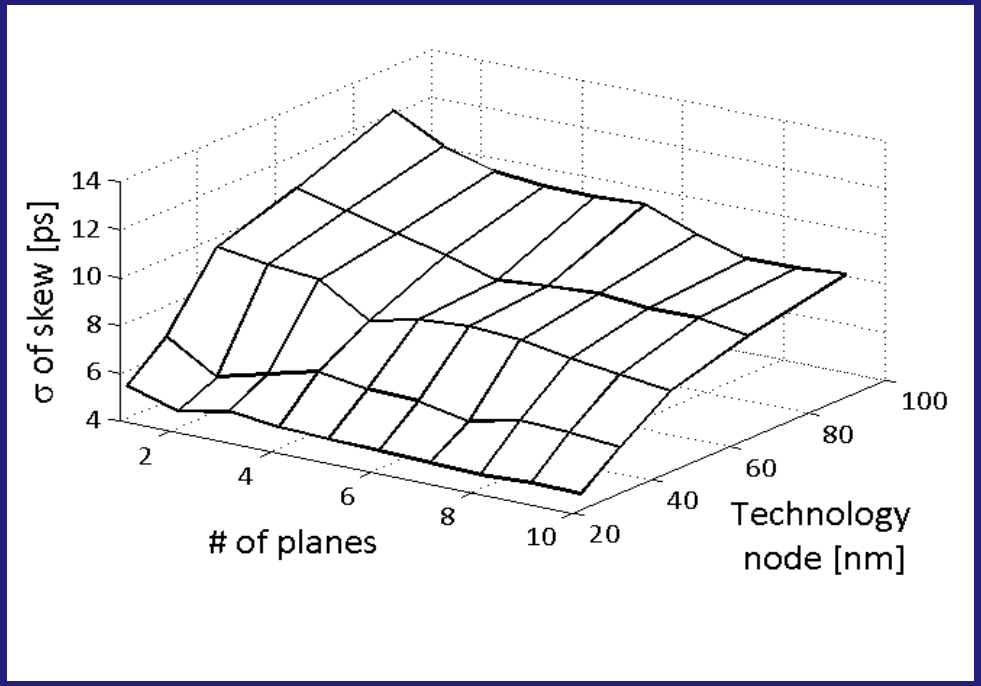
- Example of a 3-plane H-tree with 48 sinks



- σ of skew in a 8-plane H-tree

Comparison on Process-Induced Skew Variation between Technology Scaling and 3-D Integration

Tech. node	# of planes									
	1	2	3	4	5	6	7	8	9	10
90 nm	12.1	11.1	10.5	10.3	10.2	10.3	9.5	8.9	9.0	9.1
65 nm	10.6	10.1	9.6	9.1	8.5	8.7	8.8	8.6	8.6	8.3
45 nm	9.6	9.3	9.0	7.7	8.2	8.3	8.2	7.9	7.6	7.4
32 nm	6.7	5.4	6.0	6.5	6.2	6.2	5.7	6.2	6.1	5.9
22 nm	5.4	4.8	5.2	4.9	4.8	4.8	4.7	4.6	4.7	4.7



- The skew variation decreases more with technology scaling as compared to 3-D integration
- A multiplane circuit with a comparable variation can provide an alternative to aggressive technology scaling

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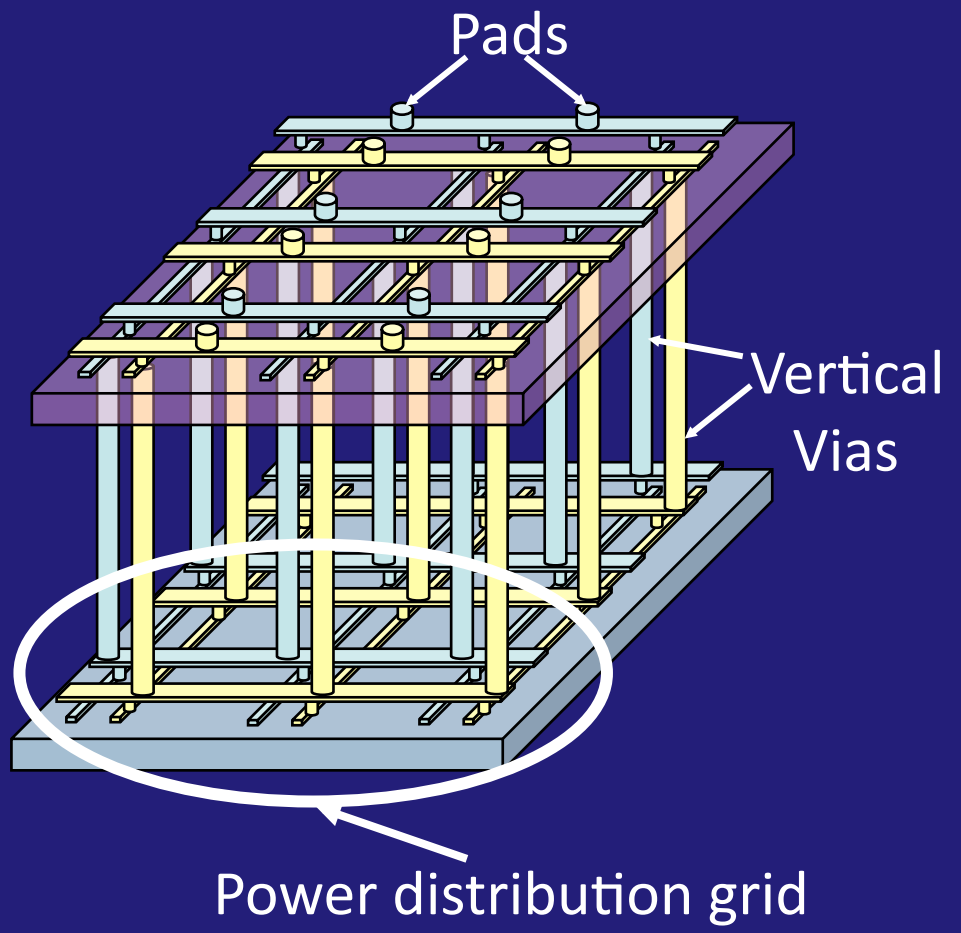
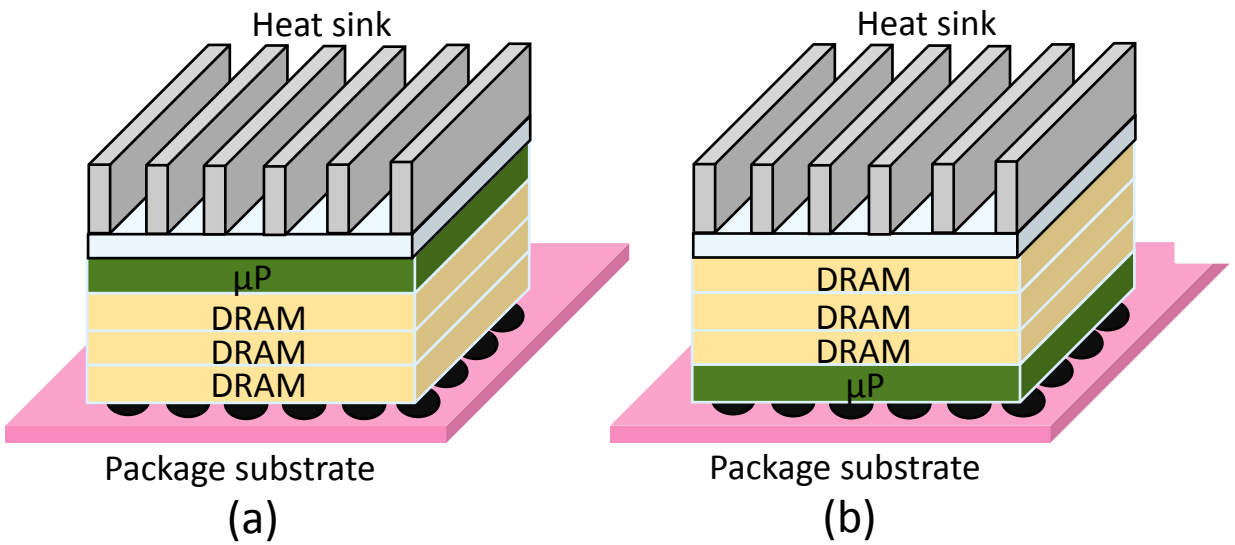
Power Integrity Challenges for 3-D ICs

- Number of P/G pads will decrease
  - Due to smaller chip footprint
- Current transients are more abrupt
  - Due to higher circuit speed
- Heterogeneous interconnect architectures
  - Disparate interconnect impedance characteristics



*V. F. Pavlidis and E. G. Friedman, "Interconnect-Based Design Methodologies for 3-D Integrated Circuits," *Proceedings of the IEEE,* Vol. 97, No. 1, pp. 123-140, January 2009.

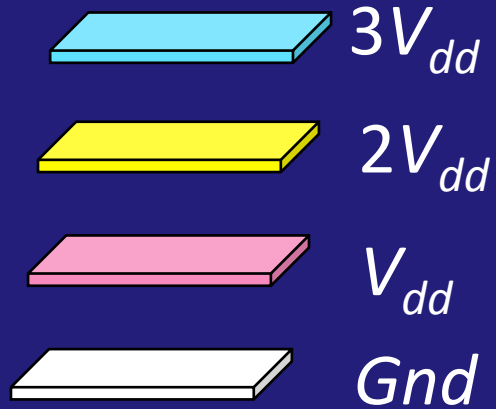
Thermal and Power Supply Noise Tradeoff

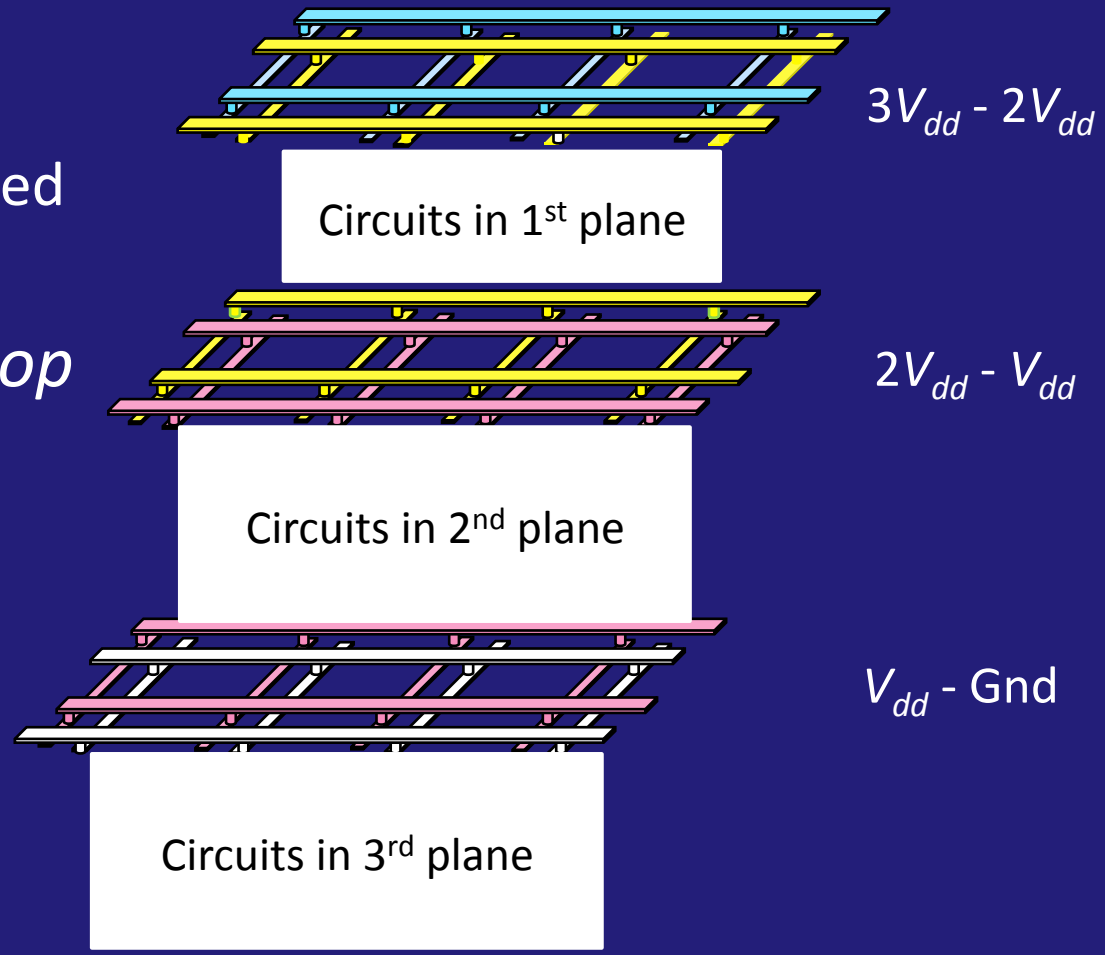


- A DRAM-µP 3-D stack is the focus of several industrial efforts
- Such a system can increase memory bandwidth
- Power consumption also decreases
- But how do we place the components in these systems?

PDN Approaches for 3-D ICs

- Multi-story V_{dd}
  - Current is recycled among planes
- Can reduce *IR drop*
- Total power consumption

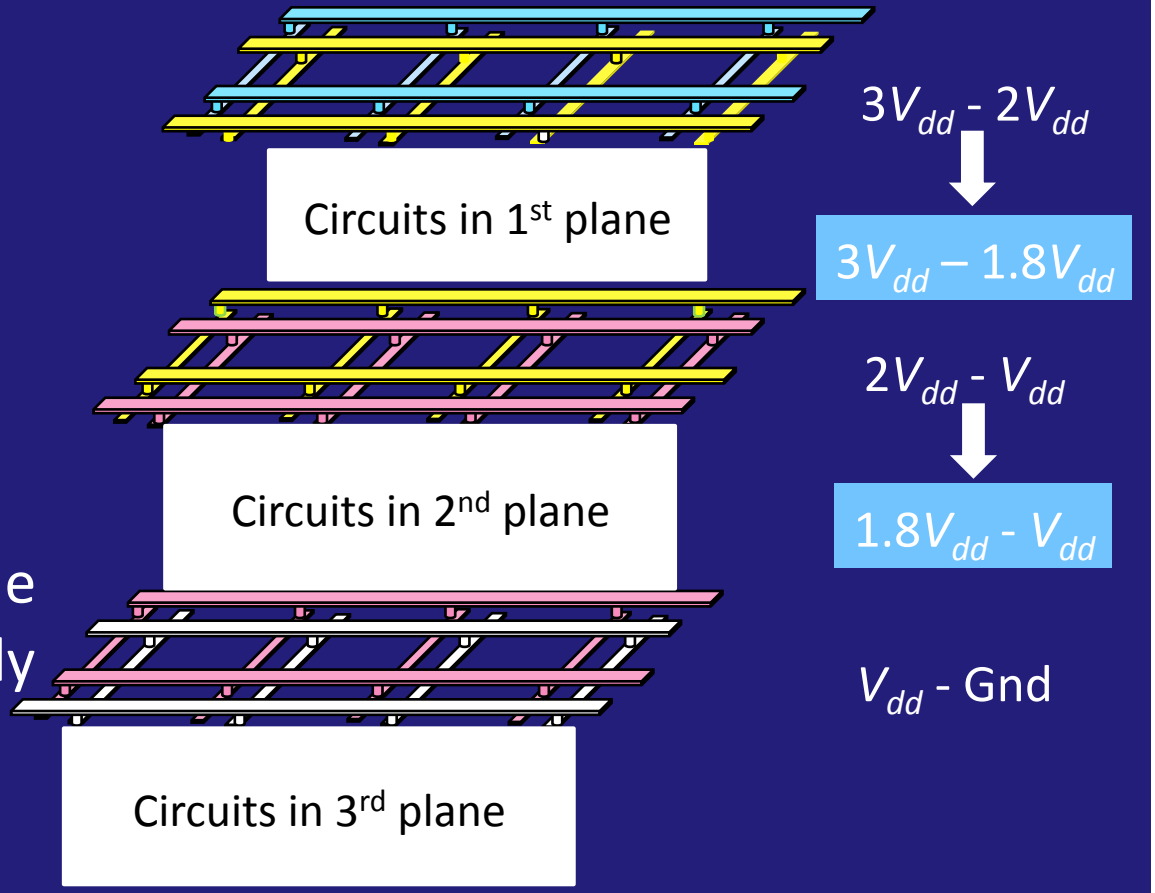




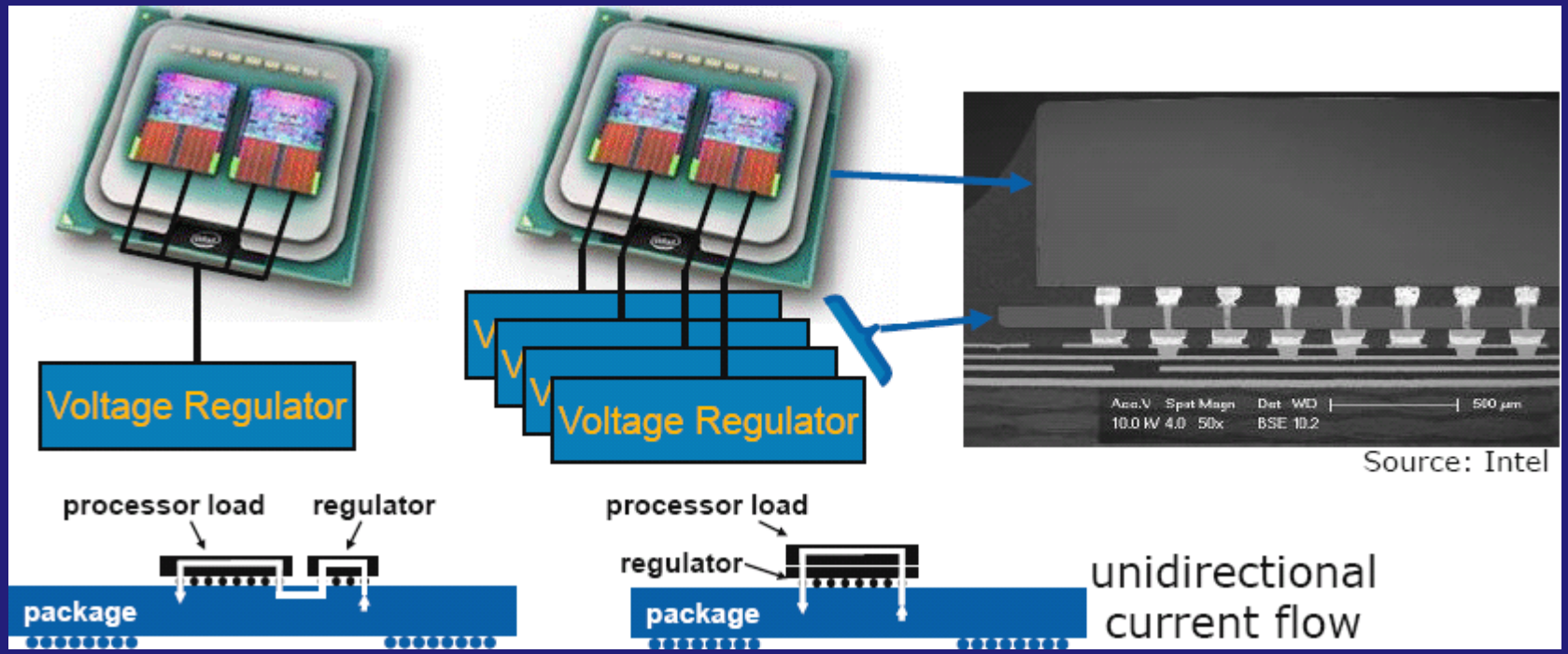
* P. Jain, T.-H. Kim, J. Keane, and C. H. Kim, "A Multi-Story Power Delivery Technique for 3-D Integrated Circuits," *Proceedings of the International Symposium on Low-Power Electronics and Design*, pp. 57-62, August 2008.

Implementation Challenges with Multi-Story 3-D PDNs

- Multiple power levels are required
  - Multiple V_{dd} pins
  - Multi-story power delivery system
- DVS is challenging
  - The voltage in one plane cannot scale individually



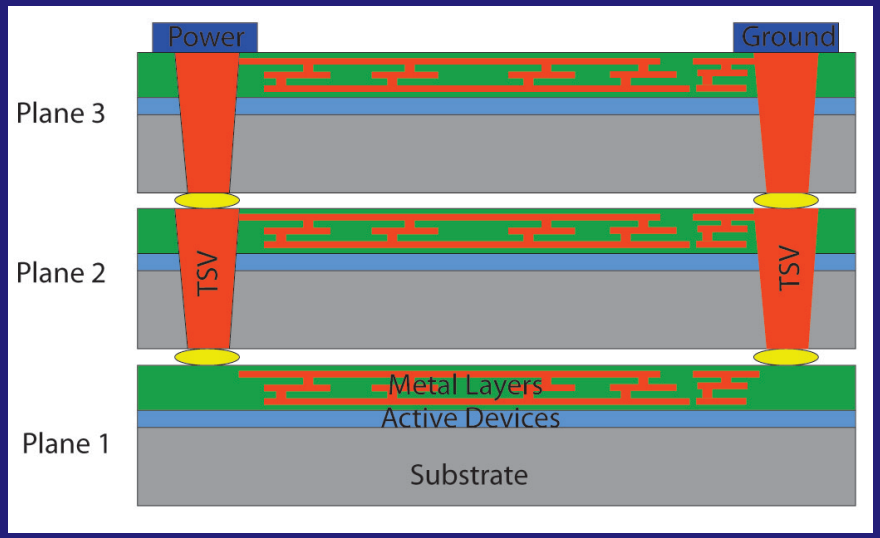
Integration of Voltage Regulators On-Chip

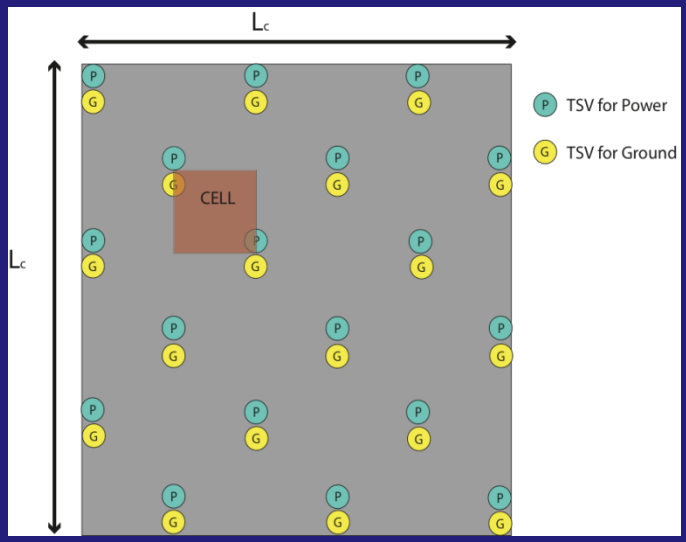


- How do you design and place such a large number of voltage regulators?

Physical Model for 3-D Power Distribution Networks

- Two different types of wiring resources
  - What is the interdependence?
  - TSV uniform allocation across planes
  - Divide stack into unit identical cells to simplify the modeling process

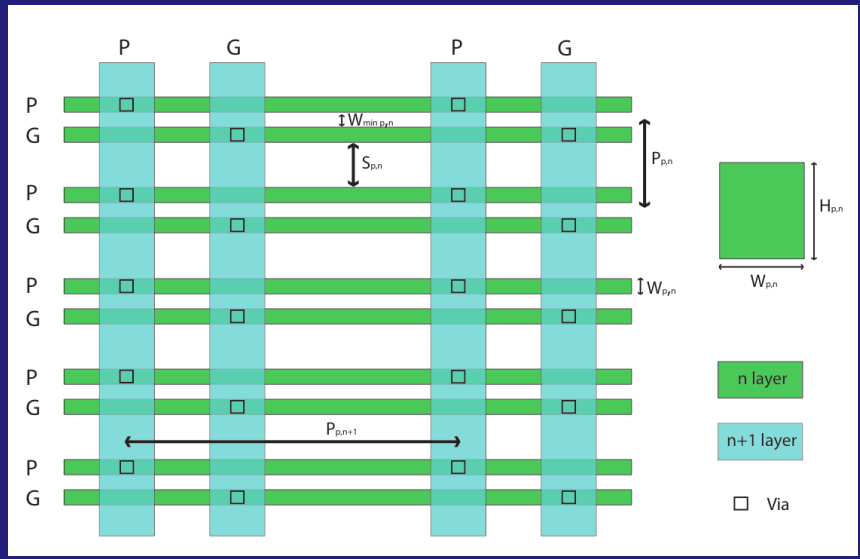




Intraplane Power Grid Modeling

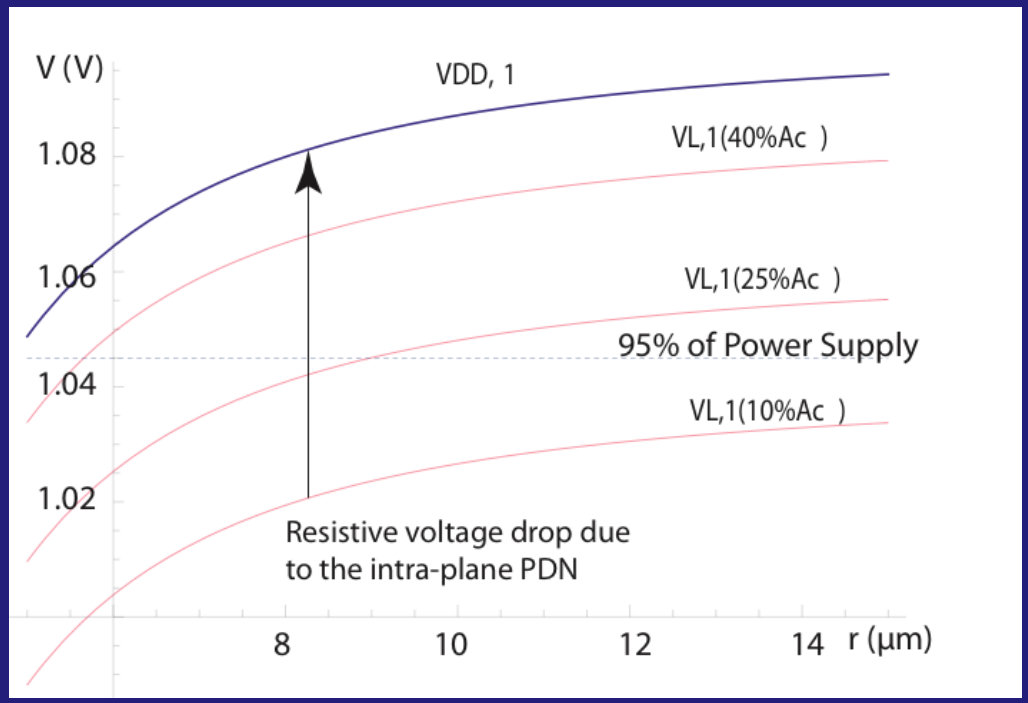
- Paired interdigitated power grid
  - How do the physical parameters of the grid affect the voltage drop in a 3-D IC?

Basic parameters of the model	
I_c	Distributed current across the area of the die.
A_c	Area of the die.
I_{cell}	Current consumed in each cell.
A_{cell}	Area of each cell.
N_{TSV}	Total number of TSVs.



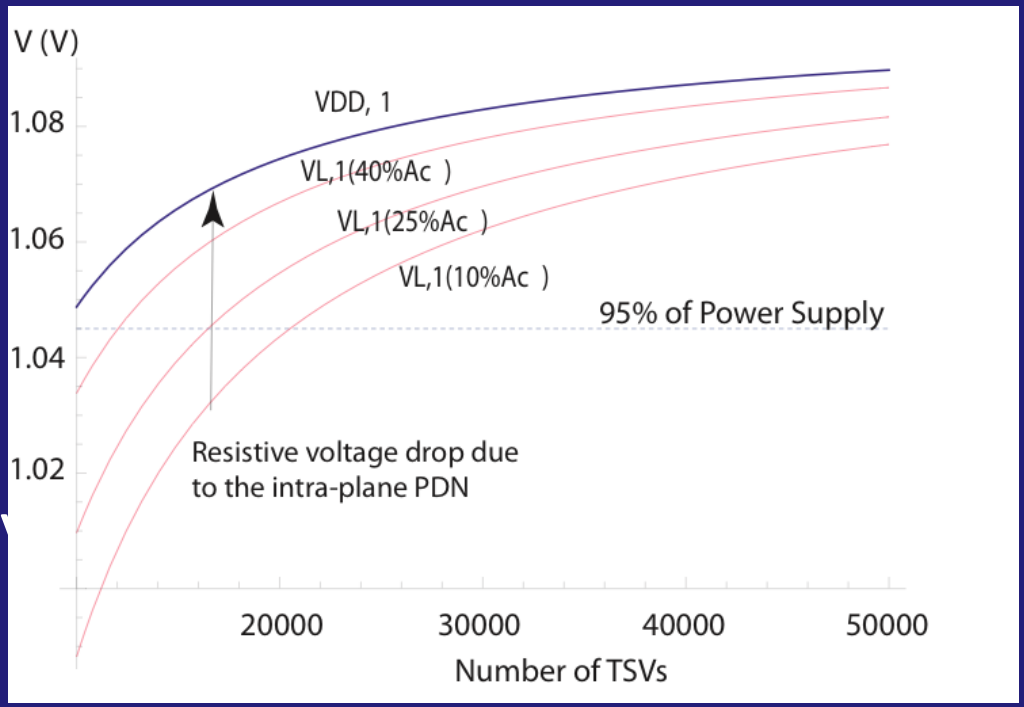
Voltage Drop vs. TSV Density

- V_{dd} = 1.1 Volts
  - Allow 5% ripple
- Ten plane 3-D IC
- Voltage measured next to the load
  - Higher TSV density
  - Smaller current density
  - Higher routing blockage



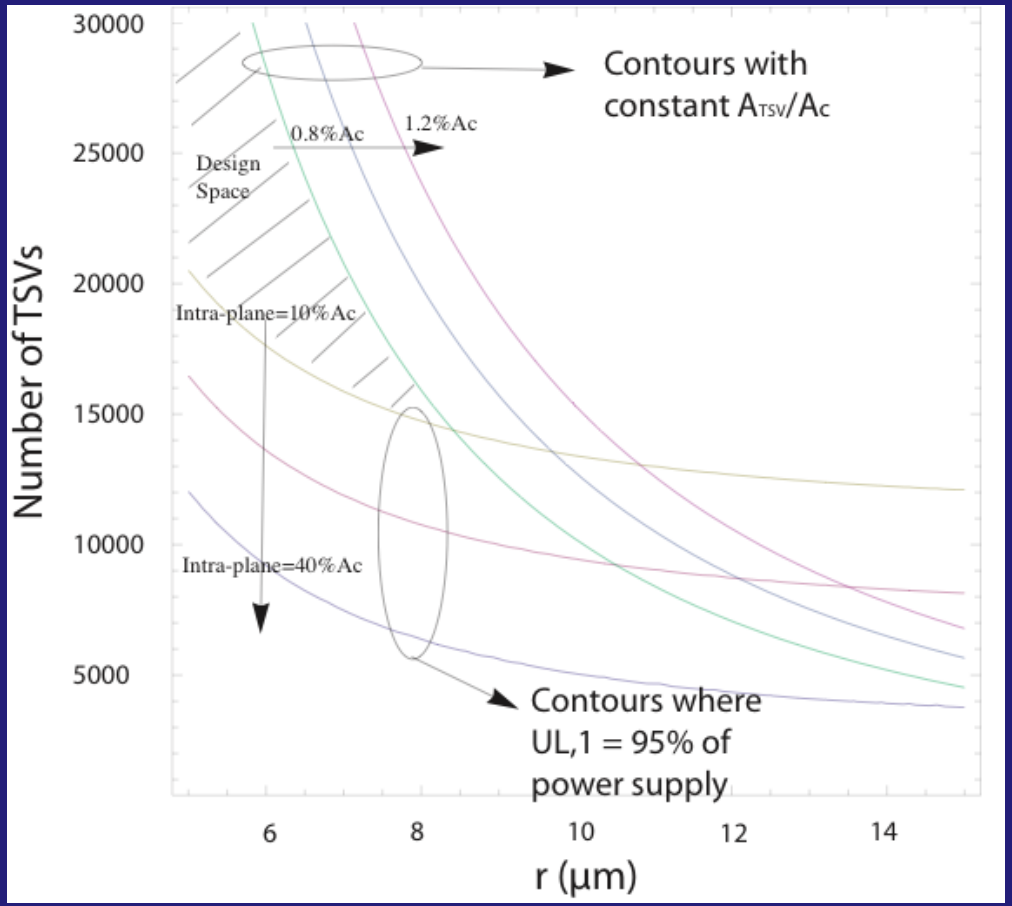
Voltage Drop vs. TSV Diameter

- In both scenarios total TSV area is the same
- Larger TSV diameter
  - Lower TSV resistance
  - Higher TSV capacitance
- TSV resistance is already sufficiently low



Design Space for 3-D PDNs

- For specific area of TSV and intraplane grids
  - A_{TSV} = 0.8% to 1.2%
  - A_{PDN} = 10% to 40%
- Inductive noise further limits the design space
  - Efficient allocation of decoupling capacitance is required



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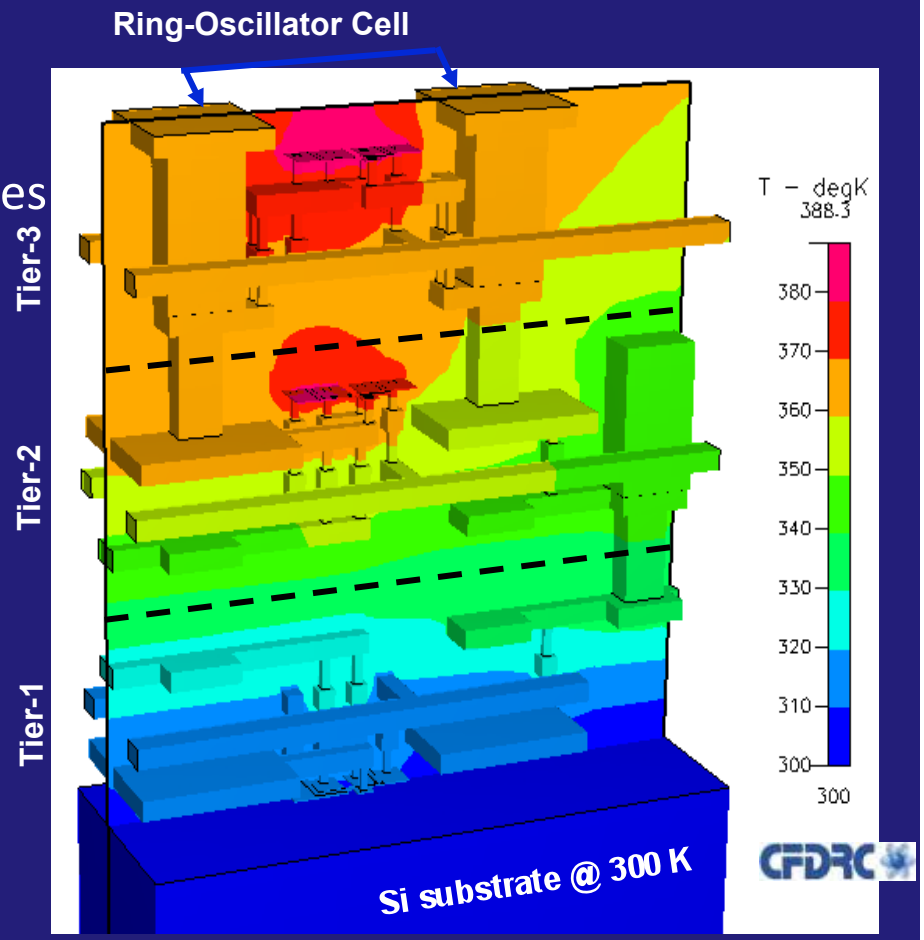
Thermal Management in 3-D ICs

- A multi-level optimization task
- Software – System level
  - How to allocate tasks on different cores
  - Frequency/voltage scaling schemes
- Architectural level
  - NoC topologies
  - Communication architectures
    - Synchronous vs. asynchronous
- Physical level
  - Circuit partition/floorplanning
  - Thermal TSV insertion techniques
- Package level
  - Novel packaging ??????
  - New cooling techniques
    - Liquid cooling?



- Simulation of temperature distribution of ring oscillator in 3D circuit*

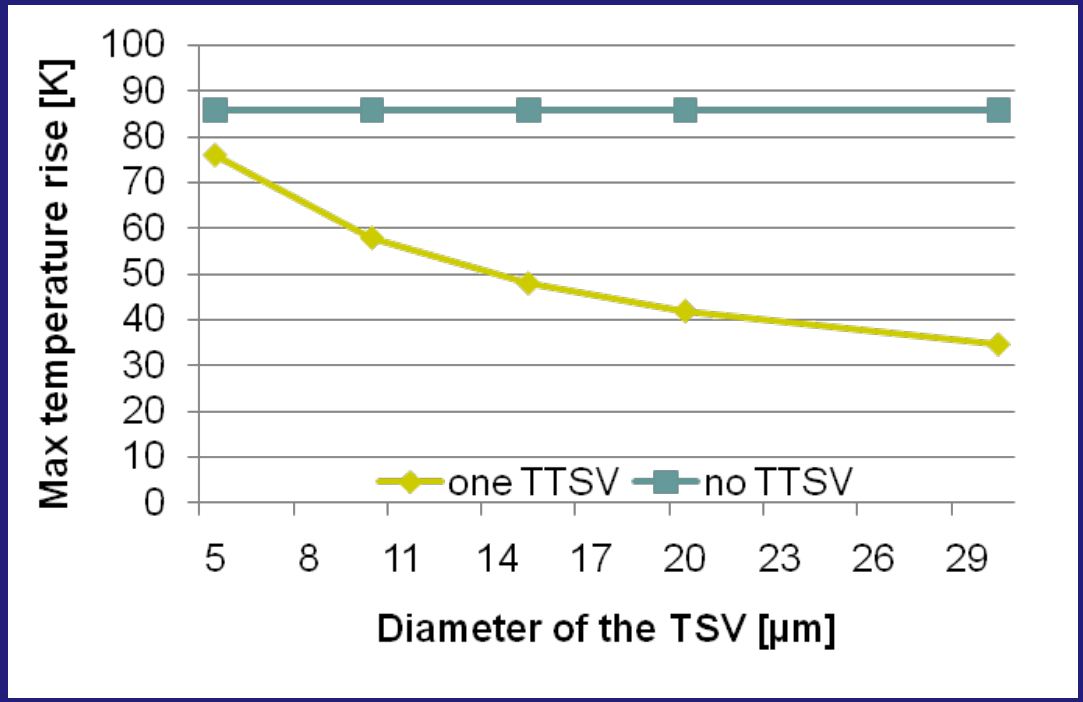
*2007 SOI Conference Papers 6.2 and 6.3 by T.W. Chen, *et al.,* and C.L. Chen, *et al.,*

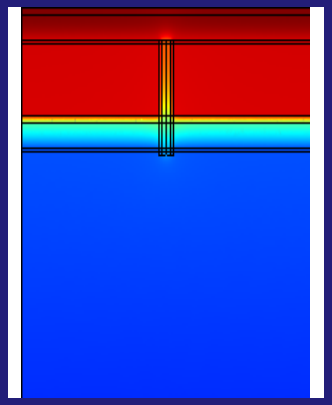
Effect of Thermal TSV on Circuit Temperature

- TTSVs are an effective means to conduct the generated heat to the heat sink through the physical planes
- The effect of the physical and technological parameters of TTSVs on the heat transfer process needs to be investigated
  - Diameter, length, dielectric thickness, density, *etc.*
- COMSOL multiphysics tool is employed

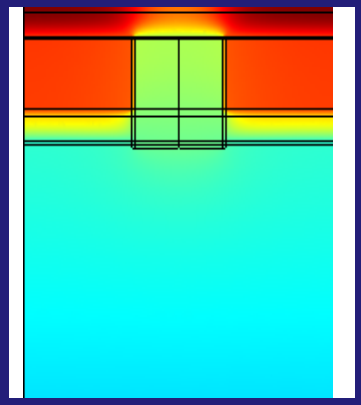
Effect of TTSV Diameter

- The maximum temperature within the 3-D IC (T_{max}) decreases as the diameter of TTSV (Φ_t) increases





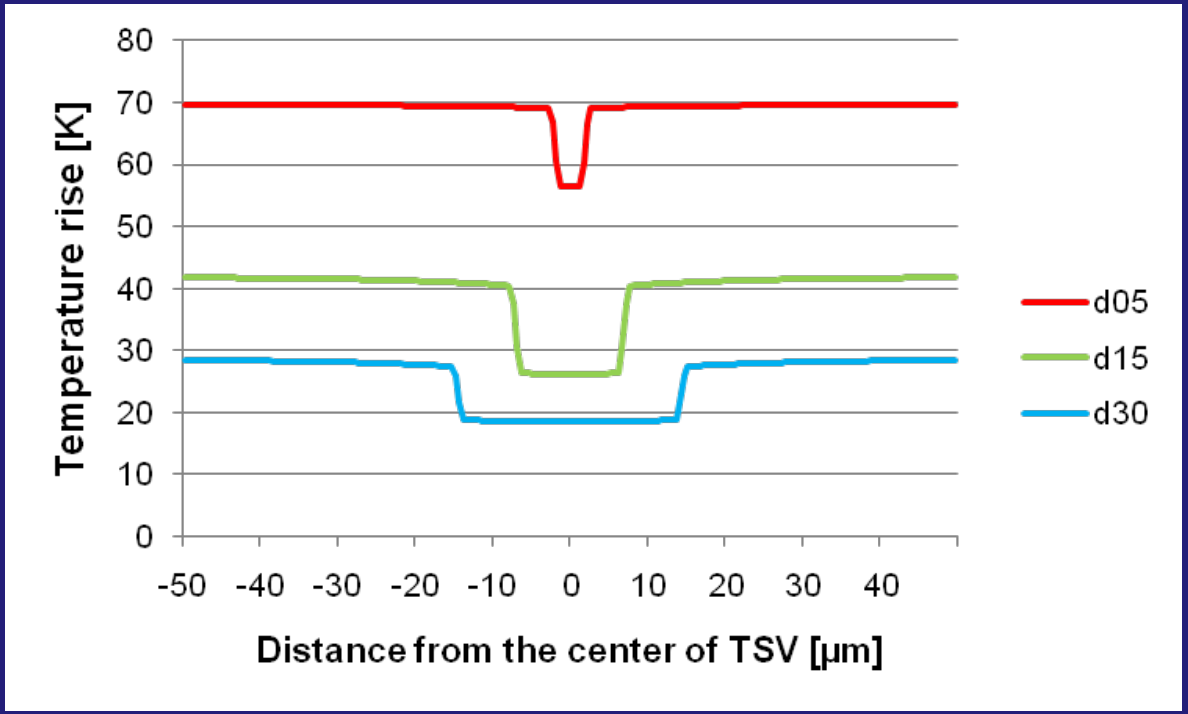
• Φ_t = 5 µm



• Φ_t = 30 µm

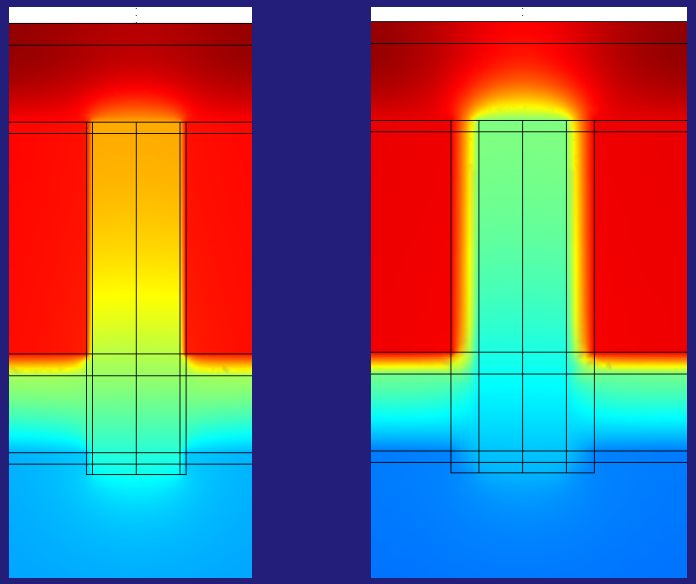
Temperature Variation with Distance from TTSV

- The temperature of a point within one plane increases with the distance from the center of the TSV
  - *d* is the diameter of the TTSV

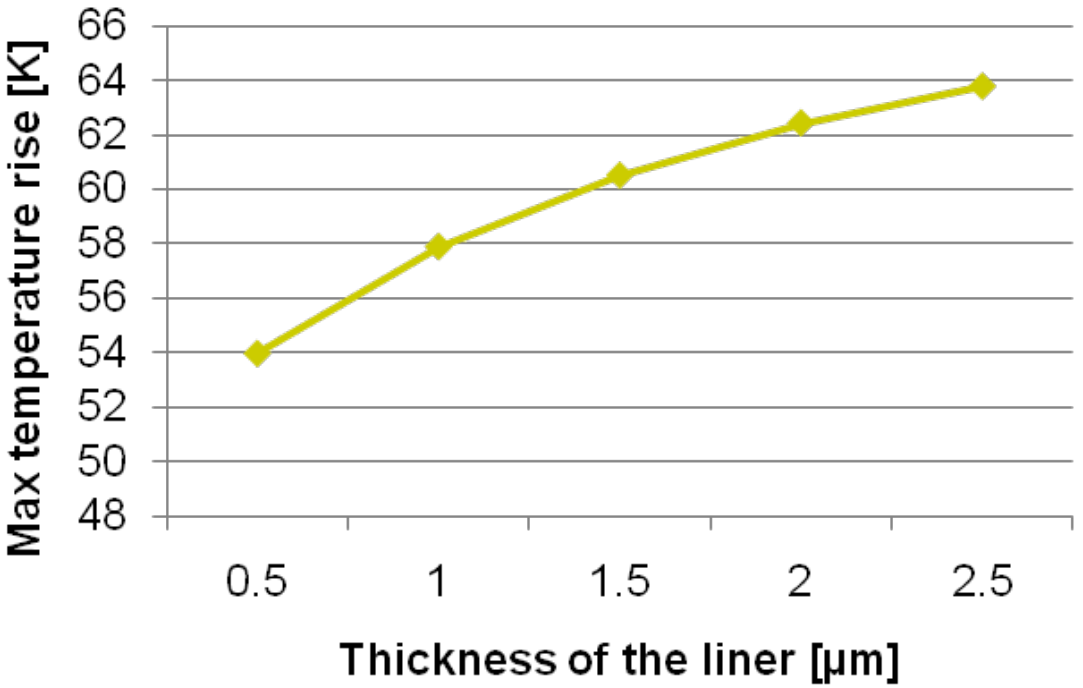


Effect of Dielectric Liner Thickness

- T_{max} increases as the thickness of the dielectric liner (t_{lnr}) increases

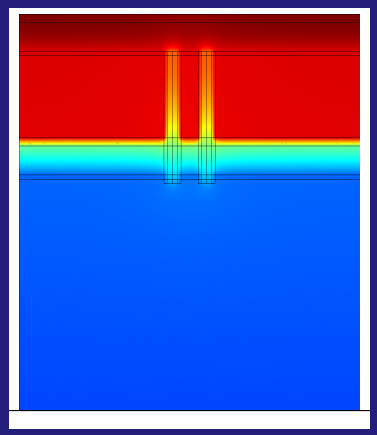


- t_{lnr} = 0.5 µm
- t_{lnr} = 2.5 µm

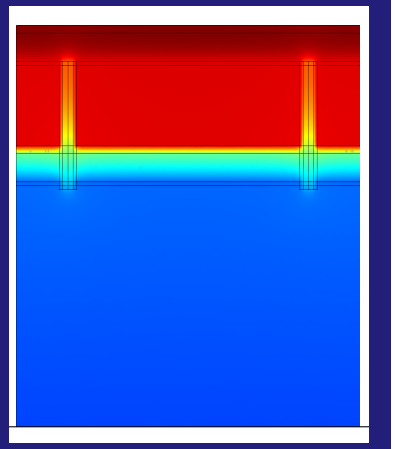


Effect of TTSV Pitch

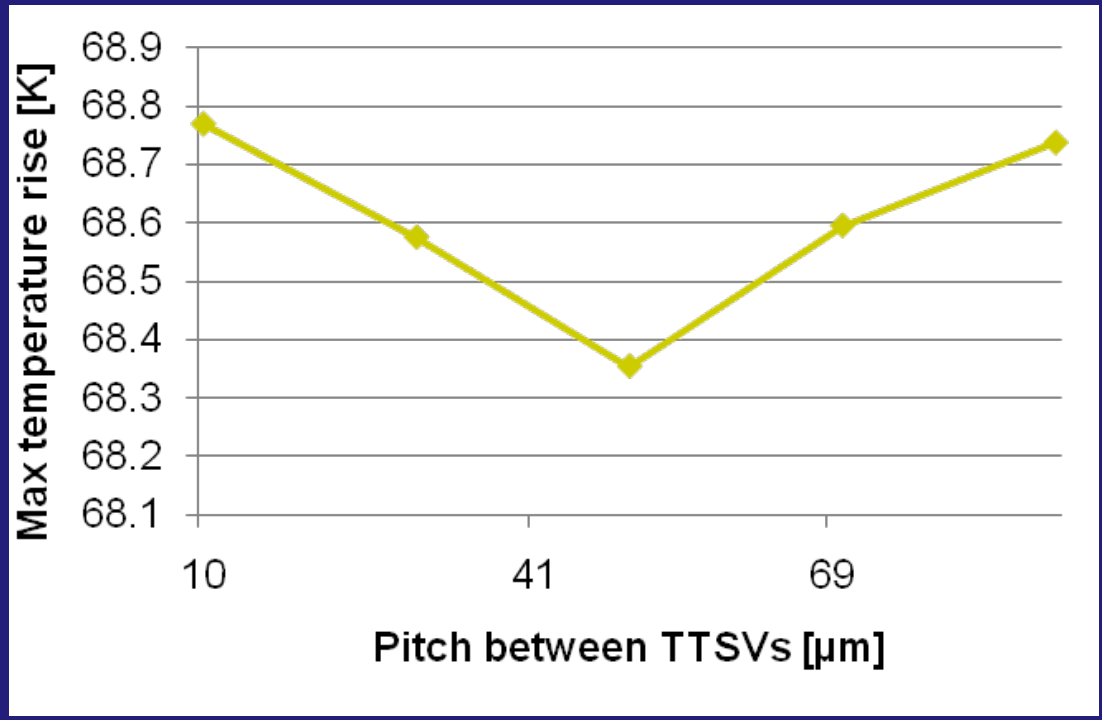
- T_{max} changes non-monotonically with the pitch between TSVs (p)
  - T_{max} first decreases, then increases
  - The effect of p is low for the example of two TSVs (< 0.2%)



• p = 10 µm

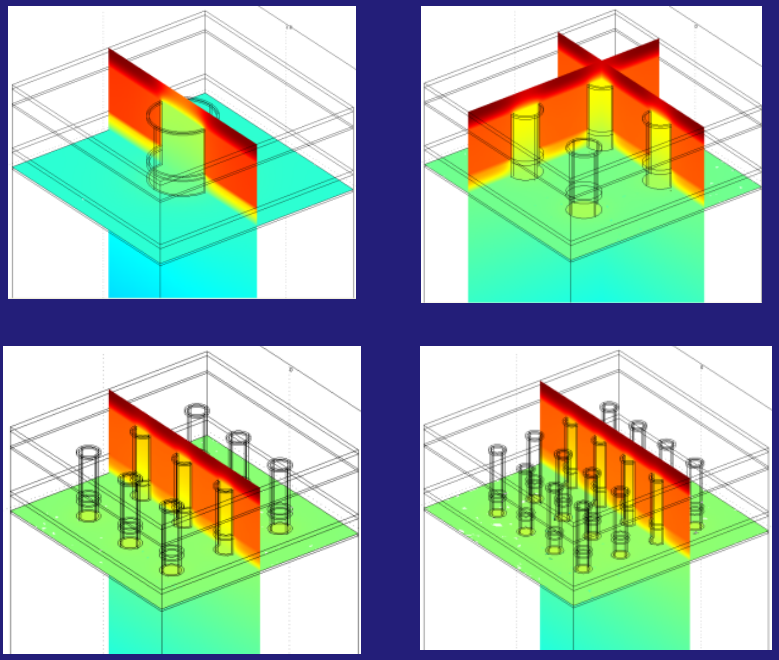


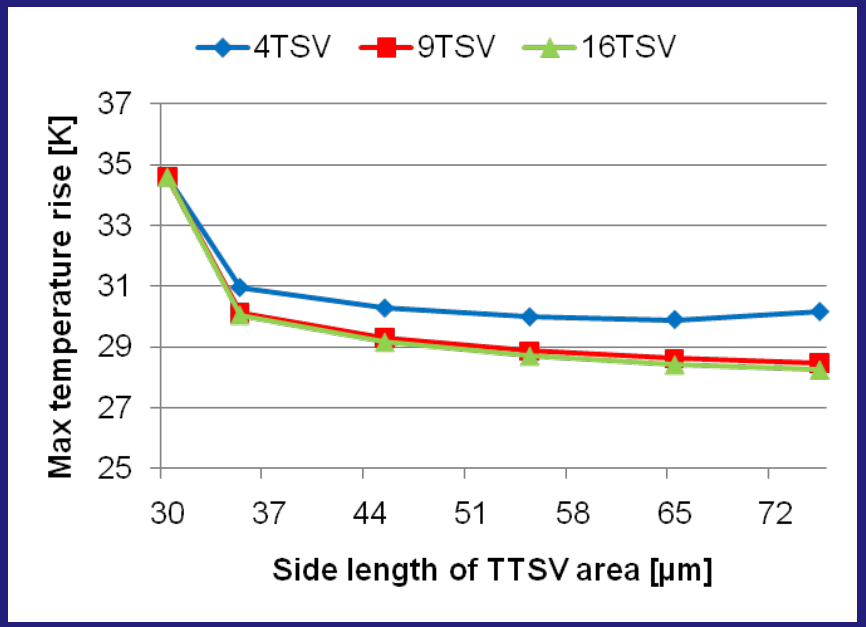
• p = 70 µm



Effect of TTSV Partition

- Dividing a large TTSV into a group of thinner TTSVs can lead to a lower maximum temperature
  - In the example, # of TTSVs does not lower the temperature significantly when # > 9
- The pitch between TTSVs does not affect the temperature significantly





Presentation Outline

- 3-D Integration: Where are we Standing Today?
- Variability Issues in Synchronization Schemes
- Power Integrity Challenges
- Thermal TSV Modeling
- Summary

Summary

- Simply increasing the number of planes does not necessarily improves skew variation
  - Absolute frequency can, however, increase
- Multi-clock schemes remain a conundrum for 3-D Ics
- 3-D power distribution network should be considered collectively rather than individually on per plane basis
- TSV density is more important than the TSV size in reducing *IR* drop
- Thermal TSVs facilitate the flow of heat from 3-D ICs
  - The efficiency of this means depends on several factors!
  - Modeling the TSV as simple linear thermal resistor may be inaccurate

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Thank you for your attention!