

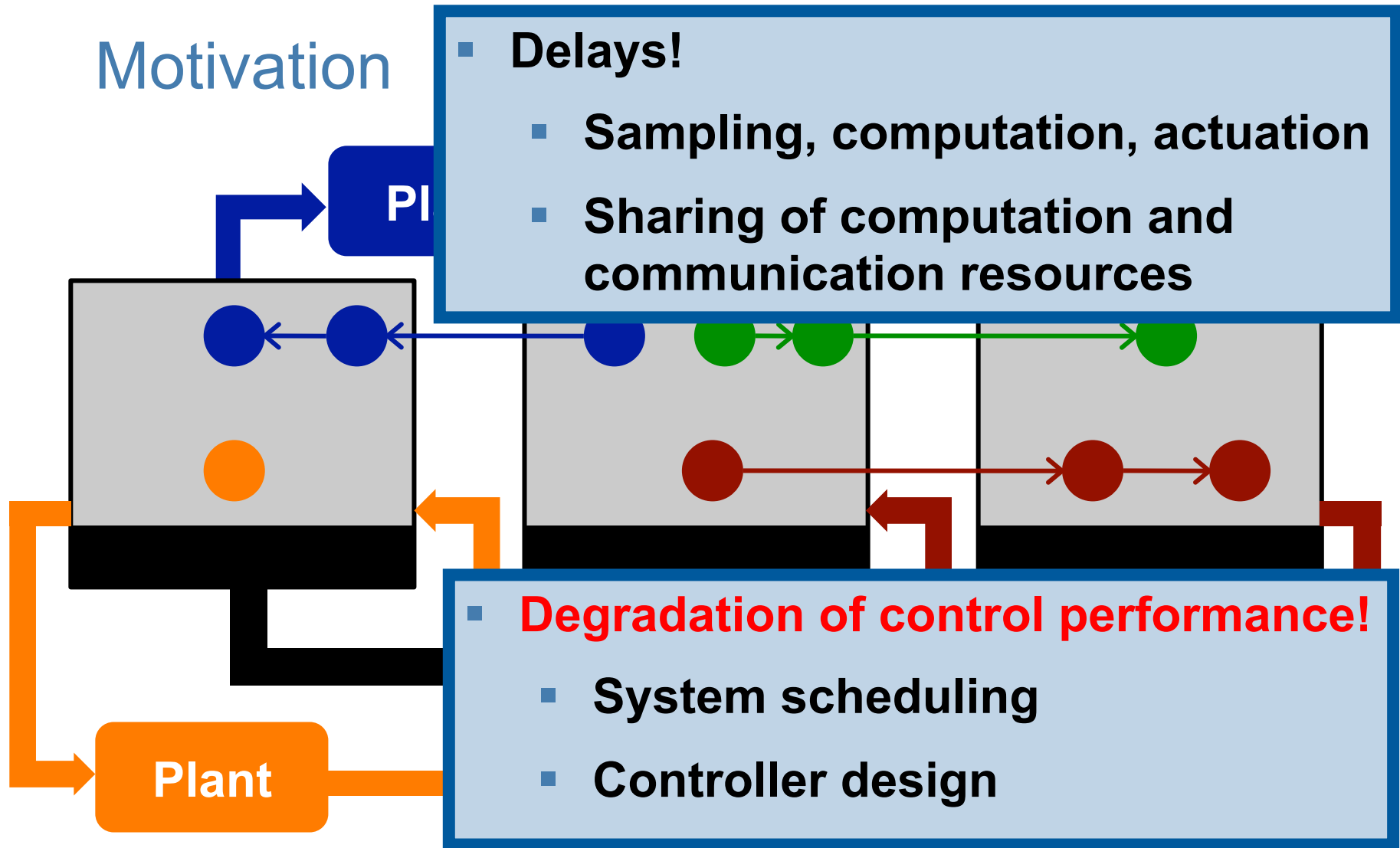
Integrated Scheduling and Synthesis of Distributed Embedded Control Applications

Soheil Samii¹, Petru Eles¹, Zebo Peng¹, Anton Cervin²

¹ Dept. of Computer and
Information Science
Linköping University
Sweden

² Dept. of Automatic Control
Lund University
Sweden

Motivation



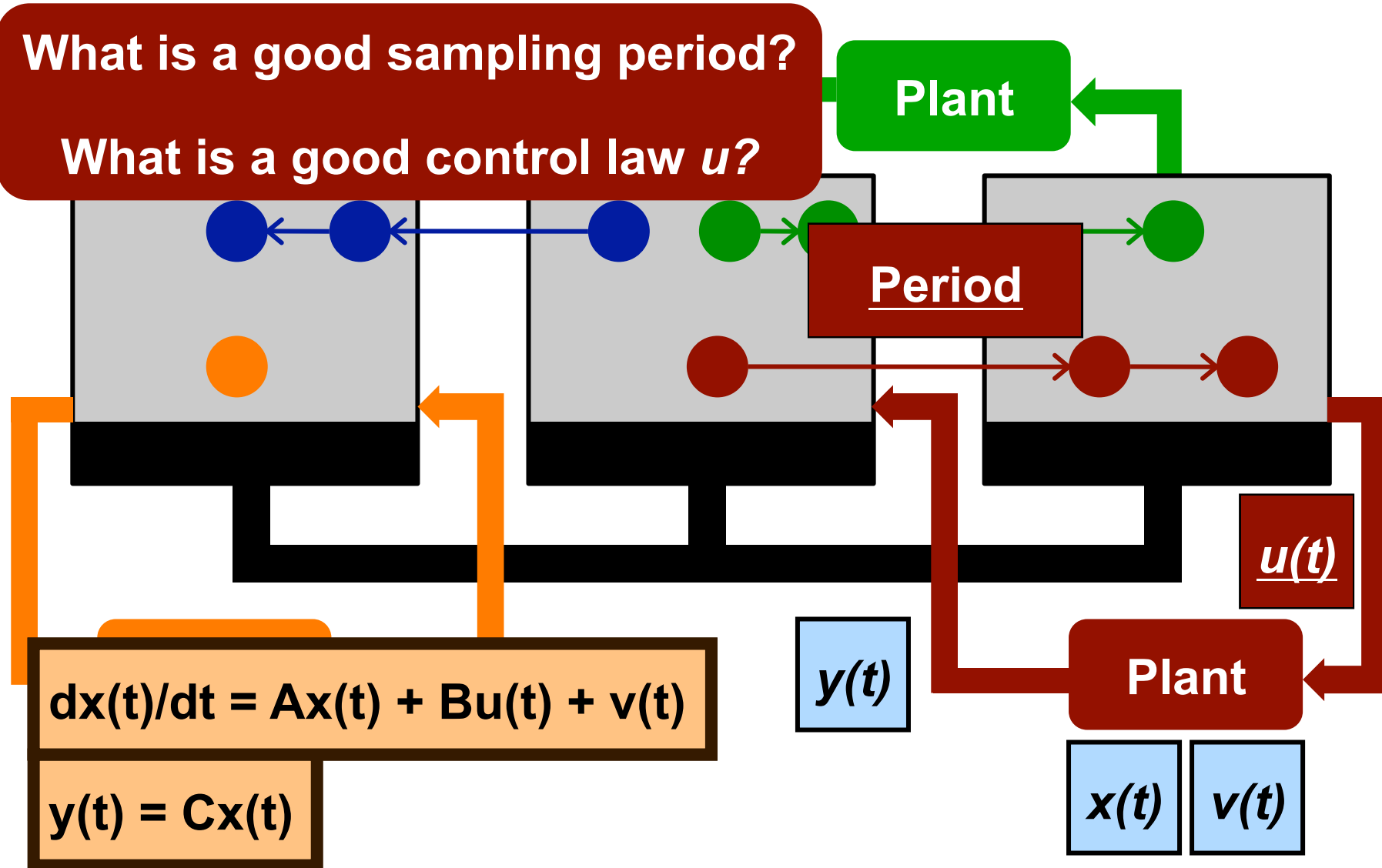
Outline

- **System model and control performance**
 - **Integrated control and scheduling**
 - **Multi-mode system synthesis**

System model

What is a good sampling period?

What is a good control law u ?



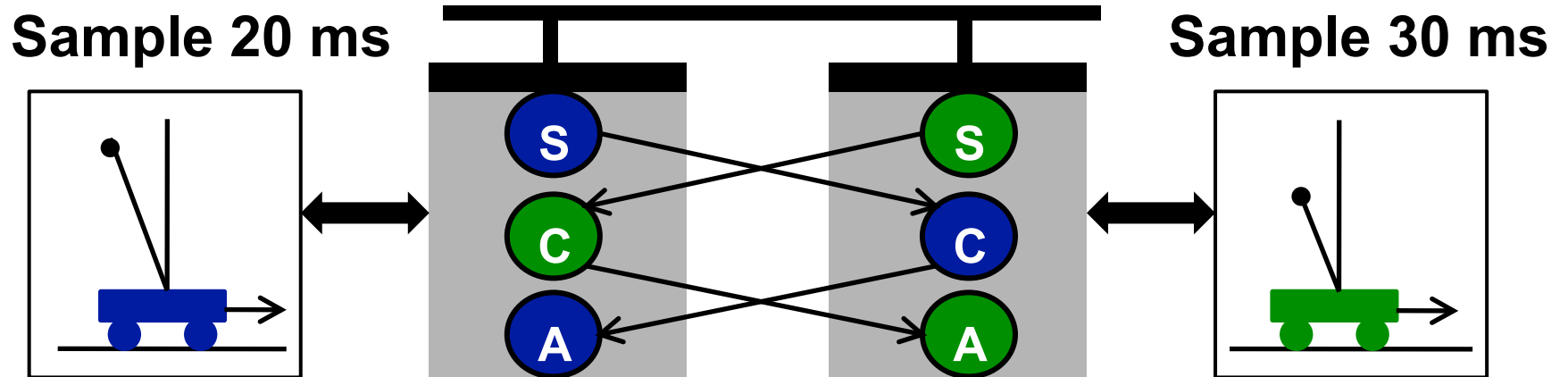
Control performance

- **Quadratic cost: $J = E\{ \mathbf{x}^T \mathbf{Q}_1 \mathbf{x} + \mathbf{u}^T \mathbf{Q}_2 \mathbf{u} \}$**
- **Depends on**
 - **the sampling period,**
 - **the control law, and**
 - **the schedule (delays between sampling and actuation)**
- **Synthesis of optimal control law for given period and constant delay**
- **”Jitterbug” (Lund University)**

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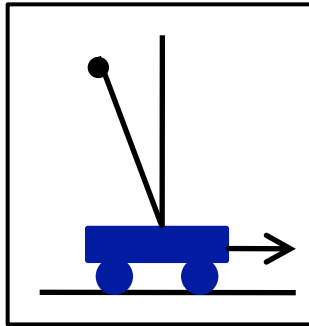
Example



- Control laws synthesized for the constant delays of each application
- $J_1=0.9$, $J_2=2.4$, *Total*=3.3

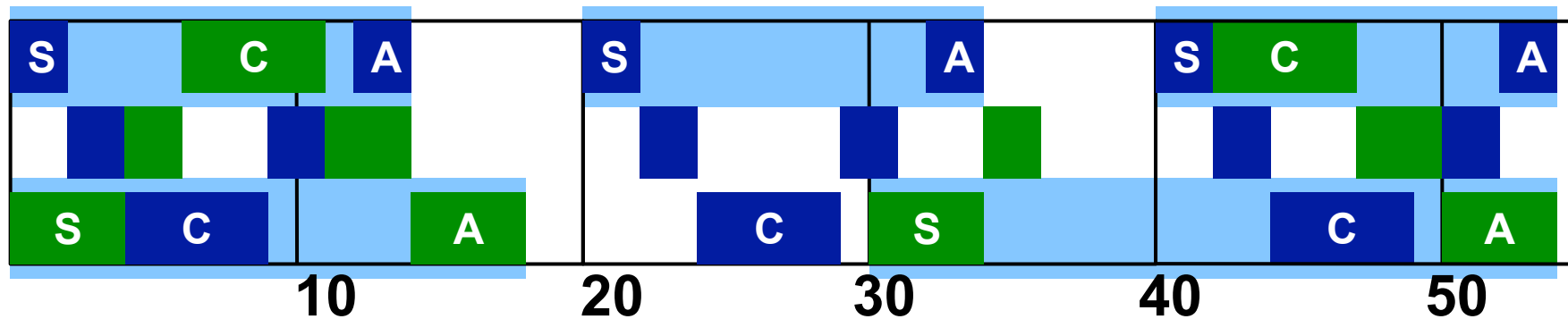
Example: Sched

Sample 20 ms



- Ideal case
 - $J_1=0.9, J_2=2.4, Total=3.3$

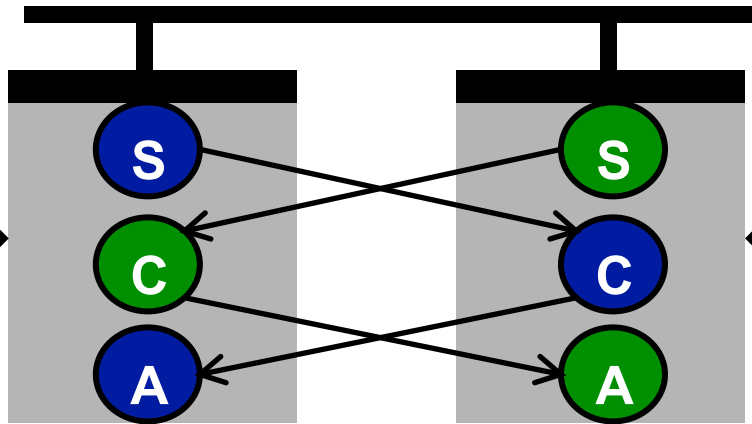
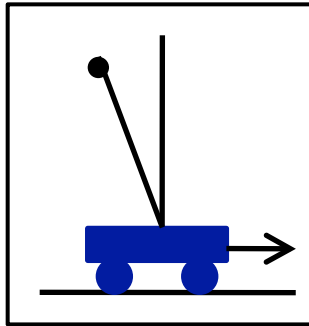
- Compensate for the delays in the schedule
 - $J_1=1.0, J_2=3.7, Total=4.7$



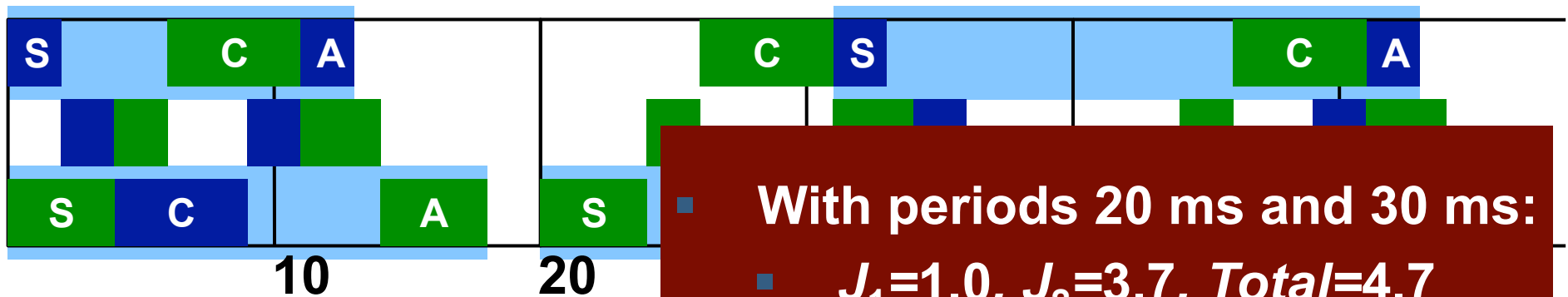
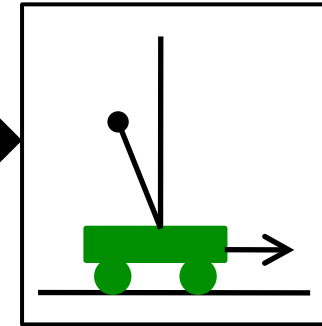
- $J_1=1.1, J_2=5.6, Total=6.7$

Example: Change periods

Sample 30 ms

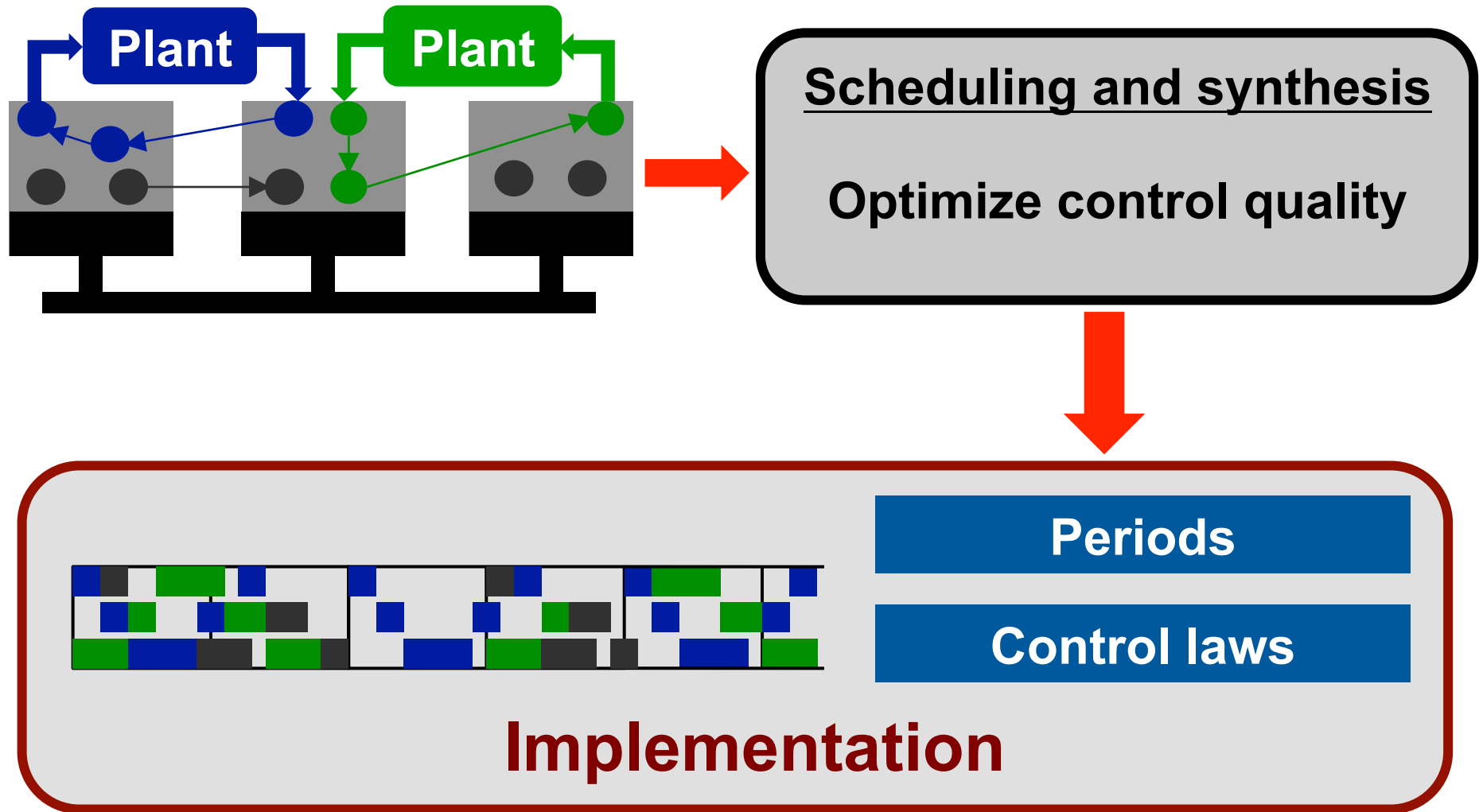


Sample 20 ms



- $J_1=1.3, J_2=2.1, Total=3.4$ (with delay compensation)

Design tool for embedded control systems



Approach

Optimization of task periods

Genetic algorithms

Task and message scheduling

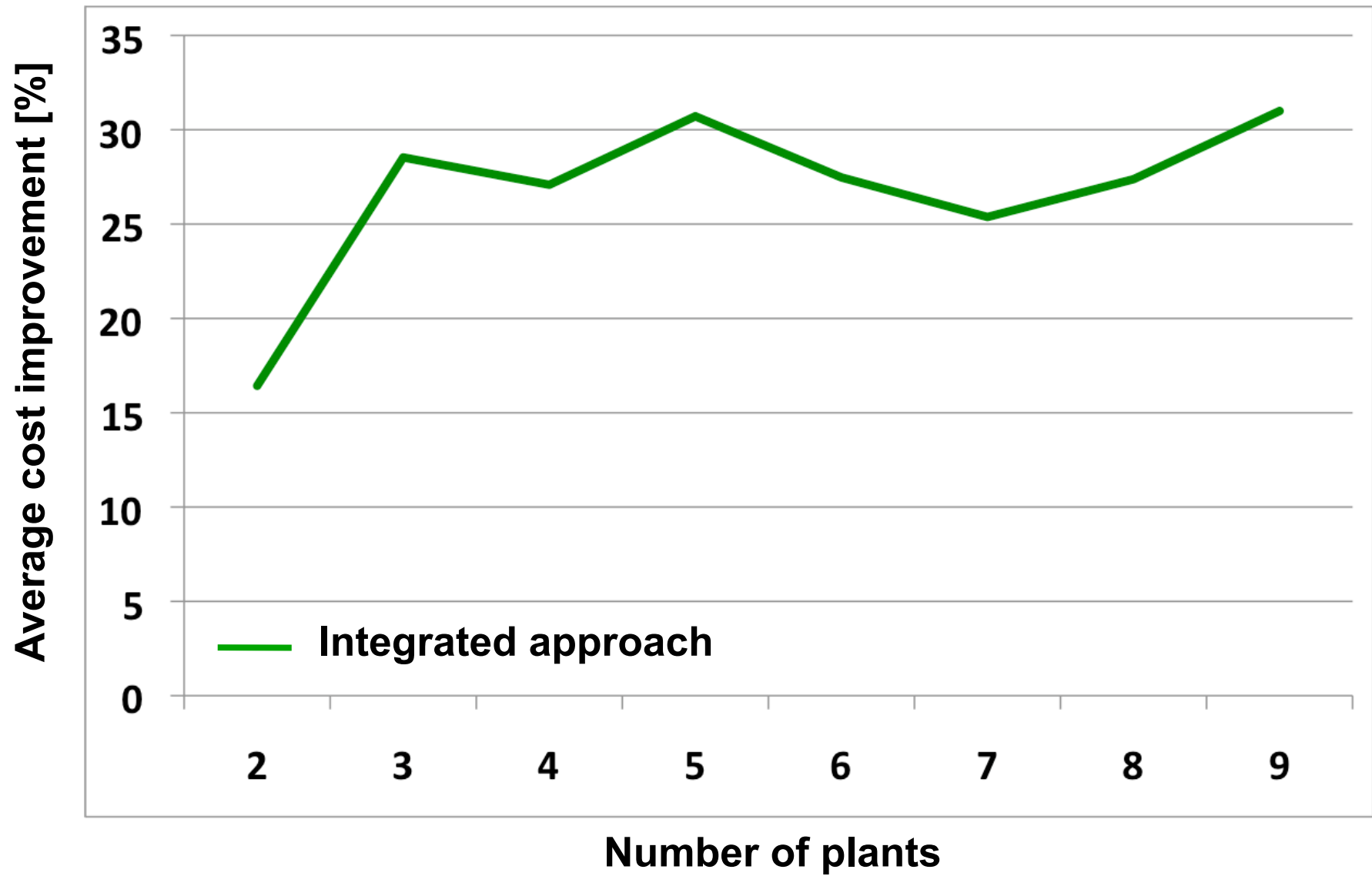
CLP solver

Synthesis of control laws

**Temporal simulation
Jitterbug toolbox**

Compute control costs

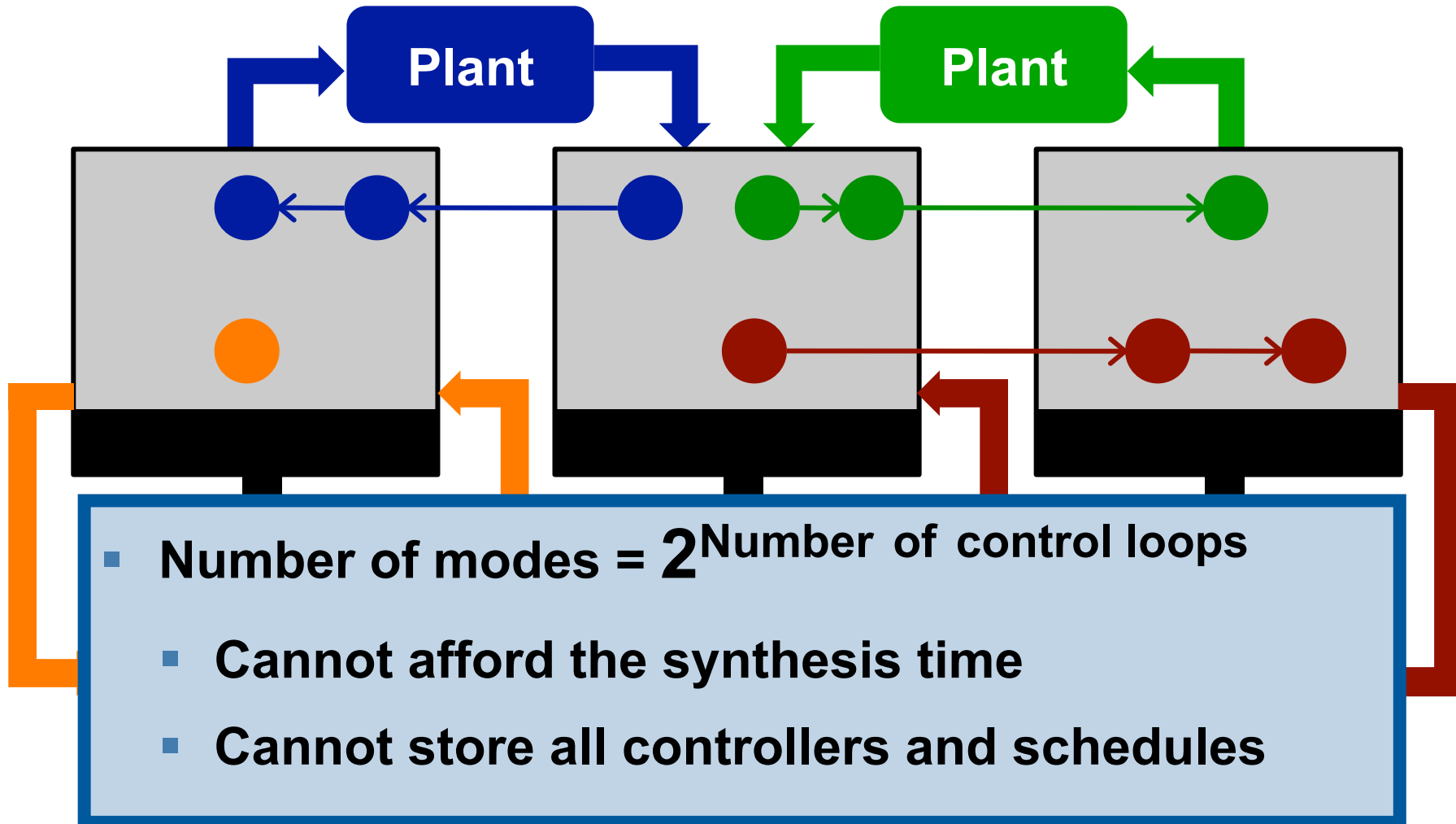
Experimental results



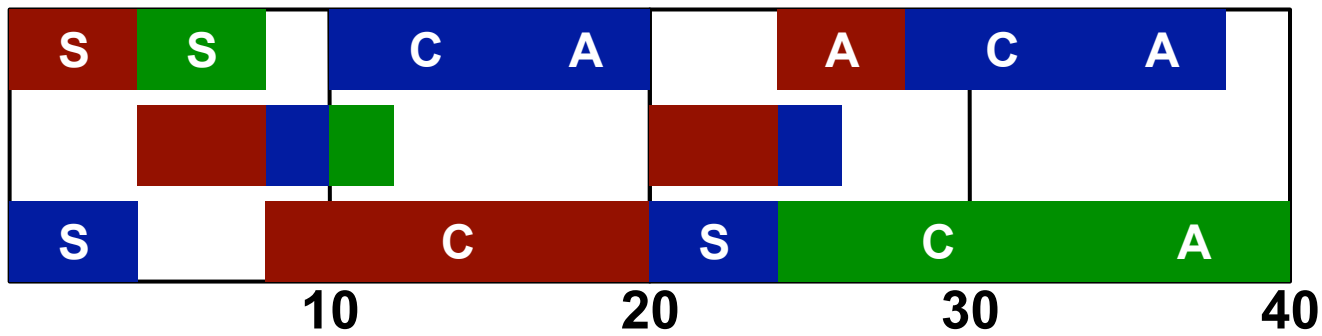
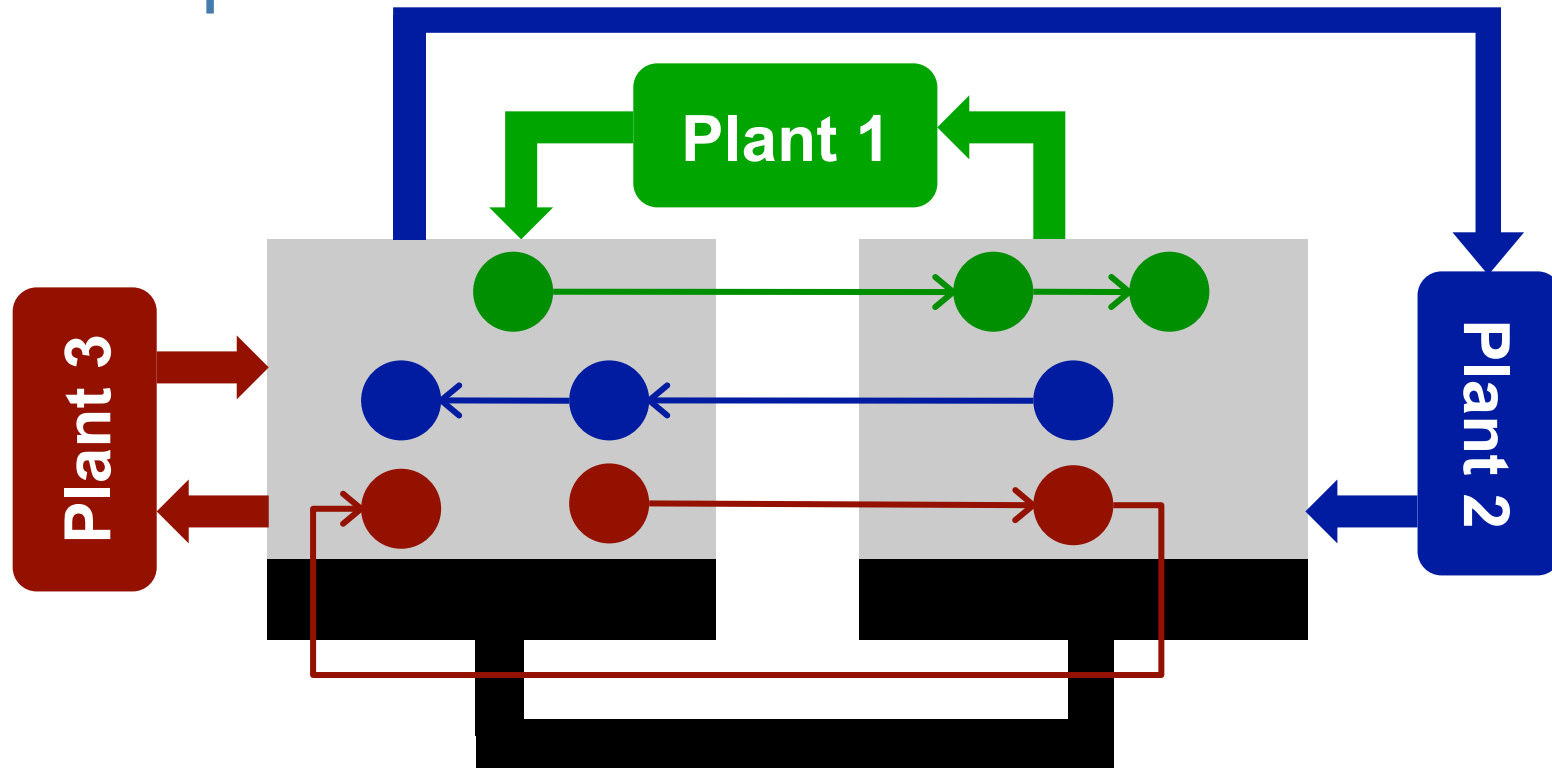
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Motivation



Example

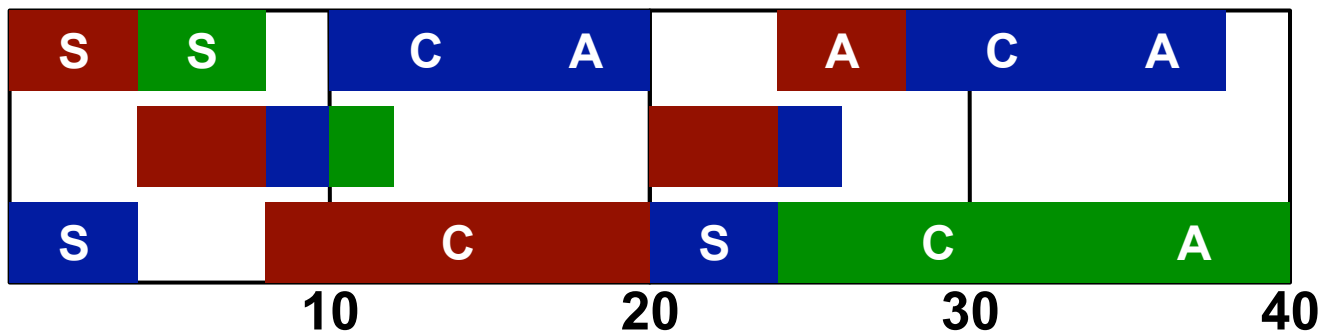
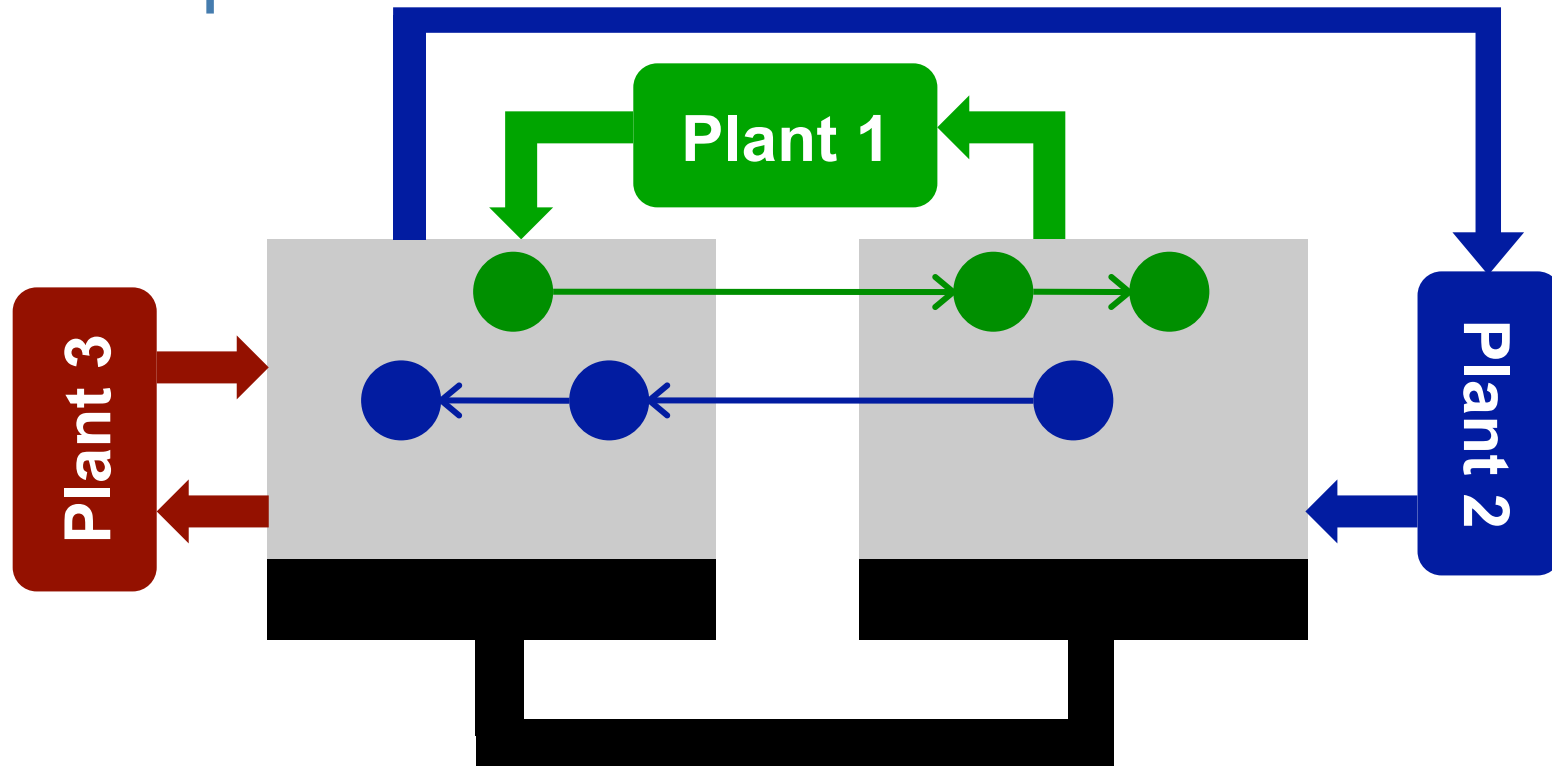


$$J_1 = 3.0$$

$$J_2 = 1.2$$

$$J_3 = 2.2$$

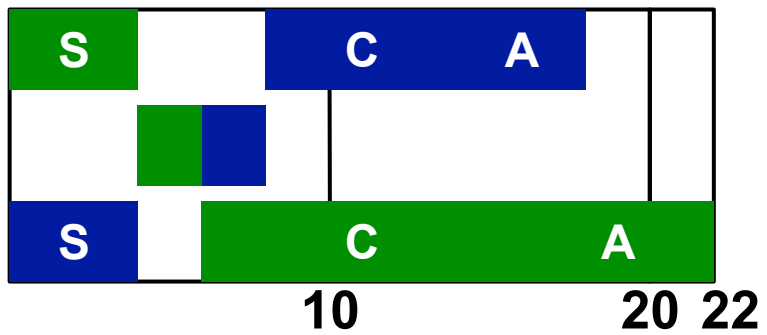
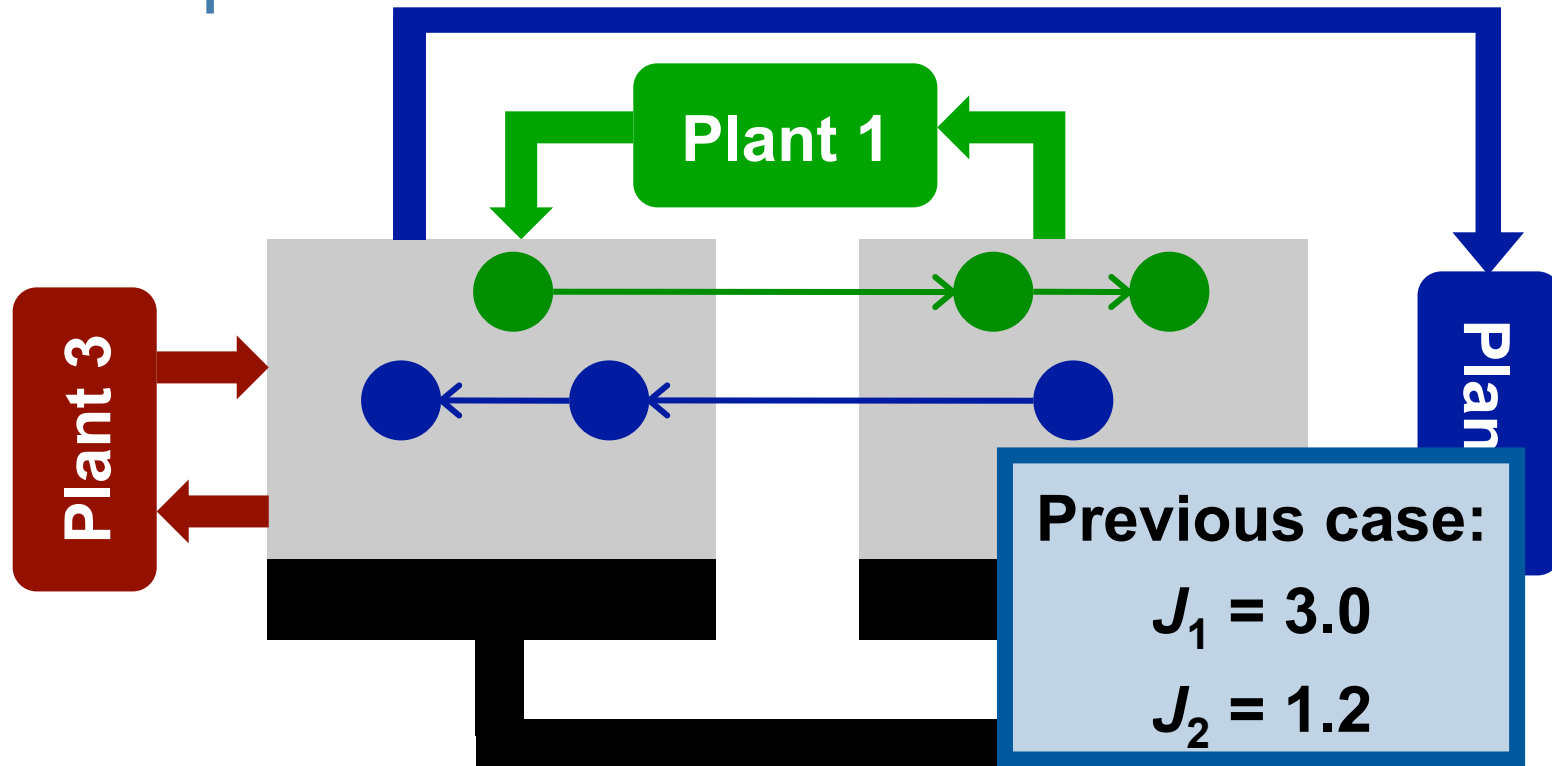
Example



$$J_1 = 3.0$$

$$J_2 = 1.2$$

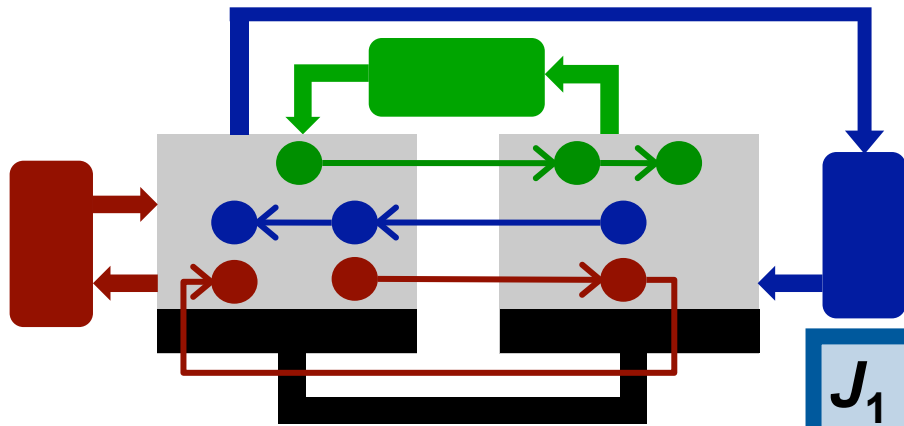
Example



$$J_1 = 1.6$$

$$J_2 = 1.4$$

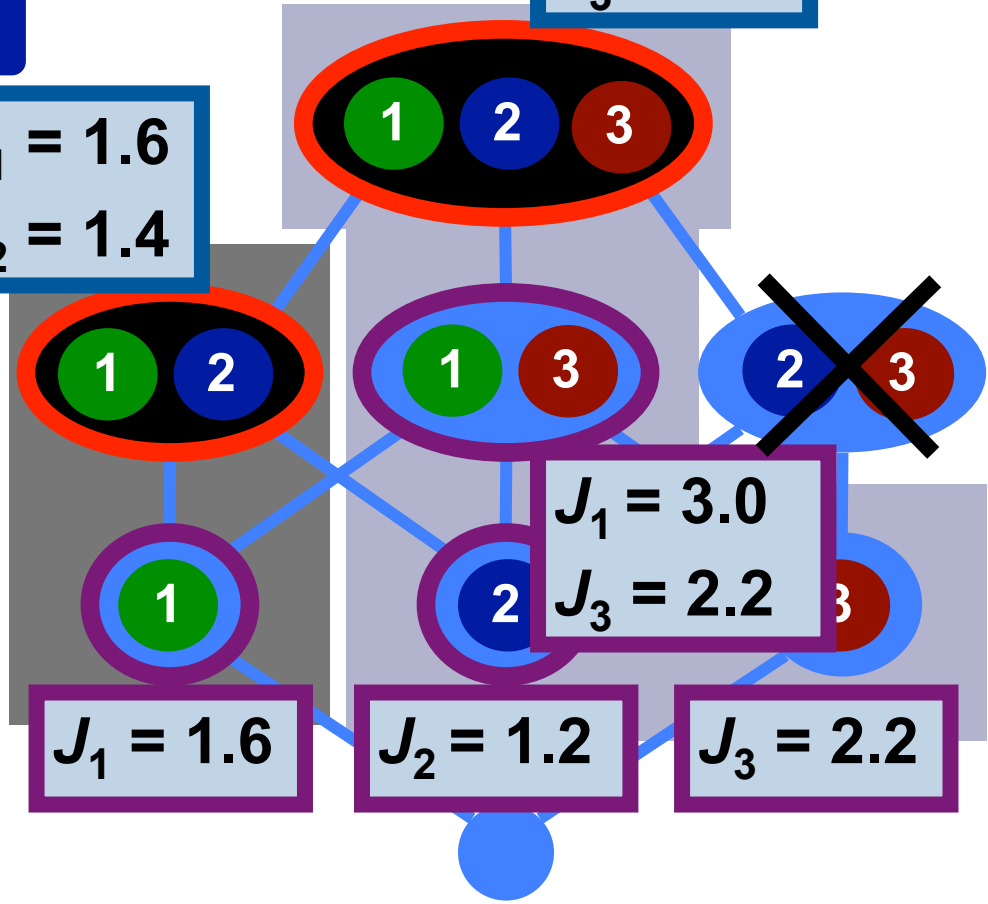
Example



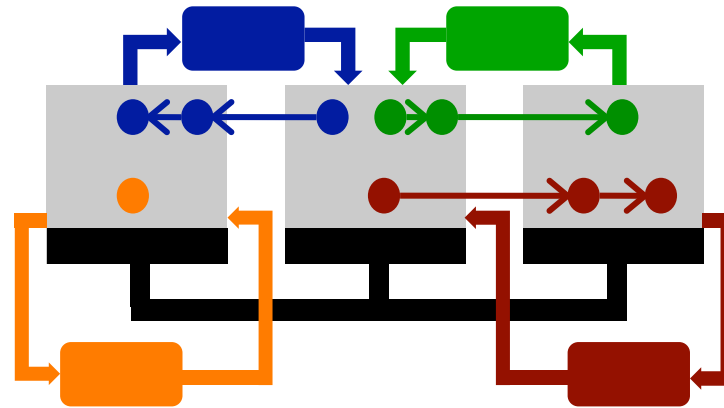
$$J_1 = 1.6$$
$$J_2 = 1.4$$

$$J_1 = 3.0$$
$$J_2 = 1.2$$
$$J_3 = 2.2$$

Cumulative cost of all modes: 19.6



Synthesis tool for multi-mode systems



**Select modes to
synthesize**

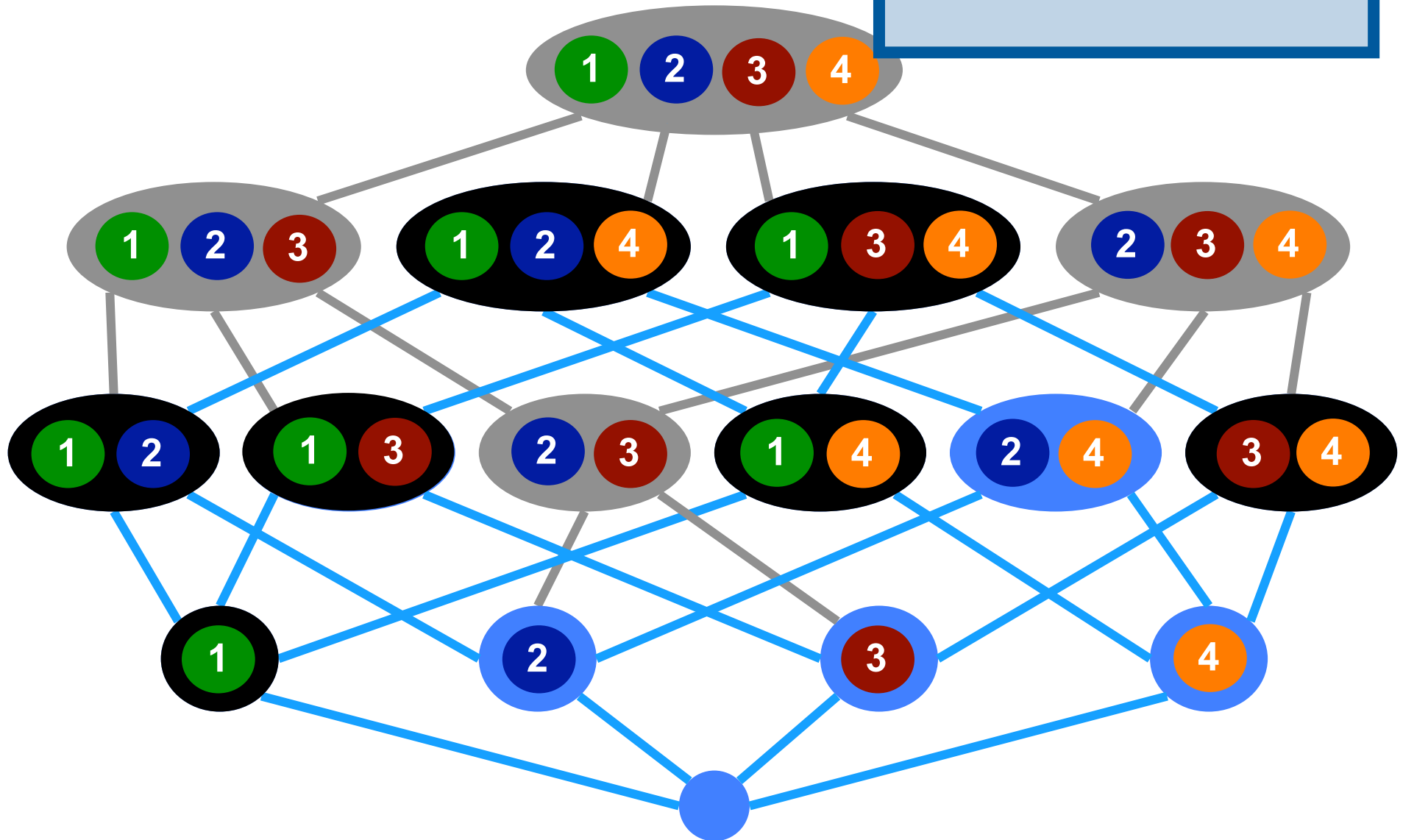
**Optimize control
performance**

Design time

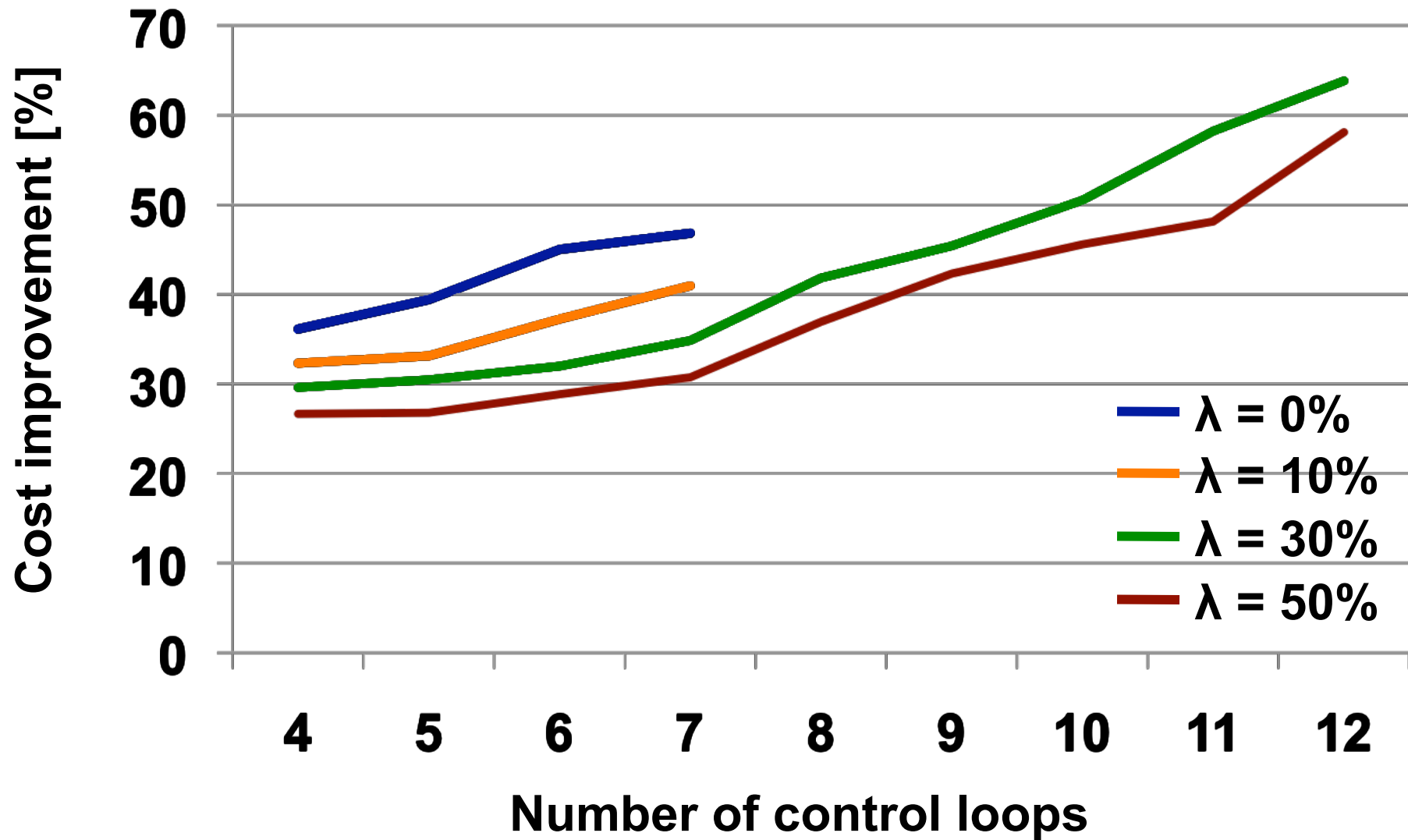
Memory limitations

Synthesis approach

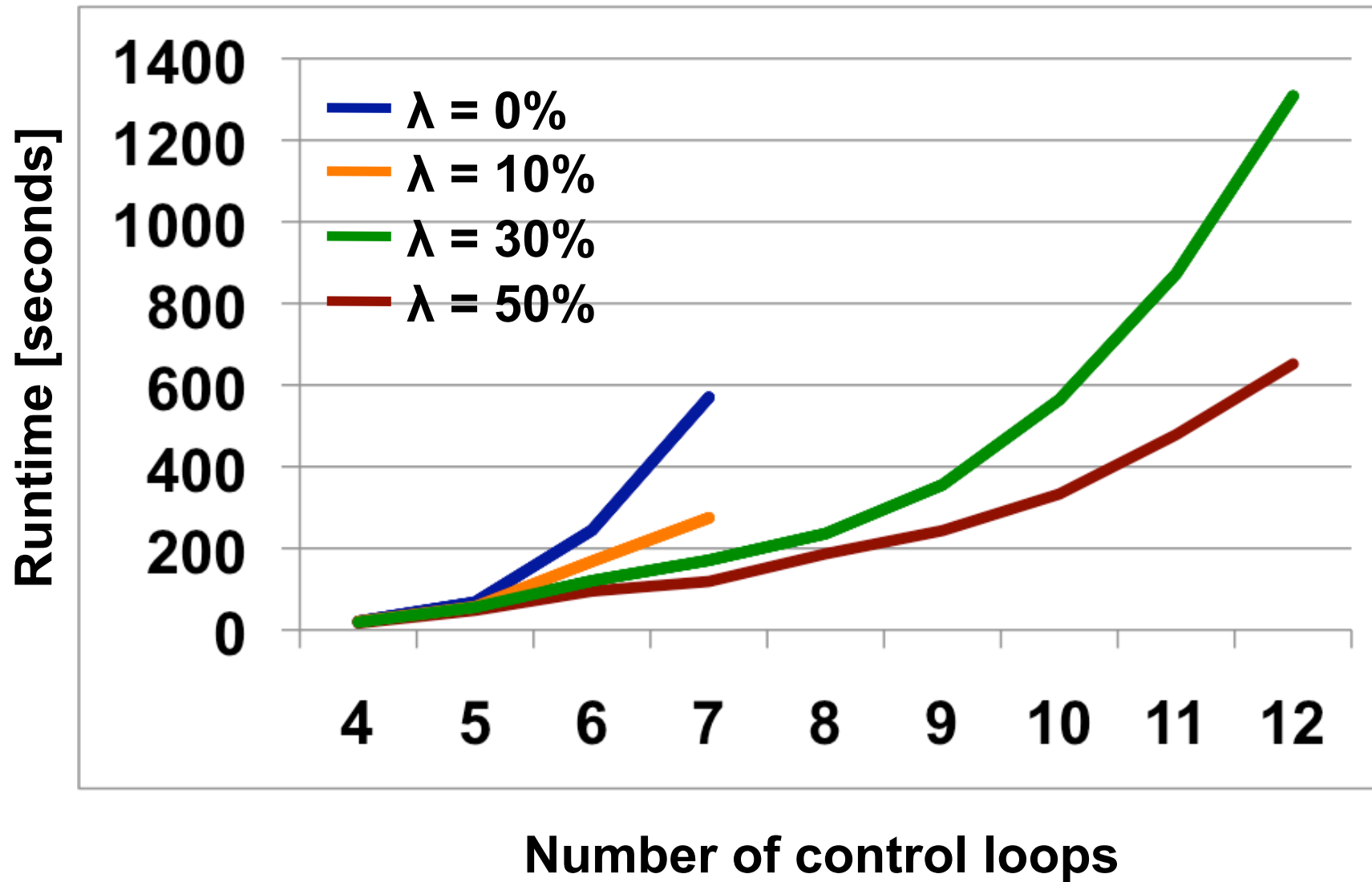
Parameter $\lambda \geq 0\%$



Experiments – Synthesis Quality



Experiments – Synthesis Time



Summary

- **Interaction between control design and scheduling**
- **Synthesis of distributed control systems**
 - **Static-cyclic scheduling**
 - **Fixed-priority scheduling**
 - **TTP, CAN, FlexRay**
- **Synthesis of multi-mode control systems**