Encoding Latency Insensitive Design in Lucy-n: first experiments

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Figures of the talk

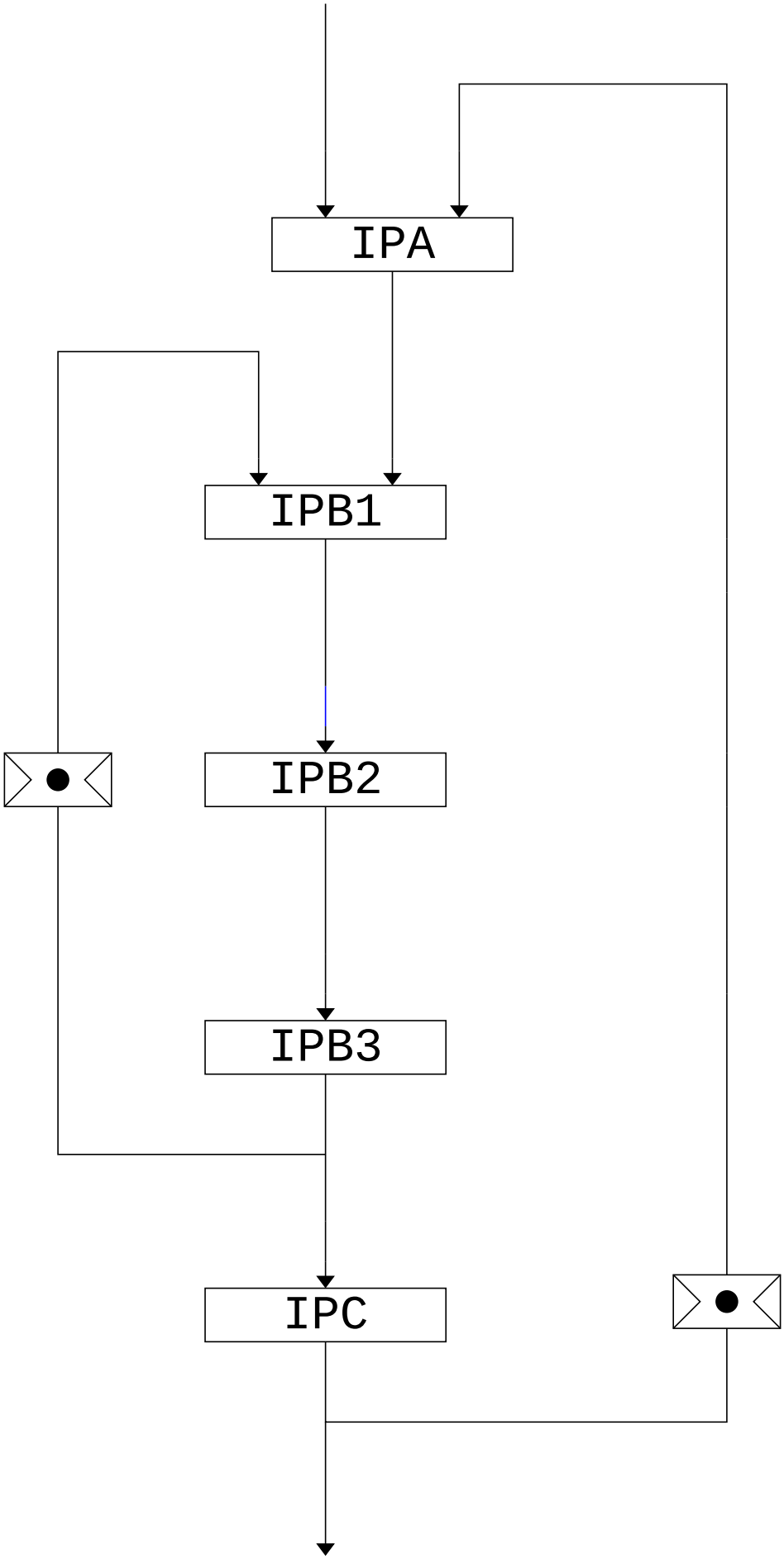


Figure 1 : Synchronous Circuit

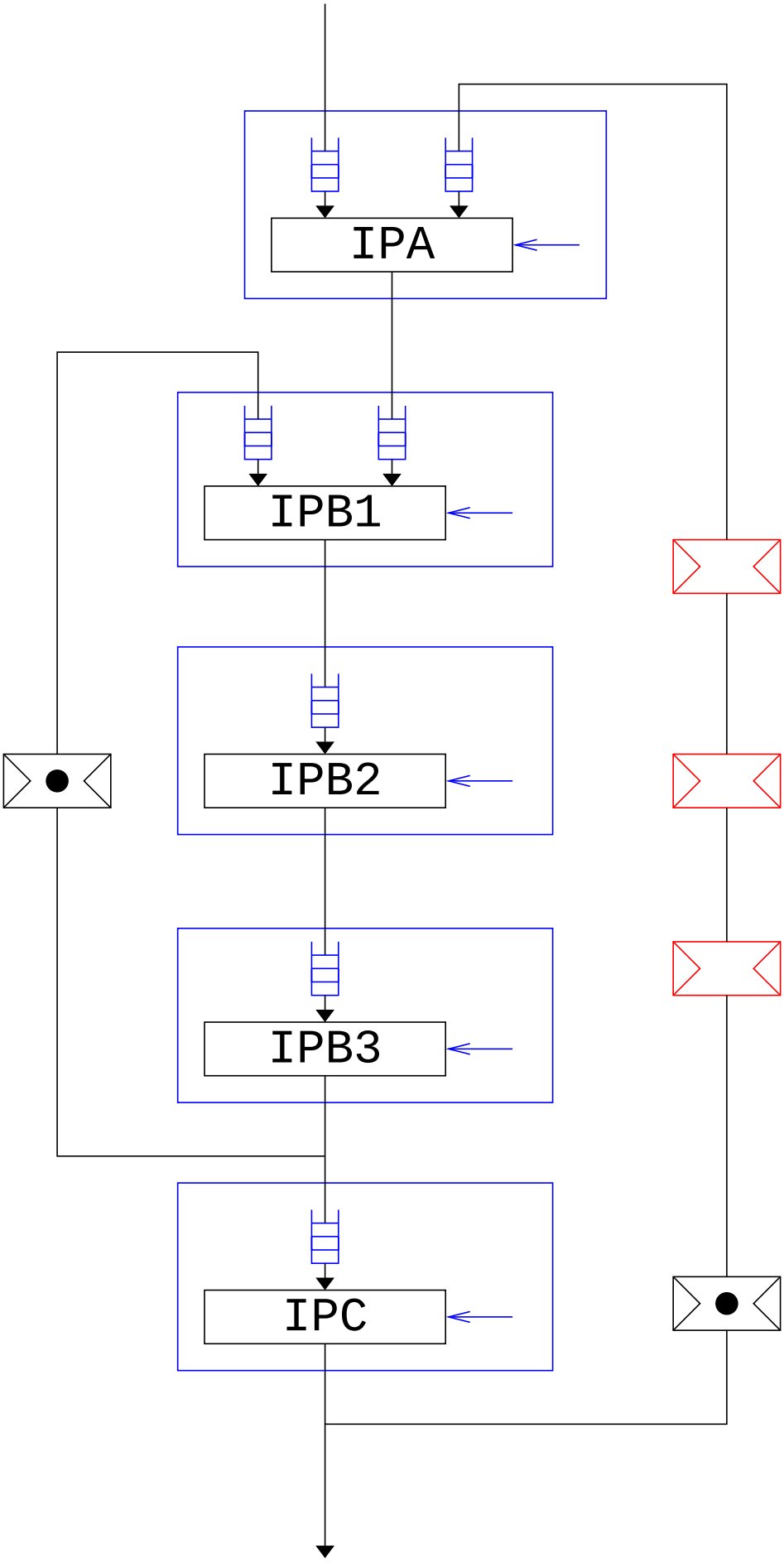


Figure 2 : Design with Latencies

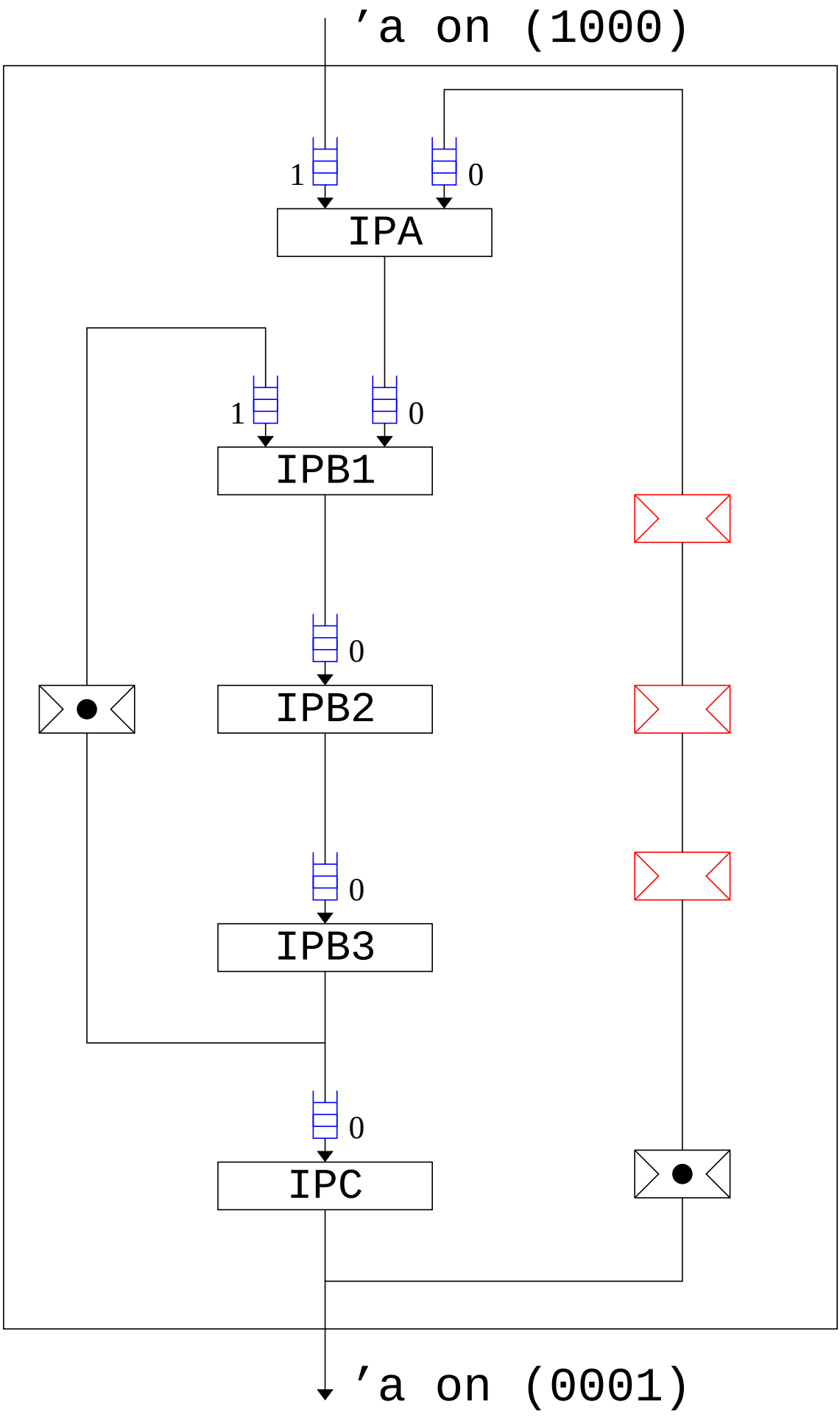
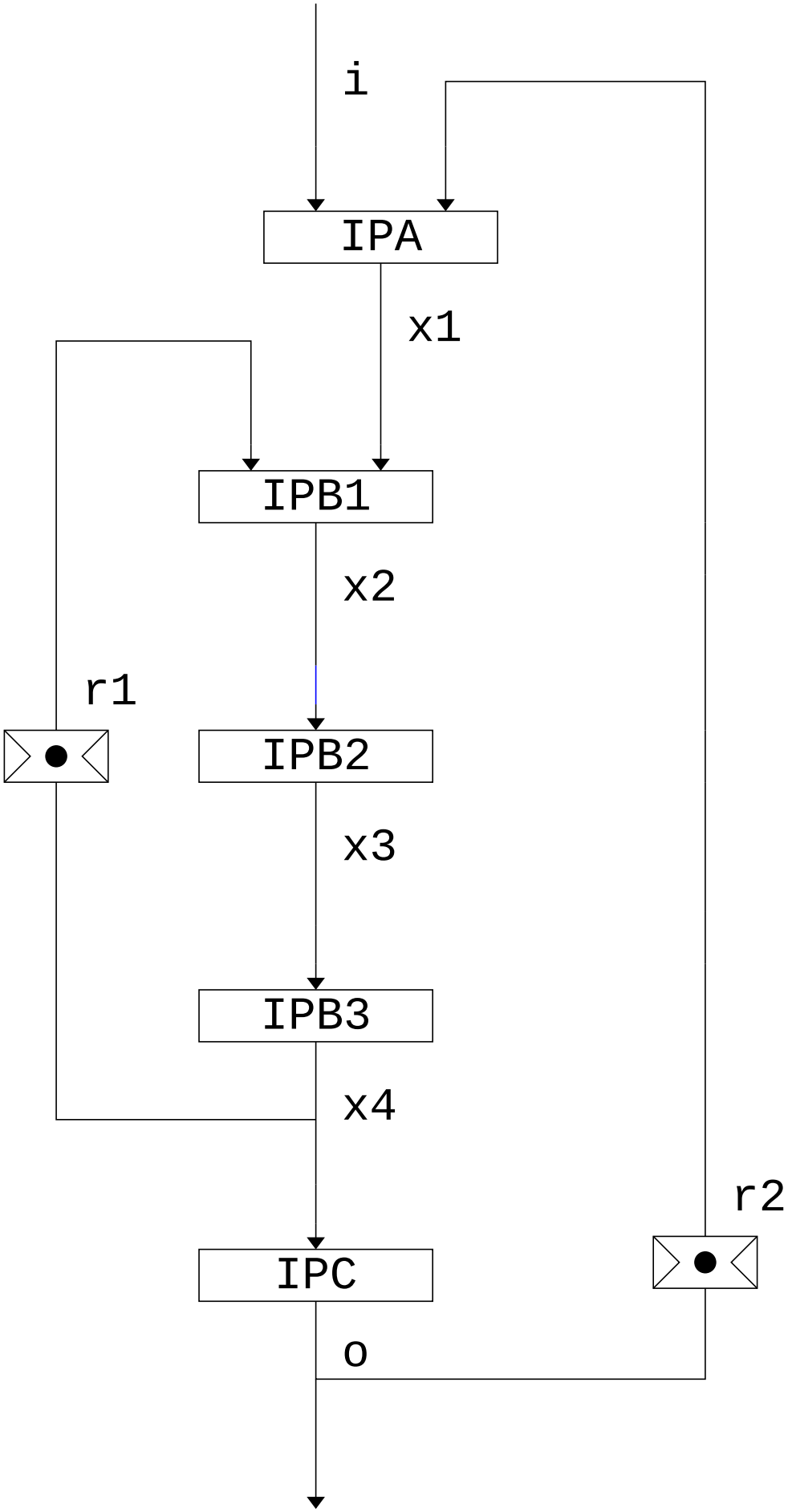
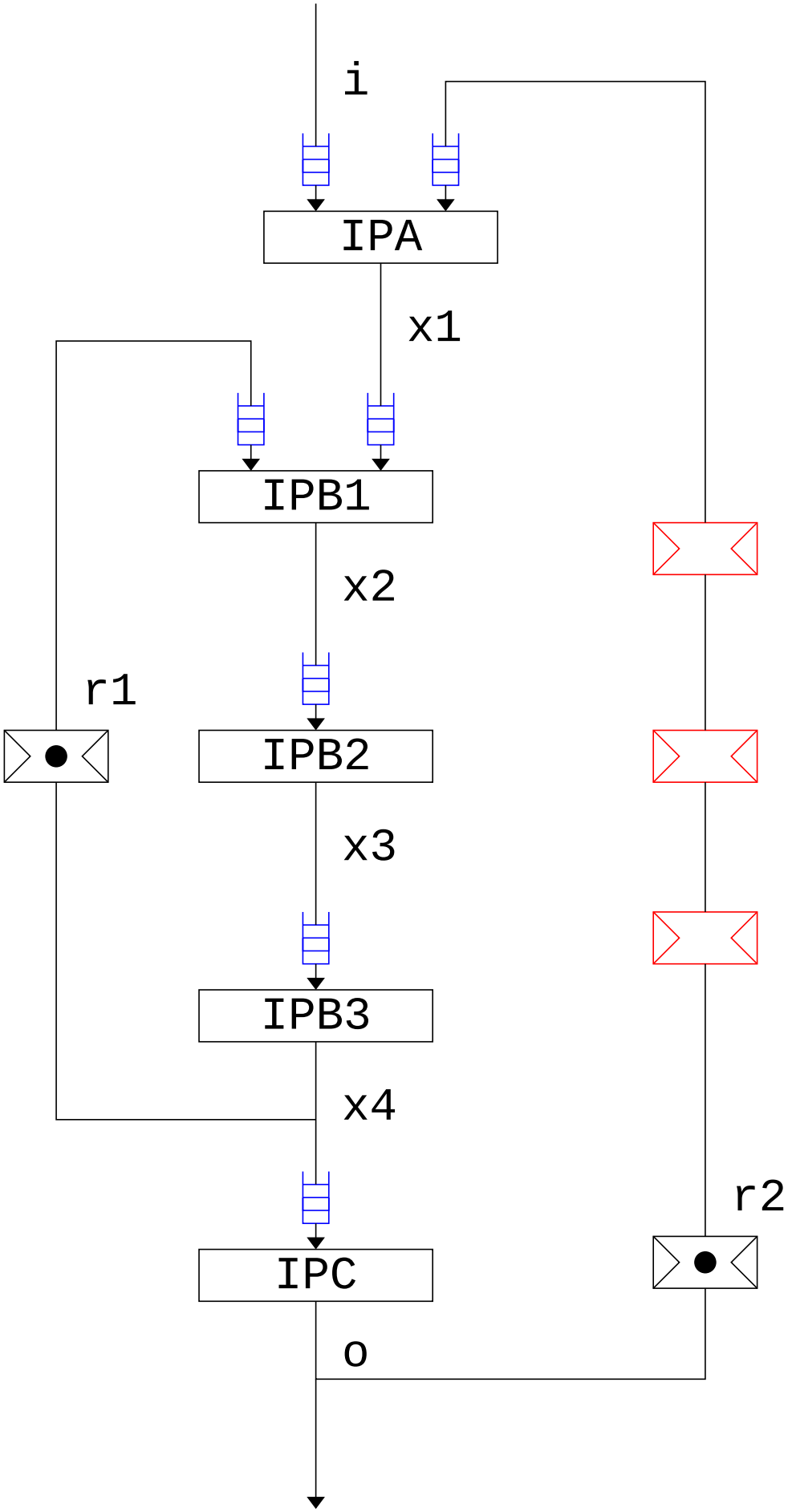


Figure 3 : Getting Schedules and Buffer Sizes from n-Synchronous Clock Typing



synchronous_circuit.ls



circuit_with_latencies.ls