ECRTS 2010
July 6-9, 2010
Brussels, Belgium

in conjunction with the
22nd Euromicro Intl Conference on Real-Time Systems
http://ecrts.eit.uni-kl.de/ecrts10

10th INT'L WORKSHOP ON WORST-CASE EXECUTION TIME ANALYSIS

Brussels, Belgium, July 6, 2010 http://www.artist-embedded.org/artist/WCET-2010.html

Important dates

Submission deadline (EXTENDED):	April 20
Notification of acceptance:	May 14
Final version of papers due:	June 10
WCET Workshop:	July 6
Euromicro Conf. on RTS:	July 7-9

Workshop chair

Björn Lisper *Mälardalen University, Sweden*

Program committee

Antoine Colin	*Rapita Systems Ltd., UK*
Amine Marref	*Mälardalen University, Sweden*
Christine Rochange	*IRIT, University of Toulouse, France*
Isabelle Puaut	*University of Rennes I / IRISA, France*
Niklas Holsti	*Tidorum Ltd, Finland*
Stefan Petters	*Polytechnic Institute of Porto, Portugal*
Heiko Falk	*Technische Universität Dortmund, Germany*
Chris Healy	*Furman University, USA*
Raimund Kirner	*Vienna University of Technology, Austria*
Daniel Grund	*Saarland University, Germany*
Abhik Roychoudhury	*National University of Singapore, Singapore*
Daniel Kästner	*AbsInt GmbH, Germany*

Steering committee

Guillem Bernat	*Rapita Systems Ltd., UK*
Jan Gustafsson	*Mälardalen University, Sweden*
Peter Puschner	*Vienna University of Technology, Austria*

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SEVENTH FRAMEWORK PROGRAMME

http://www.artist-embedded.org/artist/

Goals

The goal of the workshop is to bring together people from academia, tool vendors and users in industry who are interested in all aspects of timing analysis for real-time systems. The workshop fosters a highly interactive format with ample time for in-depth discussions. It provides a relaxed forum to present and discuss new ideas, new research directions, and to review current trends in this area. The presentations will be kept short to leave plenty of time for interaction of attendees.

Topics

The topics of the workshop include any issue related to timing analysis, in particular:

- Different approaches to WCET computation
- Flow analysis for WCET, loop bounds, feasible paths
- Low-level timing analysis, modeling and analysis of processor features
- Strategies to reduce the complexity of WCET analysis
- Integration of WCET and schedulability analysis
- Methods and benchmarks for WCET analysis evaluation
- Case studies, and industrial experience of WCET analysis
- Measurement-based WCET analysis
- Tools for WCET analysis
- Program and processor design for timing predictability
- Integration of WCET analysis in development processes
- Compiler optimizations for worst-case paths
- WCET analysis for multi-threaded and multi-core systems
- WCET analysis in the academic curriculum

Statements which are innovative, controversial, or that present new approaches are specially sought.

Submission of papers

Papers for the workshop must be written in English, should not exceed 10 pages in the specified format, and should be submitted in PDF via the EasyChair system at https://www.easychair.org/login.cgi?conf=wcet2010. Formatting instructions and templates are given at the workshop website, http://www.artist-embedded.org/artist/WCET-2010.html. Submissions not adhering to the page limit, or formatting instructions, may be rejected without further reviewing. Authors of accepted papers shall prepare and submit a final version of their paper. The deadline for these final versions is June 10, 2010. The workshop proceedings with the final papers will be published by the Austrian Computer Society (OCG, http://www.ocg.at/) as OCG Schriftenreihe (with ISBN number).