MÄLARDALEN UNIVERSITY
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Towards WCET Analysis of Multi-core Architectures Using UPPAAL

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Outline

- Motivation and Contribution
- Timed Automata and UPPAAL
- WCET analysis using UPPAAL
- Example WCET estimation
- Future work

Motivation

- Parallel software

```
thread1                thread2
{                      {

    ...                    ...

    wait for               tell thread1
      thread2                I'm here

    ...                    ...

}                      }
```

Motivation

- Parallel software
- Parallel hardware

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- Parallel software
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thread1                 thread2
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What is the WCET???

Motivation

- Parallel software
- Parallel hardware

```
thread1                 thread2
{                       {
    ...                     ...
    wait for                tell thread1
      thread2                 I'm here
    ...                     ...
}                       }
```

What is the WCET???

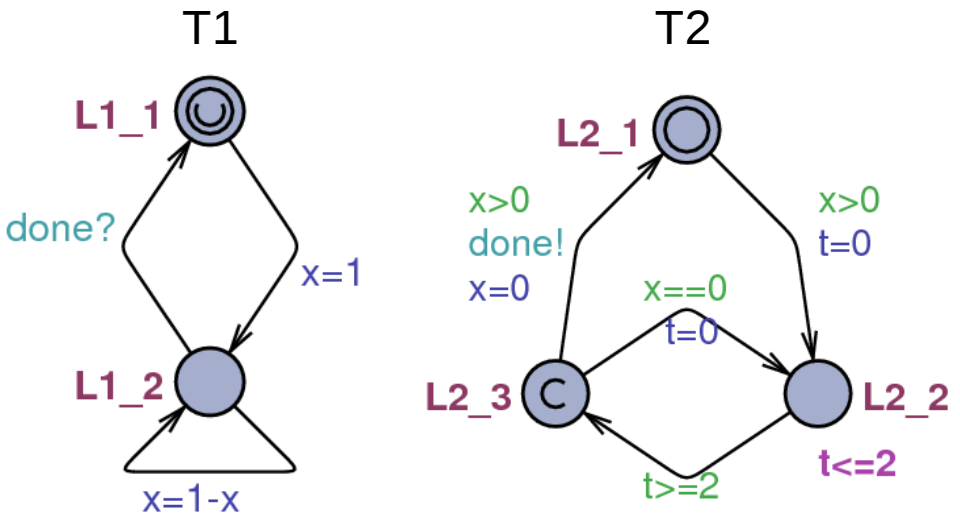
- Need new methods for WCET analysis

Contribution

- Parallel software
  - Threaded program
  - Mutual exclusion/Synchronization (spinlock)
- Parallel hardware
  - Shared Memory Multicore
- WCET analysis method: Model-checking of Timed Automata

Timed Automata in UPPAAL

- Parallel system
  - Synchronization
  - Variables
- Time is included in the formalism
- Analysis Tool
  - Query language



A[] x==1 imply T1.L1_2

E<> deadlock

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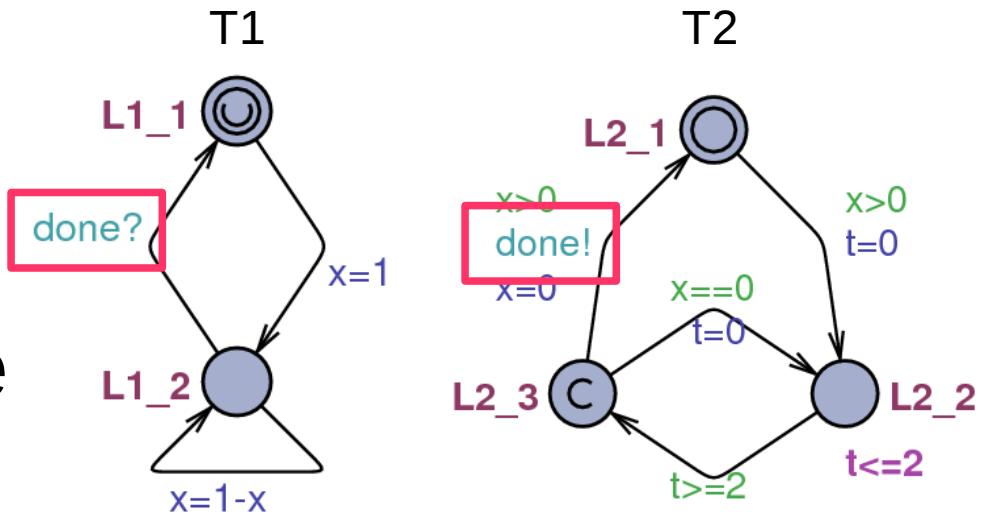

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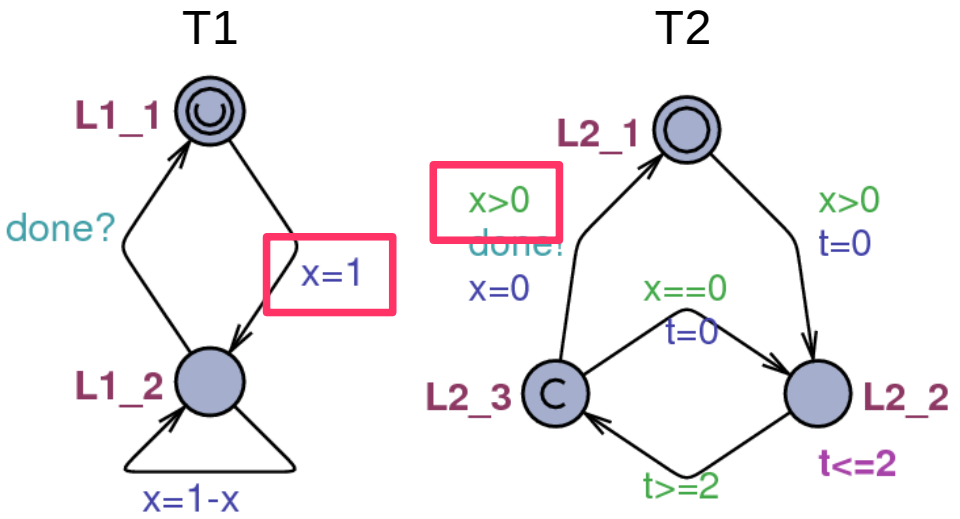


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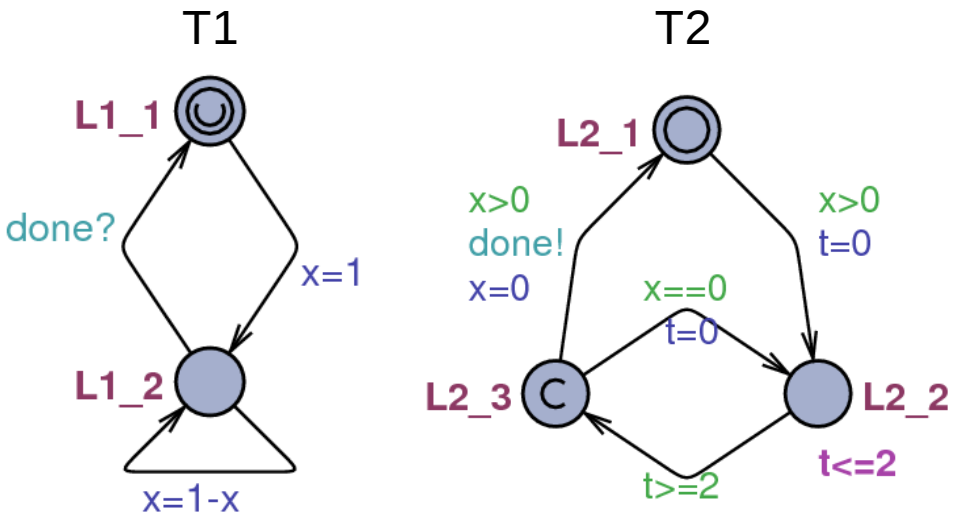

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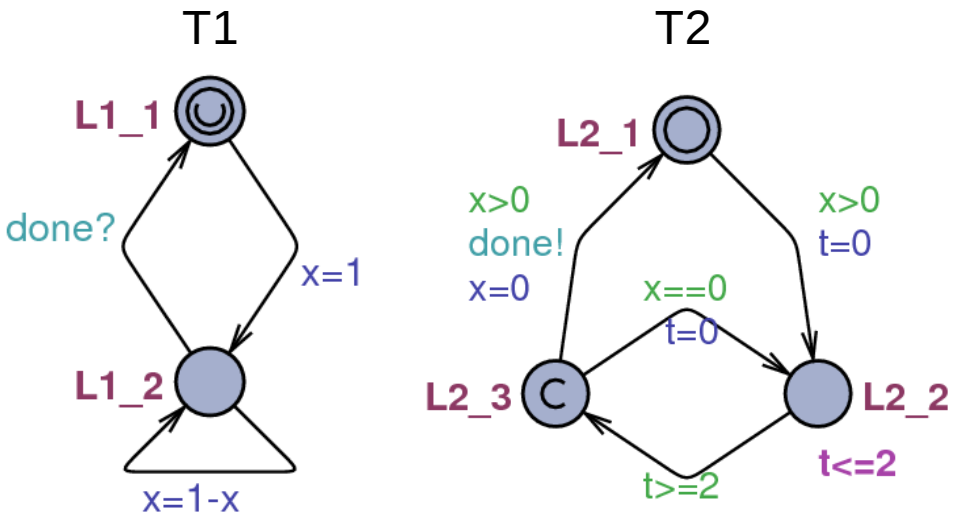


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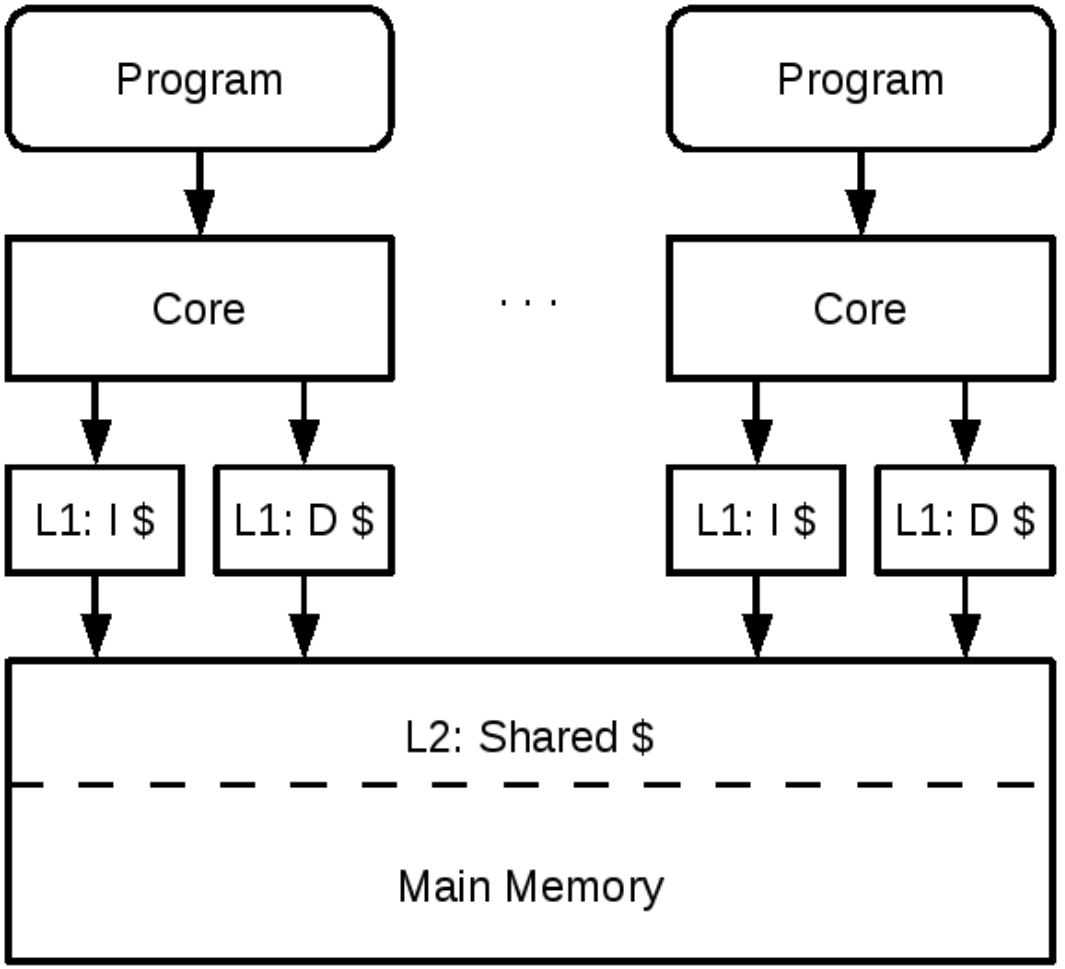
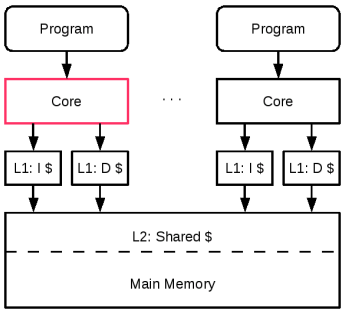
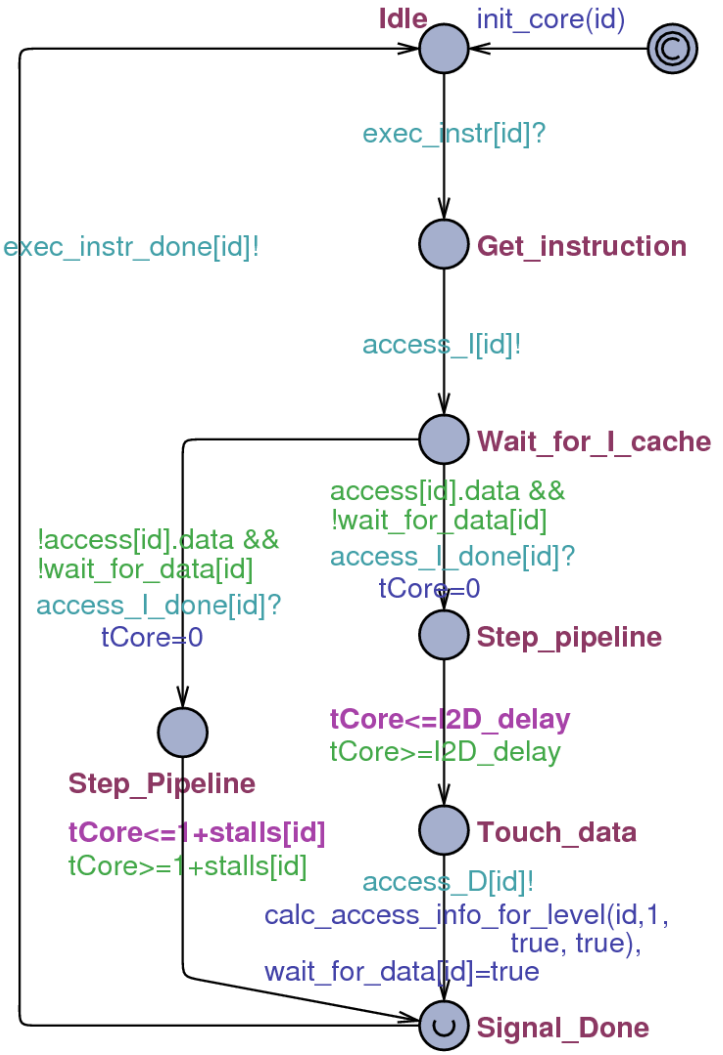
The Modeled System



The Core

- In-order execution
- The core can overlap instruction execution and data accessing





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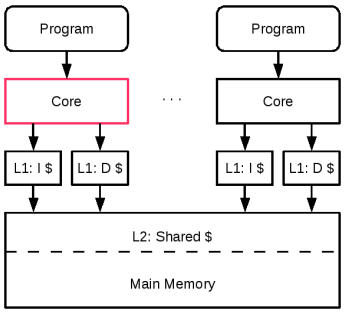

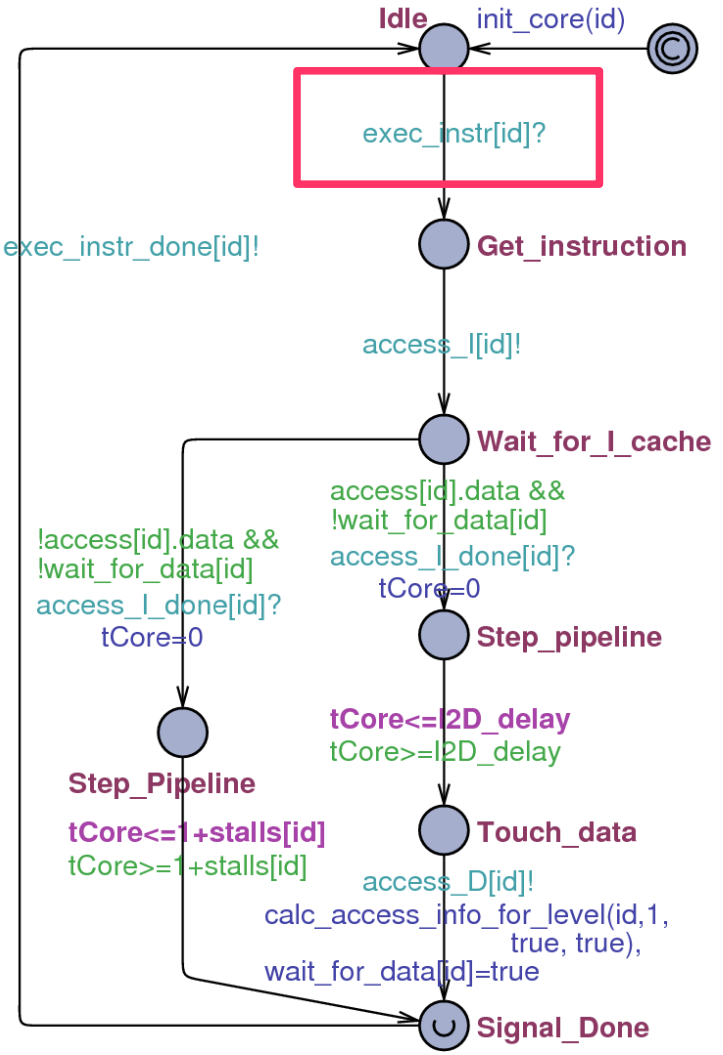

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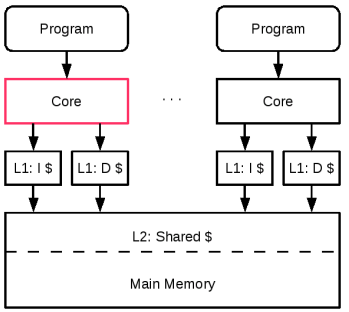
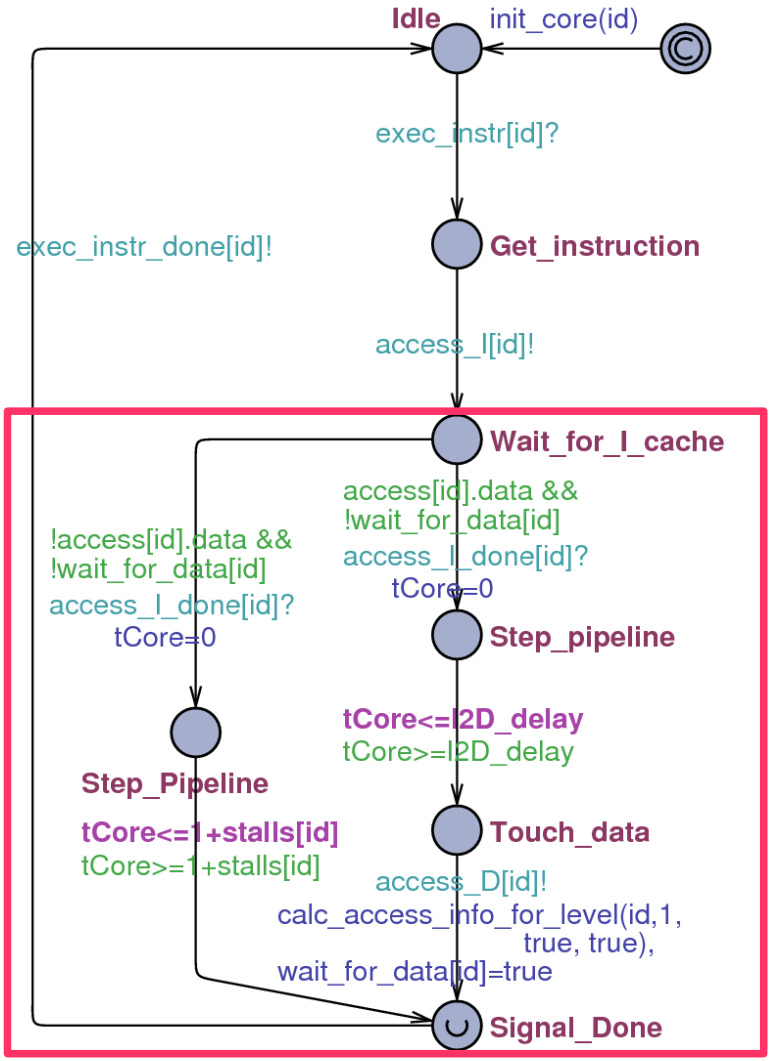
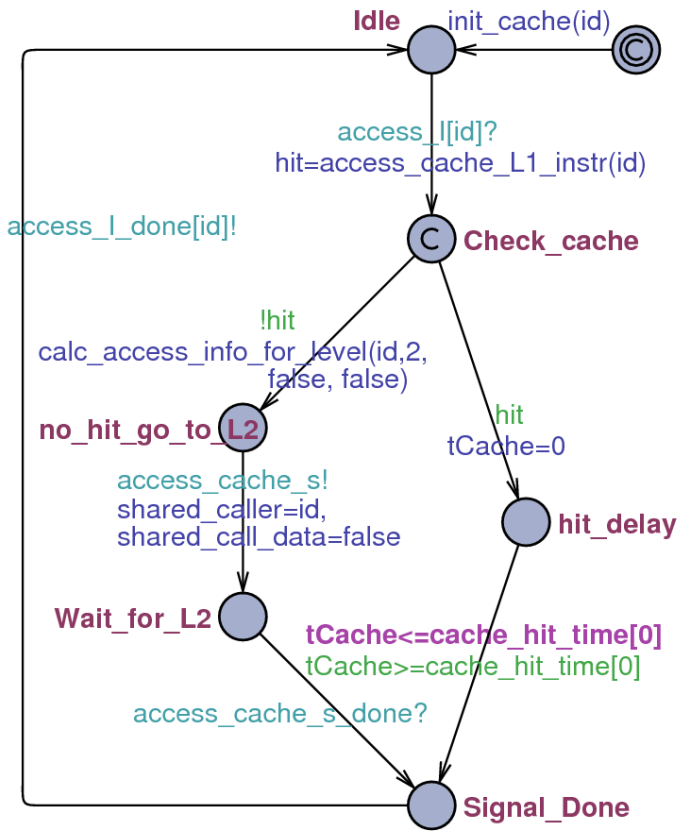
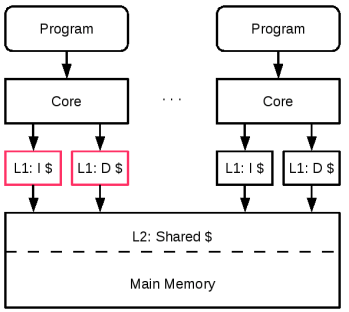
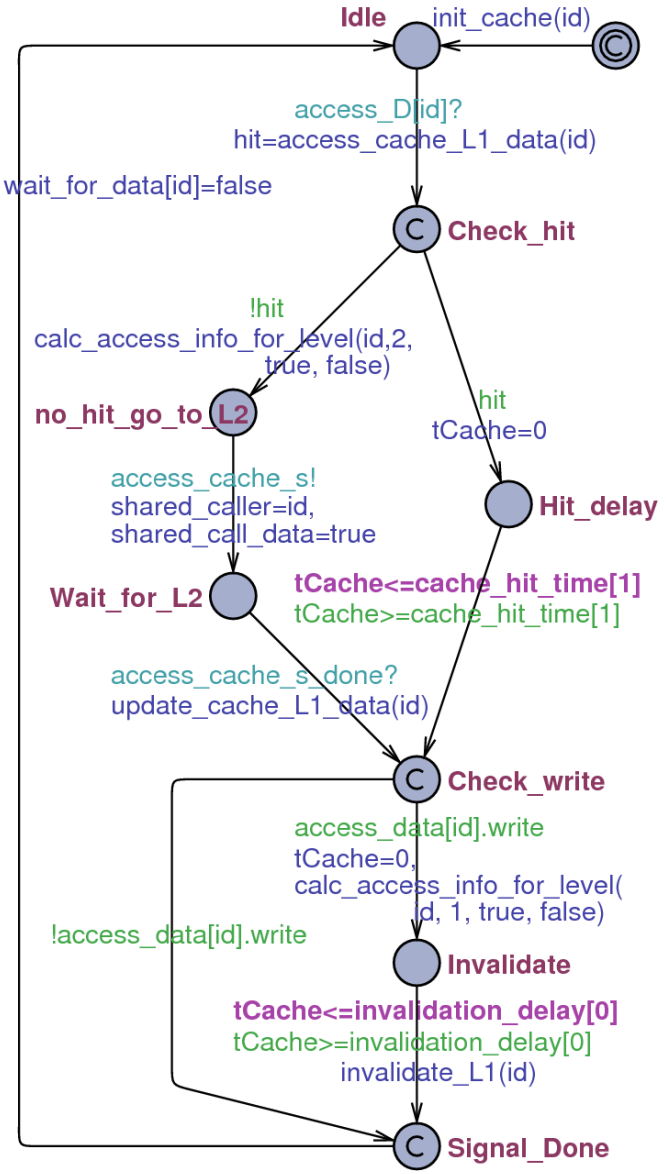




The L1 Caches







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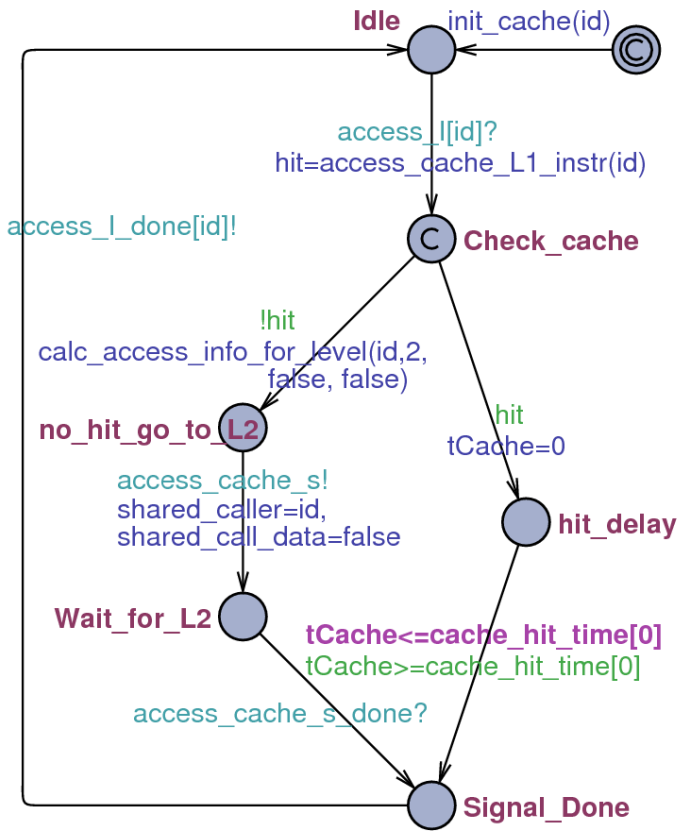

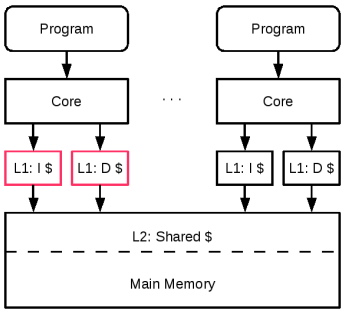

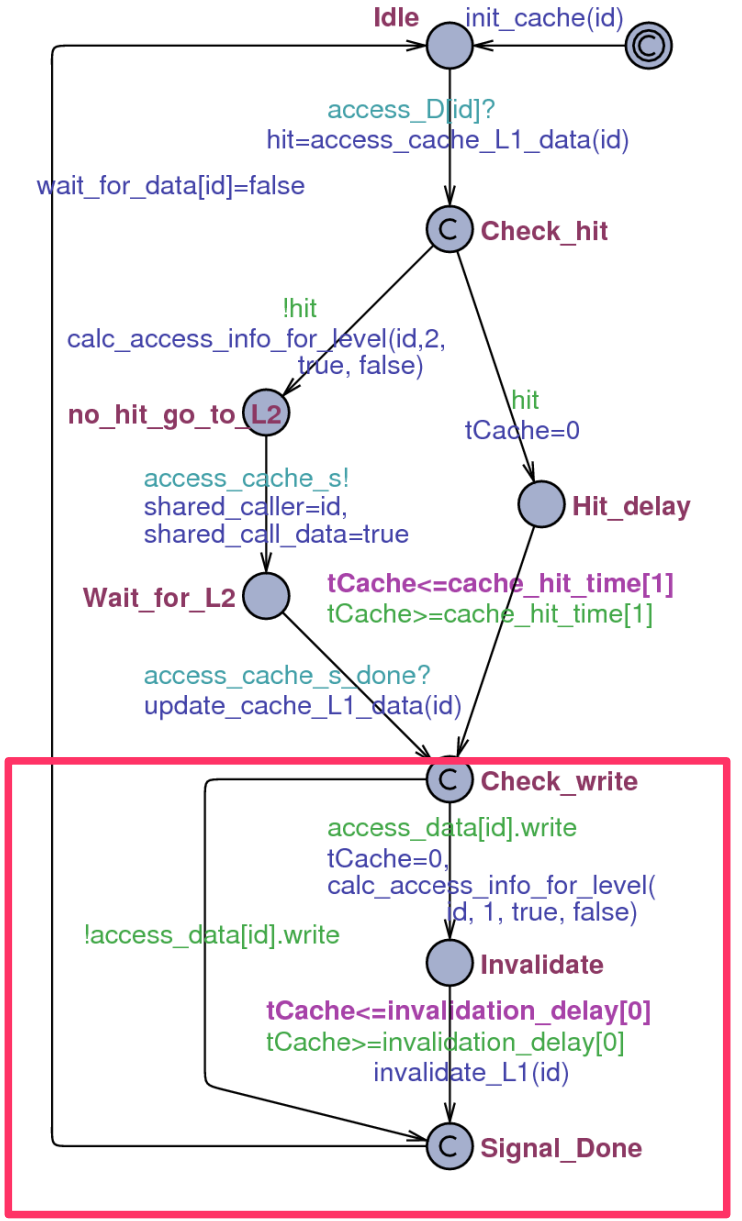

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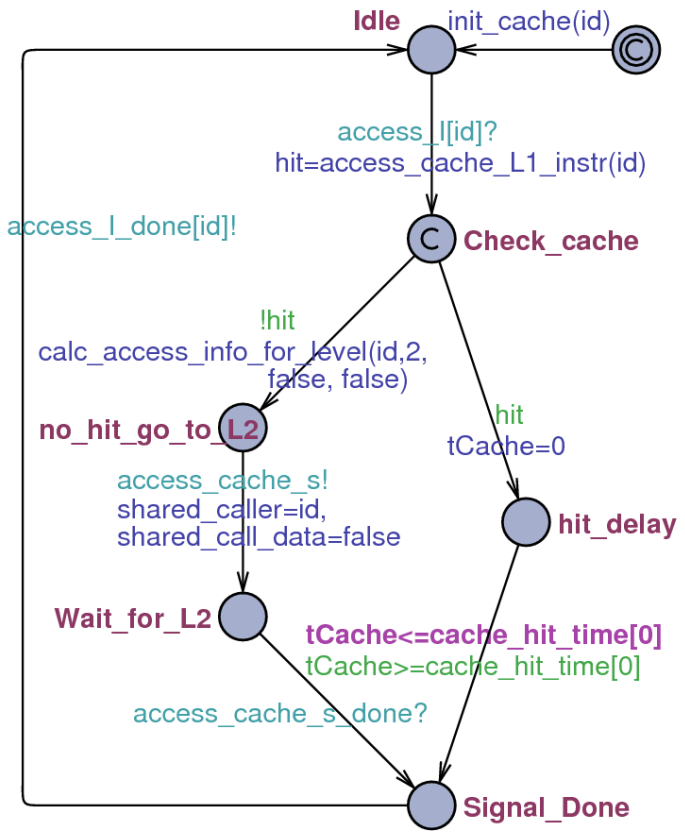
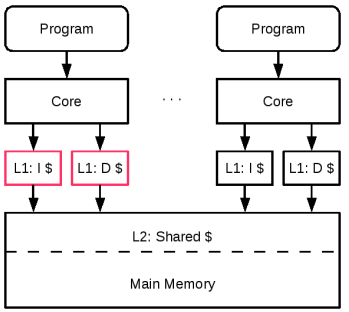
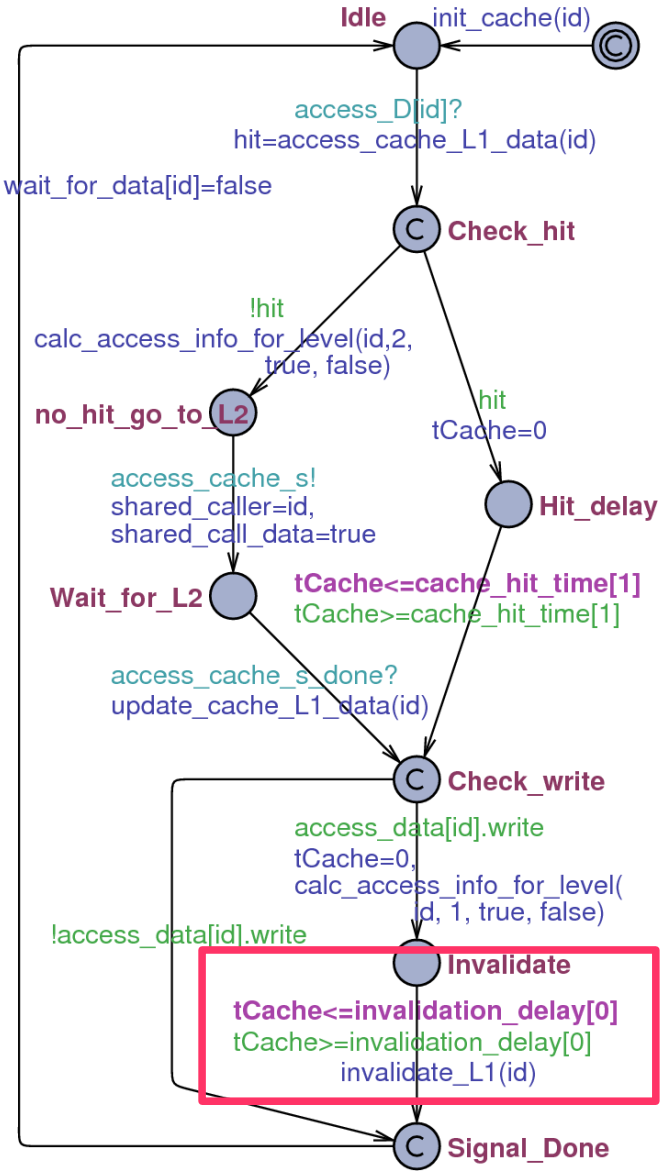
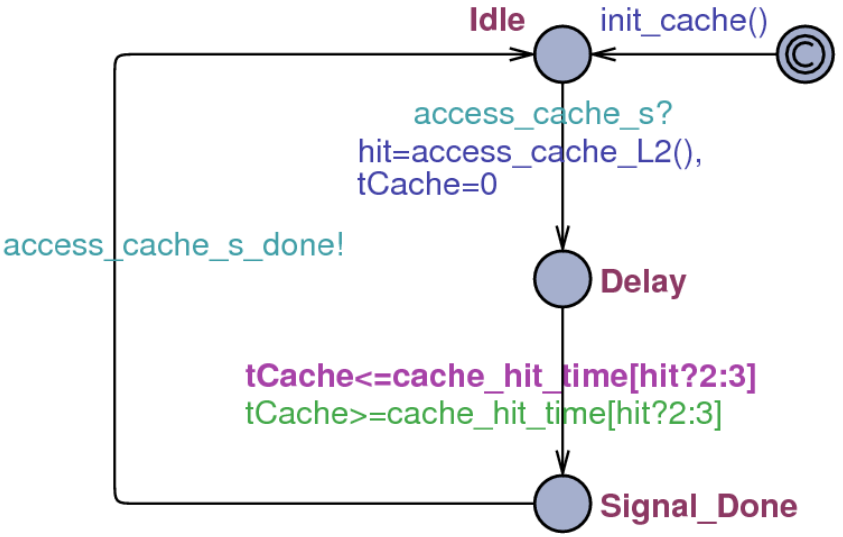


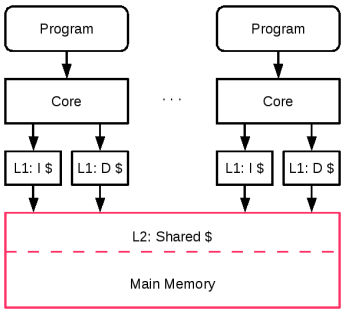




The L2 Cache

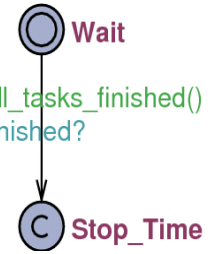
- L1 caches compete for access to the L2 cache
- Main memory is assumed to always hit

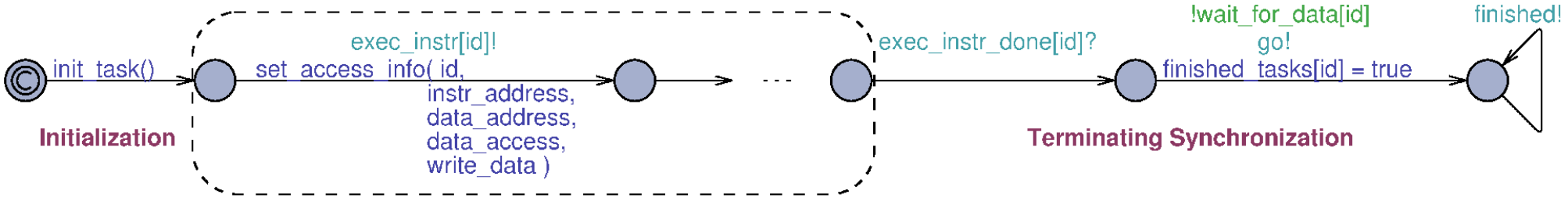


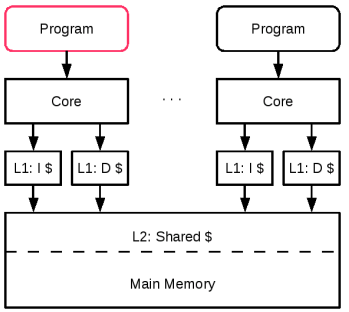


Program Model Interface

- When all programs/threads have finished, the time is stopped







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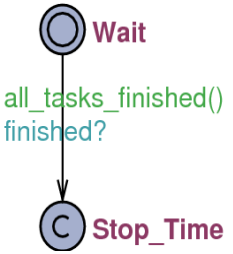

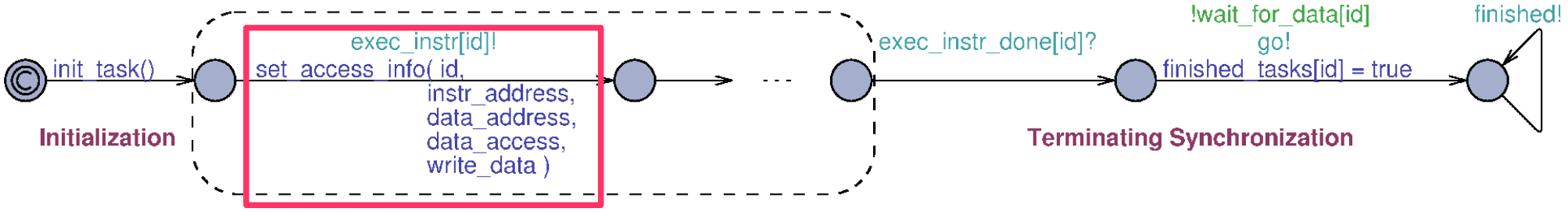

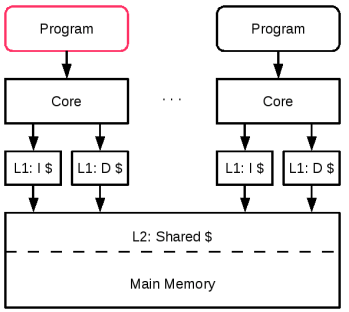

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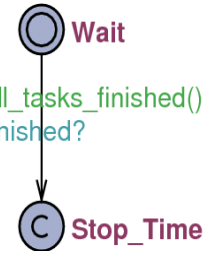

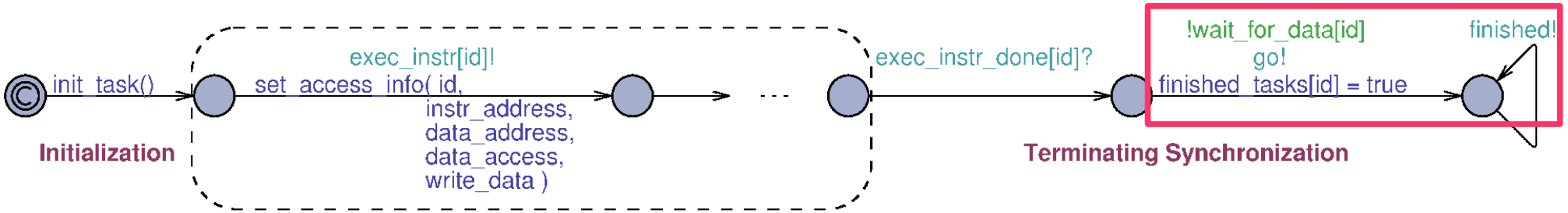

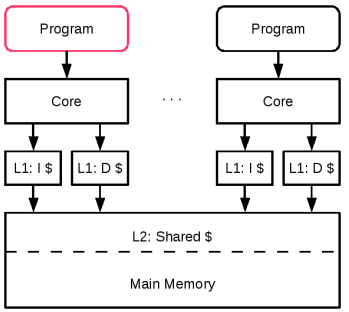

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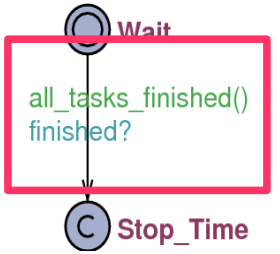

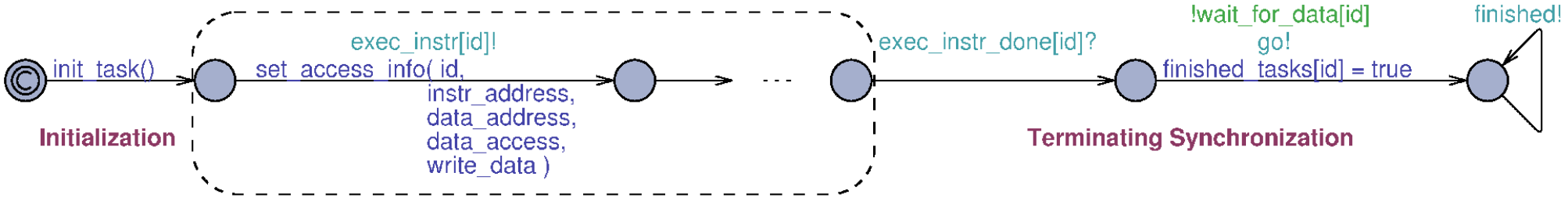

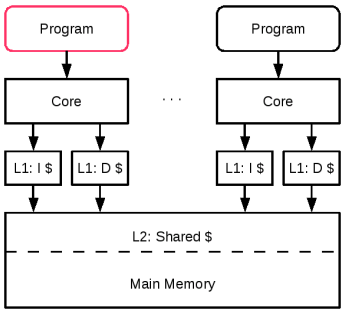

Finding the WCET

- Binary search
  - `A[] t <= estimate`

Finding the WCET

- Binary search
  - `A[] t <= estimate`
- The `sup`-operator
  - `sup: t`

Experimental Evaluation

	L1 instr.	L1 data	L2 (shared)	RAM
Lines	4	4	8	∞
Words/Line	2	2	4	-
Sets	2	4	2	-
Latency	1	1	10	80
Replacement pol.	LRU	LRU	LRU	-

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thread_body() {
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    shared_var = 0;
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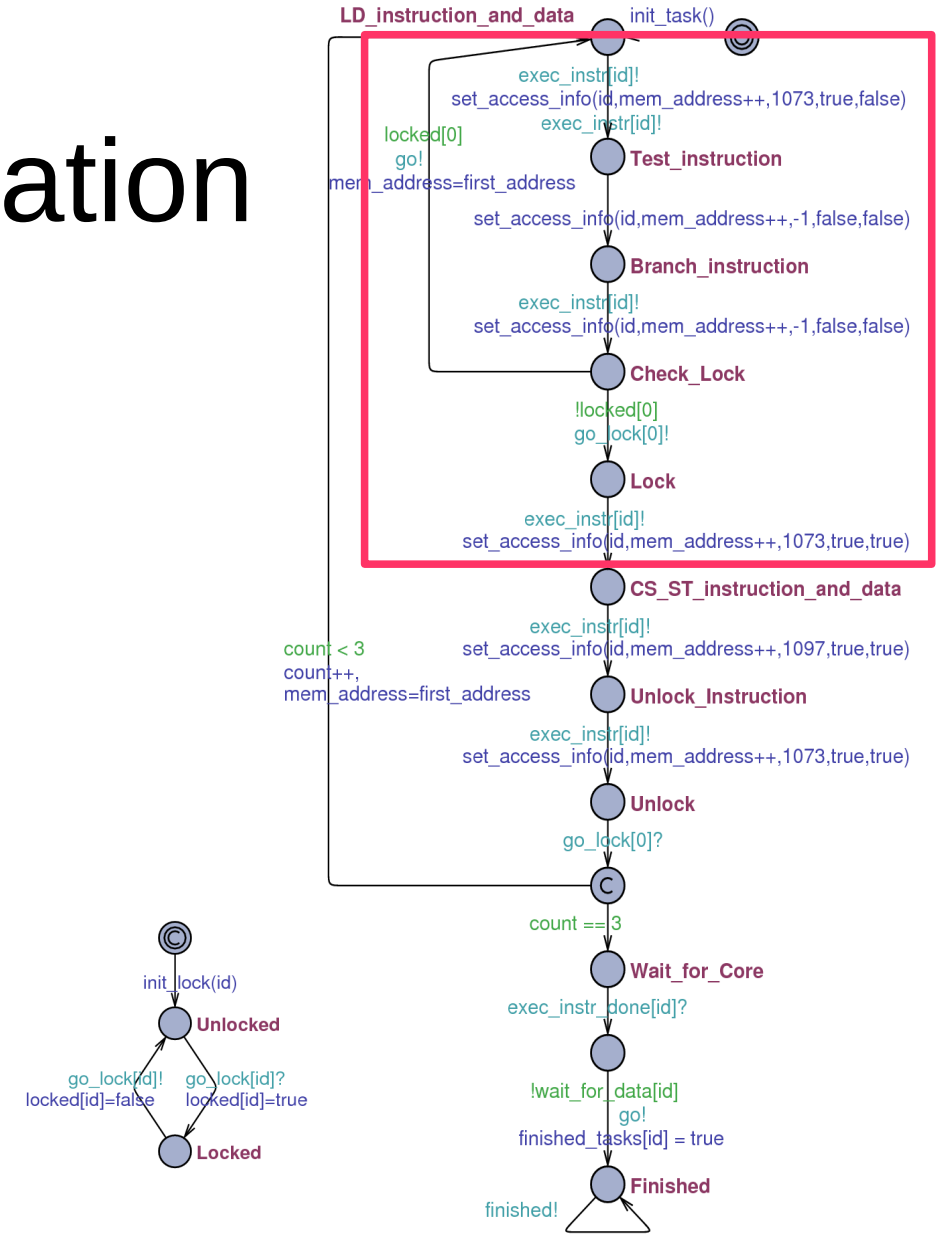

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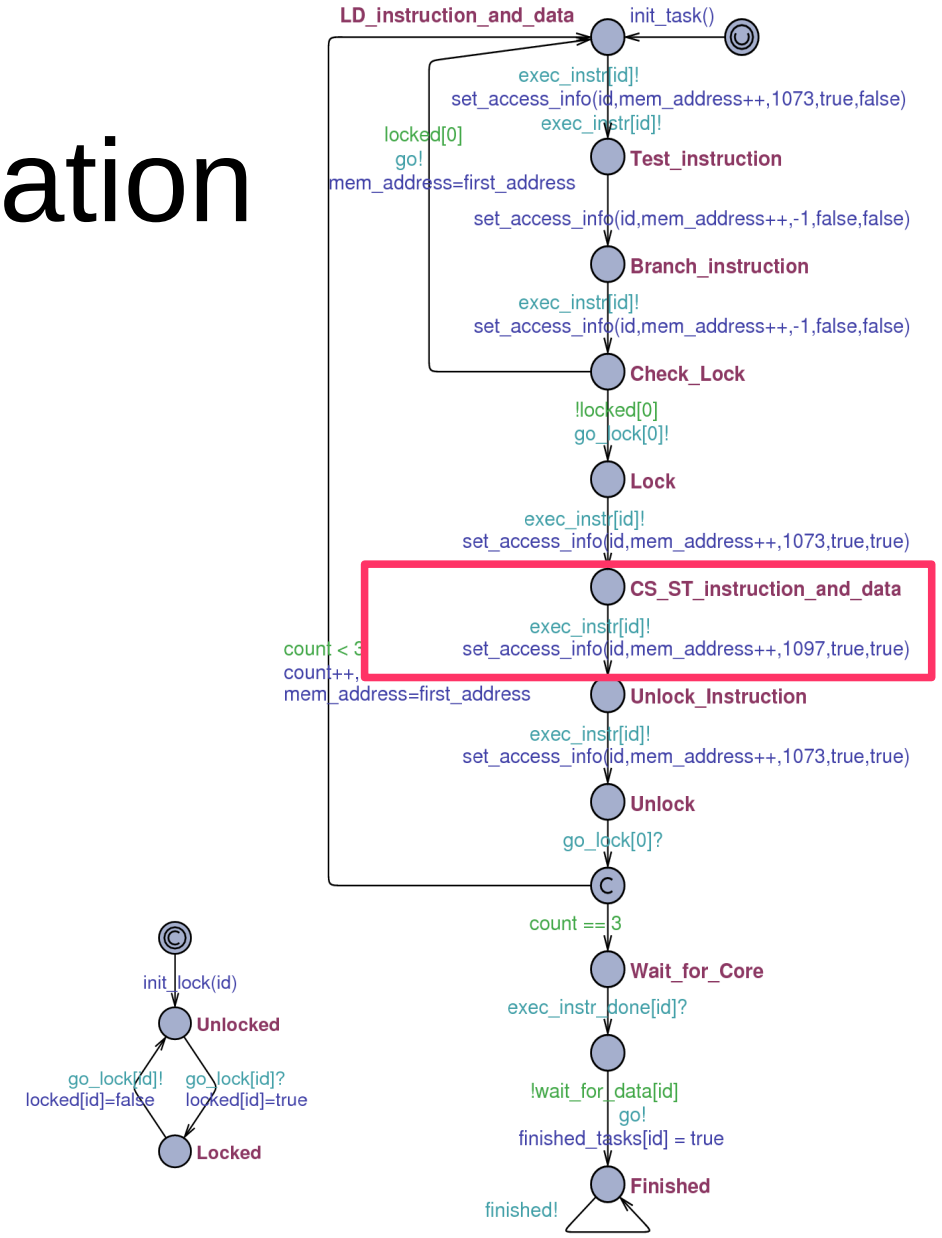

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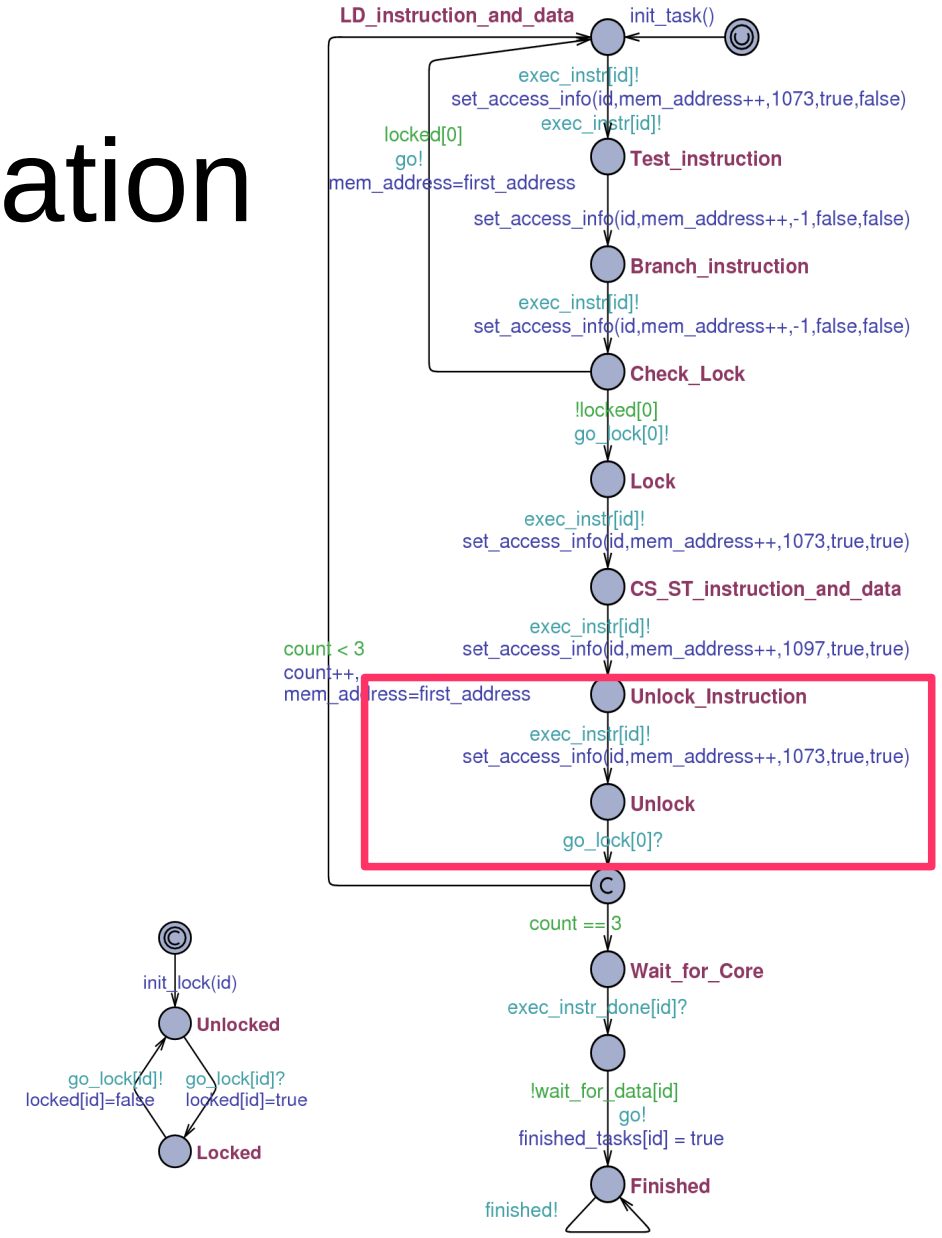

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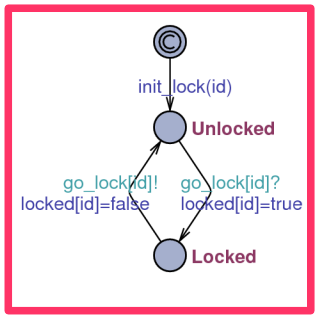

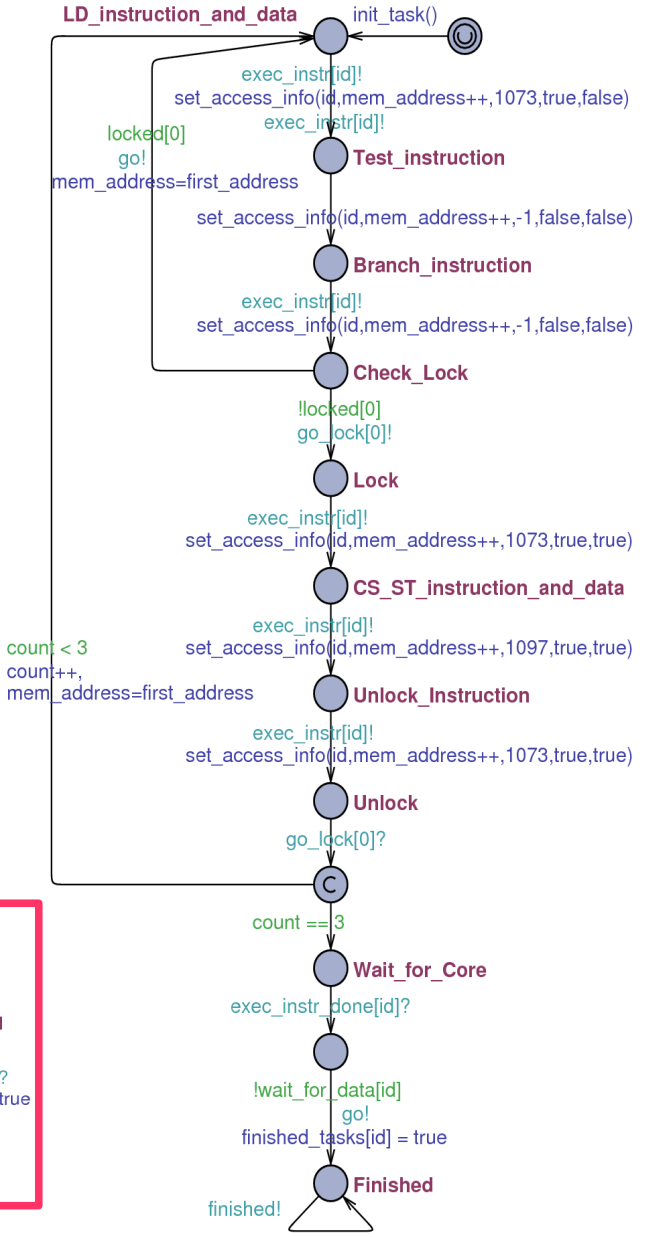

Experimental Evaluation

WCET = 636

- Base case:
  - 2 cores with corresponding caches
  - 1 thread of the program on each core
- Analysis Time:

	Binary Search	`sup`-Operator
1 step	1s	1s
Total	11s	1s

Experimental Evaluation

WCET = ???

- Scalability Test 1
  - 4 cores with corresponding caches
  - 1 thread of the program on each core
- Analysis Time:

	Binary Search	`sup`-Operator
1 step	>3h	>3h
Total	?	>3h

Experimental Evaluation

WCET = 1207

- Scalability Test 2
  - 2 cores and caches, 1 thread on each core
  - Thread 2 is released in the interval [0,1000]
- Analysis Time:

	Binary Search	`sup`-Operator
1 step	44s	42s
Total	~500s	42s

Experimental Evaluation

WCET = 619

- Scalability Test 3
  - 2 cores and caches, 1 thread on each core
  - # of cache lines are 2048 (L1-I,L1-D) and 8192 (L2)
- Analysis Time:

	Binary Search	`sup`-Operator
1 step	14s	14s
Total	~150s	14s

The Future...

- Scalability problem
  - Reduce complexity in models of HW and SW
  - Symmetry reduction
  - Partial order reduction
- Integration with SWEET
- Alternative approach
  - Model-checking as static analysis subroutine

Thank you! Questions?

- Andreas Gustavsson:
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