214373 ArtistDesign
Network of Excellence
on Embedded Systems Design

Project Management Report for Year 3

Executive Summary

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Bruno Bouyssounouse – ArtistDesign Technical Coordinator

ArtistDesign Consortium

1. Project Objectives

The ArtistDesign NoE is the visible result of the ongoing integration of a community.

The central objective for ArtistDesign is to build on existing structures and links forged in the ARTIST2 NoE, to become a virtual Centre of Excellence in Embedded Systems Design. This is achieved through tight integration between the central players of the European research community. These teams have already established a long-term vision for embedded systems in Europe, which advances the emergence of Embedded Systems as a mature discipline.

ArtistDesign is becoming the main focal point for dissemination in Embedded Systems Design, leveraging on well-established infrastructure and links. It will extend its dissemination activities, including Education and Training, Industrial Applications, as well as International Collaboration. ArtistDesign will establish durable relationships with industry and SMEs in the area.

ArtistDesign builds on existing international visibility and recognition, to play a leading role in structuring the area.

The research effort integrates topics, teams, and competencies, grouped into 4 Thematic Clusters: “Modelling and Validation”, “Software Synthesis, Code Generation, and Timing Analysis”, “Operating Systems and Networks”, “Platforms and MPSoC”. “Transversal Integration” covering both industrial applications and design issues aims for integration between clusters.

-- Changes wrt Y2 deliverable –

No changes with respect to Year 2.

2. Contact Details and Contractors Involved

2.1 Core Partners

For a complete description including web links, see:
http://www.artist-embedded.org/artist/-ArtistDesign-Participants-.html

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3	RWTH AACHEN	AACHEN	Germany
4	AALBORG UNIVERSITET	AALBORG	Denmark
6	ALMA MATER STUDORIUM - UNIVERSITA DI BOLOGNA	BOLOGNA	Italy
7	TECHNISCHE UNIVERSITAET BRAUNSCHWEIG	TUBS	Germany
8	UNIVERSIDAD DE CANTABRIA	CANTABRIA	Spain
9	COMMISSARIAT À L'ENERGIE ATOMIQUE	CEA	France
10	DANMARKS TEKNISKE UNIVERSITET	DTU	Denmark
11	UNIVERSITAET DORTMUND	DORTMUND	Germany
12	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	EPFL	Switzerland
13	EMBEDDED SYSTEMS INSTITUTE	ESI	Netherlands
14	ETH ZUERICH	ETH Zurich	Switzerland
15	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM	IMEC	Belgium
16	INSTITUT NAT. DE RECH. EN INFORMATIQUE & AUTOM.	INRIA	France
17	TECHNISCHE UNIVERSITAET KAISERSLAUTERN	TUKL	Germany
18	KUNGLIGA TEKNIKA HOGSKOLAN	KTH	Sweden
19	LINKÖPINGS UNIVERSITET	LINKOPING	Sweden
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25	SCUOLA SUPERIORE SANT'ANNA	SSSA-PISA	Italy
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27	UNIVERSITAET DES SAARLANDES	SAARLAND	Germany
28	UNIVERSITAET SALZBURG	PLU-SALZBURG	Austria
29	UPPSALA UNIVERSITET	UPPSALA	Sweden
30	TECHNISCHE UNIVERSITAET WIEN	VIENNA	Austria
31	UNIVERSITY OF YORK	YORK	UK
32	IST Austria	IST_Austria	Austria
33	University of Porto	UnivPorto	Portugal
34	University of Trento	Trento	Italy

-- Changes wrt Y2 deliverable –
No changes with respect to Year 2.

2.2 Affiliated Partners

Affiliated partners play a very strong role in the Spreading Excellence from the core partners to the research and industrial communities at large.

Affiliated partners generally play an active role in the research activities, either participating directly in research, or transferring the results directly to industry.

Each of the JPRA and JPIA activities' deliverables provides the list of the corresponding affiliated partners and roles.

Affiliated Industrial Partners

The complete set of Affiliated Industrial partners, including web links, is available online, here: http://www.artist-embedded.org/artist/-Affiliated-Industrial-Partners-.html

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3. Vision and Assessment of the Work Performed

ArtistDesign finances durable integration between teams and not the concrete elements of the JPA which most often belong to other projects. These specific technical objectives may or may not be attained (this is the essence of research as opposed to development), but we feel that the main product of ArtistDesign is the emergence of a lasting European research community, that has a significantly enhanced capacity for preparing Europe's future.

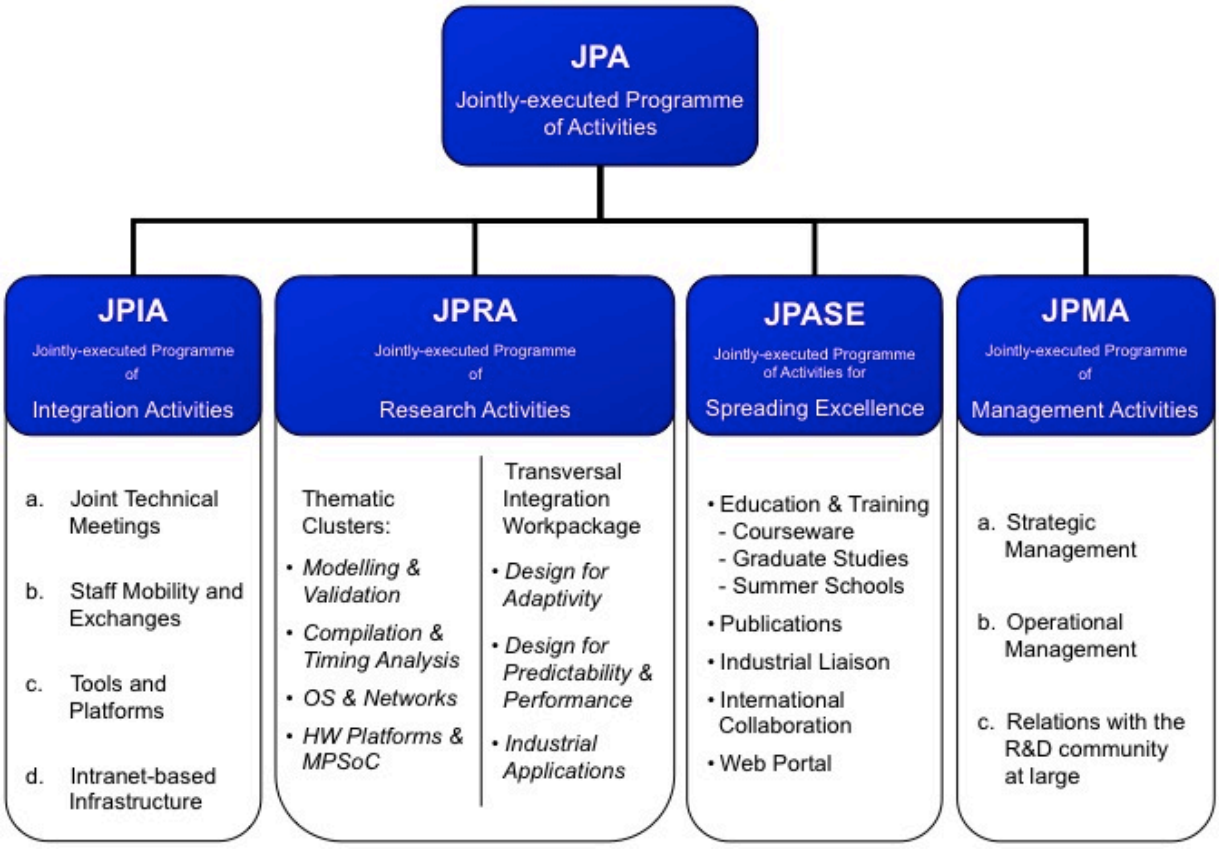
The research is completed by work in the JPIA (Jointly Executed Programme of Integration Activities) workpackage, which aims to transform research results in tangible tools and components, and bring teams closer together on a day to day basis.

We believe that the topics chosen provide a good coverage of the area, for embedded software and systems.

The ArtistDesign NoE is a complex construction assembled from world-leading communities, teams, and individuals. This is certainly an asset, but also a source of complexity in management. Each team has two essential characteristics: world-class excellence and strong interaction with top industrial players. ArtistDesign partners play a leading role in the different communities in embedded systems design, and they advance the state of the art in each of these.

It is difficult to abstract out a global synthesis of the overall technical achievements. This is due to the diversity and the low granularity of the actions to be covered (meetings, publications, attendance at workshops, visits, and platforms).

The following is a certainly non-exhaustive assessment of the work in the Joint Programme of Activities' 4 main branches.



No changes with respect to Year 2.

3.1 Joint Programme of Research Activities (JPRA)

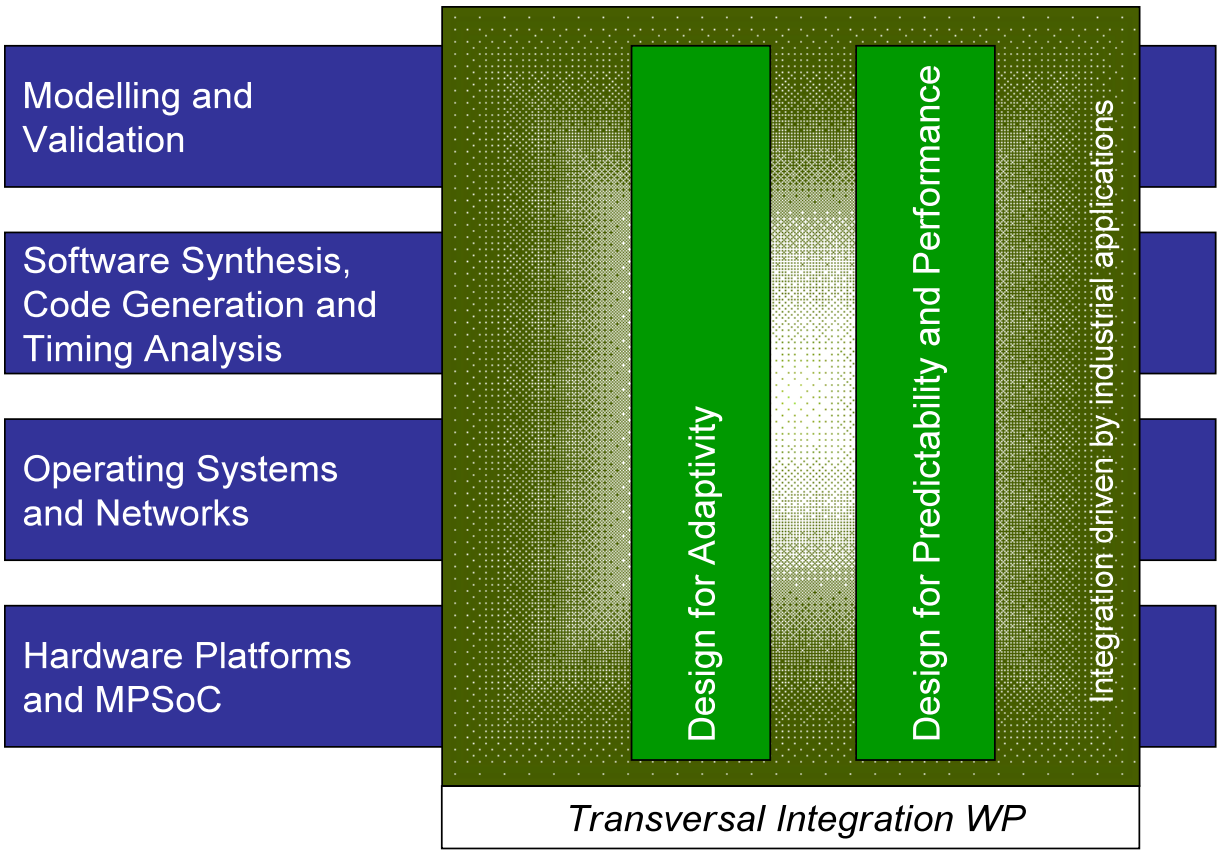
3.1.1 Structure of the Research Effort

The JPRA is composed of intra and inter-cluster research activities on cutting-edge topics in embedded systems design. While the main bulk of financing for these activities is taken up by outside programmes (Integrated Projects, National Programmes, Industrial Contracts, etc), the ArtistDesign NoE finances the extra effort derived from integrating these into a single coherent research programme.

Thus, the essential ingredient within ArtistDesign is the JPRA, which motivates the participating research teams far more than the actual financing, which is tiny in comparison with the overall research aims. It is completed by the Joint Programme of Integrating Activities (JPIA), and the Joint Programme of Activities for Spreading Excellence (JPASE), and overseen by the Joint Programme of Management Activities (JPMA).

The structure of the research activities reflects the following decomposition of the embedded systems design flow.

This design flow is composed of the following cooperating activities, starting with component-based modelling and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality. Accordingly, we have structured the area of embedded systems design into the following topics.



Modelling and Validation. Unlike other computer systems, embedded systems are strongly connected with a physical environment. A scientific foundation for embedded systems must therefore deal simultaneously with software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based. The overall objective of this activity is to develop model and component-based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. The activity brings together the most important teams in the area of model and component based design in Europe.

SW Synthesis, Code Generation and Timing Analysis. There is a continuing demand for higher performance of information processing, which stimulates using a growing amount of parallelism (including using multiple processors). This trend affects the design of embedded systems. We address issues related to multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces. Such processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Timing analysis is also affected by the trend toward the new platforms. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Also, timing analysis beyond the single processor is required. Hence, timing analysis will also consider the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors.

Operating Systems and Networks. We investigate how current real-time operating systems have to be extended or modified to support emerging real-time embedded systems characterized by a high degree of complexity, highly variable resource requirements and parallel processing such as multicores. Most embedded systems are often characterized by scarce resources in terms of processing power, memory, space, weight, energy, and cost. Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, whilst guaranteeing isolation properties. Also, to support dynamic applications with variable resource requirements or to cope with unpredictable resource availability, feedback control techniques for resource management at the operating system and application level are also investigated.

Hardware Platforms and MPSoC Design. While hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application environments is much less clear. The consequence is fragmentation: while many research teams are working on one or more of these domains, there is little communication and integration, this leads to duplication of results and overall slow progress. The teams involved in this activity have a wide-ranging research experience which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ArtistDesign will help the participants to the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion.

Design for Adaptivity. An embedded hardware-software system is adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is a cross-cutting system characteristic that affects both hardware and software. At the software-level adaptivity is mainly concerned with flexible and adaptive resource scheduling, e.g., CPU time scheduling. At the hardware-level adaptivity includes both adaptation of operation modes, e.g., supply voltage and clock frequency, processor instruction sets, and dynamic management of hardware resources, e.g., processing elements and memory.

Design for Predictability and Performance. Many applications have strict requirements on timing, and limited resources (memory, processing power, power consumption, etc.). All systems also have increasing demands on (average) performance, which has motivated the introduction of features such as caching, pipelining, and (now becoming very prominent) multiprocessor platforms. Almost all such efficiency-increasing features drastically increase variability and decrease analyzability of response-times, etc. and thus have a detrimental effect on predictability. Since the introduction of new architectural features is inevitable, it is important to: a) develop technology and design techniques for achieving predictability of systems built on modern platforms, and b) investigate the trade-offs between performance and predictability.

Integration Driven by Industrial Applications. To have a strong impact on industry and society at large, the results of the Thematic Clusters need to be harmonized in an overall design flow that can sustain the embedded design chain from conception of the product to its implementation. The design chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics). Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company.

-- Changes wrt Y2 deliverable –

No changes with respect to Year 2.

3.1.2 *Overview of the Year 3 Research Results*

-- Changes wrt Y2 deliverable –
The texts in this section are entirely new.

3.1.2.1 Modeling and Validation (Cluster)

Both research activities with the cluster – the *Modeling Activity* and the *Validation Activity* – have progressed substantially within the third year, and with significant synergy between proposed modeling formalisms and methods and validation techniques they support:

Within the sub-activity *Component Modeling* and *Compositional Validation* several partners have worked substantially and collaboratively on compositional design and verification methodologies for functional, timing and stochastic aspect. The results include

- Assume/guarantee reasoning, interface automata as well as modal transition systems for rich models.
- Theoretical foundations and coordination languages have been developed for heterogeneous systems.
- A framework for tool integration based on meta-models and model-transformations.

The work in the sub-activity *Resource Modeling (*of the *Modeling Activity)* includes:

- design space exploration,
- multi-core scheduling,
- modelling paradigms for quantitative resources
- platform models including transactional memory.

The work in the sub-activity *Quantitative Modeling (*of the *Modeling Activity)* has produced significant results on:

- design frameworks for quantitative modeling, in particular weighted automata, priced timed automata and quantitative communication models.
- synthesis of models guaranteeing quantitative properties.

Within the sub-activity *Quantitative Validation* substantial work has been made on improved schedulability analyses supporting multiprocessor and multi-core applications. The work:

- takes into account scheduler overhead for power-awareness – i.e. exploiting slacks in the system of processes to reduce power consumption while insuring deadlines are met.
- combines abstract interpretation and model-checking for timing and interference analysis of parallel programs on multi-core,
- has been applied for schedulability analysis of Safety Critical Java applications.

Within the sub-activity *Cross-Layer Validation* substantial work has been made on improved methods for model-based testing including:

- incremental testing of composite systems,
- off-line test generation from timed automata models,
- model-based test generation for data-intensive systems, as well as runtime monitoring.

3.1.2.2 Software Synthesis, Code Generation and Timing Analysis (Cluster)

In year 3, we have seen a proliferation of the basic techniques studied by this cluster. The importance of using multi-processor systems has been growing even more than it did in year 2.

Several tools for mapping of applications to MPSoCs have become available (e.g. from RWTH Aachen, IMEC, Erlangen-Nuremberg and Seoul National University). We have reached a situation where such tools can be considered state of the art. We expect such tools to leave the research labs in the not too distant future.

Within the cluster, timing analysis and timing predictability for multicore platforms have seen substantial progress. The results include

- the worst-case execution time aware compiler WCC (Dortmund, AbsInt, USAAR)
- cache-aware scheduling (USAAR, SSSA). Contacts with the MPSoC design cluster have been strengthened.
- timing analysis of multicore systems with shared caches, and to bound the context switch penalty due to cache effects in preemptive systems
- analysis on micro-architectural level has progressed, especially regarding cache replacement policies and pipeline behaviour.
- automated derivation of timing models from VHDL specifications.
- generation of timing models from observations, based on machine learning and model identification.

Concerning the goal of reconciling timing analysis with compilation, the WCET-aware compiler WCC developed at TU Dortmund has been extended beyond the initial TriCore hardware platform and toward multi-objective optimization. Collaboration between TU Dortmund, AbsInt and the ArtistDesign Cluster on Operating Systems and Networks has been strengthened. We established a new link between reliability, compilers, operating systems and real-time systems.

Finally, dissemination comprises the inclusion of educational material on software synthesis, compilers and timing analysis in the second edition of the textbook on embedded systems by P. Marwedel.

3.1.2.3 Operating Systems and Networks (Cluster)

The fruitful collaboration among the cluster participants is demonstrated by the number of joint publications, projects and events organized within the cluster. The main examples are the organized workshops and conferences, graduate courses, and the various research consortia that have led to new European projects, like ACTORS, PREDATOR, IRMOS, and SOOS.

All research activities in the cluster have progressed substantially within the third year. The following list briefly summarizes some of the major achievements for year 3. Details and more information can be found in the three activity reports by the cluster.

- **UNIBO-PISA** continued to collaborate on predictability and modularity of MPSoC for Real-Time applications. The interaction has been realized by the integrating tools developed by the partners: the Erika RTOS from SSSA has been extensively used on the MPARM platform developed by UNIBO.
- **USAAR, PISA, Dortmund, AbsInt**. Also supported be the PREDATOR project, these partners collaborated to improve the estimation of worst-case execution times considering cache-aware scheduling and WCET-aware compilers.
- **EVIDENCE-PISA**. A great effort has been done to introduce resource reservation and deadline-based scheduling (EDF) in the Linux operating system, so enabling the implementation of advanced resource reservations techniques.
- **LUND-TUKL-PISA**. Also supported by the ACTORS project, these partners collaborated to develop a design framework for partitioning real-time applications on multicore heterogeneous systems, with the objective of guaranteeing optimal usage of the available resources.
- **PISA-UPC** tightly worked together to define a laboratory platform and experiment to be integrated in the education of embedded control system engineers. The experiment consists in the control of a dynamical system on a platform supported by the Erika real-time kernel. The set up has been tested on a graduate course jointly organized in Pisa on June 14-18, 2010.
- **ULUND-PISA** continued to collaborate on event-based control systems. In this third year, the work has focused on network scheduling of event-based controllers.
- **Aveiro, UnivPorto and Malardalen** worked on a reconfigurable hierarchical scheduling framework within an enhanced Ethernet switch that allows an efficient use of bandwidth, enforcing temporal and spatial isolation.
- **York, Cantabria, Porto, Madrid, Valencia** collaborated for providing a language support for programming schedulable systems. This year the work has focused on getting support for multiprocessors into the next versions of Ada and the Real-Time Specification for Java. These have now effectively been agreed and will enter into the standards at their next releases.
- **TUKL, CSEM, Philips, Pisa, York, Porto, Prague**. Contributed on the development of timeliness in Wireless Sensor Networks. The teams at TUKL, CSEM and Philips proposed a generalized notion of timeliness, which suits the characteristics of WSN, based on the requirements in the EU IST project WASP.
- **Mallorca, UnivPorto, Catalonia, IFP** addresses the problem of robustness and timeliness in Controller Area Networks.
- **Cantabria, Madrid: UPM and UC3M, Bilbao, UnivPorto** collaborated for providing real-time support to middleware and composability. A set of timing analysis tools has been integrated with a toolset for MDE. In addition, a new approach has been explored

to integrate the real-time end-to-end flow model with the automatic generation of Ravenscar-compliant source code in distribution middleware.

- **ALL PARTNERS** contributed to a major activity (coordinated by YORK) for building a taxonomy of resources, considering multi-resource platforms and including the use of banded notions of time and hierarchical structures.
- **Madrid, Pisa, Aveiro, UnivPorto, Malardalen, NXP, TUKL** worked on protocol optimizations for embedded real-time communications. The validation showed performance improvements in comparison to currently used infrastructures. The performance has been reported to a journal in an article which now in accepted status.
- **Catania, Pisa, Evidence** have been involved in intelligent transportation systems, automatic traffic monitoring and road surveillance. Various sensors have been used to estimate traffic parameters. Catania proposed a wireless sensor network architecture based on computer vision techniques for automatic scene analysis and interpretation.

3.1.2.4 Hardware Platform and MPSoC Design (Cluster)

The activities on Platform and MPSoC Design and Platform and MPSoC Analysis have been further integrated. The following is a list of some of the major achievements for year 3 showing collaboration between teams of the Cluster and other teams of the NoE. Details and more information can be found in the two activity reports by the cluster, one on design and one on analysis.

- EPFL-UNIBO: Interaction between EPFL and UNIBO was very active in Year 3. Major problems tackled include: 1) Network on Chips models and tools; 2) 3D integration models and analysis tools; 3) Study of NoCs for 3D integration. Exchanges with University of Bologna (UNIBO) continued from the previos years. Prof. Benini spent 2 months at EPFL as Visiting Professor.
- UNIBO-SSSA: UNIBO continued to collaborate with the Scuola Superiore Sant'Anna (SSSA) on predictability and modularity of MPSoC for Real-Time applications. The interaction has been realized by the integrating tools deveoped by the partners: the Erika RTOS from SSSA has been extensively used on the MPARM platform developed by UNIBO.
- ETHZ-TUBS: There has been intense cooperation about the coupling of two performance analysis methods, namely Symta/S and MPA. The corresponding tools have been connected and joint works on hierarchical event streams have been published.
- ETHZ-VERIMAG: The system for mapping algorithms onto MPSoC platforms (DOL) has been connected to the BIP system of Verimag with the advantage of a provably correct design flwo as well as a fast performance evaluation method that supports design space exploration.
- ETHZ-UNIBO: Based on a successful cooperation in terms of energy harvesting sensor networks, several further joint investigations of application control and hardware implementation have been performed, related to the area of CPS. Major extensions have been done in terms of harvesting in distributed settings and reward-based optimization strategies. These activities resulted now in a journal publication.
- TU Braunschweig-ETHZ: Interaction between TU Braunschweig and ETHZ has been in the area of performance analysis for multiprocessor systems with shared resources. Opportunities for improvement of modelling and analysis approaches were identified.

- KTH-ETHZ: Zhonghai Lu from KTH has visited ETHZ in the period November 2009-January 2010. The visit focused on performance analysis of embedded systems, on-chip communication and wireless sensor networks and has increased the mutual understanding of the two groups research efforts in this area. It generated several ideas for focused joint research topics.
- DTU-KTH: The two groups have a tight cooperation on the topic of system level modelling, which is also part of the SYSMODEL Artemis project. The KTH modelling framework ForSyDe is used as common basis for further developing system level modelling techniques. DTU has develop the discrete time modelling domain of ForSyDe further, allowing for faster simulation as well as for parallelization of the simulation kernel, which is a key element when modelling wireless sensor networks (CPS). KTH has focused on synchronous, the untimed and continuous time domain. Mikkel Koefoed Jakobsen from DTU has visited KTH twice during 2010 for periods of several weeks to a few months to foster the joint work on the ForSyDe framework. One of the new demonstrators for this work, is a medical audio-device for adjusting hearing aids.
- CEA LIST and UNIBO have continued their collaboration for the definition and design of a Software Runtime Architecture for the management of many-core components. They also work on the design of efficient hardware support for the execution of this runtime software. This runtime SW is distributed to other prtner within the framework of SMECY project. A joint publication has been submitted on part of this collaboration.
- LINKÖPING-DTU: Linköping and DTU have continued their work on fault tolerant embedded systems. This has resulted in joint development and publications. Prof. Paul Pop from DTU has visited Linköping.
- LINKÖPING-LUND: Linköping has a close cooperation with Lund (Artist design partner Cluster: Operating Systems and Networks) in the area of modelling and QoS optimisation of control applications. This has resulted in joint development and publications. Soheil Samii and Anton cervin have visited Lund and Linköping, respectively.
- IMEC-NTUA: IMEC and NTUA have been collaborating on several MPSoC topics including a framework for automatic parallelization, static and dynamic memory optimization in MPSoC platforms, runtime system exploration for multi-standard Wireless MPSoC.
- IMEC-KTH: IMEC and KTH continued their collaboration in the context of the European project MOSART (http://www.mosart-project.org). The Co-Ware virtual multi-core platform developed by IMEC was transferred to KTH for integration of the NoC architecture in the platform model.
- IMEC-NTNU: there has been cooperation on data value driven scenario identification and reuse of epilepsy detection kernel as additional biomedical demonstrator for scenario related research.

3.1.2.5 Design for Adaptivity (Transversal Integration activity)

The partners have organized several workshops and meetings, including WARM 2010. The meetings act as the interface between the different clusters on issues related to embedded system adaptivity.

The partners have contributed to education about adaptive and feedback-based approaches. There are also several contacts between industry and academia within the activity, e.g., collaborations involving NXP, Ericsson, Volvo, IMEC, and Evidence just to name a few.

A major challenge for this activity continuous to be how to integrate the more hardware-oriented partners from, e.g., the MPSoC cluster with the more software-oriented partners from the OS and networks cluster. Currently the activity is dominated by partners from the latter cluster.

The members of the activity are organizing a special issue on Adaptive Embedded Systems for Real-Time Systems Journal with Årzén (ULUND) as guest editor. The deadline for submissions is Sep 2011 which fits quite nicely with the end of ArtistDesign, making it possible for the members of the activity to submit their work there.

We provide a list of technical achievements of the partners, both jointly and individually, during Year 3, structured in three groups: adaptive resource scheduling, adaptive networking, and hardware adaptation. In the first and largest group we also include work on modelling and analysis relevant to adaptation.

Adaptive Resource Scheduling

- Adaptive and feedback-based resource management (SSSA, ULUND, TUKL, Evidence, Ericsson)
- Adaptive resource management for uncertain execution platforms (ULUND, Ericsson)
- Feedback control of computing systems (ULUND)
- Theory of distributed performance analysis (TU Braunschweig)
- In-system sensitivity analysis for real-time systems (TU Braunschweig)
- Change impact analysis (UYork)
- Parametric WCET analysis (MDH)
- Runtime management of cache-related preemption delay (IPPorto)
- Fault tolerance in adaptive cooperative systems (IPPorto)
- Dynamic behavior of embedded systems (IMEC, NTUA)
- Adaptive control of MPEG-4 decoding (TUKL, ULUND)
- Improving real-time BIP (Verimag).
- Adaptation in service-oriented architectures (UPM)
- Adaptive servers with guarantees (ETH Zurich, SSSA)
- Adaptive power management (ETH Zurich, SSSA)
- Sampling mechanisms for event-driven control systems (UPC, ULUND, SSSA)
- Feedback scheduling vs. event-driven control (UPC)
- Optimal online sampling period assignment (ULUND, UPC)

Adaptive Networking

- Adaptivity in wireless networks (UPorto, UCatania)
- Adaptivity in distributed systems (UPorto, MDH, UAveiro, UPC)
- Adaptive management in energy harvesting systems (ETH Zurich, UBologna)
- Adaptive energy management of wireless smart camera networks (UBologna)
- Adaptive TDMA bus allocation and elastic scheduling (UBologna, SSSA)
- Fault Tolerant and Reliable Communication Platforms (KTH)

Hardware-Based Adaptivity

- eDNA: Reconfigurable self-organising and self-healing hardware platform (DTU)
- Adaptive allocation of applications on MPSoC platforms (ETH Zurich, SSSA)

3.1.2.6 Design for Predictability and Performance (Transversal Integration activity)

The technical work on Predictability has intersected work in all the Thematic Clusters. We give some examples of resulting progress on several topics:

- Novel collaborations within the PREDATOR project include context-switch-cost-aware scheduling (USaar, AbsInt, SSSA), and clarifications of the notions of predictability (USaar, ETHZ). PREDATOR partners and IST Austria succeeded in advancing the understanding predictability on a formal basis, although this topic is far from sufficiently explored.
- Several partners, including Braunscweig, ETHZ, Linköping, and Uppsala achieved substantial progress on the problem of analyzing the predictability and intereference on shared buses and memories in multi-core systems. An interesting topic for futher research is to develop a formal measure that describes predictability and efficiency in this context. This will prove necessary to compare various architectures and resource sharing methods.
- Work on reconciling timing analysis with compilation includes the development of the WCET-aware compiler WCC by TU Dortmund, in collaboration with USaar, AbsInt, ETHZ, and Pisa. WCC is now able to generate and optimize industrial code, e.g., representing an engine control system, with substantially lower WCET, compared to the GCC compiler. WCC has been extended towards code generation and optimization for multi-process systems

Finally, we organized a workshop on predictability and performance at DATE 2011.

3.1.2.7 Industrial Integration (Transversal Integration activity)

This activity groups a set of industrial interactions and collaborations with ArtistDesign teams. The long-term goal is to understand industrial design methodologies and identify the research results that could be applied in these methodologies.

The activities include both technical achievements and dissemination work on the follwowing: General Frameworks for system-level design; Applications to the Automotive Sector; Applications to Chip Design; Applications to Buildings; Applications to Wireless communication technology; Timing Analysis and Predictability; Other Applications.

The level of energy at the meetings organized to foster industrial integration was excellent. In 2009, we proposed the change from Nomadic to Energy Efficient Building has had a re-sounding success. This theme is of increased interest to the European community in response to energy conservation concerns. In this respect, in 2009 a detailed plan was drafted for meetings to be held in 2010 and a modus operandi that included international interaction. The GREEMBED Conference was a result of these efforts. In 2010, we launched a new direction in the area of Synthetic Biology, with the sponsorship and participation to the 2010 International Workshop on Bio-Desing Automation. This area is bound to have a strategic impact on research world-wide. The meetings were very well attended and strong positive feedback was received also from some of the companies involved.

3.2 Joint Programme of Integration Activities (JPIA)

3.2.1 Structure of the Integration Effort

The JPIA activities promote integration of geographically dispersed teams and have long-lasting effects:

Joint Technical Meetings. Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

Staff Mobility and Exchanges. This is essential for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. Mobility is justified by and refers to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

Tools and Platforms. A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

The detailed information regarding the JPIA activities is available in the JPIA deliverable.

-- Changes wrt Y2 deliverable –

No changes with respect to Year 2.

3.2.2 Assessment

The ArtistDesign Network of Excellence is a significant evolutionary step for integrating the leading embedded systems design research teams in Europe.

The overall assessment for the WP at the end of ArtistDesign Y3 (Jan–Dec 2010) is very positive - both in terms of impact on the overall structuring and lasting integration within the consortium and more generally within the area in Europe.

- The ArtistDesign clusters have been actively pursuing operational integration through joint meetings, staff mobility, and shared platforms and tools.
- The level of activity shows that the Cluster / Activity structure and research topics defined for ArtistDesign make sense, and are viable vehicles for integrating the area. In operational terms, they generate sufficient interest for the partners and individual researchers to participate actively in the joint meetings, to exchange personnel, and to orient the tools and platforms developed to make sense within this structure.
- There is clearly a growing level of maturity for tools and platforms – and the partner teams are actively pursuing a policy of implementing tools, demontrators, and in many cases their accompanying methodologies.
- Nonetheless, it is important to remember that these are tools and platforms for research. The aim is not necessarily always for these to lead to commercially viable tools and start-up companies. In general, they are the concrete realisation of the state-of-the-research, allowing to explore possibilities for future research and later tools (some of which may in turn lead to commercially viable products).

In particular, we have had 43 joint technical meetings, covering a broad spectrum of topics and bringing together a wide audience.

The NoE has facilitated the mobility of 33 researchers in Year 3. This is widely considered to be the best way to integrated research teams, through the phyical transfer of persons and competencies. They lead to lasting collaboration and synergy.

The level of effort started in Year 2 has been maintained. We currently have 35 platforms developed in collaboration with ArtistDesign, covering the technical domains of the NoE.

-- Changes wrt Y2 deliverable –

Updated to take into account the Year 3 results.

3.3 Jointly-executed Programme of Activities for Spreading Excellence *(JPASE)*

ArtistDesign leverages on the worldwide visibility of its activities. It is progressively creating a European embedded systems design community and spreading the "Artist culture" in all major research institutions.

To ensure that the next generation of researchers will continue in this direction we, as a consortium, devote a great deal of effort to Spreading Excellence, in both academic and industrial circles. Furthermore, through our links with both core and affiliated partners, we actively set up permanent links between industry and public research, based on existing partner collaborations with major industrial players in the area.

The JPASE activities spread excellence and structure the community at large. They are planned by the Strategic Management Board, and are implemented by ArtistDesign core and affiliated partners.

The NoE leverages on its members and teams, who play a main role in the organisation of world-class scientific events, to disseminate results in the area. We expect that the NoE's structured and authoritative dissemination will have a strong effect on the community as a whole, for orienting and creating synergy for research.

3.3.1 Education and Training

- Courseware – The NoE has the ambition to serve as a resource and point of reference for the area, including by collecting and disseminating course materials for teaching embedded systems design.
- Graduate Studies – The NoE will provide support for selected graduate studies programmes, as the means for training engineers and researchers in embedded systems design.
- Summer Schools – The NoE will actively support and participate in summer schools and seminars in embedded systems design.
- International Workshop on Embedded Systems Education – We will continue this series of international workshops, started in ARTIST2. Dortmund leads this activity.
- Implement a high-visibility International Summer School. The ArtistDesign NoE organise each year a high-visibility international Summer School, drawing top European lecturers in Embedded Systems Design. The audience is researchers, PhD students, and engineers. This year, attendance at the summer school reached selected 100 participants.
- Training Engineers – Many partners are already active in this area, such as IMEC, EPFL, ESI, and Aalborg's CSI. The ArtistDesign NoE will provide logistical, financial dissemination through the Web Portal.

3.3.2 Publications in Conferences and Journals

The ArtistDesign consortium is very active in publishing in scientific journals and conferences, as attested by the list of significant publications by the partners' teams.

The NoE leverages on its members and teams, who are strongly implicated in collaboration with industry, to organize and structure industrial relations, and develop mutually beneficial

interactions. Furthermore, through Industrial Liaison, ArtistDesign receives useful feedback about the relevance of work directions and priorities.

3.3.3 Links to Artemisia

ArtistDesign has strong links to ARTEMIS, through:

- Representation on the **ARTEMIS Industry Association Steering Board**:
  - Joseph Sifakis is the CNRS representative
  - Luca Beninni is the University of Bologna representative
- Partner membership in **ARTEMIS "B"** (Research Organisations & Universities) http://www.artemisia-association.org/member_status
  - Arne Skou is the Aalborg University representative
  - Denis Platter is the CEA representative
  - Joseph Sifakis is the CNRS-Verimag representative
  - Boudewijn Haverkort is the Embedded Systems Institute representative
  - Rudy Lauwereins is the IMEC representative
  - Jean-Pierre Banâtre is the INRIA representative
  - Eduardo Tovar is the Instituto Superior de Engenharia do Porto representative (Instituto Politécnico do Porto in ArtistDesign)
  - Gunnar Landgren is the KTH representative
  - Bernhard Josko is the OFFIS representative
  - Jan Madsen is the TU Denmark representative
  - José Carlos Gómez Sal is the University of Cantabria representative
  - Luca Benini is the University of Bologna representative
  - Farid Ouabdesselam is the Université Joseph Fourier representative

- Strong *informal* links. For example, the ArtistDesign Strategic Management Board was asked to review and comment on the latest edition of the Strategic Research Agenda, published in 2011.
- Strong representation by ArtistDesign partners in ARTEMIS projects,

3.3.4 International Collaboration

The ArtistDesign "*International Collaboration*" activities allow ArtistDesign to be visible internationally, and to monitor the evolution of the state of the art in the area worldwide.

International Collaboration fits into a global win-win strategy for achieving the participants' long-range aims. Examples of activities include:

- **High-level meetings** gathering top representatives from industry, funding agencies, and research, to discuss avenues for International Collaboration, including on R&D and standards.
- **International Summers Schools** in Y3, we organized schools in China, South America, and Morocco.
- Organization and sponsoring of international conferences and schools, to disseminate recent research results, and promote the emergence of embedded systems as a discipline.

- Sponsoring for International conferences, such as CPS Week, DATE, FORMATS and ES Week.
- International Collaboration workshops, such as WESE, ISS, MemoCode, WFCD.
- International Collaboration **Publications**.

International Collaborations is implemented through collaborations with both the USA and Asia, building on existing links developing new ones.

3.3.5 Web Portal

The ArtistDesign Web Portal is a major tool for Spreading Excellence within the Embedded Systems Community. It aims to be the focal point of reference for events and announcements of interest to the embedded systems community.

This plays a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large. We believe the web portal will be an essential mechanism for achieving integration.

It acts as a repository of knowledge in the area, including courseware, information about standards, methods and tools, research publications and results. This web portal will be made available within the NoE core and affiliated partners, and to other parties.

This repository is to be the reference for the embedded systems design community. It includes several features that help keep it coherent and up to date:

- Authorised users (principally, the ARTIST partners) can access the back end of the site to modify and update information directly. The changes are immediately visible on the site, which greatly streamlines the updating process.
- It's possible to track changes and go back to previous versions of individual web pages.
- Events are automatically sorted by date, and transferred to 'Past Events'. When appropriate.
- Structural information (hierarchy of pages) is maintained automatically.
- Ergonomics are set for the entire site. The "look and feel" of the site is always homogeneous throughout the site. It's possible to change these ergonomics, and these changes are applied homogeneously throughout the site, via automated mechanisms.

The ArtistDesign Web Portal offers information about:

- **Workshops, Conferences, Schools and Seminars**
  Provide information about the main scientific events in the area, and in particular those organised by ArtistDesign.
- **International Collaboration**
  Advertise the ArtistDesign International Collaboration events, and provide pointers to the most visible International Projects (either about significant projects outside Europe, or joint International Collaboration projects.
- **Publications**
  Publications from core partners, with emphasis on Position Papers, White Papers, etc. that may have a particularly deep impact.
- **Course Materials Available Online**
  The web portal will centralize course materials from as many sources as possible, to make them available to the general public.

-- Changes wrt Y2 deliverable –
Updated to reflect changes in Y3.

3.4 Managing the Network of Excellence (JPMA)

We believe that the current two-tiered Management structure - dividing the management amongst cluster leaders and the Strategic Management Board composed of both cluster leaders and a limited number of other selected prominent core partners – has been the right one for managing such a large research entity. It has provided the right combination of flexibility and accountability, while leaving room for innovation and evolution.

-- Changes wrt Y2 deliverable –
No changes with respect to Year 2.

4. End Results

We are achieving a significantly more integrated scientific community. Initially, there was a strong fragmentation by topics and communities, with little interaction between them. Over the course of the NoE, the clusters have evolved and merged. A gradually cohesion has taken place, through transversal “NoE Integration” activities, and more importantly through strategic alliances.

We are seeing a convergence of interests, and the gradual emergence of recognized leaders.

-- Changes wrt Y2 deliverable –
No changes with respect to Year 2.

214373 ArtistDesign
Network of Excellence
on Embedded Systems Design

Project Management Report for Year 3

Joseph Sifakis – ArtistDesign Scientific Coordinator
Bruno Bouyssounouse – ArtistDesign Technical Coordinator

ArtistDesign Consortium

Table of Contents

1. Overview

1.1 Project Objectives and Major Achievements

A detailed description of objectives, and particularly the main aims for integration, is provided for each cluster in the sections labelled « State of Integration in Europe ».

1.2 Deliverables for the Reporting Period

WP0: Joint Programme of Management Activities (JPMA)

	D2-(0.2)-Y3	Project Management Report
UJF/Verimag	D2-(0.2a)-Y3	*ch. 1* - **Executive Summary and Overview**
Aalborg	D2-(0.2b)-Y3	*ch. 2* - **Modelling and Validation**
Dortmund	D2-(0.2c)-Y3	*ch. 3* - **SW Synthesis, Code Generation and Timing Analysis**
Pisa	D2-(0.2d)-Y3	*ch. 4* - **Operating Systems and Networks**
DTU	D2-(0.2e)-Y3	*ch. 5* - **Hardware Platforms and MPSoC Design**
UJF/Verimag, Floralis	D1-(0.1)-Y3	**Periodic Report**

WP1: Joint Programme of Integration Activities (JPIA)

UJF/Verimag	D3-(1.0)-Y3	**Integration Activities Report**

WP2: Joint Programme of Activities for Spreading Excellence (JPASE)

UJF/Verimag	D4-(2.0)-Y3	**Spreading Excellence Report**

WP3: Modeling and Validation (JPRA)

UJF/Verimag	D5-(3.1)-Y3	**Modelling**
Aalborg	D6-(3.2)-Y3	**Validation**

WP4: Software Synthesis, Code Generation and Timing Analysis (JPRA)

Dortmund	D7-(4.1)-Y3	**Software Synthesis, Code Generation**
Saarland	D8-(4.2)-Y3	**Timing Analysis**

WP5: Operating Systems and Networks (JPRA)

Pisa	D9-(5.1)-Y3	**Resource-aware Operating Systems**
York	D10-(5.2)-Y3	**Scheduling and Resource Management**
Univ. Porto	D11-(5.3)-Y3	**Embedded Real-Time Networking**

WP6: Hardware Platforms and MPSoC (JPRA)

Bologna	D12-(6.1)-Y3	**Platform and MPSoC Design**
DTU	D13-(6.2)-Y3	**Platform and MPSoC Analysis**

WP7: Transversal Integration (JPRA)

Lund	D14-(7.1)-Y3	**Design for Adaptivity**
Uppsala	D15-(7.2)-Y3	**Design for Predictability**
Trento	D16-(7.3)-Y3	**Integration Driven by Industrial Applications**

1.3 Consortium Management

-- Changes wrt Y2 deliverable –

No changes with respect to Year 2.

1.3.1 Governance Structure

Scientific Coordinator:	Technical Coordinator:
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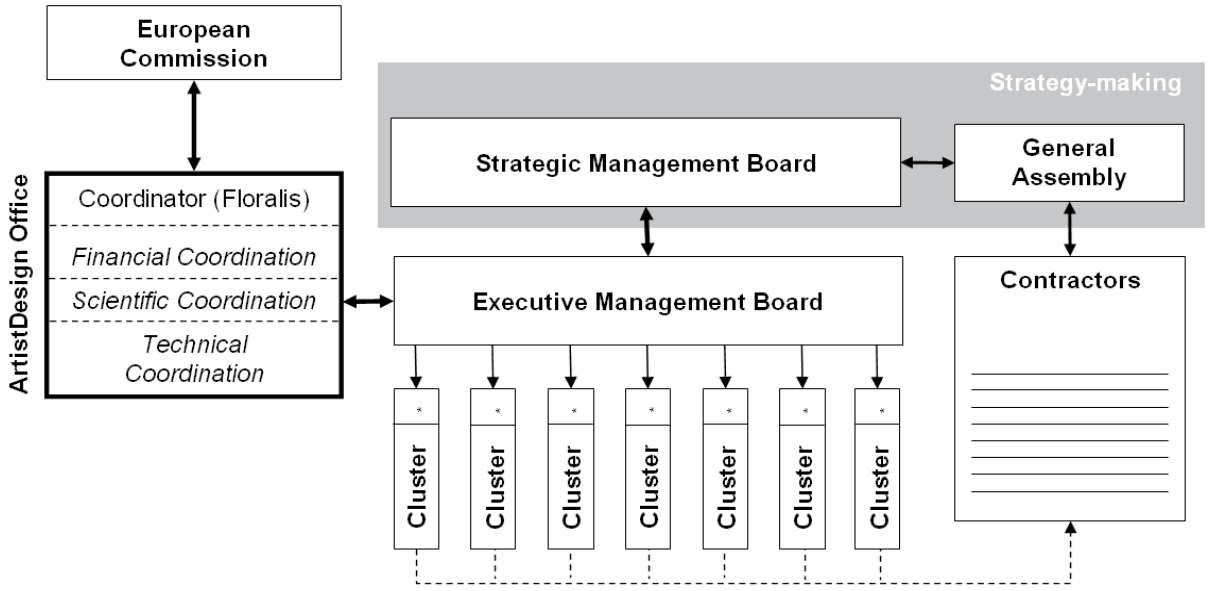
The methodology adopted for achieving the JPA objectives follows the same lines as for managing a laboratory. The activities, their objectives, their technical description, the partners involved, their roles, and the resources available have been clearly defined in the initial Description of Work, and updated in the deliverables. This will be monitored and guided by a tight and rigorous management, as defined in the diagram below:



The main governance bodies are:

The **General Assembly** is composed of one representative per core partner. It is convened at the beginning of the project and meets once per year. It is chaired by the Scientific Manager.

The **Strategic Management Board** is initially composed of the NoE cluster leaders, and a representative of the Coordinator – who attends, with no voting rights. It is chaired by the Scientific Manager, assisted by the Technical Manager. It meets at least once per year – close to the General Assembly meeting. Its members are elected by the General Assembly every two years, according to modalities to be determined in the Consortium Agreement.

The **Cluster Leaders** (who compose the Executive Management Board) are responsible for the overall coordination of the activities led by their cluster. A cluster functions as a virtual team – with a degree of autonomy for defining its internal meetings and day to day management.

1.3.2 Partners Involved

This is provided in the publishable Executive Summary, in the first part of this document.

1.3.3 Contractors

There are no changes to the consortium at the end of Year 1.

1.3.4 Project Timetable

The JPA is organized into activities. The activities should not be considered as tasks of a workprogramme, with begin/end and synchronisation dependencies. Of course, the detailed description of an activity could be decomposed into sub-tasks and intermediate milestones, but this would imply a granularity that is too fine for research activities.

1.3.5 Other Issues

None

1.3.6 Plan for using and disseminating the knowledge

The main instruments for using and disseminating knowledge are:

- Workshops and Schools organised.
  The list is quite impressive, and is provided in the deliverable on “Spreading Excellence”.
- ArtistDesign Web Portal.
  Here also, the quantity of information made available to the greater embedded systems community is quite impressive, and continuously growing. This is possible through the efforts of the entire consortium, who now have direct access for updating the contents.
- Course Materials.
  There is a growing body of course materials made available via the ARTIST web portal.
- Publications.
  The ArtistDesign consortium is very prolific in publishing research articles, surveys, textbooks, roadmaps, and position papers.