IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Workpackage Report for Year 3

Jointly-executed Programme of Integrating Activities (JPIA) Report

With input from all clusters.

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Policy Objective (abstract)

Each ArtistDesign research activity has work within both the JPIA and the JPRA workpackages. The JPIA activities are carried out on a global, NoE level, transcending the clusters. They form the supporting background for integration of the NoE, and are executed in phase and in interplay with the JPRA research activities. For instance, funds for staff mobility will be allocated taking into account the needs for research.

The activities listed here will promote integration of geographically dispersed teams. All these activities will have long-lasting effects, well beyond the duration of the initial EC funding.

These activities include Joint Technical Meetings, Staff Mobility and Exchanges, Tools and Platforms.

Versions

number	comment	date
1.0	First version delivered to the reviewers	February 4th 2010

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1. Overview of the Workpackage

1.1 ArtistDesign Participants and Affiliated Partners

Each ArtistDesign research activity contributes to achieving both research and integration goals. Thus, each has work within both the JPIA and the JPRA workpackages, and all partners and affiliated partners participate in the Joint Programme of Integration Activities.

1.2 Starting Date, and Expected Ending Date

These activities are intimately related to the JPRA (Joint Programme of Research Activities) and run for the entire duration of the NoE.

1.3 Policy Objective

The JPIA activities are carried out on a global, NoE level, transcending the clusters. They form the supporting background for integration of the NoE, and are executed in phase and in interplay with the JPRA research activities. For instance, funds for staff mobility will be allocated taking into account the needs for research.

The activities listed here will promote integration of geographically dispersed teams. All these activities will have long-lasting effects, well beyond the duration of the initial EC funding.

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-- Changes wrt Y2 deliverable --

No changes to the above text with respect to Year 2.

2. Joint Technical Meetings

Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

They are often organized around the annual General Assembly and Review, or around some of the main conferences in the area (most of which are piloted by a majority of ArtistDesign partners).

Depending on the context and in particular on the maturity of the topics under discussion, these Joint Technical Meetings may be open to the public, or by invitation (which implicitly includes all interested ArtistDesign partners).

This is all new text: this entire chapter pertains only to activity in Year 3.

2.1 SW Synthesis, Code Generation and Timing Analysis cluster

Course: Retargetable Compilation

Lugano, Switzerland, Feb. 16-19 & Feb 23-25, 2010

Objectives: Spreading excellence in memory-architecture aware compilation and processor retargetability beyond ArtistDesign partners.
Presenters: Peter Marwedel (TU Dortmund), Rainer Leupers (RWTH Aachen)
Other participants: about 20 students
Conclusion: The new, extended format turned out to be very useful.

http://www.alari.ch

ICT 4 Energy Efficiency

Brussels, Belgium – Feb. 23rd, 2010

IMEC representatives and P. Marwedel participated at a forum on energy efficiency organized by the Commission of the European Communities. The goal was to provide a contribution in the area of energy efficiency for embedded systems.

Cebit

Hannover, Germany – March 9th, 2010

P. Marwedel participated at a panel at the Cebit fair. The purpose was to contribute an embedded systems view on energy efficiency issues of ICT.

Meeting: Brief meeting at DATE

DATE 2010, Dresden – March 11th, 2010-12-10

Participants of the cluster, including members from RWTH Aachen, TU Berlin, TU Dortmund, and IMEC meet at DATE on March 11th. They discussed the state of cooperation, in particular preparations for the MAP2MPSoC flagship workshop at Rheinfels castle in June.

Special Session: Rainer Leupers (organizer), Cool MPSoC Design

DATE 2010, Dresden – March 11th, 2010

Wireless multimedia terminals are among the key drivers for MPSoC platform evolution. Heterogeneous multi-processor architectures achieve high performance and can lead to a significant reduction in energy consumption for this class of applications. However, just

designing energy efficient hardware is not enough. Programming models and tools for efficient MPSoC programming are equally important to ensure optimum platform utilization. Unfortunately, this discipline is still in its infancy, which endangers the return on investment for MPSoC architecture designs. On one hand there is a need of maintaining and gradually porting a large amount of legacy code to MPSoCs. On the other hand, special C language extensions for parallel programming as well as adapted process network programming models provide a great opportunity to completely rethink the traditional sequential programming paradigm for sake of higher efficiency and productivity. MPSoC programming is more than just code parallelisation, though. Besides energy efficiency, limited and specialized processing resources, and real-time constraints also growing software complexity and mapping of simultaneous applications need to be taken into account. The purpose of this session was to analyze the programming methodology requirements for heterogeneous MPSoC platforms and to outline new approaches. With emphasis on wireless applications, this special session has provided a blend of academia/industry presentations, including contributions from innovative startup companies in that domain. This way, it has aimed at consolidation of real life requirements and novel solutions, and stressed the need for intensified and cooperative research activities in MPSoC programming.

http://www.date-conference.com/

Poster session at DATE 2010

Dresden, Germany – March 12th, 2010

The presentation during the Friday poster session at DATE was focused on the automatic parallelization step developed in the MNEMEE project. Furthermore, the embedding of this technique into the integrated tool flow has been presented to the audience.

Winter school course: Rainer Leupers, Cool MPSoC Design

ASCI Winter School 2010, Soesterberg, The Netherlands – Mar 16-18, 2010

Wireless multimedia terminals are among the key drivers for MPSoC platform evolution. The problems of programming MPSoCs (as already described for the session at DATE above), were also discussed at a special session at the ASCI winter school. R. Leupers gave a lecture on Cool MPSoC Design at the ASCI winter school on embedded system. RWTH Aachen has analyzed the programming methodology requirements for heterogeneous MPSoC platforms and R. Leupers has outlined the approaches taken in MAPS compiler project at RWTH Aachen.

http://www.asci.tudelft.nl/pages/events.php?event_id=1

Industrial Workshop

Stockholm, Sweden – April 12th, 2010

L. Thiele, P. Marwedel, AbsInt and other members of the PREDATOR project organized an industrial workshop during the Cyber-physical systems week.

Joint demo at ACE/Compaan Booth at DAC 2010 (Anaheim), "Mapping Streaming Applications onto OMAP"

Anaheim, US - June 13-18, 2010

RWTH Aachen (Germany) and Compaan/ACE (Netherlands) have worked together to couple Compaan's technology (HotSpot Parallelizer) which transforms sequential C code into parallel process networks with the MAPS compiler towards real-life heterogeneous MPSoC backends. A joint demo has been established in this year's DAC (June 2010) to exhibit mapping multiple streaming applications to a commercial multi-processor SoC, the Texas Instruments OMAP 3530. The MAPS (MPSoC Application Programming Studio) project is a research effort to tackle the challenge of programming heterogeneous MPSoCs, ranging over multi-application

modelling, efficient scheduling/mapping and code generation. This joint work enables a complete mapping and compilation flow of streaming Kahn Process Networks (KPN) applications for the OMAP architecture. The demo showed practical scenarios such as quick mapping exploration, parallelizing sequential part and dynamic mapping, using both tools and was well received in the DAC exhibition.

http://www.dac.com

Tutorial: SystemC for Holistic System Design

Anaheim, CA – June 18th, 2010

At this year Design Automation Conference (DAC), Jürgen Teich organized a Friday tutorial covering the topic "SystemC for Holistic System Design with Digital Hardware, Analog Hardware, and Software".

Workshop: Software & Compilers for Embedded Systems (SCOPES) 2010

St. Goar, Germany – June 28-29, 2010

Objectives for the meeting: SCOPES focuses on the software generation process for embedded systems.
Organizer: Heiko Falk (TU Dortmund)
Conclusions: There were many discussions between cluster members at SCOPES (starting already on the eve before the sessions), at DATE, making the entire week the key joint event in spring.

http://www.scopesconf.org/scopes-10

Keynote: Rainer Leupers, System Level MPSoC Design: A Bright Future for Compiler Technology?

SCOPES 2010, St. Goar, Germany – June 29th, 2010-12-02

R. Leupers delivered a keynote speech regarding system level MPSoC design in the SCOPES 2010. Looking back at the SCOPES history, compiler research for embedded processors started out in the 1990s with two major ambitions: (1) more architecture aware code optimizations to better support specialized target machines such as DSPs, and (2) higher flexibility to enable compiler retargeting over a wide range of machines. These research efforts have led to numerous results, many of which are part of industrial products today. So, what is left to do in embedded compilers and who -in a world with "free" tools like GCC and LLVM- will pay for them? Naturally, the evolution of embedded processor architectures demands for a never-ending stream of code optimization innovations. However, he argued that the current trend towards ESL design of embedded MPSoC platforms opens up the most promising new opportunities for compiler research, going far beyond the obvious problem of sequential code partitioning. Increasingly complex software stacks, consolidation of the MPSoC platform market, and higher design abstraction levels induce many interesting novel compiler technology use cases, some of which have been highlighted in the keynote.

http://www.scopesconf.org/scopes-10

Meeting: 3rd Workshop on Mapping Applications to MPSoCs, 2010

St. Goar, Germany – June 29-30, 2010

Objectives for the meeting: This is the flagship workshop of this cluster. The goal of this workshop is to establish links between leading researchers in the area and to stimulate advanced research.
Organizer: Peter Marwedel (TU Dortmund)
Other participants: About 50

Conclusions: We are reaching out far beyond the ArtistDesign network. The workshop is now a key forum for discussions in this area. Attendees expressed their strong interest to continue this series of informal workshops as a platform for discussions.

http://www.artist-embedded.org/artist/-map2mpsoc-2010-.html

Tutorial: Rheinfels MNEMEE tutorial

St. Goar, Germany – June 30th, 2010

The MNEMEE tool flow was demonstrated for the second time in a MNEMEE workshop collocated with 3rd Workshop on Mapping of Applications to MPSoCs and the SCOPES Workshop. The placement of these workshops facilitated the attendance of the industrial and academic workshop participants. Besides an introductional part where an overview of the whole tool flow has been presented, interactive presentations of the MNEMEE tools have been shown by each partner.

Workshop: 10th International Workshop on Worst-Case Execution Time Analysis, 2010

Brussels, Belgium – July 6th, 2010, in connection with ECRTS 2010

Objectives for the meeting: To present and discuss recent work in WCET analysis of all kinds of systems by static or dynamic methods.
Organizer: Björn Lisper (Mälardalen)
Other participants: About 35
Conclusions: this year, the workshop had several contributions concerning WCET analysis for multicore systems, and the use of model checking techniques for timing analysis, in addition to the more traditional timing analysis topics. An invited talk by Dr. Jean Souyris from Airbus gave an industrial perspective on timng analysis of safety-critical software.

http://www.artist-embedded.org/artist/-WCET-2010-.html

Tutorial: Model-Based Embedded Systems Design

Rabat, Morocco – July 12th, 2010

P. Marwedel presented a full-day tutorial on model-based design of embedded systems at the first African ArtistDesign Summer School.

http://www.artist-embedded.org/artist/Overview,1958.html

Tutorial: Invasive Computing - Basic Concepts and Foreseen Benefits

Autrans, France, September 7th, 2010

Jürgen Teich presented a novel paradigm for organizing the computations of large scale MPSoCs of the future at the ARTIST Summer School Europe 2010. The main idea of Invasive Computing relies on the vision that applications will organize themselves and spread their computational load at run-time on processors, communication and memory resources in phases called invasion, and, depending on available degree of parallelism, dynamically changing user objectives or in dependence of the state of the underlying hardware such as temperature profile, load, permissions, or faultiness, again retreat from these.

http://www.artist-embedded.org/artist/Overview,2064.html

Workshop: IFIP Workshop on Software Technologies for Future Embedded and Ubiquitous Systems (SEUS 2010)

Waidhofen/Ybbs, Austria – Oct. 13-15, 2010

Objectives for the meeting: SEUS is a forum for practitioners and researchers to discuss experiences and ideas relating to the development of embedded and ubiquitous systems.
Organizer: Peter Puschner (TU Vienna)
Conclusions: There were some interesting contributions and discussions on the role of time in the design and construction of embedded applications, which underlined the importance of the architectural support for building time-predictable embedded systems.
http://pan.vmars.tuwien.ac.at/seus2010/index.html

Tutorial: Scottsdale MNEMEE tutorial

Scottsdale, US – October 24th, 2010

Members of the teams from Dortmund, TU Eindhoven and IMEC presented results of the MNEMEE workshop at ESWEEK. A tool flow for memory optimizations was demonstrated as a Sunday-Tutorial related to this series of Conferences. The format of a half-a-day tutorial provided in-depth presentations of the tools and techniques developed in MNEMEE.

Workshop: 6th Workshop on Embedded Systems Education, 2010

Scottsdale, US, – October 28th, 2010

Objectives for the meeting: Embedded system education is still a very young area and frequently restricted to teaching the details of microcontroller programming. A long-term objective of this workshop is to improve the visibility of work in the area and to stimulate the introduction of broader curricula.
Organizer: Peter Marwedel (TU Dortmund)
Other participants: About 30
Conclusions: Visibility was improved by the inclusion of the proceedings in the ACM digital library. Presenters included top researchers from the US and Asia. Attendees were extremely satisfied with the quality of the presentations.

http://www.artist-embedded.org/artist/-WESE-10-.html

Workshop: 2nd Workshop on Software Synthesis, 2010

Scottsdale, US, – October 29th, 2010

Objectives for the meeting: An increasing amount of software is not written manually any more. Rather, software is synthesized from abstract models of the required functionality. Software synthesis has been implemented in various disperse communities. The workshop aimed at bringing these communities together.
Organizer: Peter Marwedel (TU Dortmund); Alberto Sangiovanni-Vincentelli
Other participants: About 10
Conclusions: Presenters at this workshop presented industrial as well as academic results. Attendees agreed on the necessity of more work in this area.

http://www.artist-embedded.org/artist/-WSS-10-.html

-- The above is new material, not present in the Y2 deliverable --

2.2 Operating Systems and Networks cluster

Meeting: Cache-aware scheduling and timing analysis
City, Country: Pisa, Italy
Date: February 22-23, 2010
Objectives for the meeting: Understand how schedulability analysis and timing analysis tools can be integrated to properly select preemption points in the task code to reduce cache related overhead, stack usage and power consumption.
Organizer: Giorgio Buttazzo (Scuola Superiore Sant'Anna, Pisa)
Other participants: Marko Bertogna (Pisa), Francesco Esposito (Pisa), Mauro Marinoni (Pisa), Christoph Cullmann (Absint), Martin Kaiser (Absint), Sebastian Altmeyer (USAAR), Claire Burguiere (USAAR), Jian-Jia Chen (ETHZ), Andreas Schranzhofer (ETHZ), Martino Ruggiero (University of Bologna), Paolo Burgio (University of Bologna).
Conclusions: A set of experiments were planned using the Erika kernel on the MPARM simulator to evaluate the effects of non-preemptive scheduling on cache behavior, stack usage and power consumption. A number of suggestions were identified to improve timing analysis to provide data cache and support and stack information for ARM7.

Meeting: Developing real-time applications on multicore reservations
City, Country: Pisa, Italy
Date: June 3-4, 2010
Objectives for the meeting: Understand how to implement a parallel applications on a multicore platform abstracted on a set of virtual processors, using data flow languages.
Organizer: Giorgio Buttazzo (Scuola Superiore Sant'Anna, Pisa), Karl-Erik Årzén (Lund)
Other participants: Johan Eker, (Ericsson), Carl Von Platen (Ericsson), Charles Chen Xu (Ericsson), Enrico Bini (Pisa), Gerhard Fohler (TUKL), Stefan Schorr (TUKL), Vanessa Romero Segovia (ULUND), Anders Nilsson (ULUND), Christophe Lucarz (EPFL), Marco Mattavelli (EPFL), Ghislain Roquier (EPFL), Claudio Scordino (Evidence), Paolo Gai (Evidence).
Conclusions: A set of guidelines to be use in the development of real-time parallel applications.

Meeting: Resource management in multi-core systems
City, Country: Brussels, Belgium
Date: January 11th, 2010
Objectives for the meeting: To discuss multi-resource scheduling and how to integrate different research efforts.
Organizer: Alan Burns (University of York)
Other participants: Giorgio Buttazzo (Pisa), Giuseppe Lipari (Pisa), Eduardo Tovar (Porto), Luis Almeida (Porto) Lucia Lo Bello (Catania), Pau Marti (Catalonia), Marisol Garcia Valls (UC3-Madrid), Tullio Vardanega (University of Padova), Alejandro Alonso (UP Madrid), Gerhard Fohler (TUKL), Stefan Schorr (TUKL).
Conclusions: It was agreed that the wiki was a useful way of organizing collaboration and the exchange of research results as they apply to more complex platforms with multi-cores, buses, NoC and heterogenuois processors may all be presents, and where energy usage may also be an issue. Members agreed to add to the wiki over the coming year.

Meeting: Hierarchical scheduling in control
City, Country: Kaiserslautern*, Germany*
Date: March 3-5, 2010
Objectives for the meeting: To discuss hierarchical scheduling and contract based virtualization.
Organizer: Gerhard Fohler (TUKL).
Other participants: Giuseppe Lipari (Pisa), Alan Burns (University of York), Michael Gonzalez Harbour (University of Cantabria), Stefan Schorr (TUKL).
Conclusions: An approach was developed that would allow the approaches developed for single processor systems to be adapted and extended for multiprocessor and multicore platforms. Future research questions were identified to be worked on throughout the year. Results were discussed at a further meeting in December 2010.

Meeting: Hierarchical scheduling and contract based virtualization
City, Country: San Diego*, USA*
Date: December 1, 2010
Objectives for the meeting: To discuss hierarchical scheduling and contract based virtualization.
Organizer: Giuseppe Lipari (Pisa).
Other participants: Alan Burns (University of York), Stefan Schorr (TUKL), Gerhard Fohler (TUKL).
Conclusions: An approach was consolidated and a process for exploiting the scheme both academically and industrially was identified. Discussions will continue.

-- The above is new material, not present in the Y2 deliverable --

2.3 Hardware Platforms and MPSoC Design cluster

Meeting: Predictability Measures
Zurich, Switzerland – 30.9.2010
Objectives: Define measures for predictability and efficiency in computer architectures.
Organizer: ETH Zurich
Other participants: University Saarland
Conclusions: We have been comparing and developing several measures that allow to estimate the degree of predicvtability of complex systems in a compositional manner. There is no final conclusion yet as there are still technical problems to overcome.

Meeting: Shared Resources in Multiprocessor Systems - Modeling Concepts and Observations *Brussels, Belgium – July 5, 2010*
Objectives for the meeting: TU Braunschweig and ETH Zürich are working on similar analysis approaches for multiprocessor systems with shared resources. The main objective of this meeting was a mutual update on the research activities related to multiprocessor systems with shared resources.
Organizer: Simon Schliecker and Mircea Negrean (TUBS), and Andreas Schranzhofer (ETHZ)
Other participants: -
Conclusions: Open issues and possible improvements on the modelling and analysis approaches of multi-core systems with shared resources were identified. Results have been presented jointly by TU Braunschweig and ETHZ at the annual ArtistDesign Cluster Meeting in Leuven, Belgium. During that meeting, further ideas regarding approaches addressing shared resources in multiprocessor systems have been exchanged with partners of this activity, e.g. Linköping University.

Meeting : MPSoC Cluster Meeting
Dresden, Germany – March 2010
Objectives for the meeting: Status, plans and discussions for the cluster. The meeting was collocated with DATE 2010
Organizer: Petru Eles (LiU)
Other participants: Most members of the cluster
Conclusions : Progress accordng to plans.

Meeting : ARTIST HW Platform and MPSoC Technical Meeting
IMEC, Leuven, Belgium – July 6-7, 2010
Objectives for the meeting: The whole cluster meets once a year to share results and directions. Besides a keynote on biomedical research at IMEC, there were 11 technical presentations covering the two activities of the cluster: Design, and Analysis.
Organizer: Maja D'Hondt (IMEC)
Other participants: Karim Benchehida (CEA), Jan Madsen (DTU), Elena Maftei (DTU), Lothar Thiele (ETHZ), Andreas Schranzhofer (ETHZ), Iuliana Bacivarov (ETHZ), Maja D'Hondt (IMEC), Rudy Lauwereins (IMEC), Roel Wuyts (IMEC), Martin Palkovic (IMEC), Satya Munaga (IMEC), Rogier Baert (IMEC), Carolina Blanch (IMEC), Gert Vanmeerbeeck (IMEC), Francky Catthoor (IMEC), Robert Fasthuber (IMEC), Petru Eles (LU), Soheil Samii (LU), Simon Schliecker (TUB), Mircea Negrean (TUB), Andrea Bartolini (Unibo)
Conclusions : The cluster is very healthy with a lot of interesting research on both existing themes of the cluster, and on new directions. The collaboration with industry has increased, partly due to partners involved in Artemis projects. Progress following the plans set out in the cluster deliverable for year 2,
http://www.artist-embedded.org/artist/Agenda-Slides,2177.html

-- The above is new material, not present in the Y2 deliverable --

2.4 Design for Adaptivity Transversal Activity

Meeting: Retis Laboratory
Pisa, 22.3. – 23.3.2010
Objectives for the meeting: Discuss the current progress in the joint research program on adaptivity and servers.
Participants: ETHZ, SSSA
Organizer: Giorgio Buttazzo, RETIS Laboratory

Meeting: Retis Laboratory
Pisa, 17.12.2010.
Objectives for the meeting: Discuss the current progress in the joint research program on adaptivity and servers. Discuss PhD thesis of Luca Santinelli (was exchange student at ETH Zurich)
Participants: ETHZ, SSSA
Organizer: Giorgio Buttazzo, RETIS Laboratory

Workshop: First International Workshop on Adaptive Resource Management (WARM 2010), Cyber-Physical Systems Week 2010, April 12, 2010, Stockholm, Sweden

The focus of WARM was software-based approaches to adaptive resource management for soft or adaptive embedded real-time applications, e.g., multimedia applications or non-safety critical control applications. Special emphasis was given to multi-resource management and to multi-core platforms.

The programme included 8 submitted presentations, 3 invited presentations and one keynote on challenges and solutions for adaptive resource management in cyber-physical systems given by Prof Raj Rajkumar, CMU.

Organizers:

- Prof. Giorgio Buttazzo, Scuola Superiore Sant'Anna, Pisa
- Prof. Gerhard Fohler, TU Kaiserslautern
- Prof. Alan Burns, University of York
- Prof. Luis Almeida, University of Porto
- Prof. Karl-Erik Årzén, Lund University
- Prof. Michael Gonzalez Harbour, University of Cantabria

URL: http://www.artist-embedded.org/artist/Theme.html

In addition to the above several meetings involving the partners have been held within the projects, typically., FP7 STREP projects (COMBEST, ACTORS, PREDATOR, …), where the actual collaborative work mostly is being performed.

-- The above is new material, not present in the Y2 deliverable --

2.5 Design for Predictability Transversal Activity

Meeting : Towards a Demonstrator
Karlsruhe,Germany – <2010-07-21>
Objectives for the meeting: PREDATOR-internal meeting. Definition of a demonstrator for the review meeting, which involves several PREDATOR partners and their expertise. Identify remaining challenges.Organizer: Jian-Jia Chen (KIT)
Other participants: Daniel Grund (USAAR), Simon Kramer (Bosch), Andreas Schranzhofer (ETHZ), Claire Maiza (USAAR) Conclusions : A demonstration is feasible with respect to Bosch's DemoCar platform. It will consist of ETHZ's WCRT analysis together with AbsInt/USAAR's parameter analyses. Other potential integration opportunities have been identified as well.

Meeting : Predictable Architectures
Zürich, Swizerland – 2010-09-30 to 2010-10-01
Objectives for the meeting: Resuming the discussion (USAAR/ETHZ) on the definition of predictability; Continuing the discussion with Bosch/ETHZ/AbsInt towards the demonstrator Organizer: Lothar Thiele (ETHZ), Andres Schranzhofer (ETHZ) Other participants: Jian-Jia Chen (KIT), Reinhard Wilhelm (USAAR), Daniel Grund (USAAR), Christoph Cullmann (AbsInt), Simon Kramer (Bosch), Luca Benini (UNIBO) [on phone]
Conclusions:

- Predictability is difficult to define.
- PREDATOR Demonstrator is on the way. AbsInt delivered adapted version of aiT.
- Bosch will deriver (and by now did) the parameters, which ETHZ needs for their analysis.

Bosch's Hardware Model is difficult to analyze. Separation of communication and computations is beneficial

Meeting: Predictability Measures

Zurich, Switzerland – 30.9.2010
Objectives: Define measures to determine predictability and efficiency in computer architectures.
Organizer: ETH Zurich
Other participants: University Saarland
Conclusions: We have been comparing and developing several measures that allow to estimate the degree of predicvtability of complex systems in a compositional manner. There is no final conclusion yet as there are still technical problems to overcome.

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2.6 Integration Driven by Industrial Applications Transversal Activity

Meeting: SafeTRANS Industrial Days

Frankfurt, Germany, May 5, 2010, and Stuttgart, Germany, November 23, 2010

Within the context of SafeTRANS (including ArtistDesign Members OFFIS and TU Braunschweig) two Industrial Days were organized in 2010. The workshops provide a platform for discussion and exchange of experiences in industry across application domains. Each workshop had about 45 participants.

The first one on “Interdependency between Safety and Security in Embedded Systems” was held in May in Frankfurt at DB Netz AG. Given presentations cover security and safety aspects in railway communication, protection against manipulation regarding plant integrity, IT risk analysis concerning safety and security in civil aviation, challenges concerning safety and security for car-2-X communication, and others.

The second workshop took place on November 23 at Mercedes Event Center in Sindelfingen, Germany. The title of that workshop was "Model-based Systems Engineering”. Presentations given by industrial participants (Daimler, Volkswagen, EADS, Siemens, ESG, Esterel Technologies) cover topics like quality of software models, test systems, formal methods for model based specification of railways systems, experiences of MBSE in the development of airplane systems, seamless design process integrating system and software design.

http://www.safetrans-de.org/de_8_Industrial_Day.php

http://www.safetrans-de.org/de_9_Industrial_Day.php

Workshop: 3rd Annual ICES Conference Stockholm,

Sweden, Sept. 2nd, 2010

ICES 3rd Annual Conference was entitled -*Networked Products - a solution for the energy problems of the future!* 115 people from academia and industry gathered together for this 1-day conference at Norra Latin, Stockholm City Conference Centre, on Thursday 2nd September 2010.

A key role for ICES is that of nurturing an active network across the borders of academia and industry, with the aim of achieving synergy in education and research. ICES focuses on the thematic areas of embedded systems architecture, system and software verification and development methodology. These areas become more and more important as embedded systems become more advanced and interconnected throughout our whole society.

The theme for the 2010 ICES annual conference, “Networked Products, a solution for the energy problems of the future”, is fully in line with this ambition. Although today’s energy systems are already enabled by embedded systems, a structured approach to their integration would provide new opportunities, not only for greatly enhancing the efficiency of energy systems but also in providing innovative solutions in the search for sustainable energy provision. However, it emerged during discussions between ICES members that it is extremely rare for experts from the energy systems domain to actually meet with embedded systems experts! Thus this year’s conference set out to achieve several goals, including:

- Establishing a meeting point between the "energy" and "embedded systems" communities;

- Identifying the key challenges posed by sustainable energy systems from an embedded systems perspective

- Communicating the huge potential of embedded systems to energy related stakeholders in a contextual and informative way, leading to new discussions, collaboration, and a mutual awareness of the opportunities and challenges ahead.

The program featured an exciting blend of prominent speakers, effectively representing multiple energy system domains such as buildings, cities, smart grids, transportation and legislation. The program also included presentations of research activities in Stockholm, with a specific focus on the area of energy and embedded systems.

A condensed summary of the topics that were raised by the speakers and in the concluding panel debate is provided on the web site including presentations
http://www.kth.se/itm/centra/ices/previous-events/networked-products-conf-1.66443?l=en_UK

Meeting : **Workshop: ICES Seminar: Formalisms for Description and Visualization of Embedded Systems Architectures**

– Current State Of Practice, Needs And Research Topics

Stockholm, Sweden, April 12th, 2010

This ArtistDesign workshop was carried out as part of CPS Week at KTH, 12 April 2010, with approx. 50 participants from industry and academia.

A key fundamental challenge in developing embedded systems is that of managing their complexity while providing products of the desired quality, and at the right cost considering the whole life-cycle. As one important means to handle complexity, architecture description languages (ADL's) have emerged as a means to formally describe software and hardware architectures, providing a basis for analysis of system properties such as reliability and performance, and for synthesis (e.g. generating glue code). The dominating views provided by ADLs is that of describing the system structure, mainly with the notion of black box (SW/HW) components, following the lines of compositionality where the idea is that system properties can be derived from a configuration of components and their externally visible properties. This situation fits well for the purposes of a system integrator that specifies the system architecture and has to reason about system level properties without details of the internals of component implementations. It is clear that embedded systems expose many different types of structures. The term architecture is usually reserved for the fundamental organization of a system that determines essential non-functional properties. At the same time several graphical formalisms have been proposed with the purpose to visualize, communicate and document advanced embedded systems. Examples of early ADL's and formalisms include MetaH, Hatley-Pirbhai modeling, CoDARTS and ROOM.

Over the recent years, many development have taken place, including

- OMG development and standardization leading to UML, SysML and MARTE.
- The standardization of the AADL by SAE (based on MetaH).
- The development of Autosar and the EAST-ADL in the automotive industry.
- Further evolution and maturity of model-driven engineering, including domain-specific languages, environments, and model transformation techniques.

Obviously, each formalism is developed in a particular context, thereby emphasizing certain abstractions, relations and properties. One thrust shared by these efforts is to combine the support for visualization with that of formalized descriptions that are amenable to analysis and synthesis. Visualization, analysis and synthesis, are all key to the engineering of advanced embedded systems based products, with the goals to facilitate communication among people, early decision making and automation. However, while such formalisms have been

researched, and prototype tools been developed, there has been a slow, or only partial adoption in embedded systems industry, with varying degree of success.

The lack of adoption of such formalisms could be explained by the lack of mature tools and standards, and the "normal" gap from research to industrial take-up. It can also be noted that while behavior descriptions and design flows are quite mature for several embedded systems domains, structural descriptions a la ADLs have been lagging behind. The automotive AUTOSAR represents a new effort and departure from this state in providing a middleware standard and by pushing tool vendors to support AUTOSAR. All these efforts, in one way or another, represent efforts in the area of model and component based development. However, because of the multitude of research, standardization and industrial efforts, the current situation is, to say the least, a bit confusing.

The workshop therefore had the overall goal to bring representatives from several "architecture description language" communities together to discuss trends, issues for industrial adoption and what the key outstanding research issues are.

The workshop in addition provided a hands-on session with selected formalisms including AADL, EAST-ADL (a UML profile for embedded systems), SystemC/VHDL, and Domain specific ADL's (using a meta-modeling environment where different formalisms can be created).

http://www.artist-embedded.org/artist/Overview,1937.html

Meeting: Workshop on Green and Smart Embedded System Technology: Infrastructures, Methods and Tools at the Cyber-Physical System Week

Stockholm, Sweden, April 12th, 2010

Organizing committee, general chairs

Alberto Sangiovanni Vincentelli, Huascar Espinoza, Marco Di Natale, Roberto Passerone

Overview

Efficient production, transmission, distribution and use of energy are fundamental requirements for our modern society and the challenge of a green, low carbon economy. Embedded systems have an important role to play in increasing the energy efficiency and in reducing carbon emissions to sustainable growth. Indeed, most systems for monitoring and control of energy production, distribution and use are today interconnected and controlled by embedded devices, in areas such as industrial manufacturing, transportation systems, building automation, domestic appliances and more. This offers the opportunity for the creation of new integrated systems offering new products, processes and services with greater efficiency and better situation awareness to end-users and service and infrastructure owners.

Energy-efficient systems offer unique challenges to the embedded system community, from system-level design to dynamic and adaptive controls, optimization of architectures and communication, real-time and reliable services as well as reusable software components and systems.
Energy efficient solutions include both local and global smart solutions. Smart embedded solutions merge ubiquitous computing and the Internet of Things, i.e., the technology integration with sensors, actuators, micro-chips, micro- and nano-embedded systems that allow for collecting, filtering and producing more and more information locally, to be further consolidated and managed globally according to business functions and services. Locally, embedded systems provide information on energy consumption of every energy consuming appliance in a single location (e.g., home, building, vehicle) to be provided in real-time, in a user friendly way, thereby empowering citizens to take decisions that lead to energy savings. Globally, energy efficient solutions include smart grid concepts, which require dynamic controls

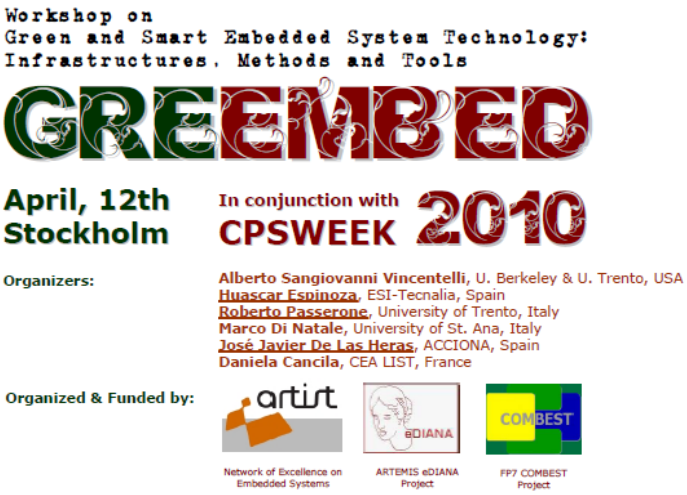
for balancing and organizing production from renewable and conventional sources, negotiating, purchasing and routing power requests, but also regulating, balancing and controlling the amount of electrical power that systems consume.

From the system-level design perspective, there is a need for simulation, modelling, analysis, and monitoring methods and tools to facilitate an integrated system approach. Today, energy efficient solutions are developed by independent companies whose products or components are tested for individual performance independently of each other. An integrated system approach to the design and implementation, where these components are integrated in a way that they reduce energy consumption through cooperation, is rarely used. This often leads to significant system-level inefficiencies. System design methods and tools, including model-based solutions, must consider the growth and evolvability of hardware and software platforms, to ease the conception, development, validation and integration of new devices and services. The challenge and opportunities not only lie in the integration issue, but also in providing methods and tools for innovative solutions that satisfy government regulations, customer expectations and meet environmental challenges.

Objectives / Agenda

GREEMBED 2010 aims at bringing together experts, researchers, and practitioners, from the embedded systems community, who are interested on research and development of embedded system infrastructures, methods, and tools for green and smart energy-efficient applications.

The topics of the proposed workshop are extremely important from an economic and social view and yet some of them still constitute emerging research areas, possibly without well-established or recognized results and require integration of knowledge and cross-fertilization from different domains. CPS Week is an excellent opportunity to bring together people from diverse embedded systems communities, such as controls, simulation and modeling, embedded computation and communication models and algorithms, software and hardware design, languages, sensor networks, real-time systems and several applications communities. Jointly, these communities can help create a critical mass of research, development and innovation in green embedded system technologies. An open exchange of ideas and experiences will benefit the global community, leading to new insights and stimulating further development.



Program: Morning session

9:00-11:00 Session 1: ICT for Energy Efficiency in Buildings

- INVITED SPEAKER: Juan Perez (Labein-Tecnalia, Spain), "*REEB - The European Strategic Research Roadmap to ICT enabled Energy-Efficiency in Building and Construction*"
- INVITED SPEAKER: Anke Weidlich (SAP, Germany), "*Enterprise Integration for Decentralized Energy Management*"
- INVITED SPEAKER: Jose-Javier De Las Heras (ACCIONA, Spain) "*EDIANA - Embedded Systems for Energy Efficient Buildings*"

11:00-12:15 Session 2: User interfaces for Energy Awareness

- INVITED SPEAKER: Régis Decorme (CSTB, France), "*IntUBE - Intelligent Use of Buildings' Energy Information – Energy Challenge Concept*"
- INVITED SPEAKER: Carin Torstensson (Interactive Institute, Sweden), "*BeAware–Boosting Energy Awareness, presentation of the pilot phase on 8 households*"
- INTERACTIVE SESSION - *Short quiz on energy awareness + brainstorming session with the audience on "user interfaces for energy awareness: content and layout*" (chaired by IntUBE and BeAware project partners)

Program: Afternoon Session:

13:30-15:15 Session 3: Smart Buildings & Smart Grids

- INVITED SPEAKER: Hakan Johansson (ABB, Sweden), "*Smart Grid Activities at ABB*"
- "*Energy Saving Information Platform: ENERsip*", Boris Kantsepolsky (MOTOROLA, Israel) and Rafael Morillo (AMPLIA, Spain)
- "*Scheduling energy consumption with local renewable micro-generation and dynamic electricity prices*", Onur Derin & Alberto Ferrante (University of Lugano, Switzerland)
- "*DSM in Spain. Results from GAD Project: Aims, Developments and Ongoing Results*", Laura Moreno (ITE, Spain), Susana Bañares (REE, Spain), Isabel Navalón (Iberdrola, Spain) and Alfredo Quijano (ITE, Spain)

15:30-17:15 Session 4: System and Control Engineering for EE in Buildings

- INVITED SPEAKER: Sylvain Robert (CEA, France), "*The CLIMB project - Implementing the Building Information Model to Optimize Energy Efficiency*" (**Cancelled**)
- "*Adopting system engineering methodology to Virtual Power System design flow*", Slobodan Lukovic, Igor Kaitovic & Umberto Bondi (University of Lugano, Switzerland)
- "*Optimised Embedded Distributed Controller for Automated Lighting Systems*", Alie El-Din Mady, Menouer Boubekeur & Gregory Provan (University College Cork, Ireland)
- "*Embedded Controllers for Increasing HVAC Energy Efficiency*", Jiri Vass, Jana Trojanova, Radek Fisera & Jiri Rojicek (Honeywell, Czech Republic)

http://www.artist-embedded.org/artist/Overview,1928.html

Meeting: IWBDA: International Workshop on Bio-Design Automation at DAC

http://cctbio.ece.umn.edu/wiki/index.php/IWBDA:International_Workshop_on_Bio_Design_Automation

Objectives/Description

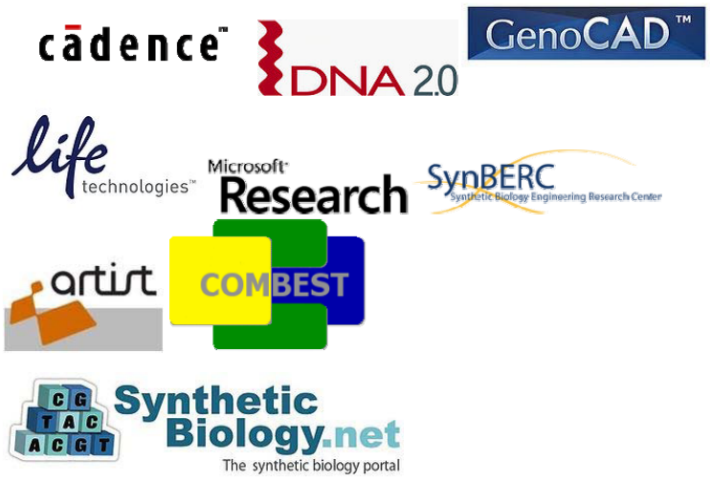
The Second International Workshop on Bio-Design Automation (IWBDA) at DAC brought together researchers from the synthetic biology, systems biology, and design automation communities. The focus is on concepts, methodologies and software tools for the computational analysis of biological systems and the synthesis of novel biological systems.

Still in its early stages, the field of synthetic biology has been driven by experimental expertise; much of its success has been attributable to the skill of the researchers in specific domains of biology. There has been a concerted effort to assemble repositories of standardized components. However, creating and integrating synthetic components remains an ad hoc process. The field has now reached a stage where it calls for computer-aided design tools. The electronic design automation (EDA) community has unique expertise to contribute to this endeavour. This workshop offered a forum for cross-disciplinary discussion, with the aim of seeding collaboration between the research communities.

Topics of interest included:

- Design methodologies for synthetic biology;
- Standardization of biological components;
- Automated assembly techniques;
- Computer-aided modeling and abstraction techniques;
- Engineering methods inspired by biology.

This workshop obtained strong interest from industry as well as scientific organizations as shown below:



We had a good number of participants (about 90), 13 talks and 18 posters including a special session that was dedicated to the topic at the Design Automation Conference.

Agenda

Monday – June 14th

- 9am - 10am, Rm. 303CD

  Opening Remarks: Marc Riedel (General Chair), Ron Weiss (http://weisswebserver.ee.princeton.edu/)

  Keynote Address: Roger Brent (http://labs.fhcrc.org/brent/people.html), Fred Hutchinson Cancer Research Center..

- 10:30 - Noon - Rm. 303CD

  - Tutorial #1 on DNA Nanostructures, Shawn Douglas (http://www.shawndouglas.com/) , Harvard.

  - Tutorial #2 on CAD for Genetic Circuits, Jean Peccoud (https://www.vbi.vt.edu/faculty/personal_pages/jean_peccoud), Virginia Tech.

- Noon - 2pm, Rm. 304A
- Lunch (Rm. 304A) and Posters Session 1 (outside of Rm. 303CD)
- 2:00pm - 4:00pm, Rm. 303CD
- Tech. Talks Session 1 - Tools for Bio-Design Automation

  - 1BDA.1 SynBioSS Designer: From DNA Sequences to Dynamic Phenotypes and Back Emma Weeding and Yiannis Kaznessis

  - 1BDA.2 TinkerCell: CAD Application with Support for Third-party Programs, Deepak Chandran and Herbert Sauro

  - 1BDA.3 Automatic Compilation from High-Level Languages to Genetic Regulatory Networks, Jacob Beal, Ting Lu and Ron Weiss

  - 1BDA.4 Designing Biological Devices in GEC, James Brown, Neil Dalchau, Michael Pedersen and Andrew Phillips

- 4:30pm - 6:00pm, Rm. 303CD
- Tech. Talks Session 2 - Modeling and Standards for Bio-Design
    - 2BDA.1 A Semantic Knowledge Base of Standard Biological Parts, Michal Galdzicki, Cesar Rodriguez, Deepak Chandran, John Gennari and Herbert Sauro
    - 2BDA.2 Modeling and Predicting the Strength of Bacterial Promoters: A Test-case with Promoters Regulated by Escherichia coli Sigma E, Virgil Rhodius, Vivek Mutalik and Carol Gross
    - 2BDA.3 Resolving Variable Dependencies in the MPDE-SSA Algorithm, Abiezer Tejeda, Chris Winstead, Eduardo Monzon, Chris Myers and Curtis Madsen
- 7:00pm - 10:00pm, Dinner - Sponsored by ArtistDesign (http://www.artist-embedded.org/artist/) and COMBEST(http://www.combest.eu)

Tuesday – June 15th

- 8:30am - 10:15am, Ballroom ABC
    - General DAC Keynote (full conference)
    - 10:30am - Noon, Rm. 303CD
    - Open Poster Session (full conference)
- Tech. Talks Session 3 - Design of Biological Circuits and Networks
    - 3BDA.1 Automatic Design of Digital Synthetic Gene Circuits, Mario Marchisio and Joerg Stelling
    - 3BDA.2 Design of In-vitro Synthetic Gene Circuits Slides, Elisa Franco and Richard Murray
    - 3BDA.3 Fan-out Considerations in Gene Regulatory Networks, Kyung Kim and Herbert Sauro
- Noon - 2pm, Rm. 203A
- Lunch (Rm. 203A or Terrance) and Posters Session 2 (Outside of Rm. 303CD)
- 2:00pm - 3:00pm, Rm. 303CD
- Tech. Talks Session 4 - Biological Pathway and Network Optimization
    - 4BDA.1s Predictably Profitable Paths in Metabolic Networks Slides, Ehsan Ullah, Mark Walker, Kyongbum Lee and Soha Hassoun
    - 4BDA.2s Robust Inference of Biological Bayesian Networks Slides, Masoud Rostami and Kartik Mohanram
    - 4BDA.3s Pathway Identification for Strain Engineering Slides, Mona Yousofshahi, Kyongbum Lee and Soha Hassoun
- 3:00pm - 4:00pm, Rm. 303CD

Panel Session - Sponsored by ArtistDesign (http://www.artist-embedded.org/artist/) and COMBEST(http://www.combest.eu)

- Alberto Sangiovanni Vincentelli, University of California at Berkeley and University of Trento - Moderator
    - Ron Weiss (MIT)
    - J.Christopher Anderson (UC Berkeley)

- Andreas Kuehlmann (Cadence Research Labs)
- Andrew Phillips (Microsoft Research)

- 4:00pm - 4:10pm, Rm. 303CD
  - Closing Remarks, Doug Densmore (http://ddensmore.net/) (General Secretary)
- 4:30pm - 6:00pm, Rm. 209AB
- Joint IWBDA/DAC Session, Invited Talks
  - Pamela Silver (http://openwetware.org/wiki/User:PamSilver), Harvard University
  - J. Chris Anderson (http://andersonlab.qb3.berkeley.edu/), Berkeley
  - Richard Murray (http://www.cds.caltech.edu/~murray/wiki/Main_Page), Caltech

Meeting: 2010 Design Automation Conference Panel: Designing the Always-Connected Car of the Future, Chair: Alberto Sangiovanni-Vincentelli - Univ. of California, Berkeley, CA, University of Trento, Italy, Organizers: Arkadeb Ghosal - General Motors, Palo Alto, CA, Paolo Giusto - General Motors, Palo Alto, CA, Alberto Sangiovanni Vincentelli

Objectives/Descriptions

The automotive industry is introducing novel features, such as seamless vehicle-to-vehicle and vehicle-to-infrastructure connectivity to improve in vehicle driver safety (e.g., forward collision) and comfort (e.g., routing to avoid congestion) while facing stricter government regulations, and shortened time-to-market. As a result, automotive Electronic Control System (ECS) architectures are becoming increasingly complex. To cope with these challenges and opportunities, the entire automotive supply chain is engaged as follows: automotive OEMs are managing complexity by reusing legacy components and enabling new technologies; tier one suppliers are increasingly up-integrating features on the same computing platform; tier two suppliers are providing multicore and other powerful technologies; academic institutions are doing research in new analysis, synthesis and optimization methods; and tool providers are trying to raise the level of abstraction for system modeling, analysis and optimization.

The panel was attended by over 400 people and was considered one of the most successful panels of the Conference.
http://www.dac.com/conference+program.aspx

Meeting: Workshop on Software Systems at ESWEEK 2010 Organizers Peter Marwedel, TU Dortmund, Germany and Alberto Sangiovanni-Vincentelli, UC Berkeley, US; University of Trento, I

This is the second year we organized this Workshop held during ESWEEK 2010. There were about 20 participants. Next year we will organize this workshop again.

Objectives/Description

An increasing amount of software is not written manually any more. Rather, software is synthesized from abstract models of the required functionality. As a result, the effort of generating software is reduced and software verification typically becomes easier.

Software synthesis has been implemented in various disperse communities.

The workshop aims at bringing these communities together and at identifying research problems which should be addressed by the scientific community.

Program

8:30 am	**Opening**	Alberto Sangiovanni-Vincentelli (UC Berkeley, US)
8:40 am	**Keynote: Synthesis of Reliable Distributed Real-Time Software**	Edward Lee (UC Berkeley, US)
9:30 am	*coffee break*	
10:00 am	**Software Synthesis in the LabVIEW Graphical System Design Framework**	Kaushik Ravindran and Hugo Andrade (National Instruments, US)
10:30 am	**Code generation or software synthesis? Are they the same?**	Alberto Sangiovanni-Vincentelli (UC Berkeley)
11:00 am	**Synthesizing Cyber-Physical Control Applications for Hybrid Communication Protocols**	Samarjit Chakraborty (TU Munich, Germany)
11:30 am	**Synthesizing real-time implementations from abstract specifications based on timed automata**	Jacques Combaz, Joseph Sifakis and Tesnim Abdellatif (IMAG, France)
11:45 am	**Are software synthesis and code generation widely accepted in industry? What are the urgent problems to solve to make it universally accepted?**	Discussion led by Alberto Sangiovanni Vincentelli
12:30	*Close*	

http://www.esweek.org/

Meeting: Two Special Sessions on Compositional Techniques at DATE2011, Organizers Alberto Sangiovanni Vincentelli and Joseph Sifakis

Grenoble, March 17th, 2011

Participants: Trento, University of California at Berkeley, Verimag, ETH, INRIA, OFFIS, IST

Alberto Sangiovanni Vincentelli and Joseph SIfakis co-organized two special sessions of the Design and Test European Conference (DATE2011) on the achievements of our group. The allocation of two special sessions to the same group is an exceptional event due to the credibility of the team and the quality of the results.

Scope and Agenda

Special Session Type: Hot Topic

Special Session Title: Foundations of Component-based Design for Embedded Systems

Special Session Description
Component-based validation techniques for parallel and distributed embedded systems should be able to deal with heterogeneous components, interactions, and specification mechanisms. This special session describes a unified composition paradigm that allows the composition of subsystems with different execution and interaction semantics, combining computational and analytic models. This paradigm focuses on constructivity, which is reasoning about global system properties based on properties of its individual components.

Special Session Organizers:

Alberto Sangiovanni Vincentelli, University of California, Berkeley and University of Trento, USA and Italy, alberto@eecs.berkeley.edu: Joseph Sifakis, VERIMAG, France, sifakis@verimag.fr

Special Session Moderator

Joseph Sifakis, VERIMAG, France, sifakis@verimag.fr

Presentations (90 min total)

- **1st Presentation**
  - **Presentation Length 30 min:**
  - **Title:** Composing heterogeneous components for system-wide performance analysis
  - **Speaker** Lothar Thiele, ETHZ, Switzerland, thiele@ethz.ch**:**
  - **1st Author** Lothar Thiele, ETHZ, Switzerland**, thiele@ethz.ch:**
- **2nd Presentation:**
  - **Presentation Length 30min**
  - **Title:** Formal Methods for Composing Components
  - **Speaker** Tom Henzinger, Institute of Science and Technology, Vienna, Austria, tah@ist.ac.at
  - **1st Author** Tom Henzinger, President, Institute of Science and Technology, Vienna, Austria, tah@ist.ac.at
- **3rd Presentation:**
  - **Presentation Length 30min:**
  - **Title:** Requirement Engineering for Composition
  - **Speaker** Albert Benveniste, INRIA, Rennes, France, benveniste@inria.fr
  - **1st Author** Albert Benveniste, INRIA, Rennes, France, benveniste@inria.fr

Special Session Title: Flows, Applications and Future of Component-based Design for Embedded Systems

Special Session Description:
It is essential that theoretical results developed by the community of researchers in the domain of compositionality be integrated in coherent component-based design flows that must validated in comparison with existing industrial practices. Furthermore, compositionality results should be implemented in scalable supporting methods and tools. The special session presents a component-based design flow, its application to specific industrial domains and to diverse areas of design endeavors such as energy efficient buildings and synthetic biology.

Special Session Organizers:

Alberto Sangiovanni Vincentelli, University of California, Berkeley and University of Trento, USA and Italy, alberto@eecs.berkeley.edu: Joseph Sifakis, VERIMAG, France, sifakis@verimag.fr

Special Session Moderator

Alberto Sangiovanni Vincentelli, University of California, Berkeley and University of Trento, USA and Italy, alberto@eecs.berkeley.edu

Presentations

- **1st Presentation**
  - **Presentation Length 30 min:**
  - **Title:** Methods and Tools for Component-based Design
  - **Speaker** Joseph Sifakis, VERIMAG, France, sifakis@verimag.fr
  - **1st Author** Joseph Sifakis, VERIMAG, France, sifakis@verimag.fr**:**
- **2nd Presentation:**
  - **Presentation Length 30min**
  - **Title** Using contract-based component specifications for virtual integration testing and architecture design
  - **Speaker** Werner Damm, OFFIS, Germany, damm@offis.de
  - **1st Author** Werner Damm, OFFIS, Germany, damm@offis.de
  - **2nd Author** Eike Thaden, OFFIS, Germany
  - **3rd Author** Ingo Stierand, OFFIS, Germany
  - **4th Author** Thomas Peikenkamp, OFFIS, Germany
  - **5th Author** Hardi Hungar, OFFIS, Germany
- **3rd Presentation:**
  - **Presentation Length 30min:**
  - **Title:** Component-based Design for the Future
  - **Speaker** Alberto Sangiovanni Vincentelli, University of California, Berkeley and University of Trento, USA and Italy, alberto@eecs.berkeley.edu
  - **1st Author** Alberto Sangiovanni Vincentelli, University of California, Berkeley and University of Trento, USA and Italy, alberto@eecs.berkeley.edu

-- The above is new material, not present in the Y2 deliverable --

3. Staff Mobility and Exchanges

From the Description of Work:
Staff Mobility and Exchanges between teams are essential for integration within and beyond the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams.

Mobility should be justified by and refer to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

This is all new text: this entire chapter pertains only to activity in Year 3.

3.1 SW Synthesis, Code Generation and Timing Analysis cluster

Visiting researcher: Dipl.-Inf.Armin Größlinger (University of Passau)
Team visited: ALCHEMY team, led by Albert Cohen (INRIA Saclay)
Orsay, France, April 2009 – March 2010
Reason for the visit: pooling forces on GPGPU programming
Conclusions/objectives reached: finalization of a prize-winning dissertation and a joint publication

Visiting researcher: Prof. Paul A. Feautrier (ENS Lyon)
Team visited: LooPo team, led by Christian Lengauer (University of Passau)
Passau, Germany, 5–23 April 2010
Approximate cost for travel and lodging: €2730 (paid for by the BFHZ)
Reason for the visit: co-authorship of an encyclopedia entry on the polyhedron model
Conclusions/objectives reached: entry submitted and accepted, publication in June 2011

Visiting researcher: Prof. Björn Lisper (Mälardalen)
Team visited: National University of Singapore, led by Abhik Roychoudhury (NUS)
Singapore – Sep. 5, 2010 to Sep. 9, 2010
Approximate cost for travel and lodging: 2000€
Reason for the visit: Examination of a PhD thesis, and to discuss potential collaborations between Mälardalen and NUS.
Conclusions/objectives reached: There are a number of possible collaboration topics. One candidate is to use Mälardalen's concept of scoped flow facts to aid the scope-ware data cache persistence analysis being developed by NUS. Another possible topic is the use of loop invariant generation techniques for timing analysis. A third topic is industrial PhD programmes, where NUS wants to build up such a programme and where Mälardalen has considerable experience.

Visiting researcher: Benedikt Huber, MSc (TU Vienna)
Team visited: Mälardalen University, led by Björn Lisper (Mälardalen University)
Västeras, Sweden – Oct. 11, 2010 to Oct. 16, 2010
Approximate cost for travel and lodging: 970 €
Reason for the visit: Discuss connections and cooperation between the flow-analysis research at Mälardalen University and the work on writing time-predictable software at TU Vienna
Conclusions/objectives reached: The precise input-data dependency analysis developed at TU Vienna provides an ideal basis to simplify the input model for Mälardalens abstract execution

engine SWEET, which has the potential to be used for an improvement of the scalability of flow analysis. From the perspective of TU Vienna, SWEET will be used to automatically derive flow facts for certain classes of programs the group at TU Vienna is investigating. We want to explore the relationship between these restricted program classes and the different merging strategies that need to be used in SWEET.

Visiting student : Volker Seeker (Technical University of Berlin)
Team visited: Compiler and Architecture Design Group, Björn Franke (University of Edinburgh)
Edinburgh,United Kingdom – October 2010 to January 2011
Approximate cost for travel and lodging: 2.500 €
Reason for the visit: Volker Seeker is a student of Computer Science at the Technical University of Berlin. He is currently spending a couple of months at the University of Edinburgh to work on his master thesis. The topic of his thesis is “Design and Implementation of an Efficient Instruction Set Simulator for an Embedded Multi-Core Architecture”. Volker’s thesis is jointly advised by Björn Franke (Edinburgh) and Sabine Glesner (Berlin).
Conclusions/objectives reached: The thesis is expected to be finished in the first quarter of 2011. Hence, we will report about is conclusions and the objectives reached in the deliverables of 2011.

-- The above is new material, not present in the Y2 deliverable --

3.2 Operating Systems and Networks cluster

Visiting researcher: PhD researcher, Gaetano Anastasi (University of Pisa)
Team visited: Distributed Real-Time Systems Lab led by Marisol García-Valls (UC3M)
Leganés, Spain – From October 2010 to July, 2010
Approximate cost for travel and lodging: 5000 €
Reason for the visit: Research collaboration on QoS-based resource management.
Conclusions/objectives reached: Joint publication of research collaboration.

Visiting researcher: Researcher, Ricardo Marau (University of Porto)
Team visited: Distributed Real-Time Systems Lab, led by Marisol García-Valls (UC3M)
Madrid, Spain– October 25-30, 2010
Approximate cost for travel and lodging: 300 €
Reason for the visit: Research on project iLAND connected to ARTISTDesign activities.
Conclusions/objectives reached: Design and implement combined resource management work in iLAND project.

Visiting researcher: Researcher, Axel Jantsch, (KTH)
Team visited: Real-Time Systems Lab (University of York)
York, UK– February 24-25, 2010
Reason for the visit: Discussion on predictable NoC architectures, real-time analysis for worst-case communication latency in NoCs, use of network calculus to provide latency bounds for traffic over NoCs.
Conclusions/objectives reached: Clearer view on the different analysis approaches (real-time analysis and network calculus) and the requirements they impose on the application and NoC platform models. Ideas to build a TLM model of a NoC which mixes analysis and simulation, aiming to high simulation speed and high accuracy

Visiting researcher: Researcher, Lothar Thiele (ETH Zurich)
Team visited: Real-Time Systems Lab, Scuola Superiore Sant'Anna (Pisa)
Pisa, Italy– March 22-23, 2010
Approximate cost for travel and lodging: 1000€
Reason for the visit: Organization of a course on real-time calculus. Research on real-time schedulability analysis.
Conclusions/objectives reached: New ideas were exchanged for the investigation of multi-mode reservation servers that guarantee timing behaviour during mode transitions.

Visiting researcher: PhD researcher, Rui Santos (Universities of Porto and Aveiro)
Team visited: MRTC, Malardalen University, (Malardalen)
Vasteras, Sweden – March 15-June 30, 2010
Approximate cost for travel and lodging: 3000€
Reason for the visit: Research on hierarchical scheduling for Ethernet switches.
Conclusions/objectives reached: A hierarchical framework for enhanced Ethernet switches was derived together with a response time analysis.

Visiting researcher: Researcher, Luis Almeida (University of Porto)
Team visited: Real-Time Systems Lab, Scuola Superiore Sant'Anna (Pisa)
Pisa, Italy– April 27-30, 2010
Approximate cost for travel and lodging: 1000€
Reason for the visit: Organization of a course on real-time networks. Research on real-time networks.

Conclusions/objectives reached: New ideas were exchanged for the development of mobile sensor networks with real-time requirements.

Visiting researcher: Researcher, Shantao Chen (Zhejiang University)
Team visited: DaRTES lab, University of Porto, (UnivPorto)
Porto, Portugal – May 1 - -July 31, 2010
Approximate cost for travel and lodging: 2250€
Reason for the visit: Research on adaptive wireless sensor networks for tracking applications.
Conclusions/objectives reached: An approach was developed to balance energy consumption and tracking accuracy/responsiveness using a dual-rate beacon scheduling technique.

Visiting researcher: Researcher, Julian Proenza (University of Balearic Islands)
Team visited: Distrib. and Real-Time Embedded Systems Lab, University of Porto (UnivPorto)
Porto, Portugal – July 1-August 1, 2010
Approximate cost for travel and lodging: 1500€
Reason for the visit: Research on projects HaRTES and CANbids related ARTISTDesign activities.
Conclusions/objectives reached: Definition of further steps in the collaboration towards fault-tolerant mechanisms for adaptive systems. Start of preparation of joint paper on formal dependability assessment of ReCANcentrate.

Visiting researcher: PhD researcher, Augusto Oliveria (University of Waterloo)
Team visited: DaRTES lab, University of Porto, (UnivPorto)
Porto, Portugal – October 11 – November 13, 2010
Approximate cost for travel and lodging: 1500€
Reason for the visit: Collaboration in the scope of the distributed resource management.
Conclusions/objectives reached: Development of a versatile tagging approach that simplifies accounting for resource consumption in a distributed setup.

Visiting researcher: Researcher, Pau Marti (University of Catalonia)
Team visited: Real-Time Systems Lab, Scuola Superiore Sant'Anna (Pisa)
Pisa, Italy– June 7-11, 2010
Approximate cost for travel and lodging: 1000€
Reason for the visit: Organization of a course on real-time control systems. Research on real-time control, event-based scheduling, and educational emebedded systems.
Conclusions/objectives reached: New ideas were exchanged on how to teach a course on real-time control that integrates control theory and real-time algorithms to develop educational real-embedded systems.

Visiting researcher: Researcher, Manel Velasco (University of Catalonia)
Team visited: Real-Time Systems Lab, Scuola Superiore Sant'Anna (Pisa)
Pisa, Italy– June 7-11, 2010
Approximate cost for travel and lodging: 1000€
Reason for the visit: Organization of a course on real-time control systems. Research on real-time control, event-based scheduling, and educational emebedded systems.
Conclusions/objectives reached: New ideas were exchanged on how to teach a course on real-time control that integrates control theory and real-time algorithms to develop educational real-embedded systems.

Visiting researcher: Researcher, Marco Caccamo (Univ. of Illinois at Urbana Champaign)
Team visited: Real-Time Systems Lab, Scuola Superiore Sant'Anna (Pisa)
Pisa, Italy– Dec. 6-12, 2010
Approximate cost for travel and lodging: 1000€
Reason for the visit: Supervision of a PhD student and discussion on limited preemption

scheduling.
Conclusions/objectives reached: New ideas were discussed on possible research extensions and technology transfer.

Visiting researcher: Researcher, Matteo G. Rossi (Politecnico di Milano)
Team visited: Real-Time Systems Lab (University of York)
York, UK– Nov. 18-19, 2010
Approximate cost for travel and lodging: 0€
Reason for the visit: Discussion of model driven development of real-time systems, including aspects of UML (MARTE) and targeting virtual platforms.
Conclusions/objectives reached: work from Modellica / UML (MARTE) and the virtual platform work (including compile-time virtualisation).

Visiting researcher: Researcher, Nigel Topham (University of Edinburgh)
Team visited: Real-Time Systems Lab (University of York)
York, UK– May 4, 2010
Approximate cost for travel and lodging: 0€
Reason for the visit: Discussion about utilisation of ASIP (Application Specific Processors) for predictable real-time systems.
Conclusions/objectives reached: identification of a promising avenue of research.

Visiting researcher: Researcher, Martin Schoeberl (Technical University of Denmark)
Team visited: Real-Time Systems Lab (University of York)
York, UK– Oct. 29, 2010
Approximate cost for travel and lodging: 900€
Reason for the visit: Discussion about time predictable multiprocessors, in the context of NoC.
Conclusions/objectives reached: identification of a promising avenue of research.

-- The above is new material, not present in the Y2 deliverable --

3.3 Hardware Platforms and MPSoC Design cluster

Visiting researcher : Vana Jelicic (Faculty of Electrical Engineering and Computing, University of Zagreb, Croatia)
Team visited: UNIBO (Micrel Lab), led by Luca Benini
Bologna,Italy – March, 2010 to June, 2010
Approximate cost for travel and lodging: 7000 €
Reason for the visit: Investigation of power aware policies for multimodal wireless sensor networks. Conclusions/objectives reached: The scientific work achived good results. An algorithm for optimizing power consumption in multimodal wireless sensor network has been developed. The WSN is based on low-power piroelectric sensors and more performant CMOS cameras capable performe good performace in security and surveillance applications. The work achieved a paper in a well-known conference.

Visiting student : Mikkel Koefoed Jakobsen (DTU)
Team visited: Electronic Systems, led by Axel Jantsch (KTH)
Stockholm, Sweden – August 2010 to November 2010
Reason for the visit: mikkel Jakobsen's work on the discrete time model in the ForSyDe framework requires tight interaction and cooperation with the ForSyDe team at KTH. Conclusions/objectives reached: Mikkel Jakobsen has developed a new way to realize the discrete time MoC within the ForSyDe framework.This modelling technique is much more efficient than the previously used one, because it does not require to communicate each fine granular timing information between processes. Hence, it allows for much more efficient modelling and simulation while still conforming completely to the semantics of the ForSyDe framework to allow for heterogeneous modelling.

Visiting researcher : Prof. Martin Radetzki, University of Stuttgart
Team visited: Electronics Systems at KTH, led by Axel Jantsch
Stockholm, Sweden, October – December 2010
Approximate cost for travel and lodging: 4000 €
Reason for the visit: Both groups have cooperated on the development of fault tolerant on-chip communication. This visit has faciluated further and deeper cooperation on this topic. The objective is to develop a complete solution for fault tolerant on-chip communication from the link level to transport level.
Conclusions/objectives reached: Solutions for fault tolerance at the network level have been thoroughly research and have resulted in several routing algorithms (a cost-based algorithm using global information, a locally adaptive algorithm, and a learning based algorithm). As a next step this work will be extended to the link level and the transport level.

Visiting researcher : Prof. Paul Pop (DTU)
Team visited: Linköping, led by Petru Eles (Linköping University)
Several short visits during 2010
Reason for the visit: Common research on predictable fault tolerant systems.
Conclusions/objectives reached: Elaborated several approaches. Two common publications for 2010.

Visiting researcher : Soheil Samii (Linköping University)
Team visited: Lund, led by Karl-Erik Årzén (Lund University)
Several short visits during 2010
Reason for the visit: Common research QoS modelling and optimisation of control applications.
Conclusions/objectives reached: Elaborated several approaches. Two common publications for 2010.

-- The above is new material, not present in the Y2 deliverable --

3.4 Design for Adaptivity Transversal Activity

Visiting researcher : Vana Jelicic (Faculty of Electrical Engineering and Computing, University of Zagreb, Croatia)
Team visited: UNIBO (Micrel Lab), led by Luca Benini
Bologna,Italy – March, 2010 to June, 2010
Approximate cost for travel and lodging: 7000 €
Reason for the visit: Investigation of power aware policies for multimodal wireless sensor networks. Conclusions/objectives reached: The scientific work achieved good results. An algorithm for optimizing power consumption in multimodal wireless sensor network has been developed. The WSN is based on low-power piroelectric sensors and more CMOS cameras for security and surveillance applications. The outcomes have been published in a well-known conference.

Visiting Researcher: Martin Radetzki (Prof. at University of Stuttgart, germany)
Team visited: KTH in Stockholm, led by Axel Jantsch
Stockholm, Sweden – October – December 2010-12-23
Approximate cost for travel and lodging: 3500 Euro
Reason for visit: Cooperation on fault tolerant on-chip communication infrastructure. In addition to technical cooperation on developing techniques for network and link-level fault tolerance we have initiated a joint survey paper reviewing the very substantial state of the art.

Visiting Student: Sergi Fernandez (UPC)
Team visited: RETIS Lab, SSSA led by Giorgio Buttazzo
Appr. Cost: 900€
Reason for visit: Attending the "ARTIST Graduate School on RT Kernels for Microcontrollers", organised and funded by ARTIST, June 14-18, 2010, at Scuola Superiore Sant'Anna, Pisa, Italy
Conclusion: The course has been an excellent opportunity to get familiar with the most important concepts and methodologies used to develop a real-time embedded system, including fundamentals of real-time scheduling, control and distributed systems. Also, it served to show how to apply these concepts in practice, using an embedded platform and a real-time operating system to developed simple control applications and make experience with wireless sensor networks.

Visiting researcher: **Michael Reibel Boesen** (DTU)
Team visited: Jet Propulsion Laboratory, Pasadena, CA
Reason for visit: Michael Reibel Boesenhas spent 5 months at NASAs Jet Propulsion Laboratory in Pasadena (CA) to integrate and implement the control and data processing algorithms of a Liquid Crystal Waveguide Fourier Transform Spectrometer on the eDNA prototype platform. A prototype was programmed on a Xilinx Virtex 5 FPGA and was later ported to a National Instruments CompactRIO embedded platform in order to interact with the spectrometer of NASA.

-- The above is new material, not present in the Y2 deliverable --

3.5 Design for Predictability Transversal Activity

Visiting researcher : Prof. Paul Pop (DTU)
Team visited: Linköping, led by Petru Eles (Linköping University)
Several short visits during 2010
Reason for the visit: Common research on predictable fault tolerant systems.
Conclusions/objectives reached: Elaborated several approaches. Written two common publications for 2010.

-- The above is new material, not present in the Y2 deliverable --

3.6 Integration Driven by Industrial Applications Transversal Activity

Visiting researcher: PhD, Lei Feng(Volvo)
Team visited: KTH led by Martin Törngren (KTH)
Approximate cost for travel and lodging: 1000 €
Reason for the visit: Continued collaboration between Volvo and KTH through the ATESST2, MAENAD and CESAR projects. Lei has since 2010 been employed by Volvo by worked part time at KTH. This has proven a fruitful cooperation.

Visiting researcher: Prof Francesco Borelli, UC Berkeley
Team visited: KTH, lead by Martin Törngren and Axel Jantsch (KTH), Stockholm, Sweden. September 1st - 4th 2010,
Approximate cost: 1000 €
Reason for the visit: Francesco Borelli was invited to provide a keynote for the ICES annual conference Conclusions/objectives reached: Apart from the keynote, collaboration between KTH and Berkeley was discussed. Several exchanges of personnel have already been performed (for example with Karl-Henrik Johansson and Mikael Johansson as visitors to Berkeley and Shankar Sastry and Claire Tomlin as a visitor to KTH)

Visiting researcher: Ass. Prof Chris Paredis, GeorgiaTech
Team visited: KTH, lead by Martin Törngren and Axel Jantsch (KTH), Stockholm, Sweden. Oct 19th - 2010,
Approximate cost: None
Reason for the visit: Chris Paredis is involved in the OMG Sysml/Modelica integration, and chose to visit KTH/Stockholm on his way to an invited talk in Gothenburg for the automotive industry. Chris Paredis is interested in setting up a collaboration with Martin Törngrens group regarding model integration. The visit has led to regular web meeting between the groups.

-- The above is new material, not present in the Y2 deliverable --

4. Tools and Platforms

From the description of work :
A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

This is all new text: this entire chapter pertains only to activity in Year 3.

4.1 SW Synthesis, Code Generation and Timing Analysis cluster

4.1.1 Tool or Platform: WCC

Objectives

WCC is the leading tool for exploring the integration of worst-case execution time-aware analysis into compilers.

Main Results

In a previous project, aiT was integrated with an experimental worst-case execution time aware compiler called WCC. During the last year, this integrated tool set was continued to be used for exploring the optimization potential for compiler optimizations using WCETs as the objective function. Work on multi-objective optimization was started.

Current work

The current work explores the optimization potential of WCC further.

Participating partners:

- TU Dortmund
  TU Dortmund designs WCC and explores the optimization potential.
- AbsInt, Saarbrücken
  AbsInt provides aiT.

Web
http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/

Related Publications

Paul Lokuciejewski, Marco Stolpe, Katharina Morik, and Peter Marwedel. Automatic Selection of Machine Learning Models for WCET-aware Compiler Heuristic Generation. In *Proceedings of the 4th Workshop on Statistical and Machine Learning Approaches to Architectures and Compilation (SMART)*, pages 3-17, Pisa / Italy, January 2010.

Sascha Plazar, Paul Lokuciejewski, and Peter Marwedel. WCET-driven Cache-aware Memory Content Selection. In *Proceedings of the 13th IEEE International Symposium on Object/Component/Service-oriented Real-time Distributed Computing (ISORC)*, pages 107-114, Carmona / Spain, May 2010.

Paul Lokuciejewski, Timon Kelter, and Peter Marwedel. Superblock-Based Source Code Optimizations for WCET Reduction. In *Proceedings of the 7th International Conference on Embedded Software and Systems (ICESS)*, pages 1918-1925, Bradford / UK, June 2010.

Heiko Falk and Paul Lokuciejewski. A compiler framework for the reduction of worst-case execution times. *Journal on Real-Time Systems*, 46(2):251-300, October 2010. DOI 10.1007/s11241-010-9101-x.

Paul Lokuciejewski and Peter Marwedel. *Worst-Case Execution Time Aware Compilation Techniques for Real-Time Systems*. Springer, November 2010.

Paul Lokuciejewski, Sascha Plazar, Heiko Falk, Peter Marwedel, and Lothar Thiele. Multi-Objective Exploration of Compiler Optimizations for Real-Time Systems. In *Proceedings of the 13th International Symposium on Object/Component/Service-oriented Real-time Distributed Computing (ISORC)*, pages 115-122, Carmona / Spain, May 2010.

-- Changes wrt Y2 deliverable --

The potential of using WCET as a cost function has been explored further.

4.1.2 MAPS

Objectives

MAPS (MPSoC Application Programming Studio) is proposed and developed in ISS, RWTH Aachen to tackle the challenge of programming future heterogeneous MPSoC platforms. It targets efficient code generation for multiple applications at a time and predefined heterogeneous MPSoC platforms.

Main Results

In 2010, MAPS has been extended with a parallel programming entry called CPN (C for Process Networks), which is a C language extension to allow to model parallel applications. A source-to-source compiler has been implemented to target various backends including pthreads, SystemC and OMAP. A joint work with Compaan has integrated Compaan's product, Hotspot Parallelizer, into the MAPS flow towards the OMAP backend. The sequential code can be firstly parallelized by Compaan into process networks which can be later compiled by MAPS for the OMAP hardware. This work has been showcased in the Compaan booth in this year's DAC. The topic of mapping and scheduling for multiple applications has also been worked on and a paper in this year's DATE conference summarized the major results using a trace-based composibility analysis method. MAPS has been also used in the Nucleus project of UMIC cluster in the context of waveform development for SDRs (Software-Defined Radios). Initial results have been published in the SDR 2010 conference.

Current work

MAPS is under development in many aspects to enhance its capabilities, such as multi-application RT scenario, fast high-level prototyping, dedicated task dispatching/scheduling, supporting more HW back-ends, etc. MAPS is part of RWTH Aachen's Ultra high speed Mobile Information and Communication (UMIC) research cluster. RWTH Aachen has been actively discussing MAPS with ArtistDesign partners at the Rheinfels workshop.

Participating partners:

- RWTH Aachen
  RWTH Aachen is designing and developing the MAPS tools.
- ACE
  ACE provides the CoSy compiler framework for use in the MAPS tools.
- Compaan
  Compaan provides the HotSpot Parallelizer to couple with the MAPS tools.

Web
http://www.iss.rwth-aachen.de/Projekte/Tools/MPSoC%20Application%20Programming%20Studio.html

Related Publications

Leupers, R.and J. Castrillon. "MPSoC Programming using the MAPS Compiler". In *Proc. of the 15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages pp. 897-902, Taipei, Taiwan, Jan 2010.

Castrillon, J., Velasquez, R., Stulova, A., Sheng, W., Ceng, J., Leupers, R., Ascheid, G., and H. Meyr. "Trace-based KPN Composability Analysis for Mapping Simultaneous Applications to MPSoC Platforms". In *Proc. of the Design, Automation and Test in Europe Conference and Exhibition (DATE 2010)*, Dresden, Germany, Mar 2010.

Leupers, R., Thiele, L., Nie, X., Kienhuis, B., Weiss, M. and T. Isshiki. "Cool MPSoC Programming". In *Proc. of the Design, Automation and Test in Europe Conference (DATE 2010)*, Dresden, Germany, March 2010.

S. Schürmans, W. Sheng, A. Stulova, J. Castrillon, R. Leupers, "C for Process Networks", In MAP2MPSOC (Mapping Applications to MPSoCs), St. Goar, Germany, June 2010

Rainer Leupers, Weihua Sheng, Jeronimo Castrillon, Chapter "Software Compilation Techniques for MPSoCs" in the book "Handbook of Signal Processing Systems", Springer, Bhattacharyya, S.S.; Deprettere, E.F.; Leupers, R.; Takala, J. (Eds.) http://www.springer.com/engineering/signals/book/978-1-4419-6344-4

Castrillon, J., Schuermans, S., Stulova, A., Sheng, W., Kempf, T., Ishaque, A., Leupers, R., Ascheid, G. and H. Meyr. "Component-based Waveform Development: the Nucleus Tool Flow for Efficient and Portable SDR". In *2010 Wireless Innovation Conference and Product Exposition (SDR'10)*. Washington D.C., USA, Dec 2010.

-- Changes wrt Y2 deliverable –

The MAPS toolset has be extended in cooperation with other partners.

4.1.3 CoSy

Objectives

CoSy is a mature commercial development compiler platform.

Main Results

RWTH integrated additional optimizations into CoSy. TU Berlin used CoSy for its research on compiler verification. IMEC used CoSy as a platform for generating compilers. RWTH Aachen used CoSy for its MAPS tools.

Current work

Work on additional optimizations continues at RWTH Aachen and so does the work at TU Berlin and IMEC. There is the trend toward using MPSoCs as the target platform.

Participating partners:

- RWTH Aachen
- TU Berlin
- IMEC vzw

Web
http://www.ace.nl/compiler/cosy.html

Related Publications

See 4.3.2.

-- Changes wrt Y2 deliverable --

CoSy is now also used as the platform for MAPS.

4.1.4 ICD-C

Objectives

ICD-C is a development platform with special support for source-to-source transformations. Source-to-source transformations can be implemented without loosing any information about the original C program. It can also be used in cases where full control over the libraries is required.

Main Results

ICD-C was used for the integration of compilers with timing analysis and the impact of optimizing the WCET was studied in a number of cases. Also, it was used for memory-architecture aware pre-pass compilation tools. For their mode analysis on C code, Saarland University uses the ICD-C compiler infrastructure developed at ICD / TU Dortmund. This semi-automatic mode derivation from C code tries to superimpose a mode structure on code which may be generated from automata, from other control models or may be handwritten.

Current work

Current work is extending the support for caches and aims at reducing the number of calls of the WCET estimator in order to speed-up optimization. Machine-learning techniques are being tried as a promising approach. Mnemee partners are using ICD-C. For their mode analysis on C code, Saarland University uses the ICD-C compiler infrastructure developed at Dortmund.

Participating partners:

- TU Dortmund
- Saarland University (via the PREDATOR project)
- U. Passau
- ICD Dortmund (via the Mnemee project)
- TU Eindhoven (via the Mnemee project)
- IMEC (via the Mnemee project)
- ICCS (via the Mnemee project)

Web

http://www.icd.de/es/index.html

Related Publications

R. Wilhelm, Ph. Lucas, O. Parshin. L. Tan, and B. Wachter. *Improving the Precision of WCET Analysis by Input Constraints and Model-derived Flow Constraints.* In *Advances in Real-Time Systems,* LNCS, 2010. To appear.

See also 4.3.1 and 4.3.11

-- Changes wrt Y2 deliverable --

None.

4.1.5 MPMH – an integration of MPA parallelization assistant and MH static memory allocation for MPSoC

Objectives

The main objectives of the framework is to offer an automatic source code parallelization (MPA tool) and memory hierarchy management (MH tool) in order to map efficiently embedded software application on MPSoC platforms. In order to tackle MPSoC programming issues in a MPSoC platform in an efficient way, a single tool performing optimized memory allocation (MH) and parallelizing sequential code (MPA) is an ideal solution. This tool suite is also used in the Platform and MPSoC Design cluster.

Main Results

The following challenges appear when integrating MPA and MH:

- information flow between MPA and MH
- interference between analyses and transformations of both tools
- MPA is not platform-aware and as a result may ruin the benefits obtained by MH
- profiling information (sequential) is hard to match with the parallelized code
- no optimization interactions between MPA and MH possible with the present implementation.

The integrated MPMH tool addresses these challenges and performs common data analyses from both tools, dependent on the Atomium Analysis framework, only once.

Current work

Currently, the affiliated partners of IMEC (i.e., NTUA/ICCS) and core partners (TU Dortmund/ICD) are integrating their tool and design flows with the IMEC MP-MH framework in the memory assignment context of the MNEMEE FP7 project.

Participating partners:

- NTUA/ICCS
  This partner is integrating the dynamic data type and dynamic memory management tools and design flows with the IMEC MPSoC mapping tool flows.
- TU Dortmund/ICD
  This partner is integrating its pre-compiler and compiler framework to the static MH tool of IMEC.

Web
http://www.mnemee.org/

Related Publications

Daniel Cordes, Peter Marwedel, and Arindam Mallik. Automatic Parallelization of Embedded Software Using Hierarchical Task Graphs and Integer Linear Programming. In *Proceedings of CODES+ISSS, 2010)*, Scottsdale / US, October 2010.

-- Changes wrt Y2 deliverable --

Improved interaction between the MH and MPA tools.

4.1.6 aiT

Objectives

aiT is the leading tool for computing worst case execution times (WCETs).

Main Results

A prototype implementation of the UCB computation as developed by Saarland University has been integrated by AbsInt into the aiT Timing Analyzer. The analysis is implemented for the ARM7 and has been tested on smaller benchmark programs.

Current work

Current work is concerned with optimising the performance of the analysis and exploring its potential on larger examples. Implementations for other processors are also underway.

Participating partners:

- AbsInt, Saarbrücken
  AbsInt provides aiT and support for aiT.
- TU Dortmund
  TU Dortmund uses aiT.

Web
http://www.absint.com

-- Changes wrt Y2 deliverable --

None.

4.1.7 Bound-T

Objectives

Bound-T is a tool for computing worst case execution time bounds (WCETs) by static analysis of machine code.

Current work and main results

Work on Bound-T in this period focused on extending the model of the computations in the program under analysis to include the finite size (number of bits) of storage elements and the bit-precise semantics of integer arithmetic and other operations on binary words. This will increase the safety of the analysis and also allow a better translation between Bound-T's models and the ARTIST2/Artist-Design common interchange languages, in particular the ALF language from Mälardalen. Unfortunately, these model extensions proved to exceed the abilities of the main analysis tool that Bound-T has used so far (Presburger Arithmetic as implemented in the Omega Calculator program) which means that other methods of analysis must be chosen and implemented. Thus the extensions are not yet completed.

Participating partners:

- Tidorum, Helsinki
  Tidorum provides Bound-T and support for Bound-T.
- Mälardalen
  Mälardalen University is defining the ALF language for modelling computations and control flow. Discussions on ALF between Tidorum and Mälardalen have been very useful.

Web
http://www.bound-t.com

-- Changes wrt Y2 deliverable --

None.

4.1.8 SWEET

Objectives

SWEET (SWEdish Execution time analysis Tool) is a prototype WCET analysis tool developed at MDH. In particular, SWEET serves as an environment for the development and evaluation of advanced methods for automatic program flow analysis. This makes the program flow analysis component of SWEET an interesting candidate to use as plug-in with other WCET analysis tools, since it can reduce the need for manual annotations.

Main Results

SWEET has been equipped with different interfaces for its program flow analysis, including the ALF code format for representing code on different levels, a novel "Flow Fact" format for expressing precise program flow constraints, and alternative backends producing program flow constraints in the AIS annotation format for aiT, and for the commercial tool RapiTime from Rapita Systems, respectively.

The interfaces have allowed SWEET to be integrated with other tools. Besides the integratation with aiT and RapiTime, enabled by the backends mentioned above, It has been equipped with a C front-end through the SATIrE tool from TU Vienna. This allows SWEET to perform program flow analysis on source code level.

Current work

SWEET is now being extended to perform a more advanced, parametric WCET analysis. An alternative C frontend, using the open LLVM compiler framework, is also being built.

Partners

- Mälardalen University
- AbsInt
- TU Vienna

Related Publications

Björn Lisper, Andreas Ermedahl, Dietmar Schreiner, Jens Knoop, and Peter Gliwa. Practical Experiences of Applying Source-Level WCET Flow Analysis on Industrial Code. In Tiziana Margaria and Bernhard Steffen, eds. *Proc. 4th International Symposium on Leveraging Applications of Formal Methods (ISOLA'10)*, Heraklion, Crete, Oct. 2010

-- Changes wrt Y2 deliverable --

Integration of SWEET with other tools.

4.1.9 LooPo

Objectives

LooPo is a tool suite for the automatic parallelization of loop programs in the polyhedron model, developed at the University of Passau. LooPo offers a number of dependence analysis tools, schedulers and allocators, and it does code generation for shared-memory and distributed-memory machines. The LooPo project has been going on since 1994 and has been funded repeatedly by the DFG.

Main results

Passau's focus has been on extending the applicability of the polyhedron model. Over the years, features like WHILE loops, conditionals, tiling and non-affinity of the loop bounds and array index expressions have been included. Substatement parallelization has been made possible and LooPo has been adapted to Grid computing. At TU Dortmund, LooPo was compared with PLUTO, a parallelization tool developed by Uday Bondhugula at the Ohio State University. The results are available as a Bachelor thesis written by Richard Hellwig. Except for one application, LooPo outperformed PLUTO with respect to minimizing energy consumption and run-time.

Current work

Current activities in the project are to optimize loop nests for the programming of GPGPUs, in particular, with scratchpad memories and to make extend the polyhedron with dynamic methods of program analysis and code generation.

Partners

- University of Passau
- TU Dortmund

Web

http://www.infosun.fim.uni-passau.de/cl/loopo/

Related Publications

Richard Hellwig. Nutzbarkeitsanalyse von Schleifenparallelisierern für GPGPU-Anwendungen in Eingebetteten Systemen (Usability Analysis of Loop Parallelizers for GPGPU-Applications in Embedded Systems), Bachelor thesis, TU Dortmund, 2010

-- The above is new material, not present in the Y2 deliverable --

4.1.10 R²G

Objectives

R²G (speak: R square G) is an extension to the open source RTEMS real-time operating system. The purpose of R2G is to remove the limitations of RTEMS and MPARM in the context of multi-threaded applications and to support IMEC's RTLib, which implements the parallelization of MPMH.

Main results

With R²G TU Dortmund established the connection between several tools. The parallelized source code produced either by MPMH (IMEC) or by the MNEMME Tool Flow (MPMH + ICD-C + TGE) can now be executed on several simulators.

In addition to year 2, were only MPARM was supported; TU Dortmund has implemented two new platforms based on the CoMET simulator (Synopsis). Due to high simulation speed of CoMET, big benchmark applications can be executed now.

The two new CoMET based platforms implement a flat respectively hierarchical memory layout. On the hierarchical platform, memory optimization and mapping tools can fully exploit their optimizations.

Partners

- TU Dortmund
- IMEC

Web

http://ls12-www.cs.tu-dortmund.de/~heinig/research/projects/r2g

Related Publications

Andreas Heinig. R²G: Supporting POSIX like semantics in a distributed RTEMS system. Technical Report 836, TU Dortmund, Faculty of Computer Science 12, December 2010.

-- The above is new material, not present in the Y2 deliverable --

4.1.11 MNEMEE Tool Flow

Objectives

The theme of intelligent ubiquitous devices will dominate the future embedded system designs and speed up the integration of multimedia and communication applications, thus creating very complex, dynamic source code. Today, it is increasingly impossible for designers to map applications cost-efficiently to any platform, without significant optimization of the initial source code. The MNEMEE Tool Flow has addressed this key challenge by introducing an innovative supplementary source-to-source optimization design layer for data management between the state-of-the-art optimizations at the application functionality and the compiler design layer.

Main results

Prototype tools are running and most parts of the tool flow run fully automatic. The integrated tool flow reduced the execution time for MPEG-4 by 30%. Scratchpad allocation techniques alone provide a 45% reduction of the energy consumption and a 40% reduction in execution time for the edge detection benchmark. More details are available in the (confidential) deliverable 5.3 of the Mnemee project.

ArtistDesign-supported man power enabled the design of R²G. This tool filled a gap within the MNEMEE project: Now the source code produced by the tool flow can be simulated on well known simulators. Hence, the individual tools as well as the overall tool flow can be evaluated. Furthermore, the simulation has the advantage of delivering the energy consumption and exact cycle counters.

Partners

- TU Dortmund
- IMEC (via the Mnemee project)
- ICCS Athens (via the Mnemee project)
- TU Eindhoven (via the Mnemee project)
- ICD Dortmund (via the Mnemee project)
- INTRACOM S.A.Telecom Solutions (via the Mnemee project)
- THALES Communications S.A. (via the Mnemee project)

Web

http://www.mnemee.org/

Related Publications

Robert Pyka, Felipe Klein, Peter Marwedel, and Stylianos Mamagkakis. Versatile system-level memory-aware platform description approach for embedded MPSoCs. In Proceedings of the ACM SIGPLAN/SIGBED 2010 conference on Languages, compilers, and tools for embedded systems (LCTES '10). 9-16, April 2010

Daniel Cordes, Peter Marwedel, and Arindam Mallik. Automatic Parallelization of Embedded Software Using Hierarchical Task Graphs and Integer Linear Programming. In *Proceedings of CODES+ISSS, 2010)*, Scottsdale / US, October 2010.

Yiannis Iosifidis, Arindam Mallik, Stylianos Mamagkakis, Eddy De Greef, Alexandros Bartzas, Dimitrios Soudris, and Francky Catthoor. A framework for automatic parallelization, static and dynamic memory optimization in MPSoC platforms. In Proceedings of the 47th ACM/IEEE Design Automation Conference – DAC, pages 549-554, Anaheim (California) / USA, June 2010. Also listed in Scheduling & Resource mgt deliverable and in Integration driven by Industrial Applications deliverable.

Christos Baloukas, Lazaros Papadopoulos, Dimitrios Soudris, Sander Stuijk, Olivera Jovanovic, Florian Schmoll, Daniel Cordes, Robert Pyka, Arindam Mallik, Stylianos Mamagkakis, François Capman, Séverin Collet, Nikolaos Mitas, and Dimitrios Kritharidis. Mapping embedded applications on MPSoCs: the MNEMEE approach. In *Proceedings of the Annual Symposium on VLSI*, ISVLSI 2010, 5-7 July 2010, Lixouri, Kefalonia, Greece. Also listed in Scheduling & Resource mgt deliverable and in Integration driven by Industrial Applications deliverable.

Christos Baloukas, Lazaros Papadopoulos, Robert Pyka, Dimitrios Soudris, and Peter Marwedel. An Automatic Framework for Dynamic Data Structures Optimization in C. In *Proceedings of the 18th international conference on Very Large Scale Integration (VLSI)*, System-on-Chip (SoC), VLSI-SOC 2010, 27-29 September 2010, Madrid, Spain

Christos Baloukas, Marijn Temmerman, Anne Keller, Stylianos Mamagkakis, Francky Catthoor, Dimitrios Soudris and Serge Demeyer. Abstract and concrete data type optimizations at the UML and C/C++ level for dynamic embedded software. Book chapter in Behavioral Modeling for Embedded Systems and Technologies: Applications for Design and Implementation. Pages 55-84, IGI Global, 2010.

-- The above is new material, not present in the Y2 deliverable --

4.2 Operating Systems and Networks cluster

4.2.1 iLAND middleware

Objectives

Design and implementation of a middleware for supporting dynamic reconfiguration in real-time networked embedded systems in the context of iLAND project.

Main Results

UC3M has provided the initial release (beta version) of the Reference Implementation of iLAND middleware which is a resource-aware communications middleware for service oriented applications. UC3M has been the sole implementor and conceptual developer of this release. Real-time platform support (by enhancing the Linux OS real-time facilities with combined distributed resource management) is to be provided by UnivPorto.

Current work

Currently, new reconfiguration and service-based composition algorithms are being implemented in the middleware.

Participating partners:

- UC3M (developer of this release) and UnivPorto (real-time platform support).

Web
http://www.iland-artemis.org

Related Publications

1. M. García-Valls, Iria Estévez-Ayres, Pablo Basanta-Val. *Dynamic priority assignment scheme for contract-based QoS resource Management* . 7th IEEE International Conference on Embedded Software and Systems. (IEEE ICESS 2010). IEEE Computer Society Press. Bradford, UK. May 29 - June 1, 2010.
2. M. García-Valls, Pablo Basanta-Val, Iria Estévez-Ayres. *A component model for homogeneous implementation of reconfigurable service-based distributed real-time applications* . In International Workshop on Distributed Architecture modeling for Novel component based Embedded Systems, DANCE 2010. IEEE Computer Society Press. Tozeur, Tunisia. May 30, 2010.
3. M. García-Valls, L. Fernández-Villar, I. Rodríguez-López, I. Estévez-Ayres, and P. Basanta-Val,. *Towards a middleware architecture for deterministic reconfiguration of service-based networked applications.* 15th IEEE ETFA 2010 (Emerging Tecnologies and Factory Automation). 13-16 September, Bilbao (SPAIN) pp 1-8. 2010
4. iLAND project deliverables D3.2, D3.4, D4.2, D4.3 and D4.5
5. P. Basanta-Val, M. García-Valls and I. Estévez-Ayres. Fine tuning of the multiplexing facilities of Java's Remote Method Invocation. Accepted for Concurrency and Computation Practice and Experience

6. P. Basanta-Val, M. García-Valls and I. Estévez-Ayres. Extending the Concurrency Model of the Real-Time Specification for Java. Accepted for Concurrency and Computation: Practice and Experience.
7. Pablo Basanta-Val, Luis Almeida, Marisol Garcia-Valls, and Iria Estevez-Ayres. A synchronous scheduling service for distributed real-time Java. IEEE Transactions on Parallel and Distributed Systems, 21(4):506-519, April 2010
8. Pedro Silva, Luís Almeida, Mário Sousa, Ricardo Marau. Temporal behavior of Ethernet communications: Impact of the operating system and protocol stack. MICS 2010 - Int. Conf. on Models of Information and Communication Systems. Rabat, Morocco. 2-4 Nov 2010.

4.2.2 FTT-SE network manager

Objectives

Provide a network operating system that supports heterogeneous types of traffic, is capable of providing temporal partitions and supports prompt dynamic reconfiguration and adaptation in real-time networked embedded systems based on Ethernet.

Main Results

This protocol has been developed in the scope of the FTT (Flexible Time-Triggered) framework, which is basically a TT framework with on-line scheduling, thus amenable to dynamic updates and integration with asynchronous events. It has been applied successfully to didactic distributed control set-ups and an industrial video surveillance system. A distribution for Linux (with or without RT-Linux) is available on SourceForge. FTT-SE was also ported to QNX, recently, in collaboration with the group of Sebastian Fischmeister from the University of Waterloo. Moreover, an utilization-based admission control for dynamic QoS management was also developed in collaboration with the group of Raj Rajkumar at CMU. Both latter works were developed partly in the scope of the iLAND project.

Current work

Currently, specific hardware adaptors are being developed to allow seamless integration of non protocol compliant nodes. Moreover, a new Ethernet switch is being developed that integrates the protocol directly (HaRTES project).

Participating partners:

- Aveiro, UnivPorto.

Web
http://paginas.fe.up.pt/~ftt/index.html

Related Publications

1. Pedro Silva, Luís Almeida, Mário Sousa, Ricardo Marau. Temporal behavior of Ethernet communications: Impact of the operating system and protocol stack. MICS 2010 - Int. Conf. on Models of Information and Communication Systems. Rabat, Morocco. 2-4 Nov 2010.

2. L. Almeida, R. Marau, K. Lakshmanan and R. Rajkumar. On the schedulability analysis for dynamic QoS management in distributed embedded systems. SEUS 2010, 8th IFIP Workshop on Software Technologies for Future Embedded & Ubiquitous Systems, Waidhofen/Ybbs, Austria, October 13-15, 2010.
3. R. Marau, L. Almeida, K. Lakshmanan, R. Rajkumar, P. Pedreiras. Utilization-based Schedulability Analysis for Switched Ethernet aiming Dynamic QoS Management. ETFA 2010, 15th IEEE Conference on Emerging Technologies and Factory Automation. Bilbao, Spain, 13-16 September 2010.
4. Ricardo Marau, Luis Almeida, Mario Sousa, Paulo Pedreiras. A middleware to support dynamic reconfiguration of real-time networks. ETFA 2010, 15th IEEE Conference on Emerging Technologies and Factory Automation. Bilbao, Spain, 13-16 September 2010.
5. Javier Silvestre, Ricardo Marau, Paulo Pedreiras, Luis Almeida. On-line QoS Management for Multimedia Real-Time Transmission in Industrial Networks, IEEE Transactions on Industrial Electronics. DOI: 10.1109/TIE.2010.2049711, May 2010 (available on-line on IEEEXplore, awaiting printing).

4.2.3 OpenZB – ZigBee for Wireless Sensor Networks

Objectives

To provide a complete set of models and tools for analyzing, dimensioning, simulating and engineering wireless sensor networks (WSNs) based on the IEEE 802.15.4 and ZigBee protocols, the most widespread technologies for Wireless Sensor Networks.

Main Results

A complete toolset has been made available on the web, with the first release being posted in November 2006. Since then, the site has already witnessed over 100 000 visits (effective visits, not just mouse clicks), with more than 6000 downloads of the toolset from all around the world (including top universities and companies). Notably, there are 4-5 downloads in average per day, almost 4 years after the first release.

Since early 2009, the synergies created by the open-ZB research team have triggered the creation of the TinyOS 15.4 and ZigBee Working Groups, in which ISEP (Porto) researchers have been actively involved since their foundation.

Current work

ISEP (Porto) continues working towards "official" implementations of the standard 15.4 and ZigBee protocols, as well as of Quality of Service add-ons (e.g. security, hidden-node avoidance, traffic differentiation, implicit GTS allocation).

Participating partners:

- Polytechnic Institute of Porto – ISEP (Porto)
- Technical University of Prague (CTU)

Web
http://www.open-zb.net

Related Publications

1. Petr Jurcik, "Real-Time Communications over Cluster-Tree Wireless Sensor Networks", PhD Thesis in Electrical Engineering and Information Technology, Faculty of Electrical Engineering of the Czech Technical University in Prague (Czech Republic) in collaboration with CISTER-ISEP Research Unit, Polytechnic Institute of Porto (Portugal). Submitted in January 2010 and defended in October 2010.
2. P. Jurcik, R. Severino, A. Koubaa, M. Alves, E. Tovar, "Dimensioning and Worst-case Analysis of Cluster-Tree Sensor Networks", ACM Transactions on Sensor Networks, Volume 7, Issue 2, Article 14, August 2010.
3. Zdenek Hanzálek, Petr Jurcik, "Energy Efficient Scheduling for Cluster-Tree Wireless Sensor Networks With Time-Bounded Data Flows: Application to IEEE 802.15.4/ZigBee", IEEE Transactions on Industrial Informatics, vol. 6, nº3, August 2010.
4. Petr Jurcik, Zdenek Hanzalek, "Simulation study of energy efficient scheduling for IEEE 802.15.4/ZigBee cluster-tree Wireless Sensor Networks with time-bounded data flows", 15th IEEE Int. Conf. on Emerging Technologies and Factory Automation (ETFA 2010), Bilbao, Spain, 13-16/SEP/2010.

4.2.4 Architecture Simulator

Objectives

Maintain and extend the multi-processor cycle-accurate architectural simulator (MPARM) developed by at the University of Bologna to support the execution of real-time concurrent applications in multicore embedded systems.

Main Results

The Erika kernel has been ported to run on top of the MPARM simulator to execute real-time concurrent applications on a multicore ARM7-based platform.

Current work

The simulator is currently being used to perform a set of experiments of non-preemptive scheduling, cache-aware scheduling, and power-aware strategies.

Participating partners:

- Scuola Superiore Sant'Anna of Pisa was responsible for the Erika porting;
- University of Bologna provided support for maintaining the simulator core;
- Evidence provided support for maintaining/adapting the Erika kernel.

Web

ERIKA: http://erika.sssup.it/
MPARM: http://www-micrel.deis.unibo.it/sitonew/research/mparm.html

Related Publications

1. P. Burgio, M. Ruggiero, F. Esposito, M. Marinoni, and G. Buttazzo, L. Benini, "Adaptive TDMA bus Allocation and Elastic Scheduling: a unified approach for enhancing

robustness in multi-core RT systems", Proceedings of the 28th IEEE International Conference on Computer Design (ICCD 2010), Amsterdam, the Netherlands, October 3-6, 2010.

4.2.5 Partitioning Tool for Multicore Platforms

Objectives

Develop a tool that supports the process of partitioning a real-time application on a set of flows running on a multicore platform, abstracted as a set of virtual processors, with the objective of minimizing the required computational resources.

Main Results

A graphic tool was developed to specify parallel applications and find possible partitions with given timing and precedence constraints.

Current work

The tool is being used to evaluate the performance of several partitioning heuristics, against the optimal algorithm.

Participating partners:

- Scuola Superiore Sant'Anna of Pisa was responsible for the tool development;
- University of Lund provided inputs on the tool requirements;
- EPFL Lausanne provided support for the specification of realistic multimedia applications.

Web
URL: http://mrr.sssup.it/mrr/

Related Publications

1. P. Burgio, M. Ruggiero, F. Esposito, M. Marinoni, and G. Buttazzo, L. Benini, "Adaptive TDMA bus Allocation and Elastic Scheduling: a unified approach for enhancing robustness in multi-core RT systems", Proceedings of the 28th IEEE International Conference on Computer Design (ICCD 2010), Amsterdam, the Netherlands, October 3-6, 2010.

4.2.6 MaRTE OS

Objectives

MaRTE OS is an open source Hard Real-Time Operating System for embedded applications that follows the Minimal Real-Time POSIX.13 subset. It provides an easy to use and controlled environment to develop Multi-Thread Real-Time applications. One of the main objectives is to support mixed language applications in Ada, C and C++.

Main Results

MaRTE OS has been succesfully used in several industrial projects, including the development of embedded controllers for satellite dishes in vehicles and for welding robots. It is also the first platform to fully support the real-time services defined in the new Ada 2005 standard. MaRTE OS is also being used for teaching in the areas of real-time operating systems and embedded applications. The main characteristics of the MaRTE OS kernel are:

- Supports mixed language applications in Ada, C and C++ (experimental support for Java as well).
- Offers the services defined in POSIX.13: pthreads, mutexes, condvars, ...
- All services have a time-bounded response (including dynamic memory allocation with TLSF).
- Single memory address space shared by the multi-thread application and MaRTE OS.
- Available under the GNU General Public License 2.
- Based on the AdaCore GNU toolchain.
- Implements the Ada2005 Real-Time Annex.

Current work

MaRTE OS is currently being extended to support real-time programming in multicore / multiprocessor platforms. As such it is being used to validate the new proposals for support of multicore platforms in the forthcoming revision of the Ada language.

Participating partners:

- Universidad de Cantabria, Spain
- Universidad Politecnica de Valencia, Spain

Web
http://marte.unican.es

-- The above is new material, not present in the Y2 deliverable --

4.3 Hardware Platforms and MPSoC Design cluster

4.3.1 Tool: SymTA/S

Objectives

SymTA/S is a tool for the development and verification of embedded multiprocessor real-time systems. The existing technology is mainly suitable for event or time-driven systems with message passing as the main task interaction. The tool shall be extended to cover the timing implications of multicore processors, or multiprocessor-systems-on-chip.

Main Results

In several previous projects (funded by german DFG, “Sureal”, funded by german BMBF, ARTIST2, and others), the compositional analysis approach has been transferred into a tool framework which is now also commercially available. The available modelling options capture typical problems in todays automotive systems (CAN bus utilization, end-to-end deadlines,…). This addresses a growing need for formal methods in the industry. The topics currently under research (see below) address future problems which can be expected to become of increasing industrial interest in the future.

Current work

The research version of the tool framework is currently being developed into several new directions: Modeling of shared resources for multiprocessor-system-on-chips (see ArtistDesign Activity 6.2: Platform and MpSoC Analysis), the modelling of hierarchical event models (in the scope of the COMBEST project), and the demonstrator platform for adaptive systems (see ArtistDesign 7.1: Design for Adaptivity). Besides the extension of the applicability into new domains, a major focus within ArtistDesign is the synergetic coupling of tools, as well as the correspoinding development of models.

Participating partners:

- TU Braunschweig.

  TU Braunschweig investigates synergies in the coupling of methods and implements prototypical implementations of the research results.

- Symtavision GmbH.

  Symtavision is the commercial co-developer of the tool framework. A focus within ArtistDesign is the coupling of with other industrially available tools (such as aiT).

- ETHZ.

  Collaboration on the coupling of MPA and SymTA/S with respect to modelling of hierarchical event models.

- Absint GmbH.

  The aiT tool supplies task timing models, which are required for system level analysis.

Web
http://www.symtavision.com/
http://www.ida.ing.tu-bs.de/index.php?id=symtas
http://www.ida.ing.tu-bs.de/en/research/projects/accord/

Related Publications

1. Simon Schliecker and Arne Hamann and Razvan Racu and Rolf Ernst. "Formal Methods for System Level Performance Analysis and Optimization." In *Proc. of the Design Verification Conference (DVCon)*, San José, CA, February 2008.
2. Jonas Rox and Rolf Ernst. "Modeling Event Stream Hierarchies with Hierarchical Event Models." In Proc. Design, Automation and Test in Europe (DATE 2008), March 2008.
3. Mircea Negrean, Simon Schliecker and Rolf Ernst, **"Response-Time Analysis of Arbitrarily Activated Tasks in Multiprocessor Systems with Shared Resources,"** in Proc. of Design, Automation, and Test in Europe (DATE), (Nice, France), April 2009
4. Simon Schliecker, Mircea Negrean and Rolf Ernst, **"Bounding the Shared Resource Load for the Performance Analysis of Multiprocessor Systems,"** in *Proc. of Design, Automation, and Test in Europe (DATE)*, (Dresden, Germany), March 2010
5. Mircea Negrean, Simon Schliecker and Rolf Ernst, "**Timing Implications of Sharing Resources in Multicore Real-Time Automotive Systems**," in *SAE World Congress*, vol. System Level Architecture Design Tools and Methods (AE318), (Detroit, MI, USA), April 2010 *(this paper was selected for SAE Journals – see next publication)*
6. Mircea Negrean, Simon Schliecker, and Rolf Ernst, **"Timing Implications of Sharing Resources in Multicore Real-Time Automotive Systems,"** *SAE International Journal of Passenger Cars - Electronic and Electrical Systems*, vol. 3, No. 1, pp. 27-40, August 2010 *(previous publication was selected for SAE Journals)*

-- Changes wrt Y2 deliverable --

Added four publications for Y3.

4.3.2 Tool: Analysis and optimisation framework for fault tolerant distributed embedded systems

Objectives

Linköping University and DTU are working on an environment and tool-set for the analysis and design optimisation of safety critical, fault tolerant real-time embedded applications. The emphasis is on the issue of transient faults and the goal is to develop tools for scheduling, mapping, and system optimisation.

Main results

A strategy for the synthesis of fault tolerant schedules has been developed. It can handle both hard and soft real-time tasks. The goal is to guarantee the deadlines for the hard processes even in the case of faults, while maximizing the overall utility. Time/utility functions are used to capture the utility of soft processes. Process re-execution is employed to recover from multiple faults. A single static schedule computed off-line is not fault tolerant and is pessimistic in terms of utility, while a purely online approach, which computes a new schedule every time a process

fails or completes, incurs an unacceptable overhead. Thus, a quasi-static scheduling strategy is used, where a set of schedules is synthesized off-line and, at run time, the scheduler will select the right schedule based on the occurrence of faults and the actual execution times of processes. An optimisation technique for the generation of schedule tables supporting such a quasi-static scheduling approach has been developed and implemented.

Current work

Ongoing work is towards development of cost-optimisation techniques by considering processors with various hardening levels and the associated tradeoffs.

During the second **year DTU** and **Linköping** have continued their cooperation related to the design and optimisation of fault tolerant mixed hard/soft real-time systems. During the second year the emphasis of the work has been on the analysis and optimisation of fault-tolerant hard real-time embedded systems, based on an approach in which hardware and software fault tolerance techniques are combined. The basic trade-off is between processor hardening in hardware and process re-execution in software which, together, have to provide the required levels of fault tolerance against transient faults with the lowest-possible system costs.

The goal for the third year is the development of new optimisation approaches for implementation of error detection techniques.

Participating partners

Linköping: Scheduling techniques, fault tolerant systems, design optimisation.

DTU: System level optimisation techniques

Publications

1. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Synthesis of Flexible Fault-Tolerant Schedules with Preemption for Mixed Soft and Hard Real-Time Systems”, 11th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN (DSD 2008), Parma, Italy, September 3-5, 2008, pp. 71-80.
2. Petru Eles, Viacheslav Izosimov, Paul Pop, Zebo Peng, “Synthesis of Fault-Tolerant Embedded Systems”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1117-1122.
3. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Scheduling of Fault-Tolerant Embedded Systems with Soft and Hard Timing Constraints”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, 915-920.
4. P. Pop, V. Izosimov, P. Eles, and Z. Peng. Design Optimization of Time- and Cost-Constrained Fault-Tolerant Embedded Systems with Checkpointing and Replication. IEEE Transactions on Very Large Scale Integrated (VLSI) Systems, 17(3):389-402. 2009.
5. V. Izosimov, I. Polian, P. Pop, P. Eles, and Z. Peng. Analysis and Optimization of Fault-Tolerant Embedded Systems with Hardened Processors. Proceedings of DATE: Design Automation and Test in Europe, IEEE, 2009, pp. 682 – 687.Tool or Platform :

-- Changes wrt Y2 deliverable --

No changes with respect to Year 2.

4.3.3 Tool: MPMH – an integration of MPA parallelization assistant and MH static memory allocation for MPSoC

Objectives

The main objectives of the framework is to offer an automatic source code parallelization (MPA tool) and memory hierarchy management (MH tool) in order to map efficiently embedded software application on MPSoC platforms. In order to tackle MPSoC programming issues in a MPSoC platform in an efficient way, a single tool performing optimized memory allocation (MH) and parallelizing sequential code (MPA) is an ideal solution. This tool suite is also used in the Platform and MPSoC Design cluster.

Main Results

The following challenges appear when integrating MPA and MH:
• information flow between MPA and MH
• interference between analyses and transformations of both tools
• MPA is not platform-aware and as a result may ruin the benefits obtained by MH
• profiling information (sequential) is hard to match with the parallelized code
• no optimization interactions between MPA and MH possible with the present implementation.

The integrated MPMH tool addresses these challenges and performs common data analyses from both tools, dependent on the Atomium Analysis framework, only once.

Current work

Currently, the affiliated partners of IMEC (ie, DUTH/ICCS and TU/e) and core partners (TUDortmund/ICD and KTH) are trying to integrate their tool and design flows with the IMEC MPA + MH MPSoC mapping framework in the memory and interconnect specific context of the MNEMEE and MOSART FP7 projects, respectively.

Participating partners:

- DUTH/ICCS
  This partner is integrating the dynamic data type and dynamic memory management tools and design flows with the IMEC MPSoC mapping tool flows.
- TUDortmund/ICD
  This partner is integrating its pre-compiler and compiler framework to the static MH tool of IMEC.
- TU/e
  This partner is integrating its SDF3 framework in the context of system scenarios with the IMEC MPSoC mapping tool flows.
- KTH
  This partner is integrating its NoC simulation and exploration framework with the MPA tool of IMEC.

Web

http://www.mnemee.org/
http://www.mosart-project.org/

Related Publications

Daniel Cordes, Peter Marwedel, and Arindam Mallik. Automatic Parallelization of Embedded Software Using Hierarchical Task Graphs and Integer Linear Programming. In *Proceedings of CODES+ISSS, 2010)*, Scottsdale / US, October 2010. (Also reported in the SSCGTA Cluster deliverable)

-- Changes wrt Y2 deliverable --

Text is updated.

4.3.4 Tool: MoVES - Modelling and Verification of Embedded Systems

Objectives

The MoVES framework is being developed to assist in the early phases of embedded systems design. The framework can be used to conduct schedulability analysis and has the potential to reason about different types of resource usage such as memory usage and power consumption.

Main Results

In several projects (MoDES, DaNES, ARTIST2, ArtistDesign) a model-based approach to analysis of embedded systems has been analyzed. This has resultet in the MoVES framework, which is now available online. The framework consists of a model- and a trace generator. From a system specification MoVES builds a model suitable for verification using an external verification back-end. In the case of e.g. verified non-schedulability, the trace generator provides the user with an understandable trace that leads to a missed deadline of the system.

Current work

The current version of the framework is based on a simple specification language where a system is modelled as an application running on an execution platform. The application is modelled through the individual tasks, and the execution platform is modelled through the processing elements, including the operating systems, and their interconnections. The tasks and processing elements are characterized by their real-time properties. Currently, verification can be conducted using two different verification back-ends, a) the original Uppaal model-checker for timed-automata models and b) a developmental Uppaal model-checker for stop-watch automata.

Participating partners:

- DTU: Provides the MoVES development environment.
- AAU: Provides the UPPAAL verification engine

Web

http://www.imm.dtu.dk/moves

Related Publications

1. Aske Brekling, Michael R. Hansen, Jan Madsen, MoVES - A Framework for Modelling and Verifying Embedded Systems, The 21st International Conference on Microelectronics, Marrakech, Morocco, 2009
2. Jan Madsen, Michael R. Hansen, Aske W. Brekling, A Modelling and Analysis Framework for Embedded Systems, Model-Based Design of Heterogeneous Embedded Systems, CRC Press, 2009
3. Aske Brekling, Michael R. Hansen, Jan Madsen, Analysis of Quantitative Properties of Hardware Specifications, The 21st Nordic Workshop on Programming Theory, Technical University of Denmark, 2009

-- Changes wrt Y2 deliverable --

No changes with respect to Year 2.

4.3.5 Tool: MPA (Modular Performance Analysis)

Objectives

The tool MPA (modular performance analysis) is based on an extension of network calculus that is termed real-time calculus (RTC). The purpose of the tool is to perform an end-to-end real-time analysis of complex distributed embedded systems. The implementation is based on a Java mathematical library for max-+ algebra with an associated Matlab interface.

Main Results

Within ARTISTDesign, the MPA tool box has been (a) extended towards the new results together with University Braunschweig (TUBS) related to hierarchical event streams and (b) it has been linked to the Symta/S tool suite as described above. In addition, the toolbox has been used in the context of various application studies from avionic and automotive domain.

Current work

We are currently working towards linking the toolbox to other performance analysis frameworks, e.g. UPPAAL from Uppsala University (Wang Yi, Bengt Jonsson). Some first promising results are available already. In addition, we are intending to use the method to investigate the interaction between memory access and computations in MPSoC platforms. This will be continued together with University Saarland (Reinhard Wilhelm).

Participating partners

ETHZ: Provides and maintains the MPA toolbox

TUBS: Link to the Symta/S tool suite, development of algorithms and methods for hierarchical event stream analysis.

Web

http://www.mpa.ethz.ch/

Related Publications

ETHZ: Kai Lampka, Simon Perathoner, Lothar Thiele: Analytic Real-Time Analysis and Timed Automata: A Hybrid Method for Analyzing Embedded Real-Time Systems. 8th ACM & IEEE International conference on Embedded software, EMSOFT 2009, CD edition, ACM, Grenoble, France, pages 107-116, October, 2009.

ETHZ: Lothar Thiele, Nikolay Stoimenov: Modular Performance Analysis of Cyclic Dataflow Graphs. EMSOFT 09: Proceedings of the 9th ACM international conference on Embedded software, Grenoble, France, pages 127-136, October, 2009.

ETHZ & TUBS: Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, Vol. 13, No. 1, pages 27-49, June, 2009.

ETHZ & TUBS: Simon Perathoner, Tobias Rein, Lothar Thiele, Kai Lampka and Jonas Rox: Modeling Structured Event Streams in System Level Performance Analysis, submitted to Conference on Languages, Compilers, and Tools for Embedded Systems LCTES, Stockholm, Sweden, April 2010

-- Changes wrt Y2 deliverable --

No changes with respect to Year 2.

4.3.6 Tool: DOL (Distributed Operation Layer)

Objectives

The DOL environment is a complete high-level compilation environment for MPSoC platforms. It consists of a graphical input specification interface for (a) application and (b) platform, a link to analytic performance analysis based on MPA, a simulation environment based on MPARM (Univeristy Bologna, Luca Benini) and a multi-objective optimization environment based on PISA (http://www.tik.ethz.ch/~sop/pisa/) for mapping (binding of application components to computation resources and communication links to paths on the platform). The environment has been successfully used to map complex applications to various platforms such as IBM Cell, MPARM (UNIBO) and ATMEL Diopsys.

Main Results

In the framework of ARTISTDesign, the DOL environment has been successfully linked and coupled to the MPARM simulation and design environment from University Bologna. This way, DOL could be used for ARM-based MPSoC architectures and extended with a state-of-the-art simulation environment. Main results are the comparison of analytic performance analysis with simulation-based performance numbers.

Current work

In the future, the coupling between MPARM and DOL will be used in order to investigate new concepts for predictable and efficient communication fabrics, including intelligent DMA controllers, scratchpad memories and flexible TDMA scheduling policies.

Participating Partners

ETH: Provides the DOL software development environment.

UNIBO: Provides the MPARM environment, including simulation capabilities and new concepts for predictable communication fabrics.

Web

http://www.tik.ee.ethz.ch/~shapes/dol.html

Related Publications

W. Haid, K. Huang, I. Bacivarov, and L. Thiele. Multiprocessor SoC Software Design Flows. IEEE Signal Processing Magazine, vol. 26, no. 6, pp. 64—71, Nov. 2009.

W. Haid, L. Schor, K. Huang, I. Bacivarov, and L. Thiele. Efficient Execution of Kahn Process Networks on Multi-Processor Systems Using Protothreads and Windowed FIFOs. In Proc. IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia), pages 35—44, Grenoble, France, Oct. 2009.

W. Haid, M. Keller, K. Huang, I. Bacivarov, and L. Thiele. Generation and Calibration of Compositional Performance Analysis Models for Multi-Processor Systems. In Proc. Int'l Conf. on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS), pages 92—99, Samos, Greece, July 2009. Awarded the Stamatis Vassiliadis Best Paper Award.

K. Huang, I. Bacivarov, J. Liu, and W. Haid. A Modular Fast Simulation Framework for Stream-Oriented MPSoC. In IEEE Symposium on Industrial Embedded Systems (SIES), pages 74—81, Lausanne, Switzerland, July 2009.

-- Changes wrt Y2 deliverable --

No changes with respect to Year 2.

4.3.7 Platform: Multicore Network on Chip Platform (McNoC)

Objectives

KTH is developing a comlete multi-core platform based on an NoC with a distributed and shared/private memory system.

Main results

A communication network with adaptive routing has been developed. Also, a programmable controller for memory and data management, called Data Management Engine (DME), has been developed and implemented. The DME, together with the Leon3 processor is part of every node. It manages the local memory and provides access to remote and off-chip memory. Furthermore, a dynamically configurable globally ratio-chronous-locally synchrounous clocking has been integrated. Finally a hierarchical power management scheme is part of the platform. The platform is modeld in Verilog/VHDL.

On the DME (as DME microcode) a cache coherency schem, several memory consistency models, a virtual address space support, and a dynamic memory allocation library has been implemented.

Current work

Ongoing work focuses on scalable and distributed cache coherency algorithms, that can by used for heterogeneous SoCs. Of particular interest are coherence mechanisms that can integrate different local cache controllers and policies in the different nodes.

Participating partners:

KTH working on the overall platform development

NTUA in Athens on dynamic memory allocation;

partners outside the NoE: NUDT, China on DME hardware.

Publications:

1. Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen, "Supporting Distributed Shared Memory on Multi-core Network-on-Chips Using a Dual Microcoded Controller", Proceedings of the confernece for Design Automation and Test in Europe, Dresden, Germany, March 2010.
2. Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen, "Supporting Efficient Synchronization in Multi-core NoCs Using Dynamic Buffer Allocation Technique", Proceedings of the IEEE Annual Symposium on VLSI, Kefalonia, Greece, July 2010.
3. Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen, "Handling Shared Variable Synchronization in Multi-core Network-on-Chip with Distributed Memory", International SOC Conference, Las Vegas, Nevada, September 2010.
4. Xiaowen Chen, Shuming Chen, Zhonghai Lu, and Axel Jantsch, "Area and Performance Optimization of Barrier Synchronization on Multi-core Network-on-Chips", 3rd IEEE International Conference on Computer and Electrical Engineering (ICCEE), Chengdu, China, November 2010.
5. Xiaowen Chen, Zhonghai Lu, Shuming Chen, and Axel Jantsch, "Run-time Partitioning of Hybrid Distributed Shared Memory on Multi-core Network-on-Chips", The 3rd IEEE International Symposium on Parallel Architectures, Algorithms and Programming (PAAP 2010), Dalian, China, December 2010.
6. Xiaowen Chen, Shuming Chen, Zhonghai Lu, and Axel Jantsch, "Multi-FPGA Implementation of a Network-on-Chip Based Many-core Architecture with Fast Barrier Synchronization Mechanism", Proceedings of the IEEE Norchip Conference, Tampere, Finland, November 2010.
7. Bernard Candaele, Sylvain Aguirre, Michel Sarlotte, Iraklis Anagnostopoulos, Sotirios Xydis, Alexandros Bartzas, Dimitris Bekiaris, Dimitrios Soudris, Zhonghai Lu, Xiaowen Chen, Jean-Michel Chabloz, Ahmed Hemani, Axel Jantsch, Geert Vanmeerbeeck, Jari Kreku, Kari Tiensyrja, Fragkiskos Ieromnimon, Dimitrios Kritharidis, Andreas Wiefrink, Bart Vanthournout, and Philippe Martin, "Mapping Optimisation for Scalable multi-core ARchiTecture: The MOSART approach", Proceedings of the IEEE Annual Symposium on VLSI, Kefalonia, Greece, July 2010.
8. Abdul Naeem, Xiaowen Chen, Zhonghai Lu, and Axel Jantsch, "Scalability of Weak Consistency in NoC based Multicore Architectures", Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS), Paris, France, June 2010.

-- Changes wrt Y2 deliverable --

New tool and text, not presented in Y2.

4.3.8 Tool: Formal System Design (ForSyDe)

Objective:

A modelling framework for heterogeneous SoC that allows to model HW and SW at different timing abstractions from continuous time to untimed. The semantic is formally defined and is the basis for formal design transformations, analysis, and synthesis.

Main results

The modelling framework has been defined and experimental implementation has been implemented in Haskell. It support continuous timed, discrete timed, synchronous and untimed Models of Computation. A VHDL back-end supports synthesis of synchronous models into HW. Several design transformations have been formulated and realized.

Current work:

Ongoing work focuses on reformulating the discrete timed MoC for more efficient modelling, Also, the framework is being implemented in SystemC as a set of templates and modelling rules.

Participating partners:

KTH: works on the SystemC implementation

DTU: focuses on the discrete timed MoC

Publications:

1. Jun Zhu, Ingo Sander, and Axel Jantsch, "Performance analysis of reconfigurations in adaptive real-time streaming applications", ACM Transactions in Embedded Computing Systems -- Special issue on Embedded Systems for Real-time Multimedia, 2010.
2. Jun Zhu, Ingo Sander, and Axel Jantsch, "Pareto Efficient Design for Reconfigurable Streaming Applications on CPU/FPGAs", Proceedings of Design Automation and Test in Europe (DATE '10), Dresden, Germany, March 2010.
3. Jun Zhu, Ingo Sander, and Axel Jantsch, "Constrained Global Scheduling of Streaming Applications on MPSoCs", Proceedings of the conference on Asia South Pacific Design Automation (ASP-DAC '10), Taipei, Republic of China, January 2010.
4. Jun Zhu, Ingo Sander, and Axel Jantsch, "HetMoC: Heterogeneous Modeling in SystemC", Proceedings of the Forum on Design Langauges (FDL), Southhampton, UK, September 2010.

-- Changes wrt Y2 deliverable --

New tool and text, not presented in Y2.

4.4 Design for Adaptivity Transversal Activity

4.4.1 SWEET (SWEdish Execution Time tool)

Objectives

SWEET is a WCET analysis tool. It is an academic prototype: the main objective is to use it as a test bench for methods in WCET analysis, and then mainly flow analysis to produce program flow constraints (upper bounds on # of loop iterations, information about infeasible paths, etc.).

Main Results

SWEET has been used to develop and test various methods for constraining program flow. It has also been used in industrial case studies. The results indicate that the developed methods do improve on the number of automatically detected program flow constraints, as well as on the precision of the resulting WCET bound. Recently, SWEET has been reengineered to use the "ALF" format for its flow analysis, and it has been provided with backends to generate program flow constraints for the commercial WCET analysis tools aiT and RapiTime from AbsInt GmbH and Rapita Systems Ltd, respectively. Translators to ALF from C, and the PPC and NECV850 binary formats, have been implemented as well.

Current work

A version of SWEET that performs parametric WCET analysis is currently being implemented. An alternative C-to-ALF translator, which uses the LLVM compiler framework, is also under implementation.

Participating partners:

- Mälardalen University
  Maintains and develops SWEET, develops methods for parametric WCET analysis.
- Saarland University
  Collaboration partner for parametric WCET analysis.

Web

http://www.mrtc.mdh.se/projects/wcet/sweet.html

4.4.2 Hardware setup to demonstrate self-protection and adaptability of embedded Real-Time Systems

Objectives

A demonstrator for self-protection and adaptability in real-time systems is being developed. It demonstrates the feasibility and cost of run-time adaptation and protection with respect to performance metrics such as end-to-end latencies. Furthermore, the demonstrator acts as a platform to evaluate performance of the proposed methodologies.

Main Results

The demonstrator consisting of a timing sensitive control application as well as a second disturbing application (audio streaming) has been completed and is used to show self-protection (audio streaming is denied access to the system) as well as self-configuration using the optimization techniques developed last year (audio streaming is allowed at low priority).

The demonstrator has been extended by a memory protection scheme using the available MMU of the PPC603e core, which efficiently isolates the runtime environment from user applications as well as user applications from each other.

Participating partners:

- TU Braunschweig
- Symtavision GmbH
- Universität Erlangen

Related Publications

Moritz Neukirchner, Steffen Stein, Harald Schrom and Rolf Ernst. A software Update Service with Self-Protection Capabilities. In Proceedings of the conference on Design, Automation and Test in Europe (DATE), Dresden, Germany, March 2010

4.4.3 TrueTime

Objectives

To provide a flexible simulation platform for networked embedded real-time systems with a particular focus on control applications. TrueTime implements simulation models for a multi-tasking real-time kernel and data link layer network protocols that execute embedded in the Matlab/Simulink environment. Using TrueTime it is possible to experiment with adaptive resource management and network protocols and investigate how this influence application performance.

Main Results

TrueTime has been continuously developed since 1999. During Y3 three new versions have been released:

- 2010-05-06 – TrueTime 2.0 Beta 5 was released. Changes to allow TrueTime to compile under Matlab R2009 and under Mac OS X.
- .2010-06-10 - **TrueTime Network for Modelica** was released.Two versions have been developed -- one based on an external C code implementation for the Dymola simulation tool and one based on native Modelica.
- 2010-07-16 – TrueTime 2.0 Beta 6 was released. Added support for the Network Code Machine by Sebastian Fischmeister et al.

Current work

The current not yet released development version also supports partitioned multicore scheduling and hierarchical schedulers. This is currently being used in the ACTORS project.

Participating partners:

- ULUND
  Toolbox development.
- SSSA, TUKL, Aveiro, KTH ...
  Users of the toolbox

Web

http://www.control.lth.se/truetime/

4.4.4 Other Tools and Platforms

BACC: Budget ACCountant (UPM)

BACC is a module for resource management, with low-level means for dynamic adaptation.The implementation has been adapted to the latest versions of the Linux kernel.It has been added support for multi-core architectures.

-- Changes wrt Y2 deliverable --

The text above only contains the tools / platforms for which something significant has changed with respect to Year 2. Tools such as SHARK, ERIKA or ForSyDe mentioned in the Year 1 and 2 deliverables are still of relevance to this activity.

4.5 Design for Predictability Transversal Activity

4.5.1 Tool or Platform: aiT

Objectives

aiT is the leading tool for computing worst case execution times (WCETs).

Main Results

A prototype implementation of the UCB computation as developed by Saarland University has been integrated by AbsInt into the aiT Timing Analyzer. The analysis is implemented for the ARM7 and has been tested on smaller benchmark programs.

Current work

Current work is concerned with optimising the performance of the analysis and exploring its potential on larger examples. Implementations for other processors are also underway.

Web
http://www.absint.com

4.5.2 Tool or Platform: WCC

Objectives

WCC is the leading WCET-aware compiler. The WCET analyzer aiT has been tightly integrated into the compiler.

Main Results

In the course of ArtistDesign, WCC has matured and is currently evaluated in an industrial context. WCC's single-task WCET-aware optimizations developed during ArtistDesign are able to outperform well-established compilers like e.g. the GCC. First steps towards WCET-aware compilation for multi-task systems are made, more work in this area and towards support of multi-core systems will be done in the near future.

Current work

The current work explores the optimization potential of WCC and extends it towards multi-task and multi-core systems.

Participating partners:

- TU Dortmund
  TU Dortmund integrates aiT into WCC and explores the optimization potential.
- AbsInt, Saarbrücken
  AbsInt provides aiT.

Web
http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/

Related Publications

[LSMM10] P. Lokuciejewski, M. Stolpe, K. Morik and P. Marwedel. *Automatic Selection of Machine Learning Models for WCET-aware Compiler Heuristic Generation*. In Proceedings of SMART '10: 4th Workshop on Statistical and Machine Learning Approaches to Architectures and Compilation, January 2010, pp. 3-17.

[PLM10] S. Plazar, P. Lokuciejewski and P. Marwedel. *WCET-driven Cache-aware Memory Content Selection*. In Proceedings of ISORC '10: 13th IEEE International Symposium on Object/Component/Service-oriented Real-time Distributed Computing, May 2010, pp. 107-114.

[LPFM+10a] P. Lokuciejewski, S. Plazar, H. Falk, P. Marwedel and L. Thiele. *Multi-Objective Exploration of Compiler Optimizations for Real-Time Systems*. In Proceedings of ISORC '10: 13th IEEE International Symposium on Object/Component/Service-oriented Real-time Distributed Computing, May 2010, pp. 115-122.

[LKM10] P. Lokuciejewski, T. Kelter and P. Marwedel. *Superblock-Based Source Code Optimizations for WCET Reduction*. In Proceedings of ICESS '10: 7th International Conference on Embedded Software and Systems, June 2010, pp. 1918-1925.

[FaLo10] H. Falk and P. Lokuciejewski. *A compiler framework for the reduction of worst-case execution times*. In The International Journal of Time-Critical Computing Systems (Real-Time Systems), 46(2):251-300, Springer, October 2010.

[LoMa10] P. Lokuciejewski and P. Marwedel. *Worst-Case Execution Time Aware Compilation Techniques for Real-Time Systems*. Springer, November 2010.

4.5.3 Tool or Platform : MAST

Objectives

The main objective of MAST is to provide a model to describe the timing behaviour of real-time applications, in such a way that automatic schedulability analysis can be performed to assess the ability of the application to meet all of its timing requirements. Also an objective is that this real-time model can be obtained from a more detailed design model described, for instance, in MARTE, the UML profile for real-time embedded systems.

Main Results

MAST defines a model to describe the timing behaviour of real-time systems designed to be analysable via schedulability analysis techniques. MAST also provides an open-source set of tools to perform schedulability analysis or other timing analysis, with the goal of assessing whether the system will be able to meet its timing requirements, and, via sensitivity analysis, how far or close is the system from meeting its timing requirements. Tools are also provided to help the designer in the assignment of scheduling parameters. By having an explicit model of the system and automatic analysis tools it is also possible to perform design space exploration. A discrete event simulator is also provided to obtain statistical performance information of the modelled system.

Current work

The original MAST model is now being enhanced to accommodate new modelling capabilities, partition-based scheduling as one of the base policies to use in the hierarchical scheduling modelling capabilities, support for clock synchronization, and support for resource reservation techniques. The new model is called MAST-2. The discrete event simulator has been redesign to accommodate the new MAST-2 model, and the schedulability analysis tools are being updated.

Participating partners:

- University of Cantabria

Web

http://mast.unican.es/

4.5.4 Tool or Platform : MPA (Modular Performance Analysis)

Objectives

The tool MPA (modular performance analysis) is based on an extension of network calculus that is termed real-time calculus (RTC). The purpose of the tool is to perform an end-to-end real-time analysis of complex distributed embedded systems. The implementation is based on a Java mathematical library for max-+ algebra with an associated Matlab interface.

Main Results

Within ARTISTDesign, the MPA tool box has been (a) extended towards the new results together with University Braunschweig (TUBS) related to hierarchical event streams and (b) it

has been linked to the Symta/S tool suite as described above. In addition, the toolbox has been used in the context of various application studies from avionic and automotive domain.

Current work

We are currently working towards linking the toolbox to other performance analysis frameworks, e.g. UPPAAL from Uppsala University (Wang Yi, Bengt Jonsson). Some first promising results are available already. In addition, we are intending to use the method to investigate the interaction between memory access and computations in MPSoC platforms. This will be continued together with University Saarland (Reinhard Wilhelm).

Participating partners

ETHZ: Provides and maintains the MPA toolbox

TUBS: Link to the Symta/S tool suite, development of algorithms and methods for hierarchical event stream analysis.

Web

http://www.mpa.ethz.ch/

Related Publications

ETHZ: Kai Lampka, Simon Perathoner, Lothar Thiele: Analytic Real-Time Analysis and Timed Automata: A Hybrid Method for Analyzing Embedded Real-Time Systems. 8th ACM & IEEE International conference on Embedded software, EMSOFT 2009, CD edition, ACM, Grenoble, France, pages 107-116, October, 2009.

ETHZ: Lothar Thiele, Nikolay Stoimenov: Modular Performance Analysis of Cyclic Dataflow Graphs. EMSOFT 09: Proceedings of the 9th ACM international conference on Embedded software, Grenoble, France, pages 127-136, October, 2009.

ETHZ & TUBS: Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, Vol. 13, No. 1, pages 27-49, June, 2009.

ETHZ & TUBS: Simon Perathoner, Tobias Rein, Lothar Thiele, Kai Lampka and Jonas Rox: Modeling Structured Event Streams in System Level Performance Analysis, submitted to Conference on Languages, Compilers, and Tools for Embedded Systems LCTES, Stockholm, Sweden, April 2010

4.5.5 Tool or Platform : MPARM

Objectives
MPARM is a virtual SoC platform almost written in SystemC, which could be used to model both HW and SW of a system. The MPARM virtual platform is highly modular and capable of simulating at cycle-accurate level an entire MPSoC, including cores, L1 and L2 caches, L3 memories and system buses.

Current work
We are working on defining and implementing new ways to enhance the predictability of MPSoC systems. We will consider both SW and HW techniques, applied to the CPU, bus and memory sub-systems.

-- Changes wrt Y2 deliverable --

Some tool descriptions updated to reflect development

4.6 Integration Driven by Industrial Applications Transversal Activity

4.6.1 Tool or Platform: SymTA/S

Objectives

SymTA/S is a tool for the development and verification of embedded multiprocessor real-time systems. The existing technology is mainly suitable for event or time-driven systems with message passing as the main task interaction. The tool shall be extended to cover the timing implications of multicore processors, or multiprocessor-systems-on-chip.

Main Results

In several previous projects (funded by german DFG, “Sureal”, funded by german BMBF, ARTIST2, and others), the compositional analysis approach has been transferred into a tool framework which is now also commercially available. The available modelling options capture typical problems in todays automotive systems (CAN bus utilization, end-to-end deadlines,…). This addresses a growing need for formal methods in the industry. The topics currently under research (see below) address future problems which can be expected to become of increasing industrial interest in the future.

Current work

The research version of the tool framework is currently being developed into several new directions: Modeling of shared resources for multiprocessor-system-on-chips (see ArtistDesign Activity 6.2: Platform and MpSoC Analysis), the modelling of hierarchical event models (in the scope of the COMBEST project), the demonstrator platform for adaptive systems (see ArtistDesign 7.1: Design for Adaptivity), and the reliability analysis (as presented in Section 3.1 Technical Achievements of the Industry-driven integrtation activity 7.3). Besides the extension of the applicability into new domains driven by industrial applications, a major focus within ArtistDesign is the synergetic coupling of tools, as well as the corresponding development of models.

Participating partners:

- TU Braunschweig.

  TU Braunschweig investigates synergies in the coupling of methods and implements prototypical implementations of the research results.

- Symtavision GmbH.

  Symtavision is the commercial co-developer of the tool framework. A focus within ArtistDesign is the coupling of with other industrially available tools (such as aiT).

- ETHZ.

  Collaboration on the coupling of MPA and SymTA/S with respect to modelling of hierarchical event models.

- Absint GmbH.

  The aiT tool supplies task timing models, which are required for system level analysis.

Web

http://www.ida.ing.tu-bs.de/forschung/projekte/symtas/

http://www.symtavision.com/

Related Publications

- Simon Schliecker, Jonas Rox, Mircea Negrean, Kai Richter, Marek Jersak and Rolf Ernst, **"System Level Performance Analysis for Real-Time Automotive Multi-Core and Network Architectures,"***Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 28, No. 7, pp. 979-992, July 2009.
- Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst and Michael González Harbour, **"Influence of different abstractions on the performance analysis of distributed hard real-time systems,"** *Journal Design Automation for Embedded Systems*, vol. 13, No. 1, pp. 27-49, June 2009
- Mircea Negrean, Simon Schliecker and Rolf Ernst, **"Response-Time Analysis of Arbitrarily Activated Tasks in Multiprocessor Systems with Shared Resources,"** in *Proc. of Design, Automation, and Test in Europe (DATE)*, (Nice, France), April 2009

-- Changes wrt Y2 deliverable --

No change.

4.6.2 COSI

Objectives

COSI (Communication Synthesis Infrastructure) is a software framework for interconnect infrastructure analysis and synthesis

Main Results

The framework allows developing specialized flows and tools for communication synthesis as exemplified by the release of COSI-NOC (Communication Synthesis Infrastructure for Network-on-Chips), a software toolkit for the automatic synthesis of synchronous networks-on-chip based on the platform-based design paradigm, and by COSI-BAD, for building automation design.

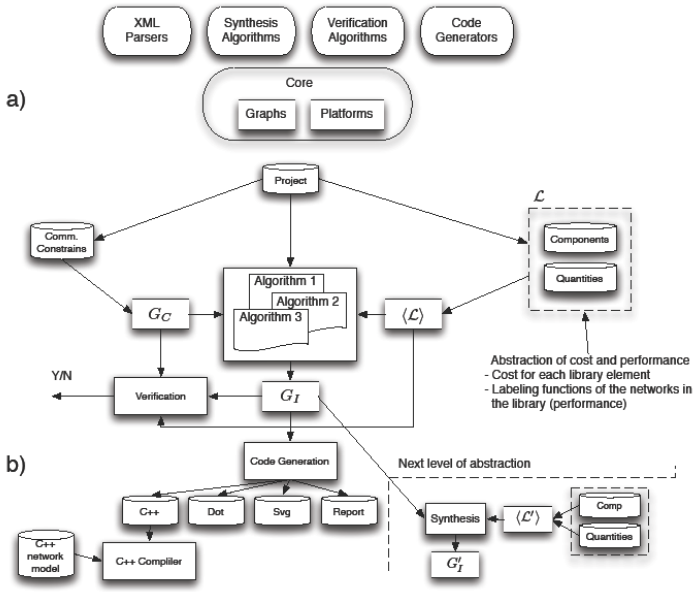


Figure 1. The COSI Platform-Based Design-like structure

	Quantities	CommStructs	Library	Models	Rules	Platforms	Environment	I/O	Algorithms
Core	Ports Bandwidth Flows...	Graphs							ShortestPath Tsp SpanningTree FacilityLocation Kmedian
On-Chip Communication	Interface IpGeometry NodeParam	Specification PltInstance Implementation	Router Link Bus	Ho-Area Ho-Power Orion	Critical length Deadlock	RouterLink BusNoc	Rectangle	Parsers SvgGen Parquet interface SyscGen	DegreeConstrained LatencyConstrained Hierarchical
Building Automation	Interface NodeParam Threads	Specification PltInstance Implementation	Sensor Actuator Controller TwistedPair	TokenRing 802.15.4	WiringRule NodePosition	DaisyChain TreeWireless	Walls CableLadder	BuildingParser SvgGen Desyre interface	DaisyChainPartition WirelessTree

Figure 2. How the COSI framework has been used to generate specific synthesis tools.

Current work

We continue to work towards expanding COSI capabilities, including better models for router delays, bus models, and support for the generation of synthesizable RTL description of the synthesized on-chip interconnection network. In this domain, we are integrating Metro with COSI. Meanwhile, we also plan to continue our work on the extension of the communication synthesis approach to the design of large-scale network for distributed embedded systems such as those that can be found in smart buildings and to airplane power distribution.

Participating partners:

- **Trento**
  Setting the directions of the framework. Methodology and theory. Integrating COSI with Metro.
- **UC Berkeley**
  Tool development and application to Network on Chip and intelligent buildings
- **Columbia**
  Participation in the development of the methodology.
- **UTC**

  Application to intelligent buildings and avionics.

Web
http://embedded.eecs.berkeley.edu/cosi/

Related Publications

[PCSV08] A. Pinto, L. Carloni and A. Sangiovanni Vincentelli, COSI: A Framework for the Design of Interconnection Networks, IEEE Design and Test of Computers, vol. 25, n. 5, Sept-Oct. 2008, pp. 402-415.

[PCVS09] A. Pinto, L.P. Carloni, and A. Sangiovanni-Vincentelli. "A Methodology for Constraint-Driven Synthesis of On-Chip Communications," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 28, No. 3, March 2009.

-- Changes wrt Y2 deliverable --

No change.

4.6.3 Metropolis and Metro II

Objectives

System-Level Design (SLD) means many different things to many different people. In our view, system-level design is about the design of a whole that consists of several components where specifications are given in terms of functionality with additional:

- constraints on the properties the design has to satisfy and on the components that are available for implementation and
- objective functions that express the desirable features of the design when completed.

This definition is general since it relates to many different application domains, from semiconductors to systems such as cars and airplanes, buildings, telecommunication and biological systems. To deal with system-level problems, our view is that the issue to address is not developing new tools, albeit they are essential to advance the state of the art in design, rather it is the understanding of the principles of system design, the necessary change to design methodologies and the dynamics of the supply chain. Developing this understanding is necessary to define a sound approach to the needs of the system and component industry as they try to serve their customers better, to develop their products faster and with higher quality.

Main Results

This contribution was about principles and how a unified methodology together with a supporting software framework, as challenging as it may seem, can be developed to bring the embedded electronics industry to a new level of efficiency. To demonstrate this view, we developed over the years Metropolis, a software framework supporting the methodology and Metro II, a second generation framework built to alleviate the problems we encountered when applying Metropolis to industrial test cases.

Current work

We are integrating this framework with the COSI framework to provide a full communication requirement capture, synthesis, verification and implementation. In parallel, we are interfacing Ptolemy to Metro II to offer a new way of entering designs using the graphical UI of Ptolemy II.

Participating partners:

- **Trento**

  Tool development, application of the framework to a UMTS case study.
- **UC Berkeley**

  Tool development, interface with Ptolemy II
- **Sun Microsystems**

  Application to multi-core development
- **UTC**

  Interface with COSI and application to smart buildings and avionics.
- **National Instruments**

  Industrial development of the ideas put forth by the frameworks
- **Intel**

Application to SoC design and development of architectural models

Web

http://chess.eecs.berkeley.edu/chess/forum/17.html

Related Publications

[DSDP09] D. Densmore, A. Simalatsar, A. Davare, R. Passerone, and A. Sangiovanni-Vincentelli. “UMTS MPSoC design evaluation using a system level design framework”. In *Proceedings of the Conference on Design, Automation and Test in Europe (DATE09)*, Nice, France, April 20-24, 2009.

[BDDD09] F. Balarin, A. Davare, M. D'Angelo, D. Densmore, T. Meyerowitz, R. Passerone, A. Pinto, A. Sangiovanni-Vincentelli, A. Simalatsar, Y. Watanabe, G. Yang and Q. Zhu. “Platform-Based Design and Frameworks: Metropolis and Metro II”. In *Model-Based Design for Embedded Systems,* chapter 10, page 259. CRC Press, Taylor and Francis Group, Boca Raton, London, New York, November 2009.

-- Changes wrt Y2 deliverable --

No changes with respect to Year2.

5. Assessment of the Workpackage at the end of Y3

This section needs to have the input from the Modeling and Validation cluster before it can be updated.

The ArtistDesign Network of Excellence is a significant evolutionary step for integrating the leading embedded systems design research teams in Europe.

The overall assessment for the WP at the end of ArtistDesign Y3 (Jan–Dec 2010) is very positive - both in terms of impact on the overall structuring and lasting integration within the consortium and more generally within the area in Europe.

- The ArtistDesign clusters have been actively pursuing operational integration through joint meetings, staff mobility, and shared platforms and tools.
- The level of activity shows that the Cluster / Activity structure and research topics defined for ArtistDesign make sense, and are viable vehicles for integrating the area. In operational terms, they generate sufficient interest for the partners and individual researchers to participate actively in the joint meetings, to exchange personnel, and to orient the tools and platforms developed to make sense within this structure.
- There is clearly a growing level of maturity for tools and platforms – and the partner teams are actively pursuing a policy of implementing tools, demontrators, and in many cases their accompanying methodologies.
- Nonetheless, it is important to remember that these are tools and platforms for research. The aim is not necessarily always for these to lead to commercially viable tools and start-up companies. In general, they are the concrete realisation of the state-of-the-research, allowing to explore possibilities for future research and later tools (some of which may in turn lead to commercially viable products).

In particular, we have had XX joint technical meetings, bringing together a wide audience. These meetings have covered a broad spectrum of topics, including XXXXXX.

The NoE has facilitated the mobility of YYYY researchers, for a total period of HHH in Year 2. This is widely considered to be the best way to integrated research teams, through the phyical transfer of persons and competencies. They lead to lasting collaboration and synergy.

The level of effort started in Year 1 has been maintained. We currently have XXX platforms developed in collaboration with ArtistDesign, covering the technical domains of the NoE.