Year 3 Review
Brussels, February 24th, 2010

Scientific Management

Achievements and Perspectives

ArtistDesign Network of Excellence

Joseph Sifakis, Bruno Bouyssounouse

VERIMAG Laboratory

artist Network of Excellence on Embedded Systems Design

ArtistDesign Year3 Review

Thursday February 24th 2011

9:00	**Project Officer & Reviewers' meeting**

ArtistDesign Review

9:30	**Project Officer's Introduction** *Rolf Riemenschneider (European Commission)*
9:35	**Scientific Management**
	Long-term Objectives and Status *Joseph Sifakis (UJF/VERIMAG)* *Bruno Bouyssounouse (UJF/VERIMAG)* ▸ NoE Principles of Construction ▸ Integration of the area ▸ Building Excellence
9:45	**Modeling and Validation Cluster**
	Achievements and Perspectives *Kim Larsen (Aalborg)* *Susanne Graf (UJF/Verimag)* ▸ Overall Aims and Achievements *(Integration, Building Excellence)* ▸ Overview of Scientific Highlights in Y3 ▸ Work planned for Y4
10:10	*discussion*
10:20	**SW Synthesis, Code Generation and Timing Analysis Cluster**
	Achievements and Perspectives - SW Synthesis, Code Generation *Peter Marwedel (Dortmund)* *Björn Lisper (Mälardalen)* ▸ Overall Aims and Achievements *(Integration, Building Excellence)* ▸ Overview of Scientific Highlights in Y3 ▸ Work planned for Y4
10:45	*discussion*
10:55	*break*
11:05	**Operating Systems and Networks Cluster**
	Achievements and Perspectives *Giorgio Buttazzo (Scuola Sant'Anna - Pisa)* *Alan Burns (York)* *Luis Almeida (U.Porto)* ▸ Overall Aims and Achievements *(Integration, Building Excellence)* ▸ Overview of Scientific Highlights in Y3 ▸ Work planned for Y4
11:30	*discussion*
11:40	**Hardware Platforms and MPSoC Design Cluster**
	Achievements and Perspectives *Jan Madsen (DTU)* *Luca Benini (Bologna)* *Lothar Thiele (ETHZ)* ▸ Overall Aims and Achievements *(Integration, Building Excellence)* ▸ Overview of Scientific Highlights in Y3 ▸ Work planned for Y4
12:05	*discussion*
12:15	*lunch*
13:30	**[Design for Adaptivity**
	Achievements and Perspectives *Karl-Erik Årzen (Lund)* ▸ Overall Aims and Achievements *(Integration, Building Excellence)* ▸ Overview of Scientific Highlights in Y3 ▸ Work planned for Y4
13:55	*discussion*
14:05	**Design for Predictability and Performance**
	Achievements and Perspectives *Bengt Jonsson (Uppsala)* ▸ Overall Aims and Achievements *(Integration, Building Excellence)* ▸ Overview of Scientific Highlights in Y3 ▸ Work planned for Y4
14:30	*discussion*

14:40	*break*
14:50	**Integration Driven by Industrial Applications**
	Achievements and Perspectives *Alberto Sangiovanni (TRENTO)* ▸ Overall Aims and Achievements *(Integration, Building Excellence)* ▸ Overview of Scientific Highlights in Y3 ▸ Work planned for Y4
15:15	*discussion*
15:25	**Spreading Excellence**
	Achievements and Perspectives *Bruno Bouyssounouse (UJF/VERIMAG)* ▸ Vision: Long-term impact ▸ ArtistDesign Web Portal ▸ Year 3 Events ▸ Events planned for Year 4
15:45	**Administration, Budget and Efforts**
	Bruno Bouyssounouse (UJF/VERIMAG) ▸ Principles / procedures ▸ Main efforts in Y3
	GLOBAL DISCUSSION (to be refined, timings to be adjusted)

Reviewer's Meeting

16:00	**Reviewer's Meeting**
17:00	**Conclusions and Feedback** *Project Officer and Reviewers*
17:30	closing

Reviewers' Recommendations

from the Y2 Review Report

Reviewer's Recommendations (1/10)

Recommendation 1:

Previous Y1-recommendation 2 is to be reconsidered.

The Common Technical Baseline is extremely promising. In fact, it would be useful considering extending its goal and scope, and creating an international activity patterned after the UMLS (Unified Medical Language System) in the medical field. (http://www.nih.gov/research/umls/). It could be an interesting topic for US-EU collaborative activities, and very beneficial for the educational organizations.

DONE

- The Common Technical Baseline is not part of the ArtistDesign DoW
- It has been financed by other means
- To ensure its viability a distinct business model is needed

Reviewer's Recommendations (2/10)

Recommendation 2:

Previous Y1-recommendation 3:
Concerning technical deliverable for Year 2 reporting period onwards and in order to avoid redundancy, we would like to propose the possibility of having just incremental documents containing what is new for that reporting period and referring to previous year's documents for the unchanged sections.
Taken into consideration mentioning the evolution or not of the content of paragraphs with respect to Y1 deliverables.
It would be beneficial having a standard presentation: The indication on what has changed between Y1 deliverable and Y2 deliverable would benefit to be always either at the beginning of the chapter (3.1.2) or at the end (3.2.1), as this eases clearly the analysis of the document.

DONE

- An incremental presentation of the results would be an incomplete picture and would be impossible to evaluate - Changes are indicated at the end of each section.
- The deliverables are all done along templates, according to the type of deliverable:
  i) Cluster deliverables, ii) activity deliverables, iii) transversal activity deliverables

Reviewer's Recommendations (3/10)

Recommendation 3:

Put emphasis on links on levers towards Industry standardization organizations, as this is a key lever to spread and get visibility and feedback on the works and achievements.

Preparing the future is a key task for Y3, so the good work and network will not fade away.

DONE

Partners are heavily engaged in standardization bodies:

- Programming Languages (ADA, Java RT, MARTE, SysML, META metalanguage)
  - York and ISEP participate to the Ada standardization process, and in the forthcoming ISO report on Vulnerabilities in Programming Languages
  - DTU and York are involved in the Real-Time Java standardization
  - University of Cantabria is involved in the POSIX real-time system services working group, in the SysML 1.3 Revision Task force and is responsible for two chapters in MARTE 2.1.
  - Trento is participating to the META II program for semantics metalanguage tu support system design
  - Catania is actively participating to IEC Technical Committee SC65C, WG17 -Coexistence in Wireless Industrial communication networks
- OFFIS is a development Partner of AUTOSAR subgroups of the Methodology Working Group Timing and Safety responsible to bring results from CESAR. TUB is an Attendee.
- KTH is part of the ARTEMIS-IA Tool Platforms Working Group which has as goal to harmonize long term efforts and standards on tool platforms across Artemis research

Reviewer's Recommendations (4/10)

Recommendation 4:

Presentations during the review meeting should be shorter, leaving more time for interaction.

DONE

Suggestion: 10 minutes for discussion after each presentation, instead of 5 last year.

Reviewer's Recommendations (5/10)

Recommendation 5:

About modelling and validation:

- Tool integration should go beyond individual projects; the team should at least formulate conditions for integrability
- One should think about the solution for "saving the tools" produced by the community as outcome of research

DONE

- Prerequisites
  - Individual tools need well-defined API's (syntax & semantics)
- Three approaches
  - Common Formats (standardization)
  - Gateways between tools
  - Derive global results from partial results produced by different tools
- Challenges for tools to survive
  - Industrial take-up
  - Lack of technical support for maturing/sustaining academic tools
  - Open source?
- Survival of the fittest

Reviewer's Recommendations (6/10)

Recommendation 6:

About Synthesis_Code_Generation_and_Timing_Analysis:

- There is a need for a vision for new generation of software synthesis and code generation tools,
- There should be a deeper integration of results inside the cluster,
  A better structured interface with other clusters (operating systems, hardware platforms, etc.) is welcome.

DONE

There has been increased emphasis on software synthesis:

- In addition to the 2nd workshop on software synthesis, partners worked on a special issue of the IEEE Journal on Industrial Informatics on software synthesis. Alberto Sangiovanni-Vincentelli, Peter Marwedel and Affiliate Soonhoi Ha temporarily became Associate Editors of this journal.
- A tighter integration of tools, for example from Dortmund, IMEC, Saarbrücken and Passau is available.
- In cooperation with the cluster on operating systems, timing analysis and worst case execution time aware compilation have been extended to include the analysis of multi-tasking.

Reviewer's Recommendations (7/10)

Recommendation 7:

In the framework of Operating Systems and Networks:

- It seems that increased interaction with the Modelling cluster would be beneficial. OS and network properties are essential for composition and verification, so the opportunity for interaction is there.

DONE

Some activity on modeling Operating Systems has already started in the cluster:

- Pisa and TUKL started collaborating (within the ACTORS project) to model the behavior of a resource manager that performs resource adaptation in multicore platforms.
- A model has been proposed by Pisa to abstract resource reservation for single and multicore platforms, which has been used by Ericsson to develop resource management for next generation cell phones.
- A workshop on Compositional Theory and Technology for Real-Time Embedded Systems has been organized by Pisa at RTSS 2010, with a Keynote Talk by Edward A. Lee, Professor at University of California, Berkeley, on "Compositional Timing in Concurrent, Parallel, and Distributed Real-Time Systems":
- CRTS 2010 - 3rd Workshop on Compositional Theory and Technology for Real-Time Embedded Systems November 30, 2010, San Diego, CA, USA (co-located with RTSS 2010) http://retis.sssup.it/crts2010/
- Research activity on modelling real-time systems will continue in the OSN cluster trying to establish a stronger connection with the Cluster on Modelling.

Reviewer's Recommendations (8/10)

Recommendation 8:

In the framework of hardware and MPSoC design:

- Increased interaction with software synthesis and code generation
- Approaches for platform modelling: how to do it to help software synthesis?

DONE

- The MPSoC cluster has increased its interaction with
  - the Software Synthesis and Code Generation cluster leading to joint work on parallelizing compilers (IMEC/Dortmund) and energy aware compilers (ETHZ/ Dortmund),
  - the RTOS cluster, leading to energy aware mapping based on multi-objective optimization (ETHZ/SSSA) and new scheduling techniques (UNIBO/SSSA).

- The MPSoC cluster has increased its focus on software synthesis support through runtime layers (CEA/UNIBO), execution/simulation environments (ETHZ/KTH/DTU) and MPSoC programming models (DTU).

Reviewer's Recommendations (9/10)

Recommendation 9:
Progress of the clusters design for adaptivity and predictability would be stimulated by writing an annual position paper about the new/emerging insights. This is a very complex issue and taking stock periodically of the status of current thinking would be very helpful not only for the cluster but also for the research community.

DONE

Design for Adaptivity

- Annual position paper is too ambitious. Instead, a White Paper / Survey will be written at the end of Y4 summarizing the work done within ArtistDesign and the experience gained
- Authors have been decided and an outline is available
- Main common activity for Y4

Design for Predictability

A technical paper will be written on timing predictability for single- and multiprocessor platforms. In connection with the PPES workshop at DATE. An outline is available.

Reviewer's Recommendations (10/10)

Recommendation 10:

ARTEMIS link is somewhat fuzzy. This should be improved or clarified.

DONE

ArtistDesign has strong links to ARTEMIS, through:

- Representation on the **ARTEMIS Industry Association Steering Board**:
  - Joseph Sifakis is the CNRS/CEA representative
  - Luca Benini is the University of Bologna representative
- Partner membership in **ARTEMIS "B" (Research Organisations & Universities)**
  - Representatives from ArtistDesign partners: Aalborg, CEA, CNRS-Verimag, ESI, IMEC, INRIA, Porto, KTH, OFFIS, TU Denmark, Cantabria, UJF.
- **Alberto Sangiovanni was one of the evaluators for ARTEMIS and ENIAC**
- **Strong informal links**.
  For example, the ArtistDesign Strategic Management Board was asked to review and comment on the latest edition of the Strategic Research Agenda, published in 2011.
- **Strong representation by ArtistDesign partners in ARTEMIS projects**:
  CESAR, SMECY, MBAT, RECOMP, iFEST, Encourage, ASAM, IoE, SysModel, Smart, Emmon, iLand, Symbeose, Scalopes, Indexys, Chiron

Overview of the NoE

Concepts and Objectives – Main Ideas

Main Idea 1

- *Embedded systems are essential to ensuring a leading position for Europe in key industrial sectors services.*
  This is well-recognized in the ICT FP7 priorities, and through the ARTEMIS ETP.

Main Idea 2

- *Embedded systems design is an emerging scientific discipline, mobilizing a large international community, around a set of fundamental challenging and multi-disciplinary problems.*
- *For this discipline to emerge, a considerable focused research effort by the best teams is needed.*

Objectives

Reinforce and strengthen scientific and technological excellence in Embedded Systems Design:

- The NoE acts as a Virtual Center of Excellence
- **Two levels** of integration
  to create critical mass from selected European teams
  - **Strong integration** within selected topics
    by assembling the best European teams,
    to advance the state of the art in the topic.
  - Integration **between** topics
    to achieve the multi-disciplinary excellence and skills required for the development of future embedded technologies.
- Integration is around a Joint Programme of Activities

Core Participants (1/2)

N°	Beneficiary name	Beneficiary short name	Country
1	UJF FILIALE	FLORALIS	France
2	UNIVERSITE JOSEPH FOURIER GRENOBLE 1	UJF/VERIMAG	France
3	AACHEN	AACHEN	Germany
4	AALBORG UNIVERSITET	AALBORG	Denmark
6	ALMA MATER STUDORIUM - UNIVERSITA DI BOLOGNA	BOLOGNA	Italy
7	TECHNISCHE UNIVERSITAET BRAUNSCHWEIG	TUBS	Germany
8	UNIVERSIDAD DE CANTABRIA	CANTABRIA	Spain
9	COMMISSARIAT À L'ENERGIE ATOMIQUE	CEA	France
10	DANMARKS TEKNISKE UNIVERSITET	DTU	Denmark
11	UNIVERSITAET DORTMUND	DORTMUND	Germany
12	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	EPFL	Switzerland
13	EMBEDDED SYSTEMS INSTITUTE	ESI	Netherlands
14	EIDGENOESSISCHE TECHNISCHE HOCHSCHULE ZUERICH	ETH Zurich	Switzerland
15	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	Belgium
16	INRIA	INRIA	France
17	TECHNISCHE UNIVERSITAET KAISERSLAUTERN	TUKL	Germany
18	KUNGLIGA TEKNIKA HOGSKOLAN	KTH	Sweden

Core Participants (2/2)

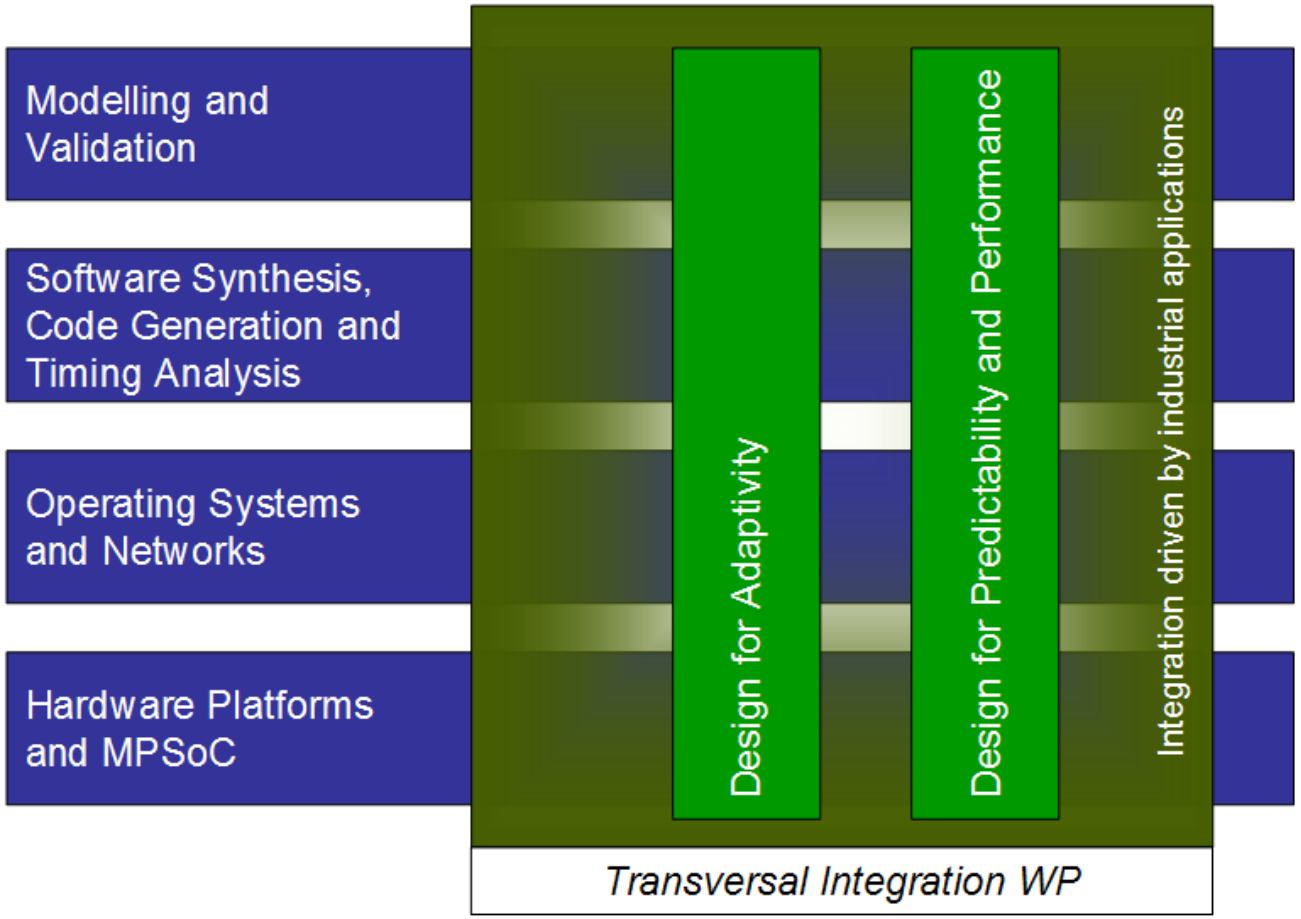
N°	Beneficiary name	Beneficiary short name	Country
19	LINKÖPINGS UNIVERSITET	LINKOPING	Sweden
20	LUNDS UNIVERSITET	ULUND	Sweden
21	MAELARDALENS HOEGSKOLA	MDH	Sweden
22	OFFIS E.V.	OFFIS	Germany
24	UNIVERSITAET PASSAU	PASSAU	Germany
25	SCUOLA SUPERIORE DI STUDI UNIVERSITARI E DI PERFEZIONAMENTO SANT'ANNA	SSSA-PISA	Italy
26	INSTITUTO SUPERIOR DE ENGENHARIA DO PORTO	PORTO	Portugal
27	UNIVERSITAET DES SAARLANDES	SAARLAND	Germany
28	UNIVERSITAET SALZBURG	PLU-SALZBURG	Austria
29	UPPSALA UNIVERSITET	UPPSALA	Sweden
30	TECHNISCHE UNIVERSITAET WIEN	VIENNA	Austria
31	UNIVERSITY OF YORK	YORK	UK
32	IST-AUSTRIA	IST-Austria	Austria
33	UNIVERSITY OF PORTO	UnivPorto	Portugal
34	UNIVERSITY OF TRENTO	TRENTO	Italy

Jointly-executed Programme of Research Activities (JPRA)

Clusters are autonomous entities, with specific objectives, teams, leaders, and a dedicated yearly budget.

The set of Thematic Clusters cover all the main topics in Embedded Systems Design. The thematic activities in the Transversal Integration workpackage focus on Design methodologies, with specific objectives (Predictability, Adaptivity).

Each cluster may have one or several Activities, as appropriate.



Theory, Methods and Tools for ES Design

Design flow involves topics leading from initial requirements to a final implementation satisfying them. The objective is to study specific needs for these design activities, as well the possibility of integrating them in a coherent design flow.

We distinguish four essential topics, for which existing techniques should be adapted and extended :

- **Modelling and Validation**: We need formal modelling techniques that take into account the characteristics of a system's external and execution environments. These techniques should support component-based construction for heterogeneous components to be applicable throughout the design process. For embedded systems, validation focuses on testing and verification of non functional properties, including performance and dependability.
- **Software Synthesis, Code Generation and Timing Analysis**: Strong integration should be sought for these interrelated topics. The aim is to study and implement resource-aware synthesis and code generation techniques. These techniques allow the generation of an implementation meeting given user requirements from a functional description of an application (e.g. application software) and a model of a target platform.
- **Real-Time Operating Systems Scheduling and Networks**: The aim is to develop theory methods and tools for new real-time software infrastructures, for the execution and communication between embedded applications. The main problems include adaptive resource management and dependability techniques, in particular to improve robustness to deviations from nominal conditions.
- **Platforms and MPSoC Design**: The aim is implementation of complex applications on multi-core HW platforms. It raises a number of problems for ensuring predictability and efficiency. These include adaptive techniques for resource management, and the study of reliable programming models for multi-core architectures.

Long Term Integration

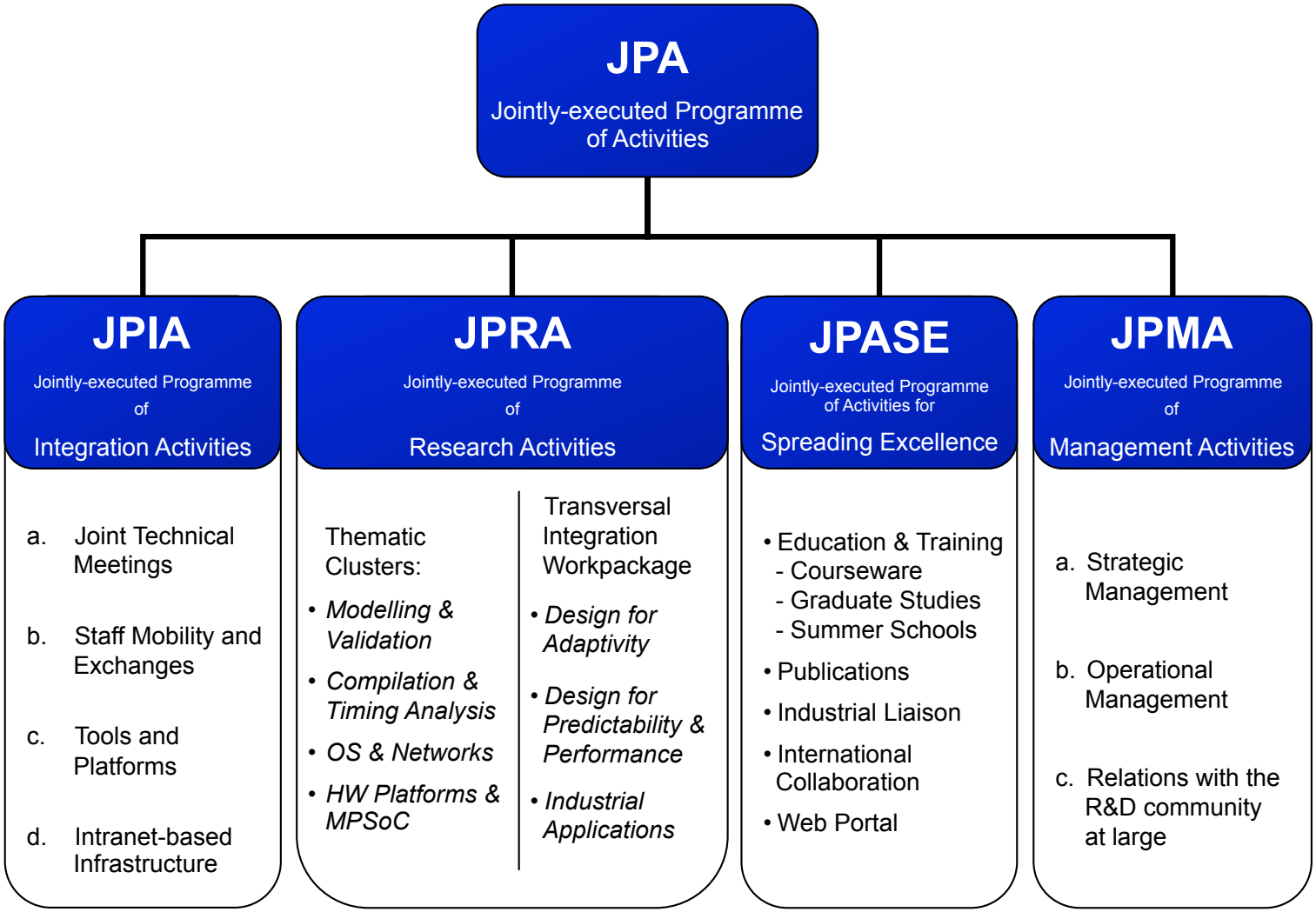
Embedded systems design is a multidisciplinary area requiring competences from hardware engineering, operating systems and networks, programming and compilation, modelling and software engineering, control engineering. The ArtistDesign NoE gathers together leading European teams from all these areas.

ArtistDesign continues and extends these activities, both quantitatively and qualitatively. In setting up the consortium, we have the right balance between critical mass, excellence, and commitment from the core partners.

- **Critical Mass**
  We have a sufficient number of partners, to achieve a fair coverage of the main topics in the area, as well as the capacity to impact the European research landscape. Nonetheless, to ensure efficiency, we have limited the number of core partners, based on previous experience. At the same time, our impact is amplified through the large number of affiliated academic, SME, industrial, and international collaboration partners.
- **Excellence**
  The ArtistDesign core partners include the main European leading teams, as attested by their leadership in their respective areas, as well as their strong involvement in national and European projects and initiatives.
- **Commitment**
  The majority of the ArtistDesign core partners were already involved as core partners in the Artist2 NoE. They have demonstrated a high degree of investment to achieve the workprogramme objectives, by committing the resources needed, which are an order of magnitude larger than those provided by the NoE financing. We estimate that the effort for implementing the JPA is roughly 10 times the financial contribution for integration.

Joint Programme of Activities

ArtistDesign acts as a Virtual Centre of Excellence, composed of a set of virtual teams, called clusters. Each cluster gathers together selected teams from partners, to create the critical mass and expertise in one of the essential topics for embedded systems design.



Jointly-executed Programme of Management Activities (JPMA)

- In order to ensure correct integration and coordination of activities, and coordination between the partners, the Consortium carries out a Joint Programme of Management Activities (JPMA). It includes:

  - **Strategic Management**
    The Strategic Management Board (SMB) plays a key role in ensuring ongoing integration at 3 levels: I) within the cluster; II) between clusters; III) with the larger European Embedded Systems Design community.

  - **Operational Management**
    is ensured by the ArtistDesign Office, and the Executive Management Board (composed of the Cluster Leaders). The ArtistDesign Office ensures that all aspects of the NoE are running smoothly, and that progress is made towards the overall NoE objectives. It is composed of the Scientific Coordinator, the Technical Coordinator, the Financial and Administrative Coordinator from Floralis.

  - **Relations with the R&D community at large**
    The NoE has a very strong presence within the embedded systems design community, at all levels. High-level interaction with the main institutions and bodies such as ARTEMIS/ ARTEMISIA, professional organisations such as ACM TECS, NSF, DARPA, large conferences, are ensured and supported by various members of the Strategic Management Board, and the Scientific and Technical Coordinators.

Jointly-executed Programme of Integrating Activities (JPIA)

- Each ArtistDesign research activity has work within both the JPIA and the JPRA workpackages. Funds for staff mobility are allocated by taking into account the needs for research.

  - **Joint Technical Meetings**
    Present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

  - **Staff Mobility and Exchanges**
    Mobility is justified by and refer to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

  - **Tools and Platforms**
    Research platforms lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. Some of these have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

Joint Programme of Activities for Spreading Excellence (JPASE)

These NoE-level activities serve as a relay between the NoE and the international embedded systems design community at large.

- **Education and Training**
  These actions serve as incubators for developing integrated curricula and materials, and to disseminate results and spread excellence well beyond the partners and affiliated partners of ArtistDesign.

- **Publications in Conferences and Journals**
  Implemented through publication in the main conferences on Embedded Systems Design of the area, as well as the active participation for the organization and management of these events.

- **Industrial Liaison**
  This consists of actions oriented towards affiliated industrial partners, to transfer results follow and get feedback on the research and integration activities in the JPA (JPRA, JPIA).

- **International Collaboration**
  These activities play a dual role: showcase the participants' results, and reinforce the NoE's leadership role worldwide. They will also collect relevant information about evolution of the state of the art outside Europe.

- **Web Portal**
  This plays a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large, and be an essential mechanism for achieving integration and recognition.

Workpackages

WP0	Jointly-executed Programme of **Management** Activities (JPMA)	MGT	Floralis
WP1	Jointly-executed Programme of **Integration Activities** (JPIA)	RTD	VERIMAG
WP2	Joint Programme of Activities for **Spreading Excellence** (JPASE)	OTHER	VERIMAG
WP3	Thematic Cluster: **Modeling and Validation** (JPRA) • *Activity: Modelling* • *Activity: Validation*	RTD	Aalborg + VERIMAG
WP4	Thematic Cluster: **Software Synthesis, Code Generation and Timing Analysis** (JPRA) • *Activity: Software Synthesis, Code Generation* • *Activity: Timing Analysis*	RTD	Dortmund
WP5	Thematic Cluster: **Operating Systems and Networks** (JPRA) • *Activity: Resource-Aware OS* • *Activity: Scheduling & Resource Mgt* • *Activity: Embedded RT Networking*	RTD	Pisa
WP6	Thematic Cluster: **Hardware Platforms and MPSoC** (JPRA) • *Activity: Platform and MPSoC Design* • *Activity: Platform and MPSoC Analysis*	RTD	DTU
WP7	**Transversal Integration** (JPRA) • *Activity: Design for Adaptivity* • *Activity: Design for Predictability and Performance* • *Activity: Integration Driven by Industrial Applications*	RTD	TRENTO

Thematic Cluster: Modeling and Validation

cluster leaders: Kim Larsen (Aalborg) + Susanne Graf (Verimag)

JPRA Activity: "Modeling"

Suzanne Graf (Verimag - France)

Develop model- and component-based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. Simultaneously address software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based.

JPRA Activity: "Validation"

Kim Larsen (Aalborg - Denmark)

Designing scalable techniques allowing for efficient and accurate analysis of performance and dependability issues with respect to the various types of (quantitative) models considered, covering a range of model-based validation techniques ranging from simulation, testing, model-checking, compositional techniques, refinement and abstract interpretation.

Thematic Cluster:

Software Synthesis, Code Generation and Timing Analysis

cluster leader:
Peter Marwedel (Dortmund)

JPRA Activity: "Software Synthesis, Code Generation "

Peter Marwedel (Dortmund - Germany)

Software generation has evolved to a level where compilers are key components, but not the only components that are useful for generating executable code. New models of computations such as data-flow based models aim at avoiding the well-known disadvantages of imperative programming styles. It can also be expected that the link between software engineering and embedded systems will become stronger.

JPRA Activity: "Timing Analysis"

Björn Lisper (Mälardalen - Sweden)

Timing analysis of MPSoC systems is a new scientific field, and is very timely from an application perspective as MPSoC and Multicore architectures rapidly are becoming mainstream. A research effort in this area will thus establish European dominance in a field that rapidly is becoming very important.

Thematic Cluster: Operating Systems and Networks

cluster leader:
Giorgio Buttazzo (Pisa - Italy)

JPRA Activity: "Resource-Aware Operating Systems" *Giorgio Buttazzo (Pisa - Italy)*

Investigate how RTOS have to be extended or modified to support emerging RT embedded systems (high complexity, highly variable resource requirements and parallel processing). Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, while guaranteeing isolation properties.

JPRA Activity: "Scheduling and Resource Management" *Alan Burns (York - UK)*

Provision of models of embedded platform resources and policies, and the necessary analysis for undertaking the run-time scheduling of these resources and policies. A key scientific challenge is to link this resource-centred analysis with models of the application (and their resource usage policies) and the performance profiles of the hardware platform itself.

JPRA Activity: "Real-Time Networks" *Luis Almeida (U. Aveiro – Portugal)*

This activity addresses numerous research challenges in the frameworks of Networked Embedded Systems (NESs), Wireless Sensor Networks (WSNs) and Mobile Ad-hoc Networks (MANETs).

Thematic Cluster: # Hardware Platforms and MPSoC

cluster leader:
Jan Madsen (DTU - Denmark)

JPRA Activity: "Platform and MPSoC Design"

Luca Benini (U. Bologna - Italy)

The main scientific challenges addressed in this activity are focused on how to map complex applications onto multi-core hardware platforms. This includes addressing allocation and scheduling issues like: scalability, flexibility, composability, predictability, design-time reduction and increased dynamism. The problem is complex and multi-faceted. On one hand, we have static (design/compile time) approaches, where applications are analyzed and optimal mapping decisions are taken before the platform is deployed in the field. On the other hand, we have dynamic, runt-time approaches where mapping decisions are taken online, and they are triggered by environmental and workload variations.

JPRA Activity: "Platform and MPSoC Analysis"

Jan Madsen (DTU - Denmark)

Establish a set of models and analysis methods that scales to massively parallel and heterogeneous multiprocessor architectures, is applicable to distributed embedded systems as well, allows for the analysis of global predictability and efficiency system properties and takes the available hardware resources and the corresponding sharing strategies into account.

Transversal Integration

WP leader:
Alberto Sangiovanni (Trento - Italy)

JPRA Activity: "Design for Adaptivity"

Karl-Erik Årzén (Lund University – Sweden)

An embedded hardware-software system is adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is required both off-line at design-time and on-line at run-time. Off-line adaptivity is required to handle changing system specifications and to support platform-based or product-family based development.

JPRA Activity: "Design for Predictability and Performance"

Bengt Jonsson (Uppsala - Sweden)

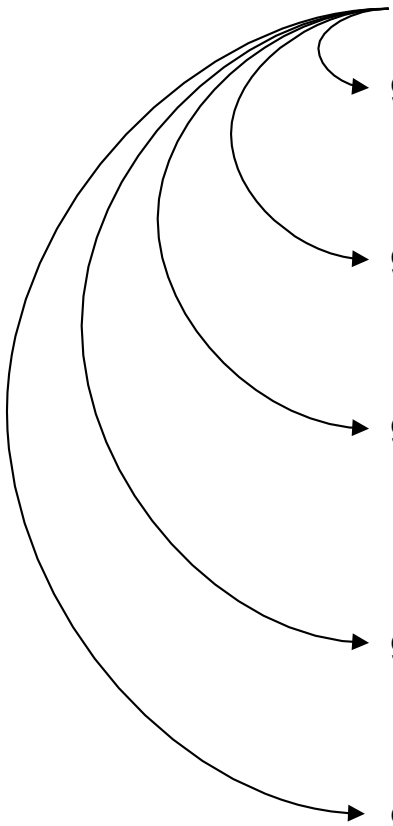
The technical achievements contribute to a suite of techniques across the abstraction levels of embedded system design, including application modelling and analysis, scheduling support, compilers, and platform design techniques. The achievements will also entail interfacing of existing tools for design of embedded systems.

JPRA Activity: "Integration Driven by Industrial Applications"

Alberto Sangiovanni (Trento – Italy)

The ultimate goal of this activity is to provide the "meta rules" according to which the design transformations are carried out and interfaces are built and hence to provide strong guidance to the clusters to make their results more relevant and applicable.

Budget



7% **WP0: Jointly-executed Programme of Management Activities (JPMA)**

36% **WP1: Jointly-executed Programme of Integration Activities (JPIA)**
- 12% Transversal Integration
- 6% Each Thematic Cluster

12% **WP2: Joint Programme of Activities for Spreading Excellence (JPASE)**

9% **WP3: JPRA/Thematic Cluster: Modeling and Validation**
- Activity: Modelling
- Activity: Validation

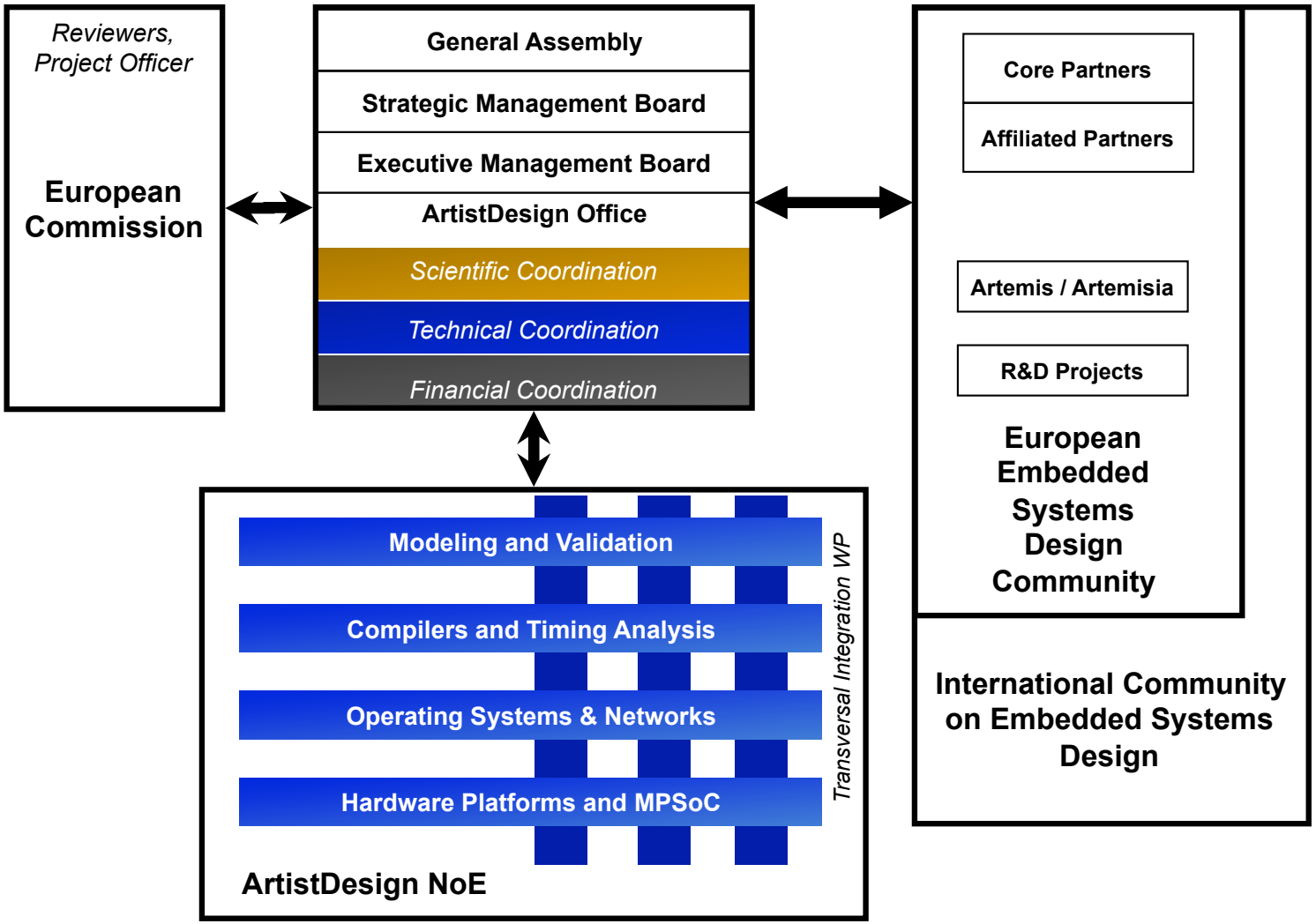
9% **WP4: JPRA/Thematic Cluster: Compilers and Timing Analysis**
- Activity: Software Synthesis and Code Generation for Embedded Systems
- Activity: Timing Analysis

9% **WP5: JPRA/Thematic Cluster: Operating Systems and Networks**
- Activity: Real-Time Operating Systems
- Activity: Scheduling and Resource Management
- Activity: Embedded Real-Time Networking

9% **WP6: JPRA/Thematic Cluster: Hardware Platforms and MPSoC**
- Activity: Execution Platform and MPSoC Analysis
- Activity: Platform and MPSoC Design

9% **WP7: Transversal Integration Activities**
- Activity: Design for Predictability
- Activity: Design for Adaptivity
- Industrial Integration

Management Structure



Summary of Main Achievements

Cluster: Modeling and Validation

Interaction and Research activities have progressed substantially :

- *Component Modeling and Compositional Validation*: compositional design and verification methodologies for functional, timing and stochastic aspect
  - Assume/guarantee reasoning, interface automata, modal transition systems for rich models.
  - Theoretical foundations and coordination languages have been developed for heterogeneous systems.
  - A framework for tool integration based on meta-models and model-transformations
- *Resource Modeling (of the Modeling Activity)*
  - design space exploration,
  - multi-core scheduling,
  - modelling paradigms for quantitative resources
  - platform models including transactional memory.
- *Quantitative Modeling (of the Modeling Activity)*
  - design frameworks for quantitative modeling, in particular weighted automata, priced timed automata and quantitative communication models.
  - synthesis of models guaranteeing quantitative properties.
- *Quantitative Validation:*
  - improved schedulability analyses supporting multiprocessor and multi-core applications
- *Cross-Layer Validation*
  - improved methods for model-based testing

Cluster: SW Synthesis, Code Gen and TA

Interaction and Research activities have progressed substantially :

- Tools: RWTH Aachen, IMEC, Erlangen-Nuremberg and Seoul National University
- WCET-aware compiler “WCC” (Dortmund, AbsInt, USAAR)
  extension towards multi-objective optimization
- Cache-aware scheduling (USAAR, SSSA).
- Contacts with MPSoC design strengthened.
- timing analysis of multicore systems with shared caches, and to bound the context switch penalty due to cache effects in preemptive systems
- analysis on micro-architectural level has progressed, especially regarding cache replacement policies and pipeline behaviour.
- automated derivation of timing models from VHDL specifications.
- generation of timing models from observations, based on machine learning and model identification.
- collaboration between TU Dortmund, AbsInt and OS&NW cluster
  new link between reliability, compilers, operating systems and real-time systems.

2nd edition of the textbook on embedded systems by P. Marwedel

Cluster: Operating Systems and Networks (1/2)

Interaction and Research activities have progressed substantially :

- UNIBO-predictability and modularity of MPSoC for Real-Time applications.
- USAAR, PISA, Dortmund, AbsInt: improve estimation of WCET considering cache-aware scheduling and WCET-aware compilers.
- EVIDENCE-PISA: introduce resource reservation and deadline-based scheduling (EDF) into Linux enabling the implementation of advanced resource reservations techniques.
- LUND-TUKL-PISA: developed a design framework for partitioning real-time applications on multicore heterogeneous systems, to guaranteeing optimal usage of the available resources.
- PISA-UPC: education of embedded control system engineers, using a platform supported by the Erika real-time kernel
- ULUND-PISA: event-based control systems focusing on network scheduling of event-based controllers.
- Aveiro, UnivPorto and Malardalen: reconfigurable hierarchical scheduling framework within an enhanced Ethernet switch to allow efficient use of bandwidth, enforcing temporal and spatial isolation.
- York, Cantabria, Porto, Madrid, Valencia: language support for programming schedulable systems: support for multiprocessors into the next versions of Ada and the Real-Time Specification for Java.

Cluster: Operating Systems and Networks (2/2)

Interaction and Research activities have progressed substantially :

- TUKL, CSEM, Philips, Pisa, York, Porto, Prague: development of timeliness in Wireless Sensor Networks, incl a generalized notion of timeliness.
- Mallorca, UnivPorto, Catalonia, IFP : robustness and timeliness in Controller Area Networks.
- Cantabria, Madrid: UPM and UC3M, Bilbao, UnivPorto : real-time support for middleware and composability.
- ALL PARTNERS contributed to a major activity (coordinated by YORK) for building a taxonomy of resources, considering multi-resource platforms and including the use of banded notions of time and hierarchical structures.
- Madrid, Pisa, Aveiro, UnivPorto, Malardalen, NXP, TUKL: protocol optimizations for embedded real-time communications.
- Catania, Pisa, Evidence have : intelligent transportation systems, automatic traffic monitoring and road surveillance. Various sensors have been used to estimate traffic parameters. Catania proposed a wireless sensor network architecture based on computer vision techniques for automatic scene analysis and interpretation.

Cluster: HW Platform and MPSoC Design (1/2)

Interaction and Research activities have progressed substantially :

- EPFL-UNIBO: 1) Network on Chips models and tools; 2) 3D integration models and analysis tools; 3) Study of NoCs for 3D integration.
- UNIBO-SSSA: predictability and modularity of MPSoC for Real-Time applications.
- ETHZ-TUBS: coupling of two performance analysis methods, Symta/S and MPA.
  Tools have been connected and joint works on hierarchical event streams have been published.
- ETHZ-VERIMAG: mapping algorithms onto MPSoC platforms (DOL) connected to BIP (provably correct design flow & fast performance evaluation method supporting design space exploration.
- ETHZ-UNIBO: energy-harvesting sensor networks, application control and HW implementation in CPS.
- TU Braunschweig-ETHZ: performance analysis for multiprocessor systems with shared resources.
- KTH-ETHZ: performance analysis of embedded systems, on-chip communication and WSN
- DTU-KTH: tight cooperation on system level modelling, faster simulation & parallelization of the simulation kernel, for modelling wireless sensor networks (CPS). KTH has focused on synchronous, the untimed and continuous time domain.

Cluster: HW Platform and MPSoC Design (2/2)

Interaction and Research activities have progressed substantially :

- CEA/LIST-UNIBO: definition and design of a Software Runtime Architecture for mgt of many-core components, and design of efficient HW support for the execution of this runtime software.
- LINKÖPING-DTU: fault tolerant embedded systems..
- LINKÖPING-LUND: modelling and QoS optimisation of control applications.
- IMEC-NTUA: MPSoC topics including a framework for automatic parallelization, static and dynamic memory optimization in MPSoC platforms, runtime system exploration for multi-standard Wireless MPSoC.
- IMEC-KTH: The Co-Ware virtual multi-core platform developed by IMEC was transferred to KTH for integration of the NoC architecture in the platform model.
- IMEC-NTNU: cooperation on data value driven scenario identification and reuse of epilepsy detection kernel as additional biomedical demonstrator for scenario related research.

Transversal Integration: Design for Adaptivity (1/2)

Adaptive Resource Scheduling

- Adaptive and feedback-based resource management (SSSA, ULUND, TUKL, Evidence, Ericsson)
- Adaptive resource management for uncertain execution platforms (ULUND, Ericsson)
- Feedback control of computing systems (ULUND)
- Theory of distributed performance analysis (TU Braunschweig)
- In-system sensitivity analysis for real-time systems (TU Braunschweig)
- Change impact analysis (UYork)
- Parametric WCET analysis (MDH)
- Runtime management of cache-related preemption delay (IPPorto)
- Fault tolerance in adaptive cooperative systems (IPPorto)
- Dynamic behavior of embedded systems (IMEC, NTUA)
- Adaptive control of MPEG-4 decoding (TUKL, ULUND)
- Improving real-time BIP (Verimag).
- Adaptation in service-oriented architectures (UPM)
- Adaptive servers with guarantees (ETH Zurich, SSSA)
- Adaptive power management (ETH Zurich, SSSA)
- Sampling mechanisms for event-driven control systems (UPC, ULUND, SSSA)
- Feedback scheduling vs. event-driven control (UPC)
- Optimal online sampling period assignment (ULUND, UPC)

Transversal Integration: Design for Adaptivity (2/2)

Adaptive Networking

- Adaptivity in wireless networks (UPorto, UCatania)
- Adaptivity in distributed systems (UPorto, MDH, UAveiro, UPC)
- Adaptive management in energy harvesting systems (ETH Zurich, UBologna)
- Adaptive energy management of wireless smart camera networks (UBologna)
- Adaptive TDMA bus allocation and elastic scheduling (UBologna, SSSA)
- Fault Tolerant and Reliable Communication Platforms (KTH)

Hardware-Based Adaptivity

- eDNA: Reconfigurable self-organising and self-healing hardware platform (DTU)
- Adaptive allocation of applications on MPSoC platforms (ETH Zurich, SSSA)

Dissemination

- Several WS and meetings, incl WARM 2010 (interface between the different clusters on issues related to embedded system adaptivity)
- Education on adaptive and feedback-based approaches
- Contacts with industry, e.g., NXP, Ericsson, Volvo, IMEC, and Evidence just to name a few.
- Striving to integrate hw-oriented partners from, e.g., the MPSoC cluster with the more sw-oriented partners from the OS and networks cluster.
- Special issue on Adaptive Embedded Systems for Real-Time Systems Journal with Årzén (ULUND) as guest editor.

Transversal Integration:

Design for Predictability and Performance

Intersection with all the thematic clusters, eg:

- PREDATOR project:
  - context-switch-cost-aware scheduling (USaar, AbsInt, SSSA)
  - clarifications of the notions of predictability (USaar, ETHZ)
  - formal definition of predictability
- analyzing the predictability and interference for shared buses and memories in multi-core systems (Braunscweig, ETHZ, Linköping, and Uppsala). Further research to develop a formal measure that describes predictability and efficiency in this context. .
- Work on reconciling timing analysis with compilation includes the development of the WCET-aware compiler WCC by TU Dortmund, in collaboration with USaar, AbsInt, ETHZ, and Pisa.
  WCC is now able to generate and optimize industrial code, e.g., representing an engine control system, with substantially lower WCET, compared to the GCC compiler. WCC has been extended towards code generation and optimization for multi-process systems

Transversal Integration:

Industrial Integration

- Industrial interactions and collaborations with ArtistDesign teams has increased substantially with the participation of Partners to Artemis Projects (more than 10 projects) and with the participation of the industrial activities in start-ups (more than 8).
- Activities included both technical achievements and dissemination work on:
  - General Frameworks for system-level design;
  - Applications to the Automotive Sector;
  - Applications to Chip Design;
  - Applications to Buildings;
  - Applications to Wireless communication technology;
  - Timing Analysis and Predictability.
- Global impact on design methodologies, formal techniques and modelling: META and MuSyC projects in the US.
- Move to Energy Efficient Building has had a re-sounding success. The GREEMBED Conference was a result of these efforts.
- New direction in the area of Synthetic Biology launched in 2010, with the sponsorship and participation to the 2010 International Workshop on Bio-Desing Automation. This area is bound to have a strategic impact on research world-wide.

Spreading Excellence

ARTIST Summer School in Europe 2010 - 6th edition

- high quality technical programme, excellent feedback from participants
- 100 selected participants and 14 invited speakers.

International ARTIST Summer School in China 2010 – 5th edition

International ARTIST Summer School in South America 2010 – 4th edition

International Summer School in Rabat, Morocco 2010

Graduate Schools:

- **ARTIST Graduate School on RT Kernels for Microcontrollers**
  June 14-18, 2010 Scuola Superiore Sant'Anna - Pisa, Italy
- **ARTIST Graduate Course: Automated Formal Methods for Embedded Systems – 2010**
  June 14-22, 2010 DTU - Lyngby, Denmark
- **Quantitative Model Checking 2010**
  March 2-5, 2010 IT University Copenhagen, Denmark

Conferences: support for CPS Week, ES Week, FORMATS, MEMOCODE, DATE, EuroSys

ARTIST Workshops

Synchron, UML&FM, WSS, WESE, WFCD, FIT, WCET, OSPERT, HW Platforms and MPSoC Technical Meeting, Mapping Applications to MPSoCs, SCOPES, GREEMBED, FESA, WARM

ARTIST web portal

Deliverables

Deliverables (1/2)

WP0: Joint Programme of Management Activities (JPMA)

Floralis	D1-(0.1)-Y3	**Periodic Report**
	D2-(0.2)-Y3	Project Activity Report
UJF/Verimag	D2-(0.2a)-Y3	*ch. 1* - **Executive Summary and Overview**
Aalborg	D2-(0.2b)-Y3	*ch. 2* - **Modelling and Validation**
Dortmund	D2-(0.2c)-Y3	*ch. 3* - **SW Synthesis, Code Generation and Timing Analysis**
Pisa	D2-(0.2d)-Y3	*ch. 4* - **Operating Systems and Networks**
DTU	D2-(0.2e)-Y3	*ch. 5* - **Hardware Platforms and MPSoC Design**

WP1: Joint Programme of Integration Activities (JPIA)

UJF/Verimag	D3-(1.0)-Y3	**Integration Activities Report**

WP2: Joint Programme of Activities for Spreading Excellence (JPASE)

UJF/Verimag	D4-(2.0)-Y3	**Spreading Excellence Report**

WP3: Modeling and Validation (JPRA)

UJF/Verimag	D5-(3.1)-Y3	**Modelling**
Aalborg	D6-(3.2)-Y3	**Validation**

Deliverables (2/2)

WP4: Software Synthesis, Code Generation and Timing Analysis (JPRA)

Dortmund	D7-(4.1)-Y3	**Software Synthesis, Code Generation**
Saarland	D8-(4.2)-Y3	**Timing Analysis**

WP5: Operating Systems and Networks (JPRA)

Pisa	D9-(5.1)-Y3	**Resource-aware Operating Systems**
York	D10-(5.2)-Y3	**Scheduling and Resource Management**
UnivPorto	D11-(5.3)-Y3	**Embedded Real-Time Networking**

WP6: Hardware Platforms and MPSoC (JPRA)

Bologna	D12-(6.1)-Y3	**Platform and MPSoC Design**
DTU	D13-(6.2)-Y3	**Platform and MPSoC Analysis**

WP7: Transversal Integration (JPRA)

Lund	D14-(7.1)-Y3	**Design for Adaptivity**
Uppsala	D15-(7.2)-Y3	**Design for Predictability**
Trento	D16-(7.3)-Y3	**Integration Driven by Industrial Applications**

Summary of Achievements

Artist has achieved a level of real integration between leading teams that would have been unimaginable before the NoE's

Integration can be measured by:

- Number of joint publications
- Number and quality of collaborative submitted and funded projects
- Number of dissemination events including workshops, graduate schools, and international summer schools
- A common vision for structuring the effort in the area

Unprecedented level of interaction with industry as attested by

- Participation of industrial partners in the projects and technical meetings
- Active participation in setting up Artemis and Artemisia
- Transfer of methods and tools

International recognition as attested by

- collaborations with leading research teams in the US and Asia
- active involvement of Artist teams in steering main flagship events in the area

Year 4 : Wrapping Up the NoE

We would like a 3-month extension, to :

- Finalize ongoing work and all partners to use up their funding
- Hold the Final Review and a Public Event co-located with DATE in March 2012

We will prepare a Special Issue including synthesis of the main results and position papers *(either in Proceedings of the IEEE, or Transactions on Embedded Computing Systems)*.

We will prepare a video on Embedded Systems Design, intended for the General Public.

Beyond Artist

- Artist has clearly met and well exceeded its goals
- The level of integration and excellence achieved through Artist are well beyond the funding allocated
- Unfortunately, the recent call did not include funding for NoE in the Artist topic.
- Alternatives based on auto-financing would have required a completely different structure and a business-oriented approach which is fundamentally incompatible with an academic profile.
- We are currently exploring the possibility for setting up an ArtistDesign European association.

THANK YOU