Year 3 Review
Brussels, February 24th, 2011

Cluster

Achievements and Perspectives :

Hardware Platforms and MPSoC Design

leader : Jan Madsen (DTU)

Luca Benini (UNIBO)

High-Level Objectives

- Focus on Design and Analysis
- Hardware architecture and software components in their interaction
- Tools for accurate estimation
- Growing importance of resource awareness in embedded systems
- Design methodology
  - Scales to massively parallel and heterogeneous multiprocessor architectures
  - Allows for predictable system properties
  - Uses the available hardware resources in an efficient manner
- Adaptivity
  - Robustness
  - Life-time management
  - Resilience

State of the Integration in Europe

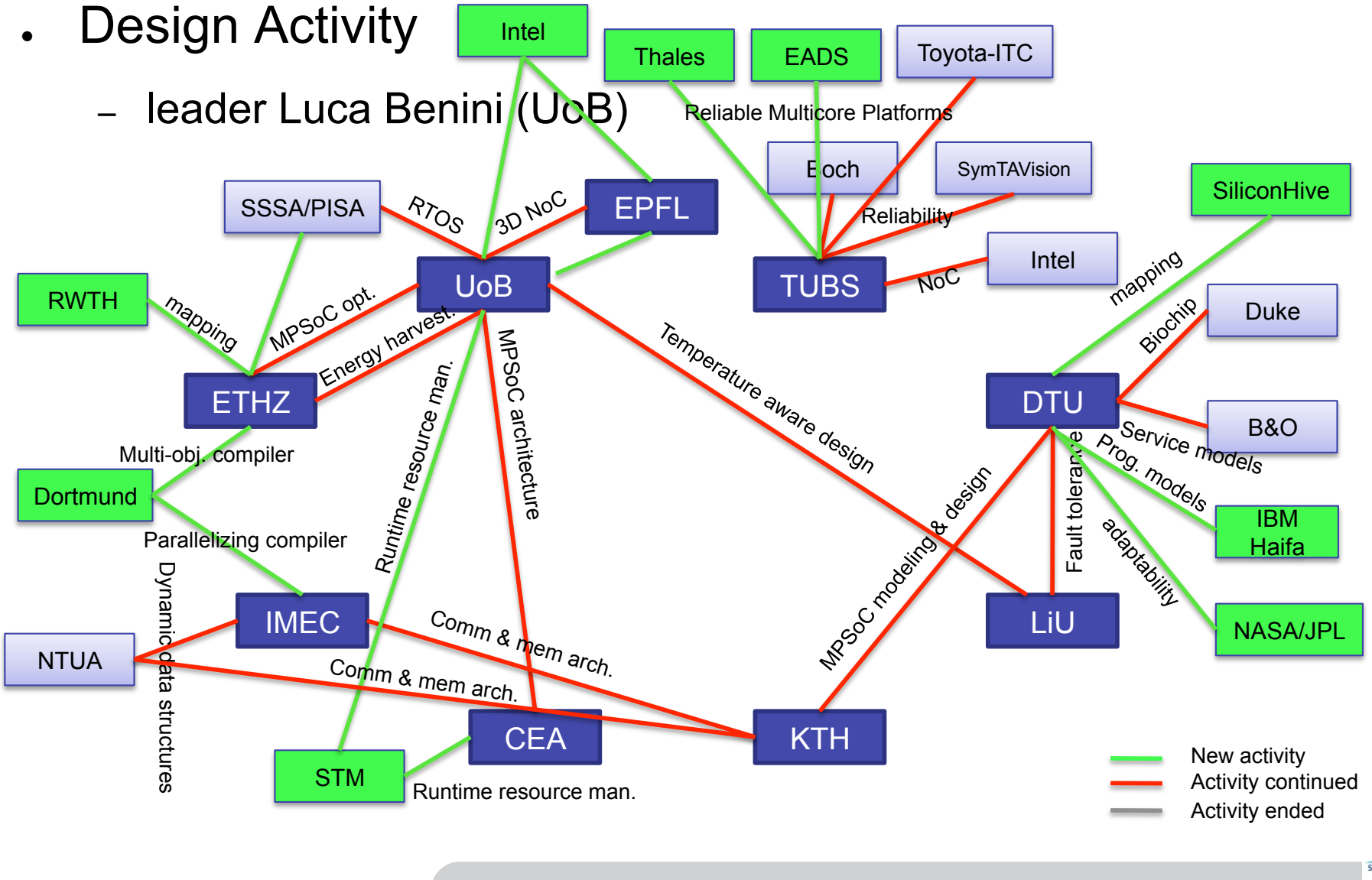
- Distributed, communication-centric embedded systems
  - Multi- and Many-core System-on-Chip (MPSoC)
  - Networked embedded systems
  - Emerging platform technologies
- Hardware platforms for embedded applications will continue to be multi- and many-core
- Programming models, design-time and run-time application environments are less clear
- Growing maturity of scalable performance analysis algorithms and tools
- New challenges, platform robustness and adaptivity

Building Excellence

- High interaction among partners in the cluster
- Increased interaction with other ArtistDesign partners
- Large involvement of researchers outside of ArtistDesign
- Joint publications in 2010
  - 20 out of 94
- Strong impact on international conferences
  - DATE, CODES+ISSS, EMSOFT, CASES, ASP-DAC, MPSoC, …
- Joint organization of workshops, tutorials, and special sessions
- Strong involvement in Artemis JU and Artemis-IA
  - New Artemis SRA
- Organization of national industry networks and SIGs

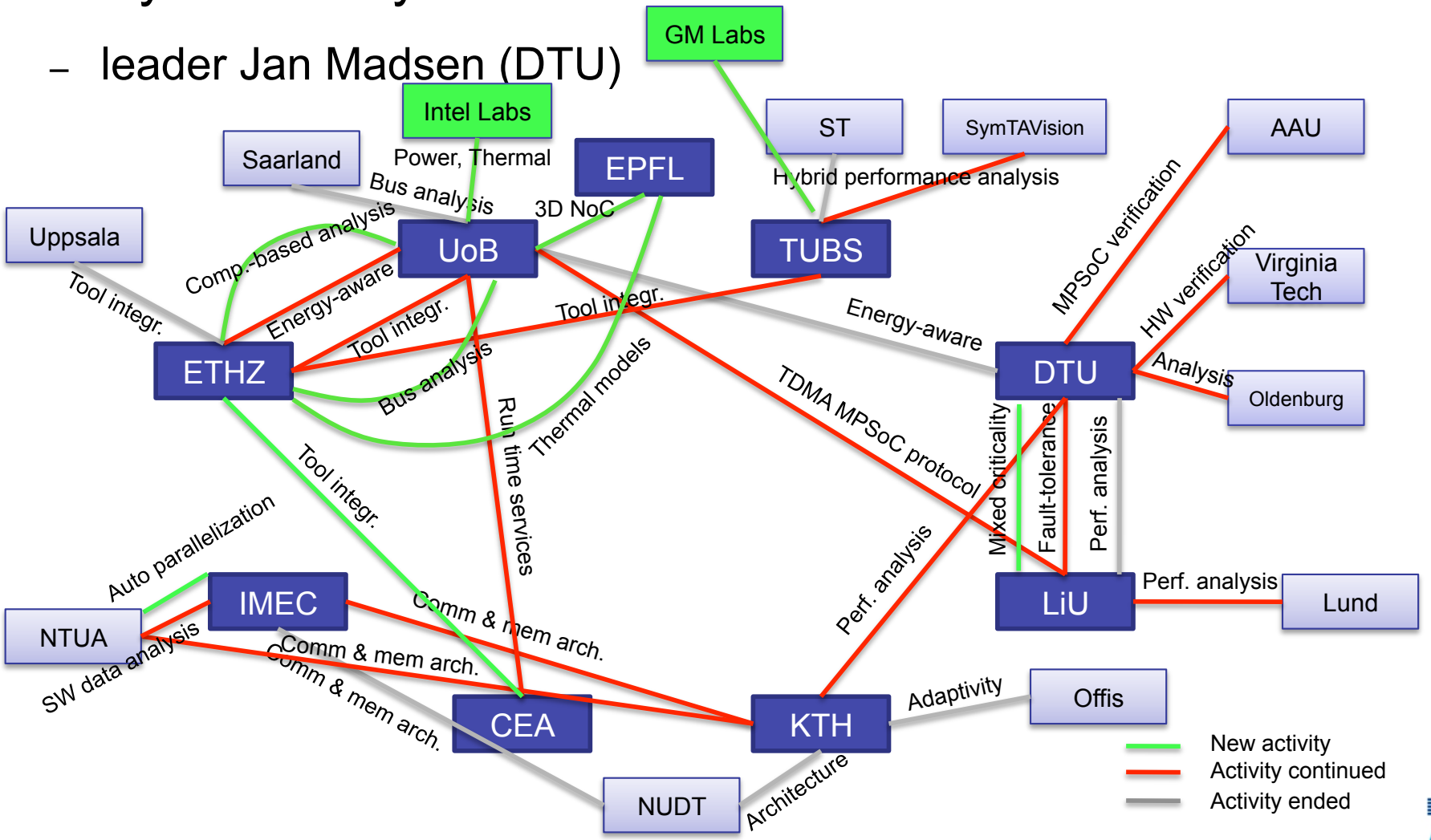
Building Excellence

- Design Activity
  - leader Luca Benini (UoB)



Building Excellence

- Analysis Activity
  - leader Jan Madsen (DTU)



Overall Assessment and Vision at Y0+3

- Strong research collaboration within cluster
  - 20 joint publications
  - 8 tools (2 added in 2010)
- Increased research collaboration with other clusters
  - In particular on compilers and mapping tools
- Joint participation in many European projects
  - RECOMP, SMECY, ASAM, iFest, SYSMODEL, SCALOPES
  - PREDATOR, COMBEST, PRO3D, EURETILE, GALAXY

Overall Assessment and Vision at Y0+3

Visions:

- to increase predictability and adaptability for multi-core platforms
  - Predictable and reliable NoCs (RECOMP, COMPOSE)
  - Self-healing architecture (patent pending)
  - Robust scheduling and allocation
- energy-aware embedded systems
  - Thermal models and management in MPSoC
  - Energy aware compilers and mapping for MPSoC
- fault-tolerance in distributed embedded systems
  - Energy/reliability optimization for MPSoC
  - Reliable MPSoC for smart buildings

Overall Assessment and Vision at Y0+3

Visions:

- Programming models for multi- and many-core platforms
  - Extensions to distributed operation layers
  - Parallelizing compilers
  - Programming tool for optimizing the performance of parallel programs
- new technologies
  - 3D NoC – energy and thermal awareness, integration with memory systems
  - Biochips – droplet- and flow-based architectures

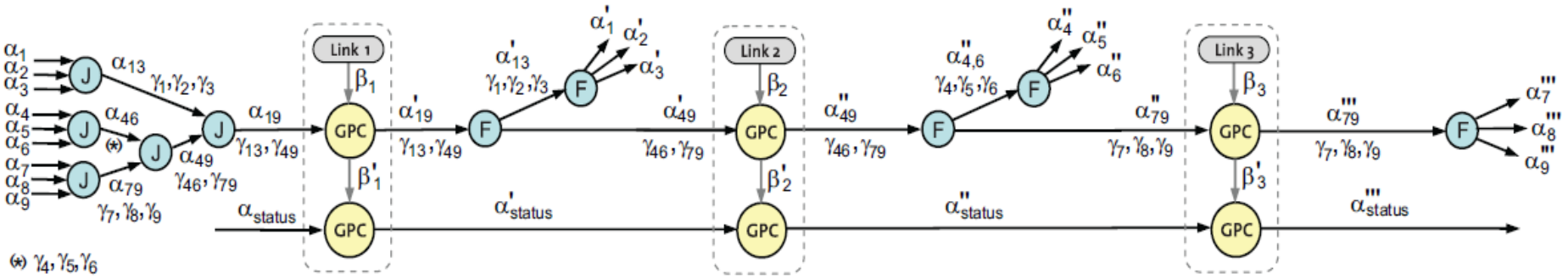
Scientific Highlights

- Performance analysis of complex MPSoC (TUBS, ETHZ)
- Predictable RT MPSoC (UNIBO, SSSA, Linkoping)
- Energy/Reliability optimization for MPSoC (DTU)
- Robust MPSoC (DTU, NASA/JPL)

Hierarchical Event Models (TUBS, ETHZ)

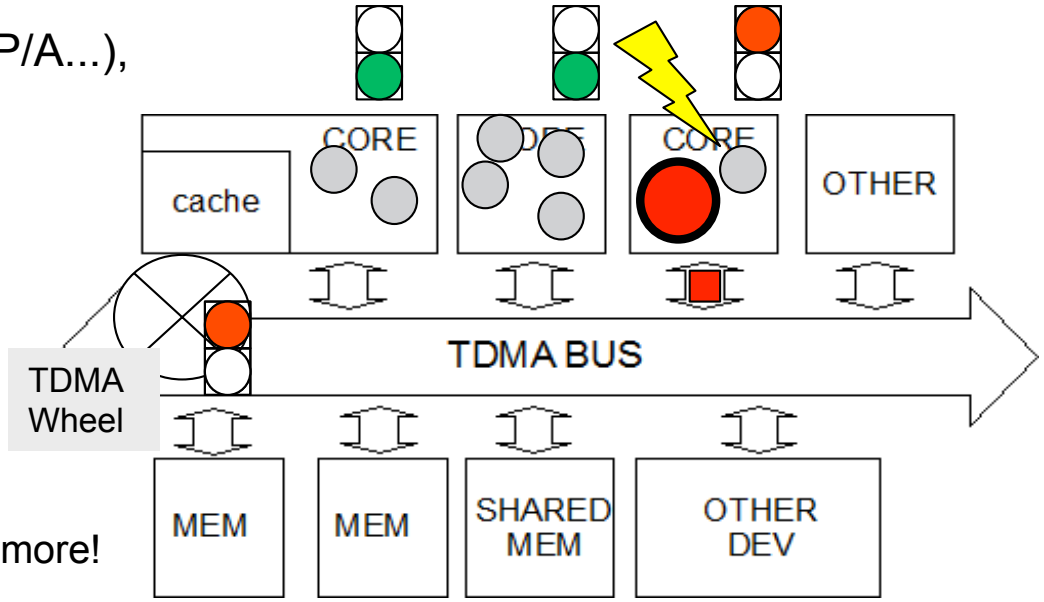
- ***Problem:*** Improve accuracy and modeling power of performance analysis of complex MPSoC systems

- ***Solution:*** Combine expertise and model approaches in MPA and Symta/S and introduce hierarchical event models. Compare different modeling approaches and integrate the two tools.



Unified approach for enhancing robustness in Multi-Core RT Systems (UNIBO, SSSA / UNIBO, Linkoping)

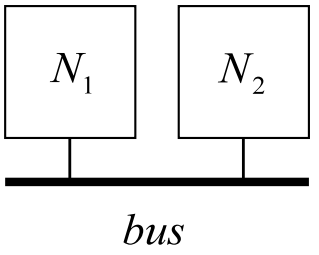
- RT MPSoC platforms
  - *predictable* HW (TDMA bus, TTP/A...), and RT-Tasks (Elastic Tasks)
  - Predictability vs. Robustness & Performance
  - Task triggered by an interrupt
    - Bus workload changes
      => No longer optimal!
    - Task set changes
      => May not be schedulable anymore!



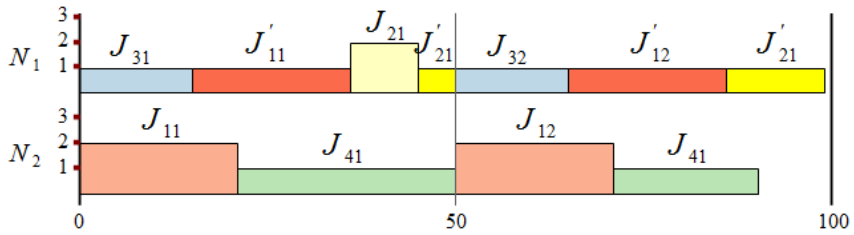
- Reconfigurable system, where TDMA bus and OS scheduler work *synergistically* in case of run-time workload changes, to ensure the highest utilization of processors

Energy/Reliability tradeoff optimization for MPSoC

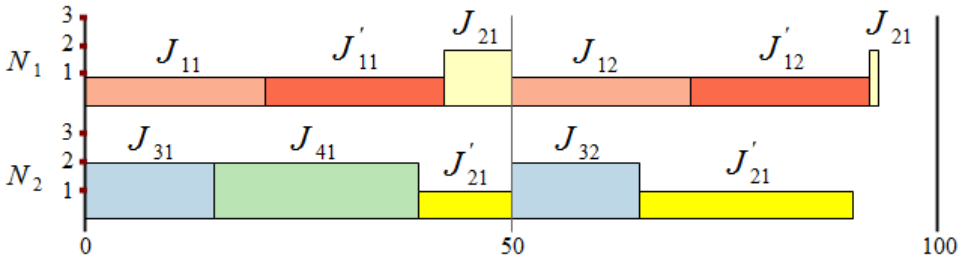
- New technology is resulting in circuits with
  - higher power consumption
  - higher probability of transient faults



- Scaling voltage and frequency can reduce the energy consumption, but increase the number of transient faults exponentially.

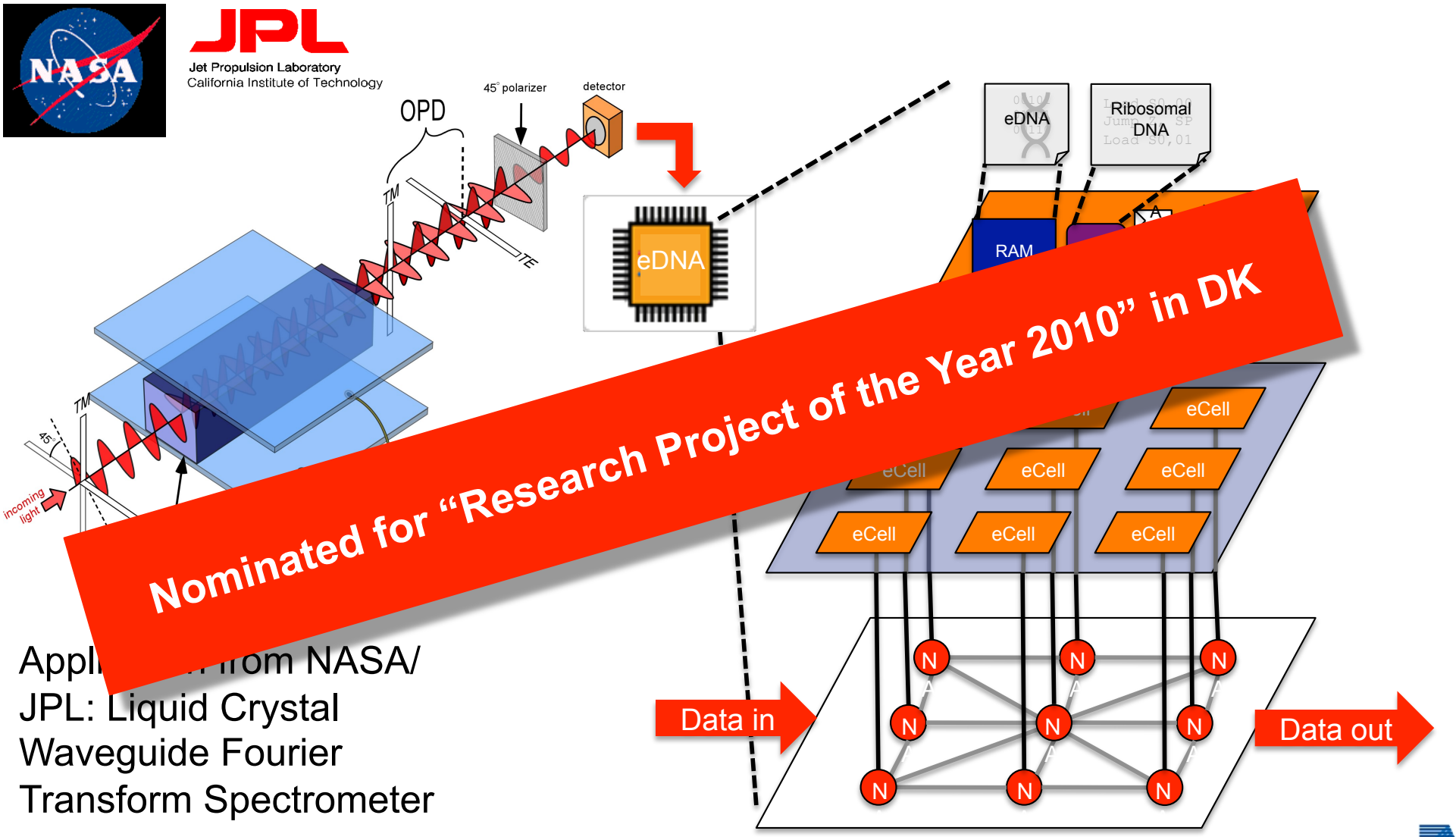


Not considering reliability:
- 42.6% energy reduction
- Failure prob. Increased by 160x



Considering reliability:
- 42.1% energy reduction
- Failure prob. Increased by 7x

Self-healing computer (DTU, NASA/JPL)



Nominated for "Research Project of the Year 2010" in DK

Appli[illegible] from NASA/
JPL: Liquid Crystal
Waveguide Fourier
Transform Spectrometer

Joint Technical Meetings

- Meeting: Predictability Measures, *Zurich, Switzerland – 30.9.2010*. Define measures to determine predictability and efficiency in computer architectures
- Meeting: Shared Resources in Multiprocessor Systems - Modeling Concepts and Observations, *Brussel, Bergium – July 5, 2010*
- Meeting : MPSoC Cluster Meeting, *Dresden, Germany – March 2010*. Status, plans and discussions for the cluster
- Cluster meeting : ARTIST HW Platform and MPSoC Technical Meeting, *IMEC, Leuven, Belgium – July 6-7, 2010*
- Workshop on temperature aware 3D MPSoc in Lausanne, Switzerland
- Workshop on modelling methodologies in Kista, Sweeden

Joint Technical Meetings

- Tutorial on sensor networks in environmental applications at DATE, Dresden, Germany, 2010.
- Tutorial at ESWeek in Scottsdale, USA, 2010.
- Tutorial at ASPDAC in Taipeh, Taiwan, 2010.
- Tutorial on performance analysis in Rabat, Morocco, 2010.
- Tutorial on multicore architectures at RSP in Fairfax, USA, 2010.
- Keynote at ARTEMIS Summer Camp in Rom, Italy, 2010.
- Summer School on Models for Embedded Signal Processing Systems in Leiden, The Netherlands, 2010.
- PhD course on Automated Formal Methods in Embedded Systems, Lyngby, Denmark, 2010.
- 15 keynotes and invited talks at conferences and workshops, including ARTEMIS Summer Camp, ARTIST Summer School, RSP, and MPSoC.

Tools and Platforms

- SymTA/S: Development and verification of embedded multiprocessor real-time systems (TUBS,ETHZ,SymtaVision,AbsInt)
- Analysis and optimization framework for fault tolerant distributed embedded systems (LiU,DTU)
- MPHP: An integration of MPA parallelization assistant and MH static memory allocation for MPSoC (IMEC,KTH,Dortmund,TU/e,DUTH)
- MoVES: Modelling and verification of embedded systems (DTU,AAU)
- MPA: Modular Performance Analysis (ETHZ,TUBS)
- DOL: Distributed operation layer (ETHZ,UNIBO)
- McNoC: Multicore network on chip (KTH,NTUA,NUDT)
- ForSyDe: Formal system design (KTH,DTU)

Plans for Y4

- Continue the ongoing joint research
- With the current trend in mind:
  - Mega MPSoC platforms
    - Consolidation of European R&D activities on a few mega MPSoC platforms (e.g., P2012, Embedded Systems for Smart Mobility)
    - HW: Predictable, reliable, configurable, low energy, thermal control
    - Platform SW: Scheduling, virtualization, segregation (real-time, safety, predictability), platform control
  - Green and sustainability
    - Green ICT needs Embedded Systems for monitoring and control
    - 30% of total value of car will be on SW and HW

Current trend