Timing and Performance Analysis of Embedded Systems using Model Checking

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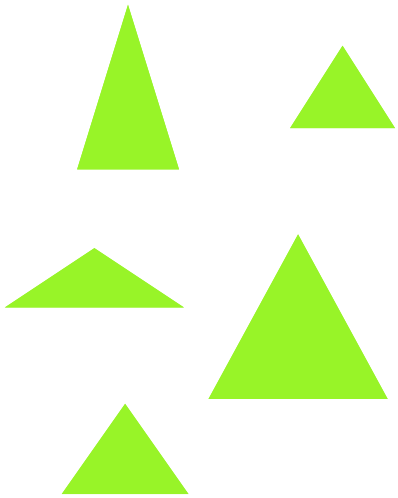
Embedded Systems

Tasks:
Computation times
Deadlines
Dependencies
Arrival patterns
uncertainties

Scheduling Principles (OS)
EDF, FPS, RMS, DVS, ..



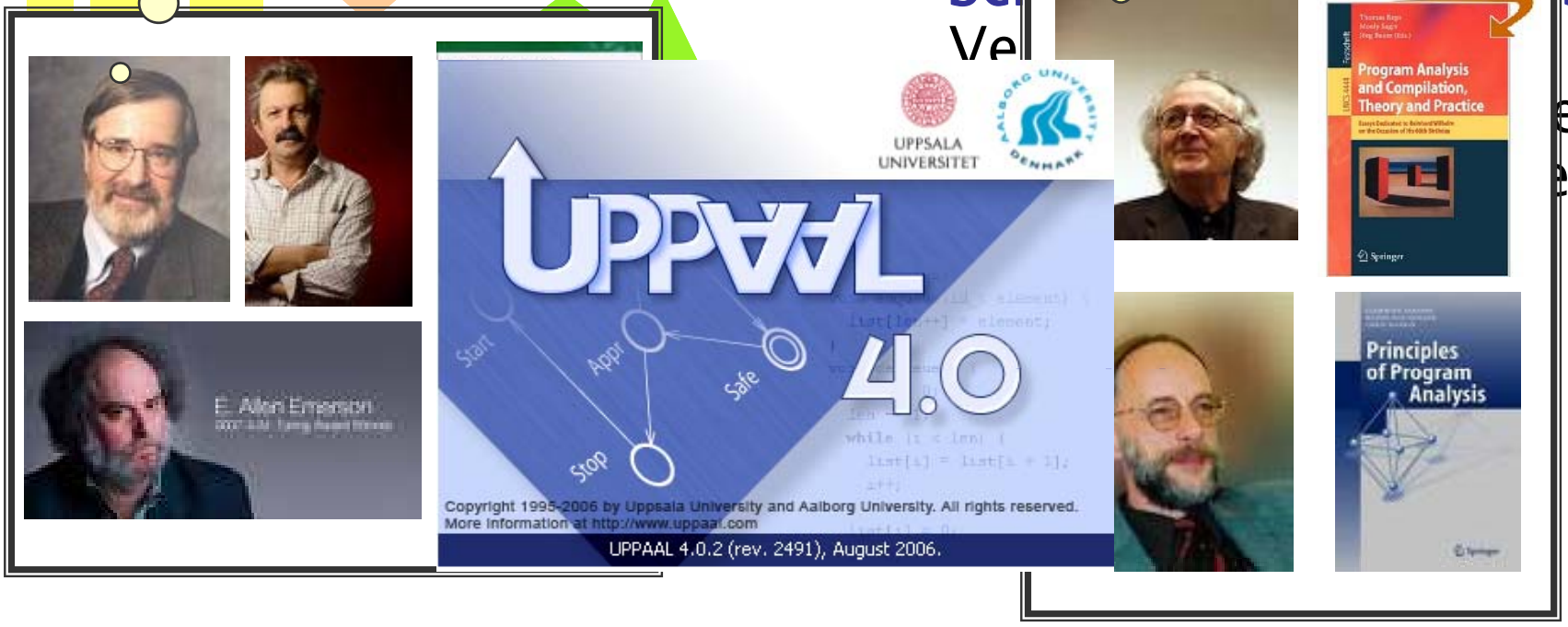
Resources
Execution platform
PE, Memory
Networks
Drivers
uncertainties

Timing Analysis

Model checking *is fixpoint iteration without dynamic abstraction and using set union to collect states.*

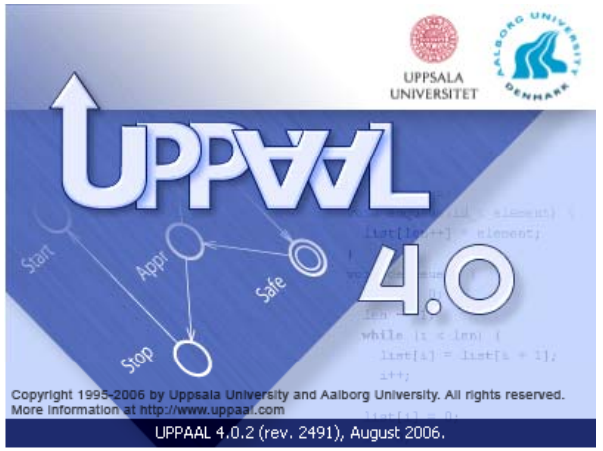
Abstract Interpretation *is fixpoint iteration with dynamic abstraction using lattice join to combine abstract states.*

- Sch… …s:
  Ve… …el …ed.



Overview

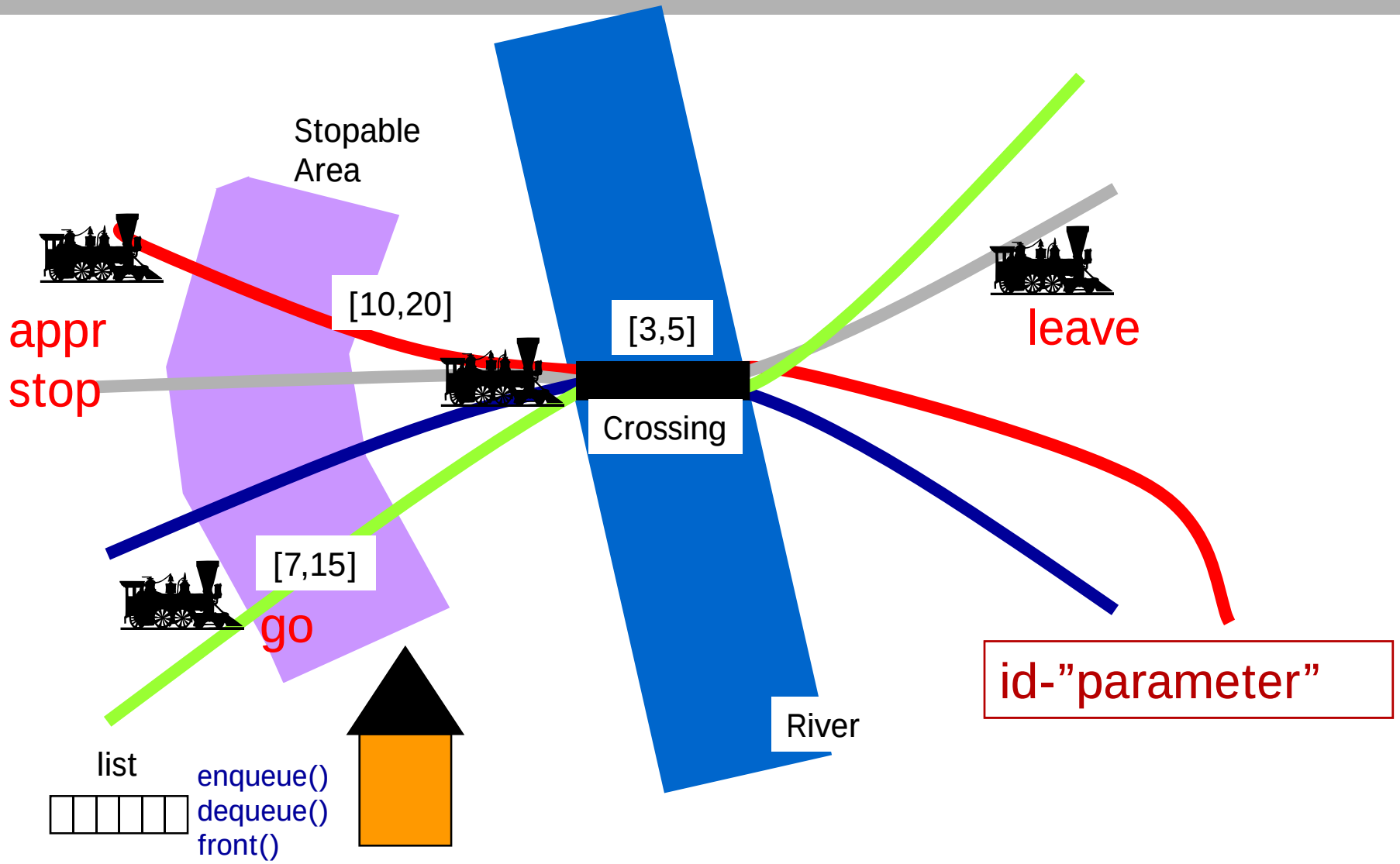
- Timed Automata
- Scheduling
  - Task Graph Scheduling
- Schedulability Analysis
  - Single Processor
  - Multi Processor
- WCET Analysis
- Performance Analysis
  - Statistical Model Checking



Timed Automata

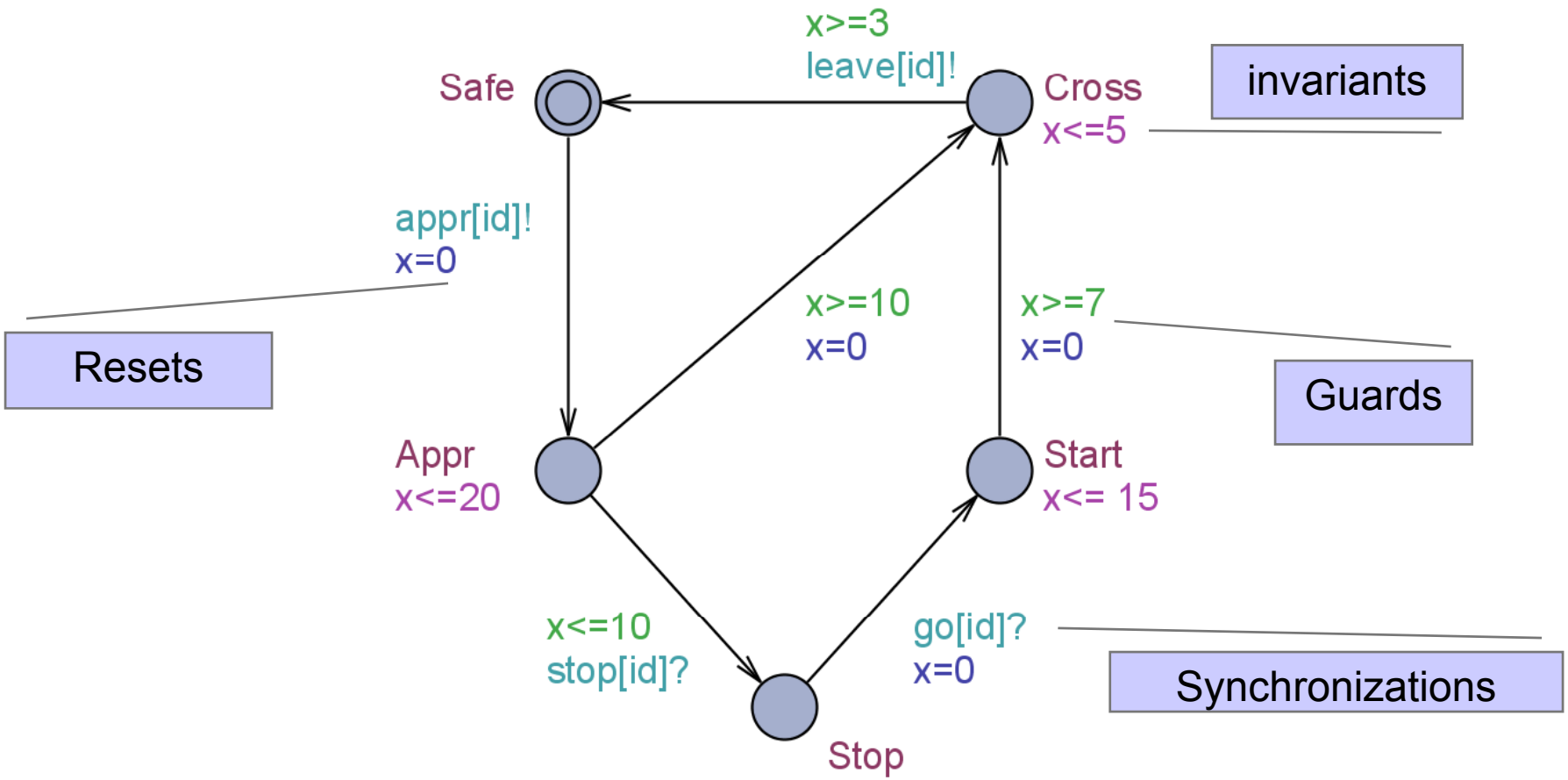
Train Crossing

Communication via channels!



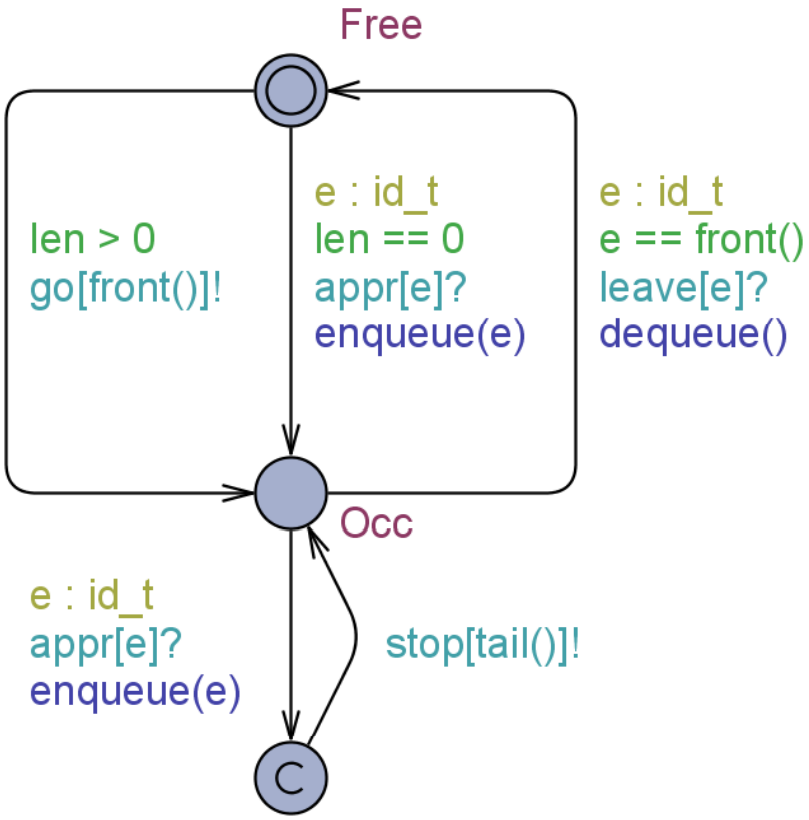
Timed Automata [Train]

= Finite State Control
+ Real Valued Clocks



Timed Automata [Gate]

= Finite State Control
+ Real Valued Clocks
+ Discrete Variables




```
id_t list[N+1];
int[0,N] len;

// Put an element at the end of the queue
void enqueue(id_t element)
{
        list[len++] = element;
}

// Remove the front element of the queue
void dequeue()
{
        int i = 0;
        len -= 1;
        while (i < len)
        {
                list[i] = list[i + 1];
                i++;
        }
        list[i] = 0;
}
```

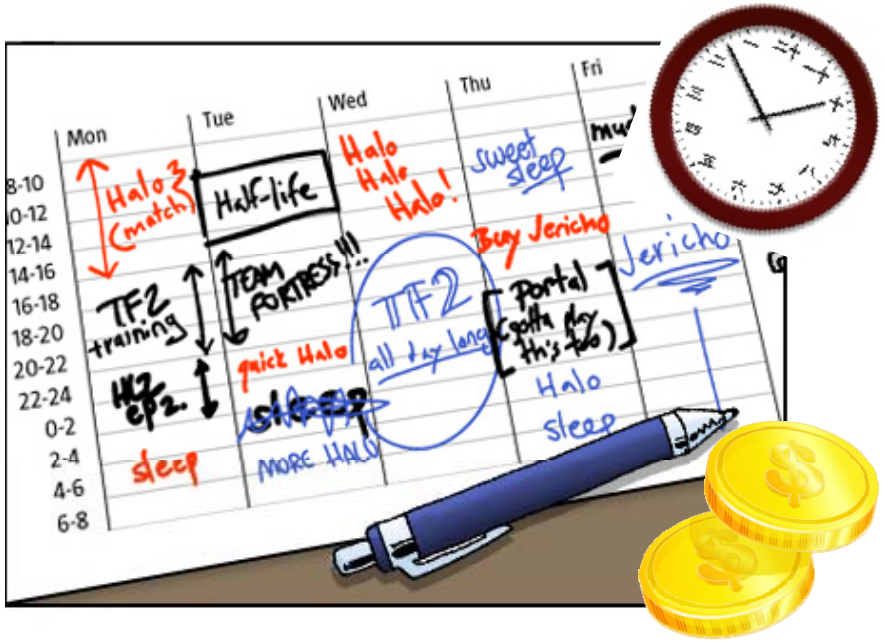
Logical Specifications

- Validation Properties
  - Possibly: E<> *P*
- Safety Properties
  - Invariant: A[] *P*
  - Pos. Inv.: E[] *P*
- Liveness Properties
  - Eventually: A<> *P*
  - Leadsto: P → *Q*
- Bounded Liveness
  - Leads to within: $P \rightarrow_{\leq t} Q$

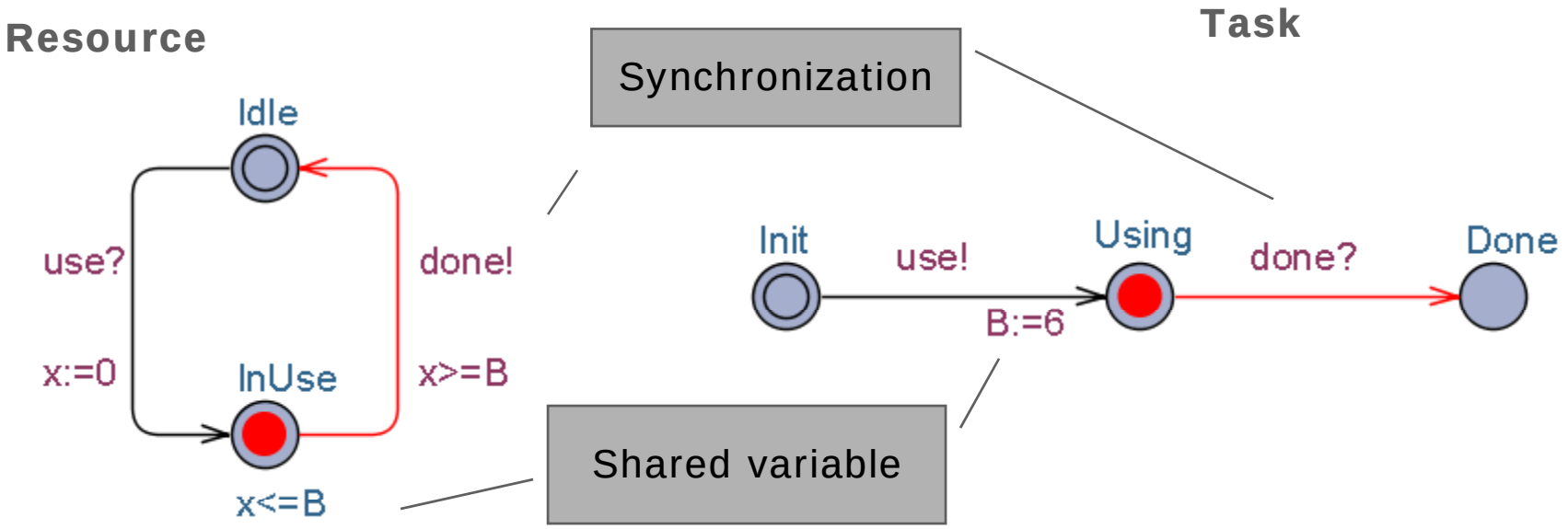
The expressions *P* and *Q* must be type safe, side effect free, and evaluate to a boolean.

Only references to integer variables, constants, clocks, are allowed (and arrays of these).

Scheduling


Mon
Tue
Wed
Thu
Fri
8-10
10-12
12-14
14-16
16-18
18-20
20-22
22-24
0-2
2-4
4-6
6-8
Halo 3 (match)
Half-life
Halo Hate Halo!
sweet sleep
Buy Jericho
Jericho
TF2 training
TEAM FORTRESS!!!
TF2
all day long
Portal
quick Halo
Halo
sleep
sleep
MORE HALO

Composition



Semantics:

(Idle , Init , B=0, x=0)

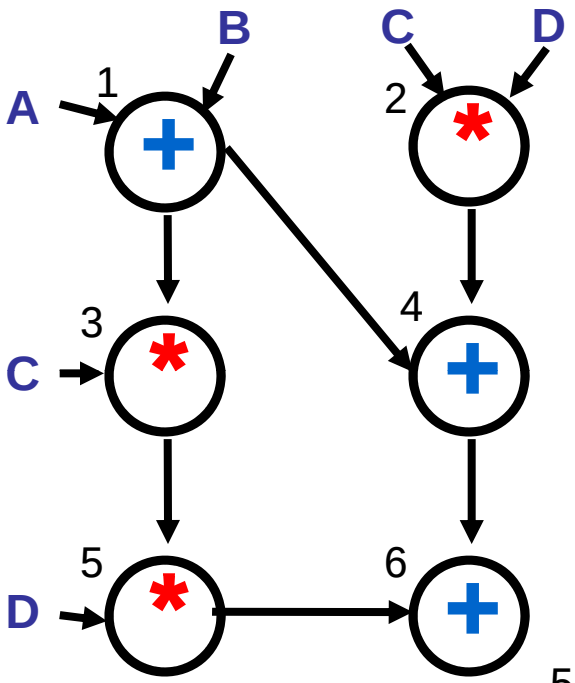
d(3.1415) → (Idle , Init , B=0 , x=3.1415)

use → (InUse , Using , B=6, x=0)

d(6) → (InUse , Using , B=6, x=6)

done → (Idle , Done , B=6 , x=6)

Optimal Scheduling – TIME



Compute :

$$(D * (C * (A + B)) + ((A + B) + (C * D))$$

4

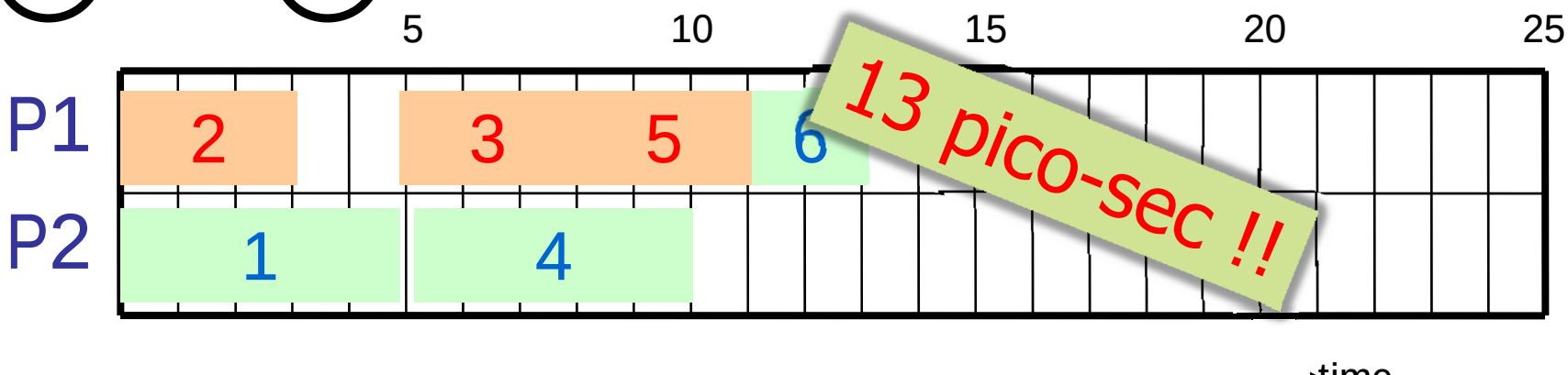
using 2 processors

P1 (fast)

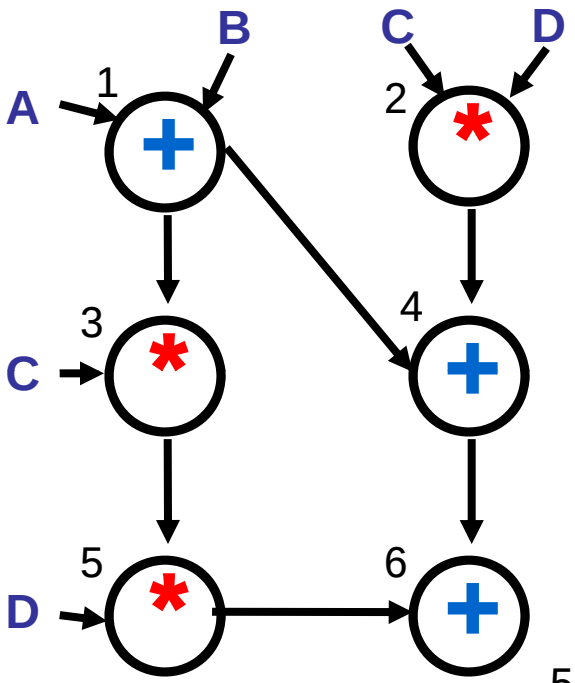
+	2ps
*	3ps

P2 (slow)

+	5ps
*	7ps



Optimal Scheduling – TIME



Compute :
(D * (C * (A + B)) + ((A + B) + (C * D))

using 2 processors

P1 (fast)

+	2ps
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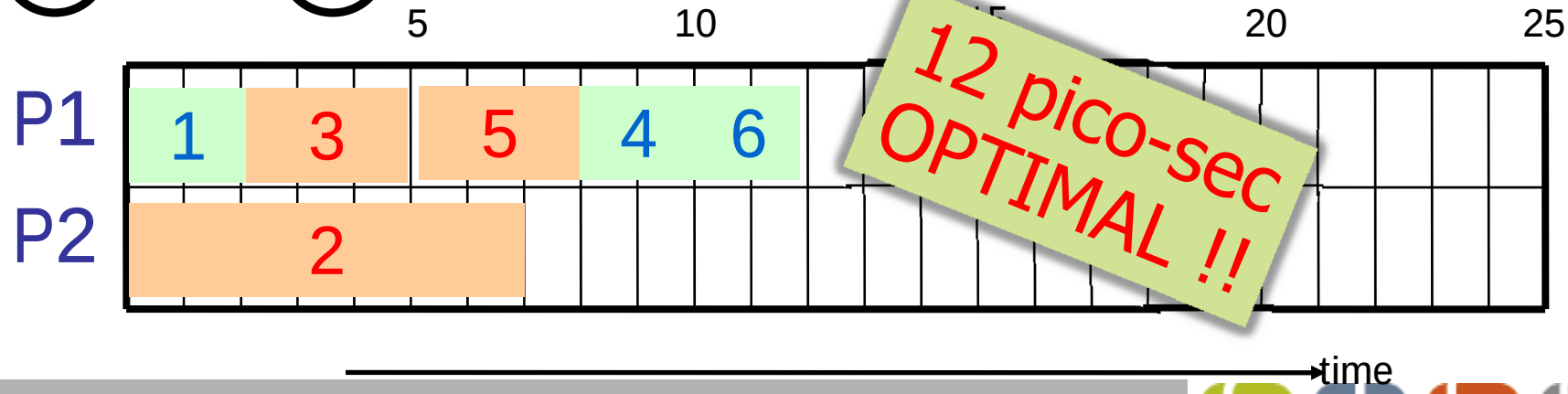
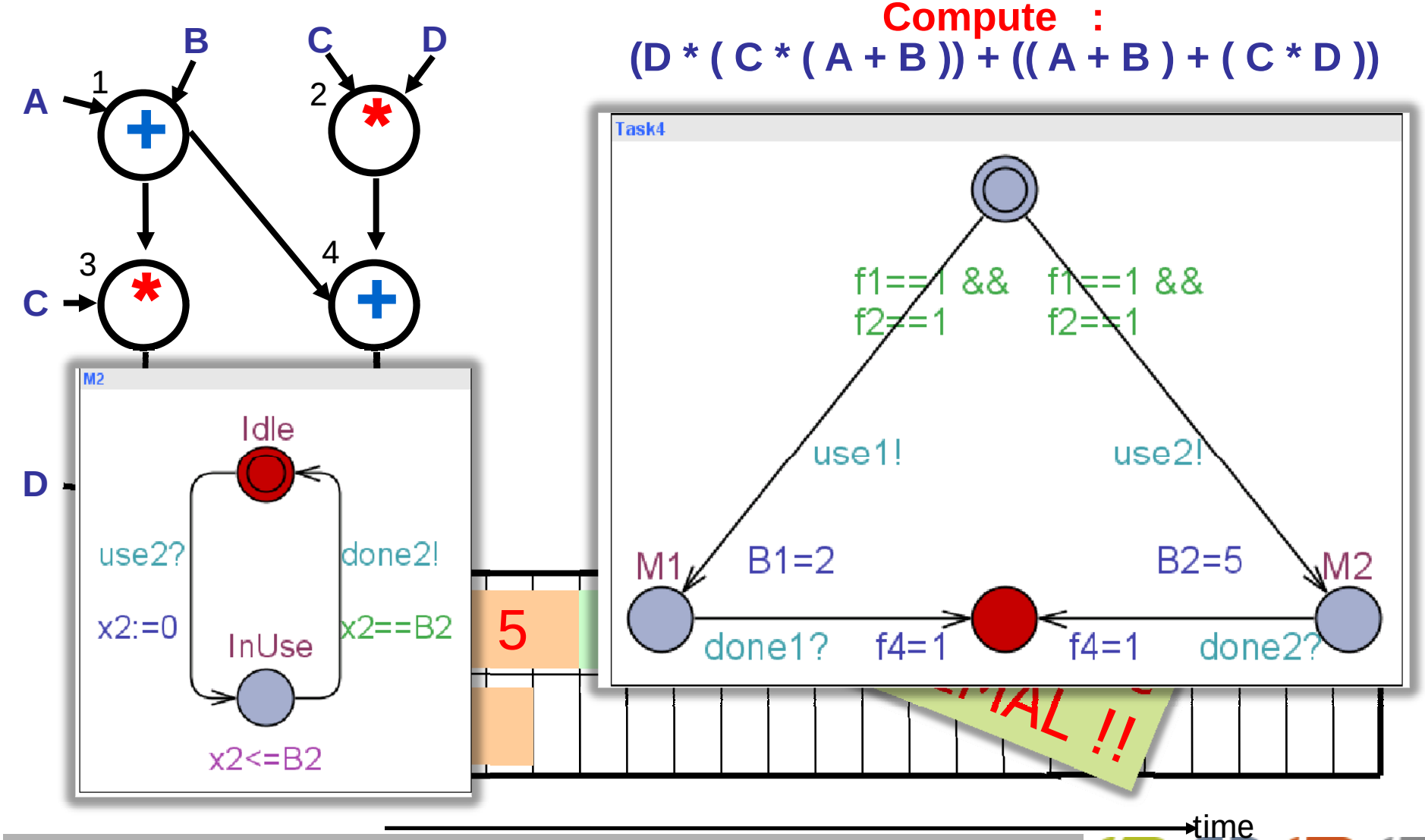
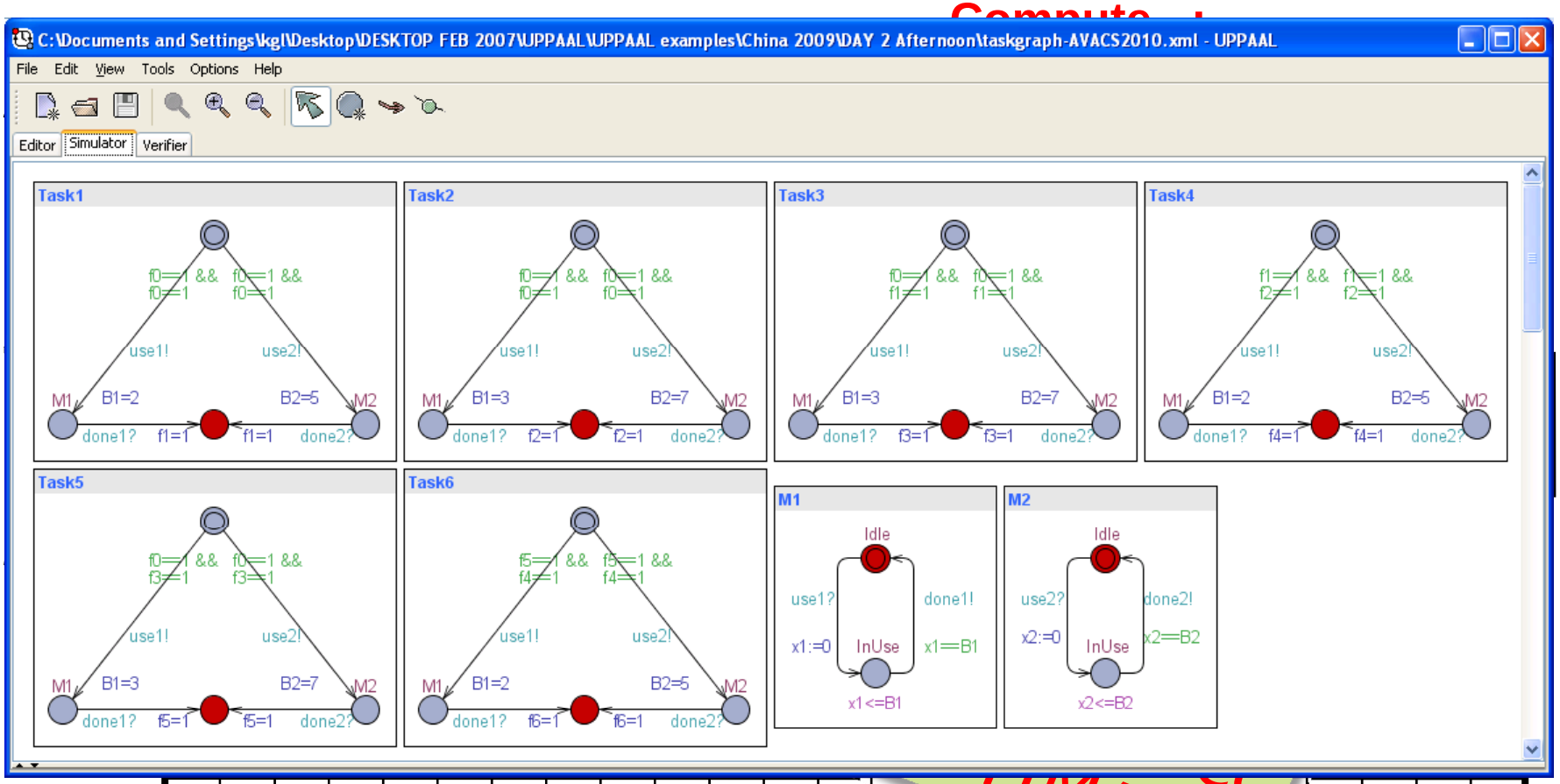
*	7ps



Optimal Scheduling – TIME



Optimal Scheduling – TIME



P2

E<> (Task1.End and … and Task6.End)

time

Experimental Results

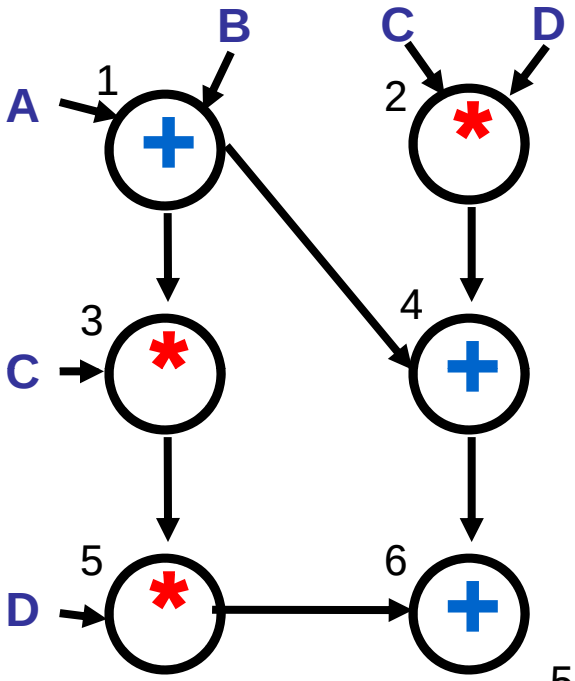
name	#tasks	#chains	# machines	optimal	TA
001	437	125	4	1178	1182
000	452	43	20	537	537
018	730	175	10	700	704
074	1007	66	12	891	894
021	1145	88	20	605	612
228	1187	293	8	1570	1574
071	1193	124	20	629	634
271	1348	127	12	1163	1164
237	1566	152	12	1340	1342
231	1664	101	16	t.o.	1137
235	1782	218	16	t.o.	1150
233	1980	207	19	1118	1121
294	2014	141	17	1257	1261
295	2168	965	18	1318	1322
292	2333	318	3	8009	8009
298	2399	303	10	2471	2473

AMETIST
advanced methods for timed systems

Symbolic A*
Branch-&-Bound
60 sec

Abdeddaïm, Kerbaa, Maler

Task Graph Scheduling – Revisited



Compute :
(D * (C * (A + B)) + ((A + B) + (C * D))

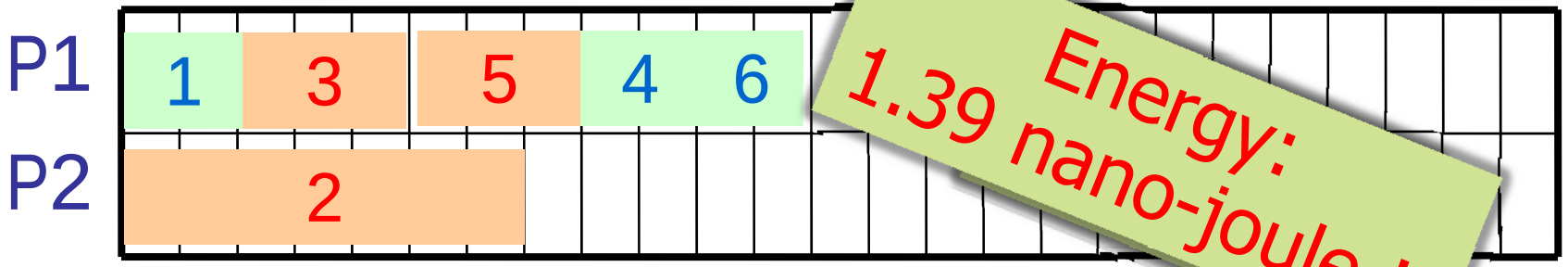
using 2 processors

P1 (fast) **P2** (slow)

+	2ps
*	3ps
Idle	1oW
In use	90W

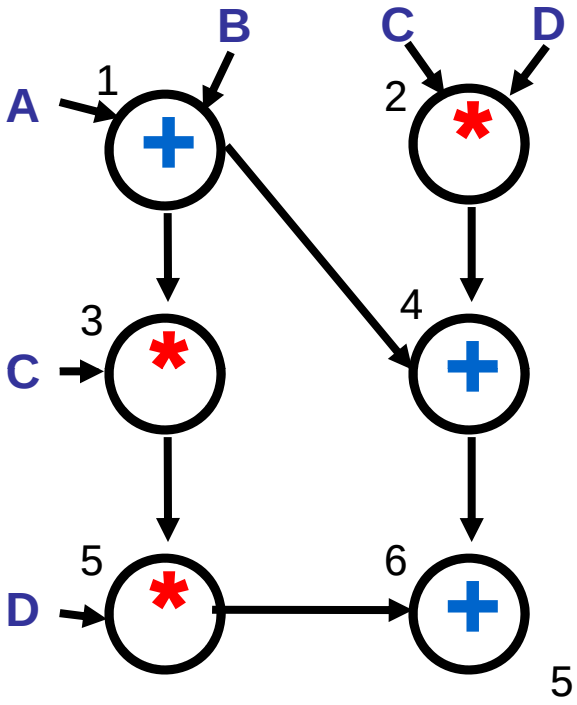
+	5ps
*	7ps
Idle	20W
In use	30W

ENERGY:



Energy:
1.39 nano-joule !!

Task Graph Scheduling – Revisited



Compute :
(D * (C * (A + B)) + ((A + B) + (C * D))

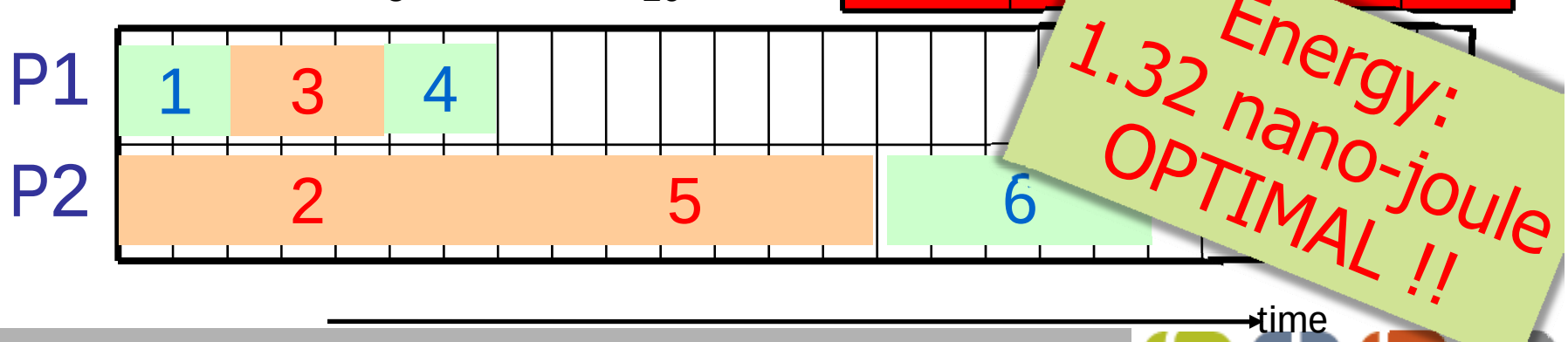
using 2 processors

P1 (fast) P2 (slow)

+	2ps
*	3ps
Idle	10W
In use	90W

+	5ps
*	7ps
Idle	20W
In use	30W

ENERGY:
10

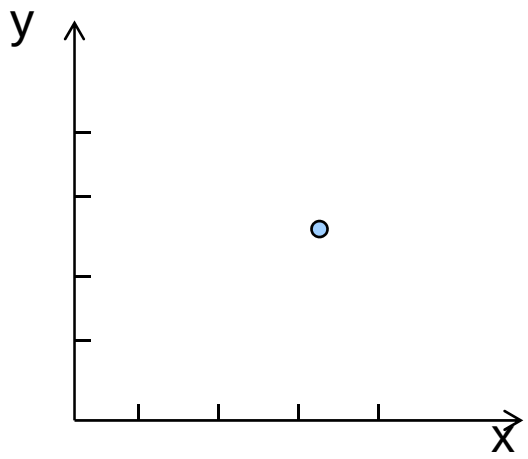


Energy:
1.32 nano-joule
OPTIMAL !!

Zones – from infinite to finite

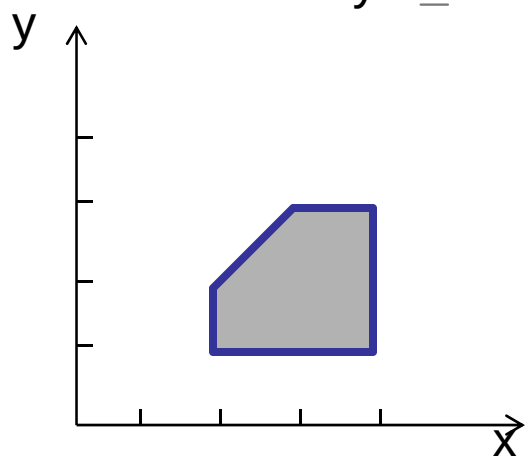
State

(n, x=3.2, y=2.5)

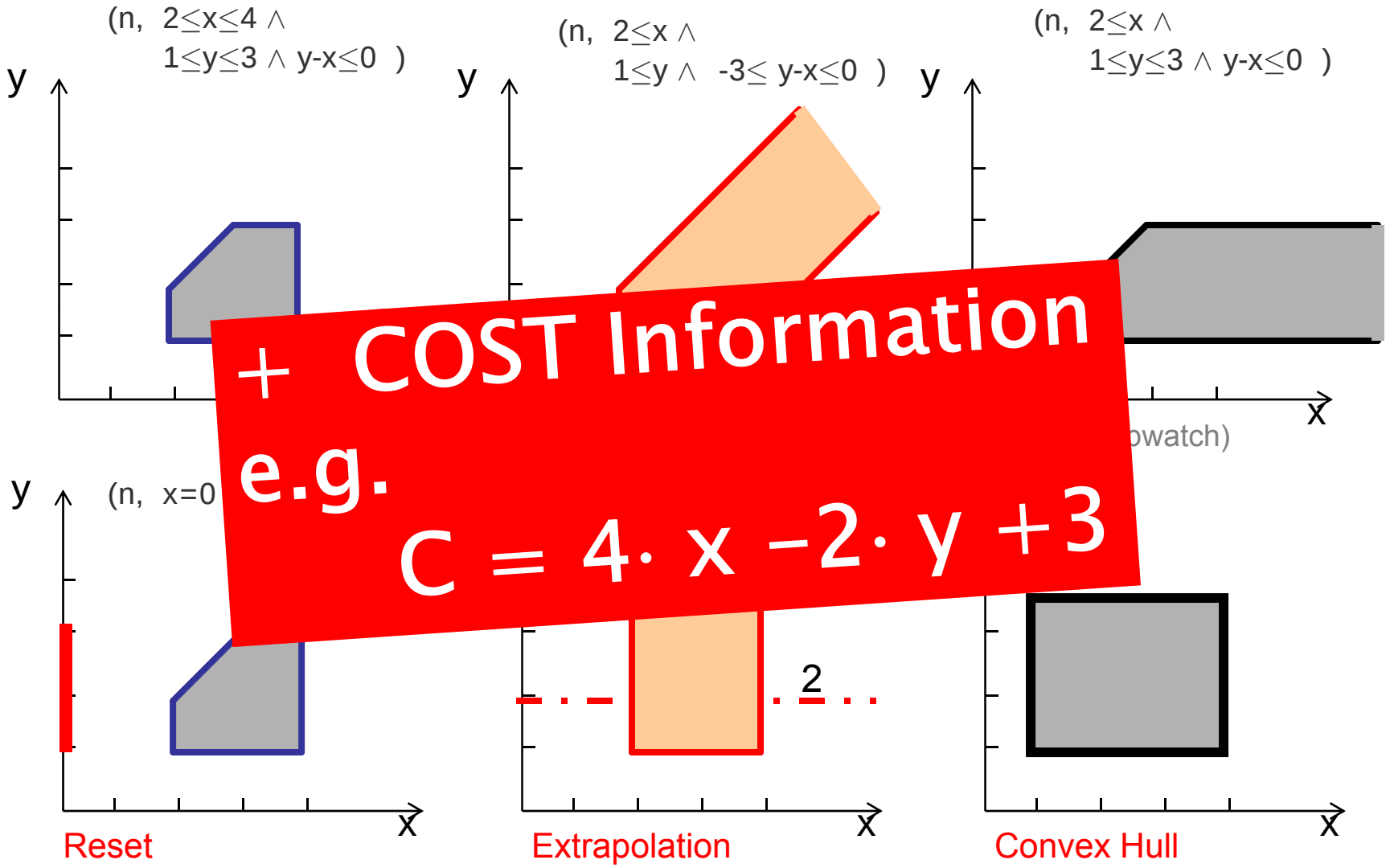


Symbolic state (set)

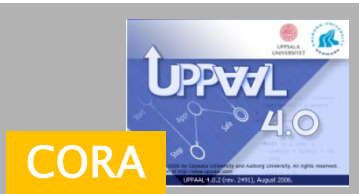
(n, $2 \leq x \leq 4 \wedge$
$1 \leq y \leq 3 \wedge$
$y-x \leq 0$)



Zones – Operations



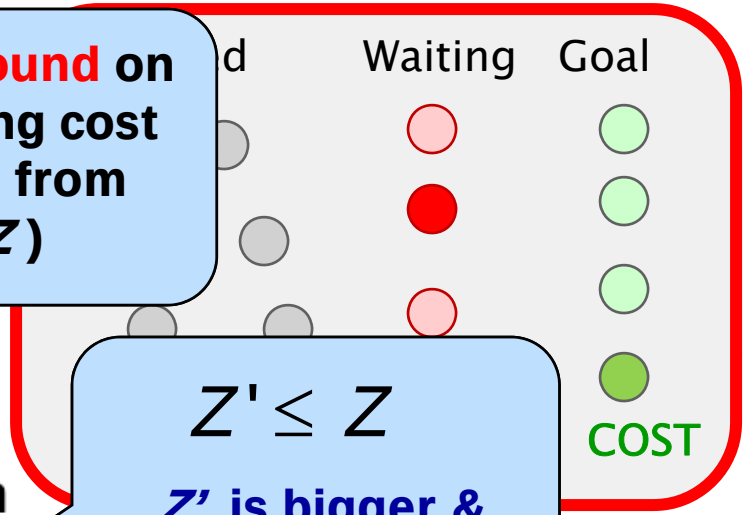
Symbolic B & B Algorithm



CORA

Cost := ∞
Passed := $\emptyset$
Waiting := $\{(l_0, Z_0)\}$
while Waiting $\neq \emptyset$ **do**
  select (l, Z) from Waiting
  if $l = l_g$ and minCost(Z) < Cost **then**
    Cost := minCost(Z)
  if minCost(Z) + $\text{Rem}_{(l,Z)} \geq$ Cost **then** break
  if for all (l, Z') in Passed: $Z' \not\leq Z$ **then**
    $\rightarrow (l', Z')$

Lower bound on remaining cost to goal from (*l,Z*)



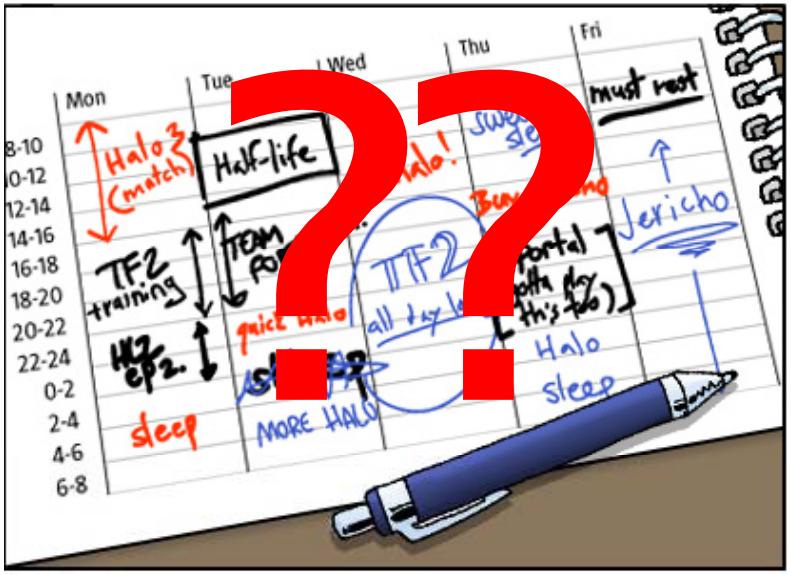
$Z' \leq Z$

Z'* is bigger & cheaper than *Z

Competitive to MIPL on a number of benchmarks, e.g. Aircraft Landing

$\leq$ is a well-quasi ordering which guarantees termination!

Schedulability Analysis



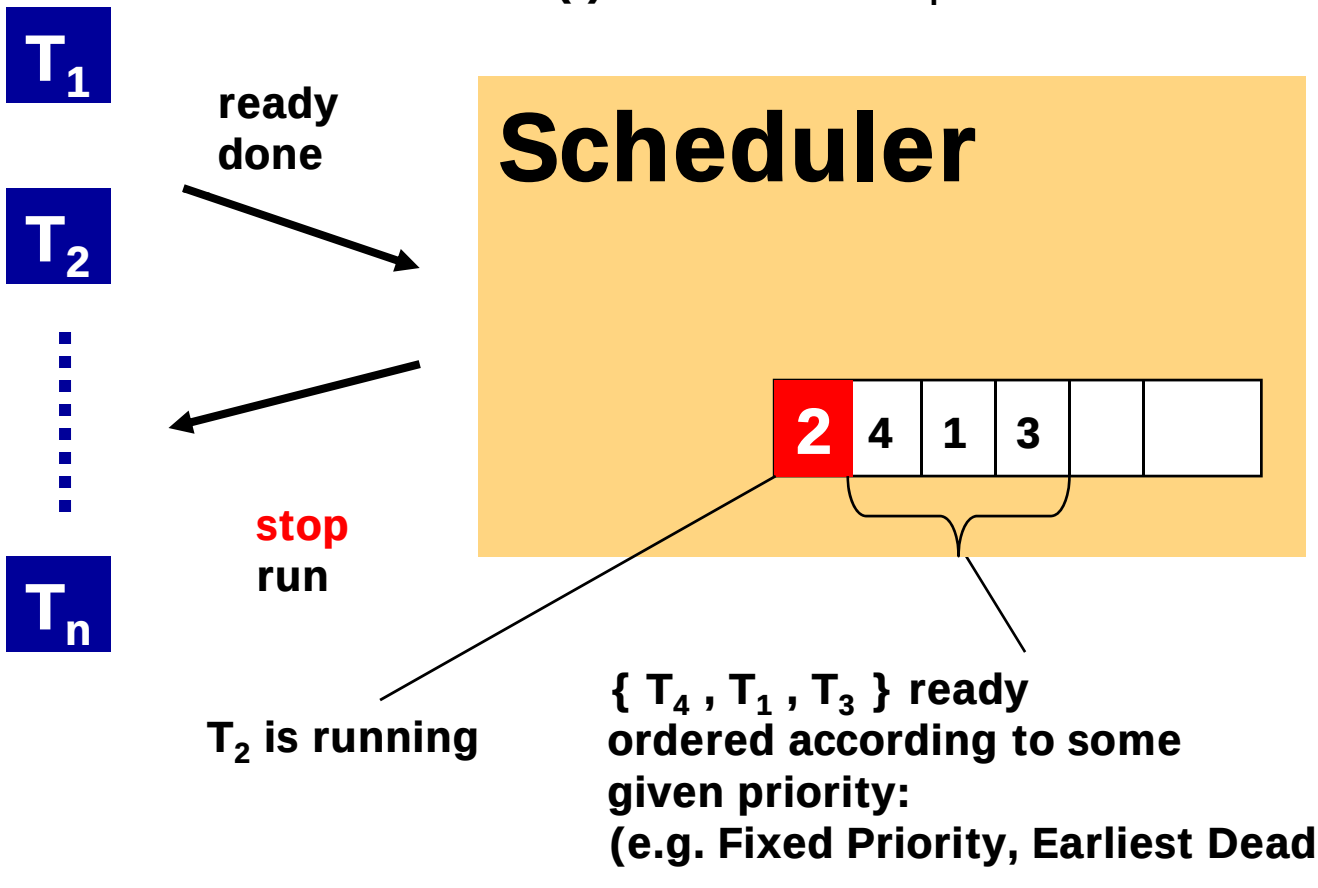
Task Scheduling

utilization of CPU

P(i), [E(i), L(i)], .. : period or earliest/latest arrival or .. for T_i

C(i): execution time for T_i

D(i): deadline for T_i



Classical Scheduling Theory

Utilisation-Based Analysis

- A simple sufficient but not necessary schedulability test exists

$$U \equiv \sum_{i=1}^{N} \frac{C_i}{T_i} \leq N\,(2^{1/N} - 1)$$

$$U \leq 0.69 \text{ as } N \to \infty$$

Where C is WCET and T is period

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Response Time Equation

$$R_i = C_i + \sum_{j \in hp(i)} \left\lceil \frac{R_i}{T_j} \right\rceil C_j$$

Where $hp(i)$ is the set of tasks with priority higher than task i

Solve by forming a recurrence relationship:

$$w_i^{n+1} = C_i + \sum_{j \in hp(i)} \left\lceil \frac{w_i^n}{T_j} \right\rceil C_j$$

The set of values $w_i^0, w_i^1, w_i^2, \ldots, w_i^n, \ldots$ is monotonically non decreasing
When $w_i^n = w_i^{n+1}$ the solution to the equation has been found, w_i^0 must not be greater that R_i (e.g. 0 or C_i)

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Classical WCRT Analysis

Quasimodo

- "Classical" scheduling analysis technique
- *For all tasks i: WCRT$_i \leq$ Deadline$_i$*

$$R_i = B_i + C_i + \sum_{j \in hp(i)} \left\lceil \frac{R_i}{T_j} \right\rceil C_j$$

Blocking times for priority inheritance protocol (BSW):

$$Blocking(i) = \sum_{r=1}^{R} usage(r,i)\,WCET_{CriticalSection}(r)$$

Blocking times for priority ceiling protocol (ASW):

$$Blocking(i) = \max_{r=1}^{R} usage(r,i)\,WCET_{CriticalSection}(r)$$

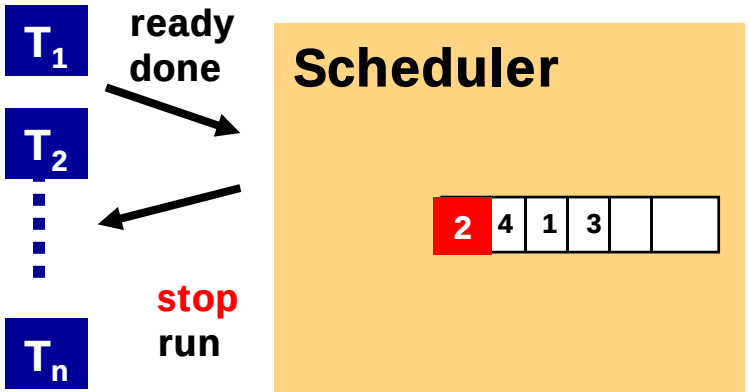
Quasimodo Workshop, Eindhoven, Nov 6, 2009 Page 21

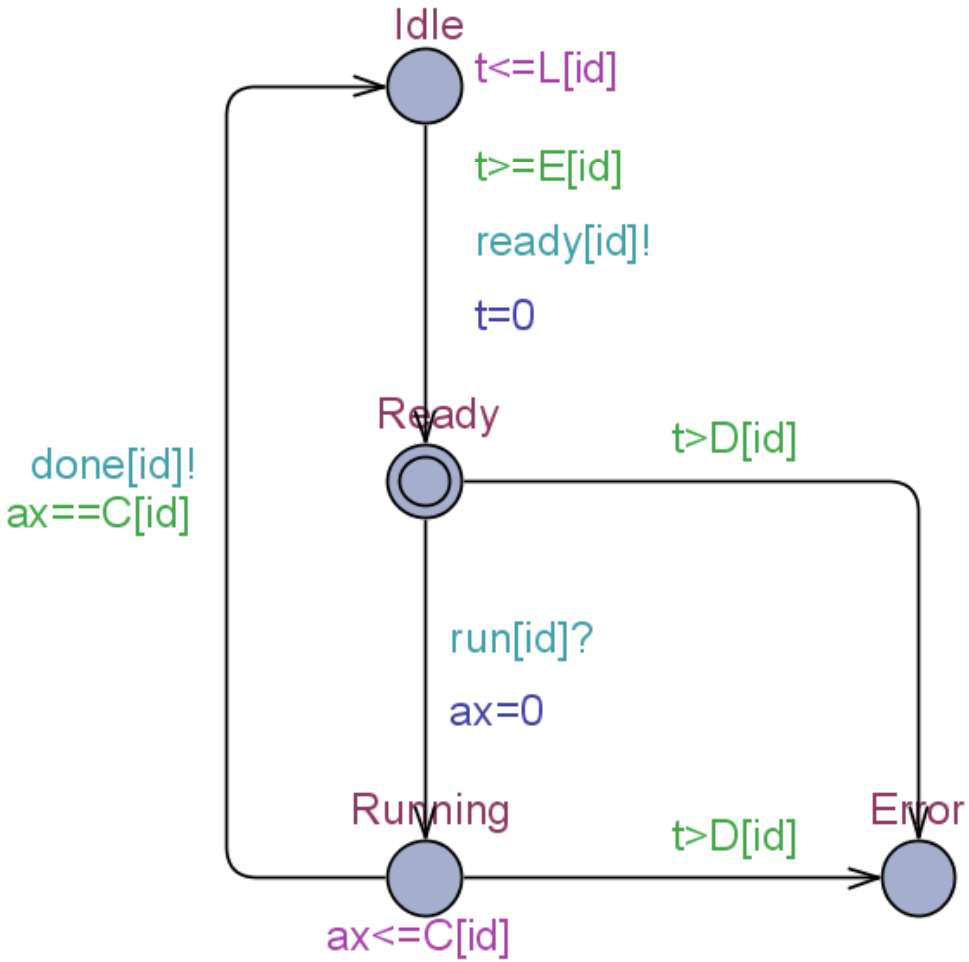
✓ Simple to perform

– Overly conservative
– Limited settings
– Single-processor

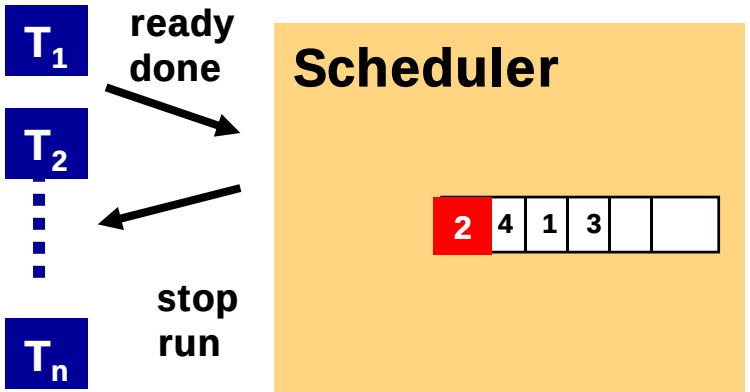
✓ Tomorrow: Sanjoy Baruah

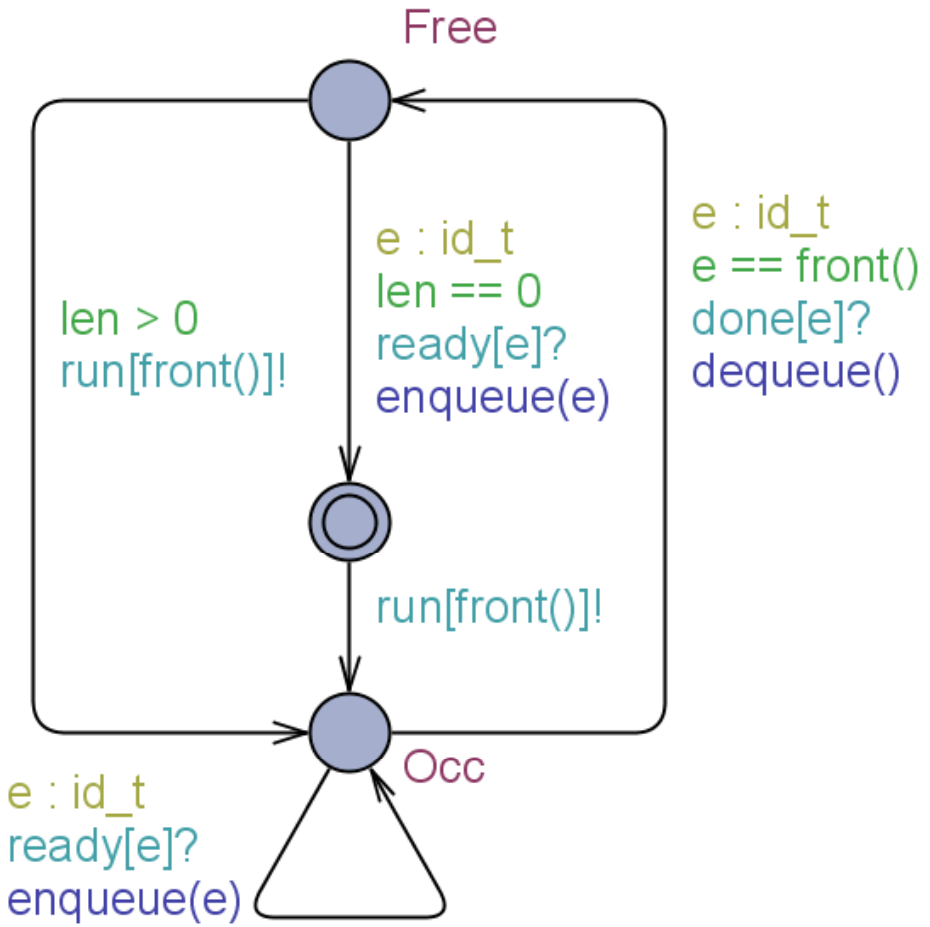
Modeling Task





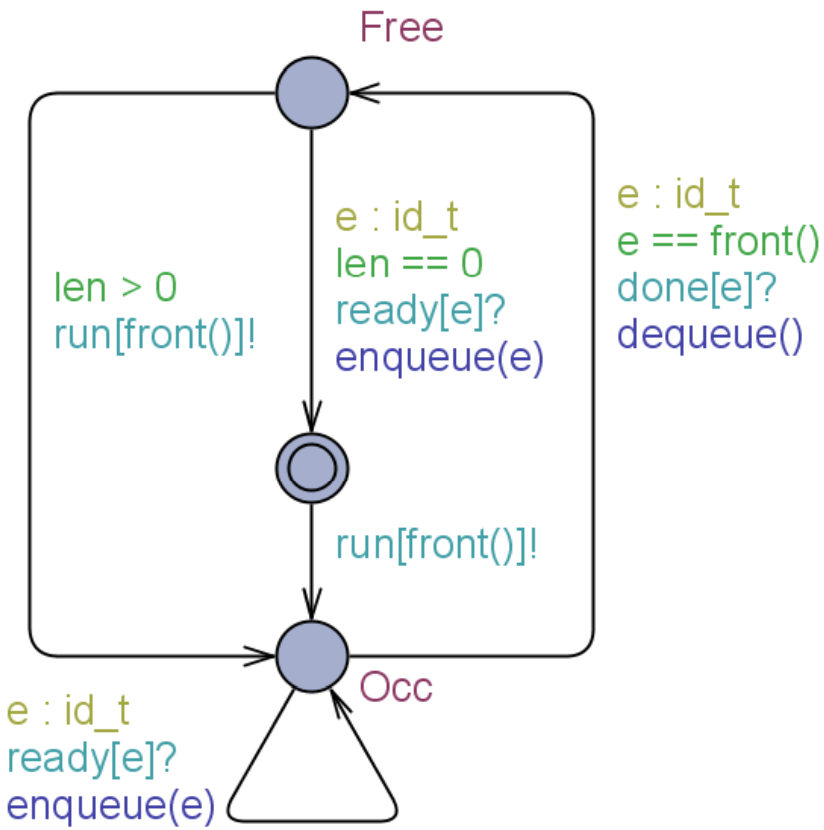
Modeling Scheduler





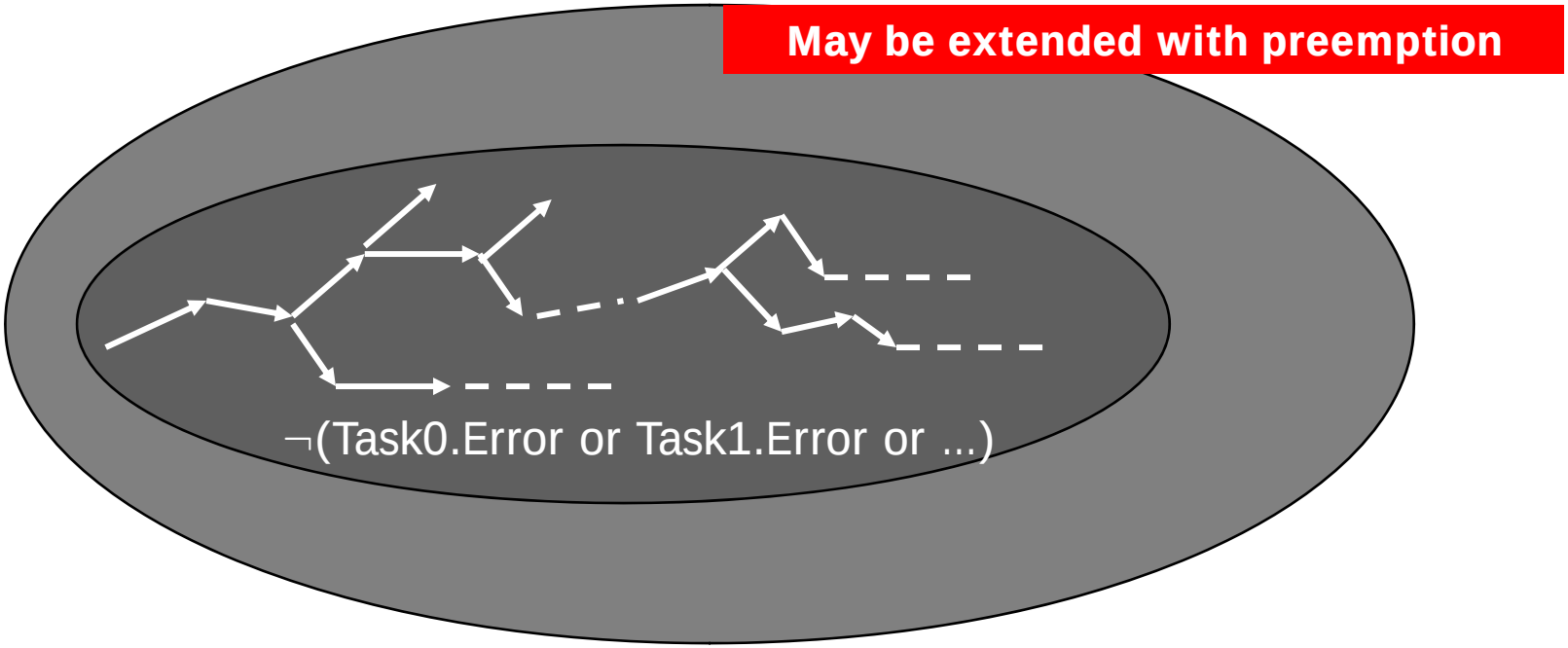
Modeling Queue

In UPPAAL 4.0
User Defined Function



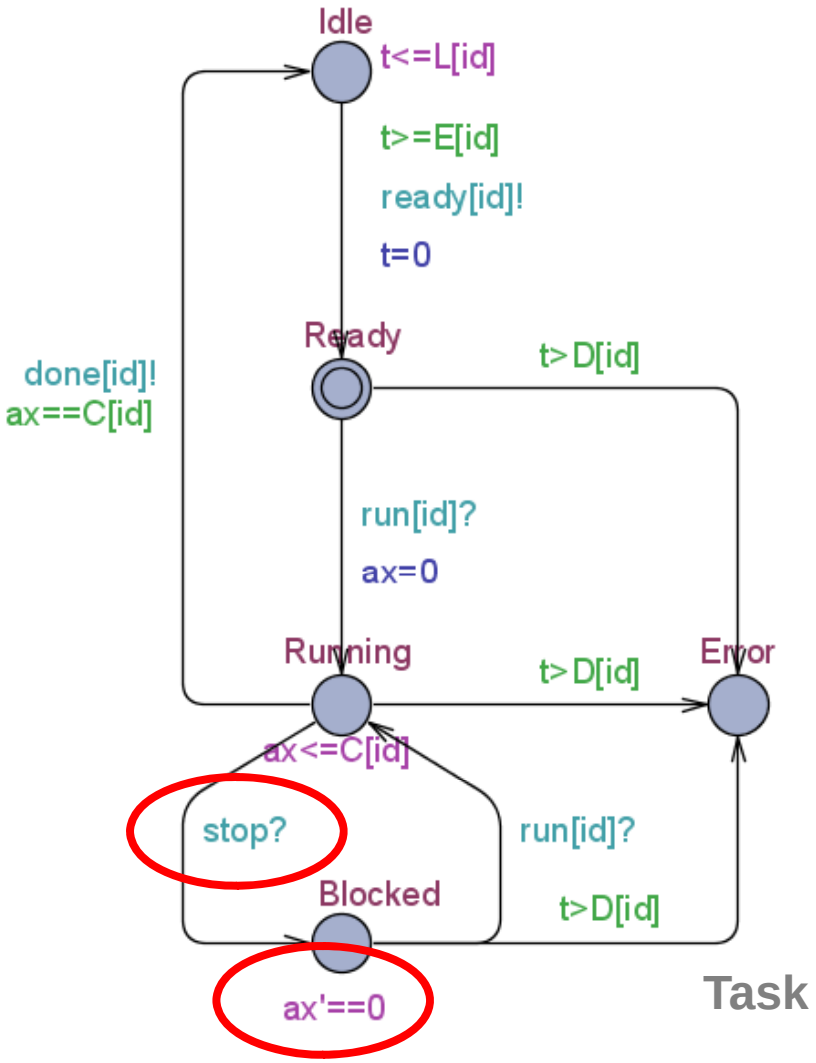

```
// Put an element at the end of the queue
void enqueue(id_t element)
{
int tmp=0;
list[len++] = element;
if (len>0)
{
        int i=len-1;
        while (i>1 && P[list[i]]>P[list[i-1]])
        {
                tmp = list[i-1];
                list[i-1] = list[i];
                list[i] = tmp;
                i--;
        }
}
}

// Remove the front element of the queue
void dequeue()
{
  .....
```

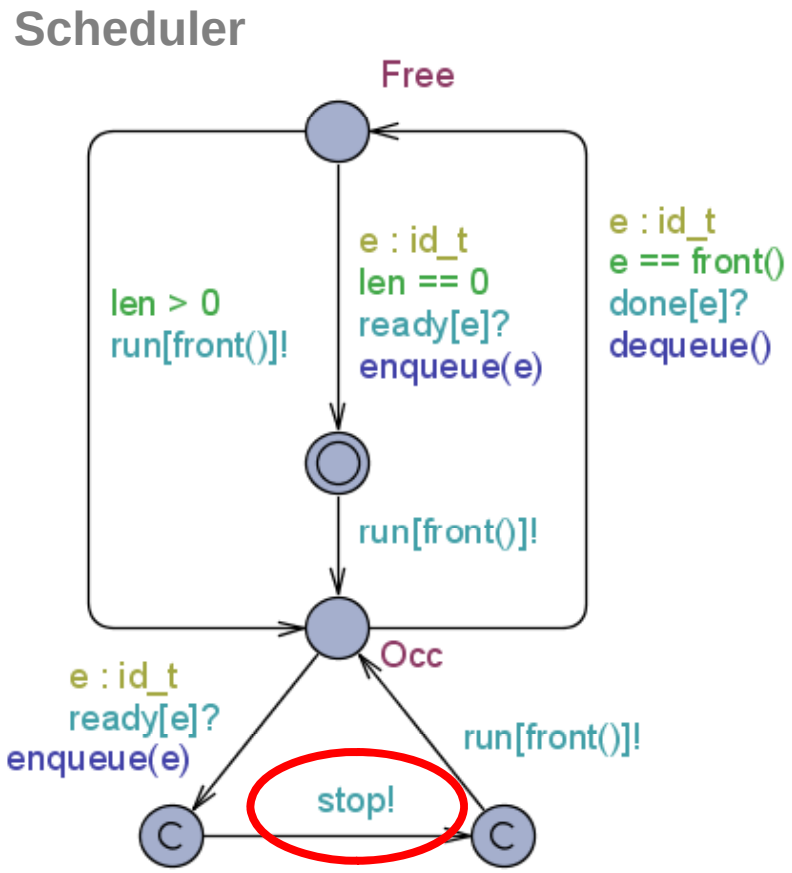
Schedulability = Safety Property



A□ ¬(Task0.Error or Task1.Error or ...)

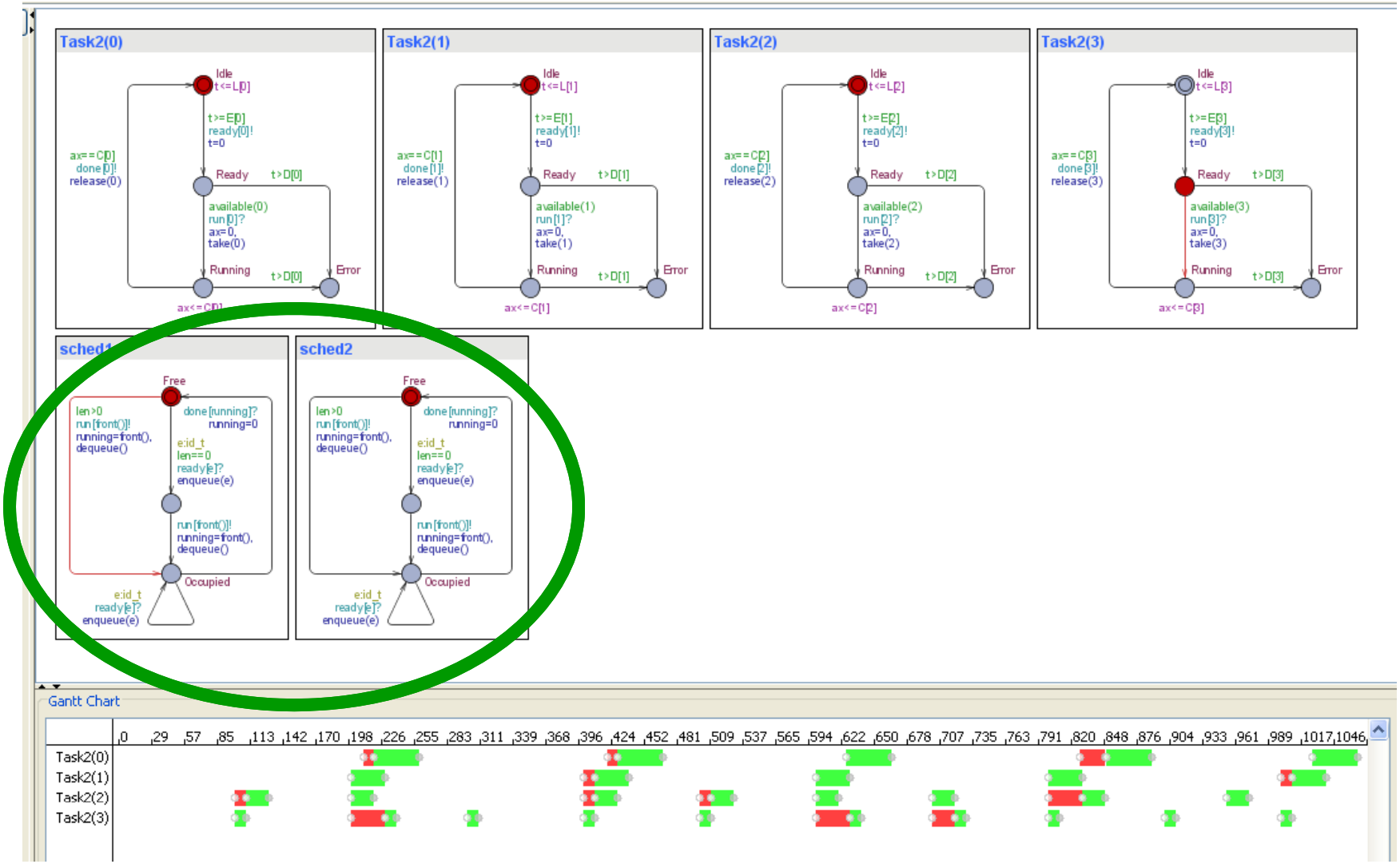
Preemption – Stopwatches!





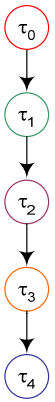
Defeating undecidability ☺

Multi-Processor

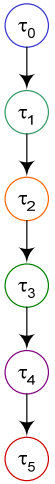


Handling realistic applications?

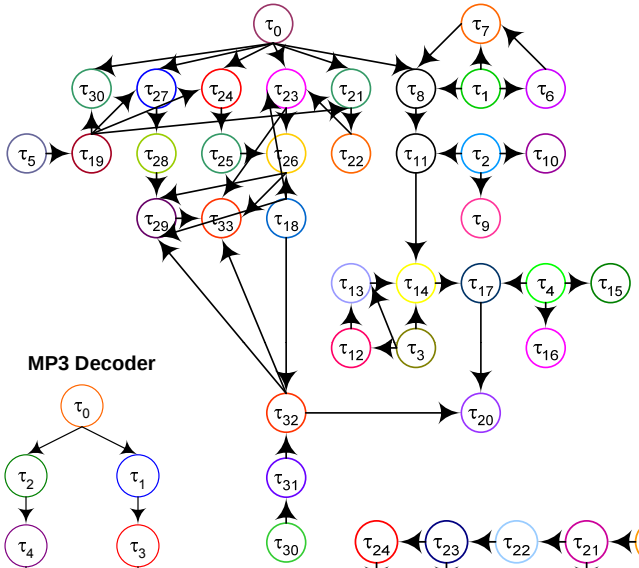
JPEG Encoder



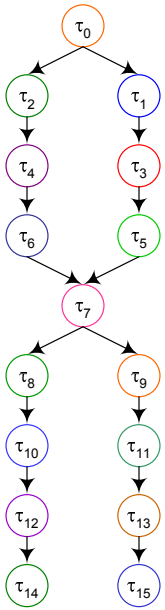
JPEG Decoder



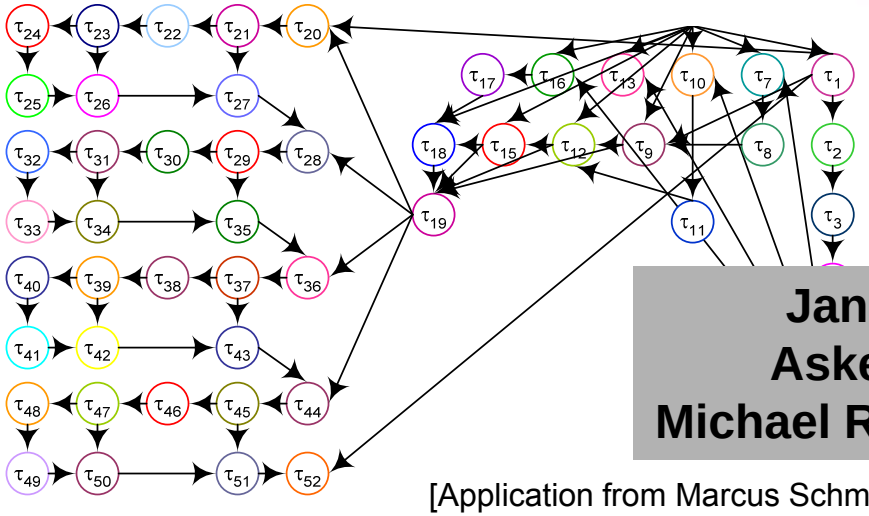
GSM Decoder



MP3 Decoder



GSM Encoder

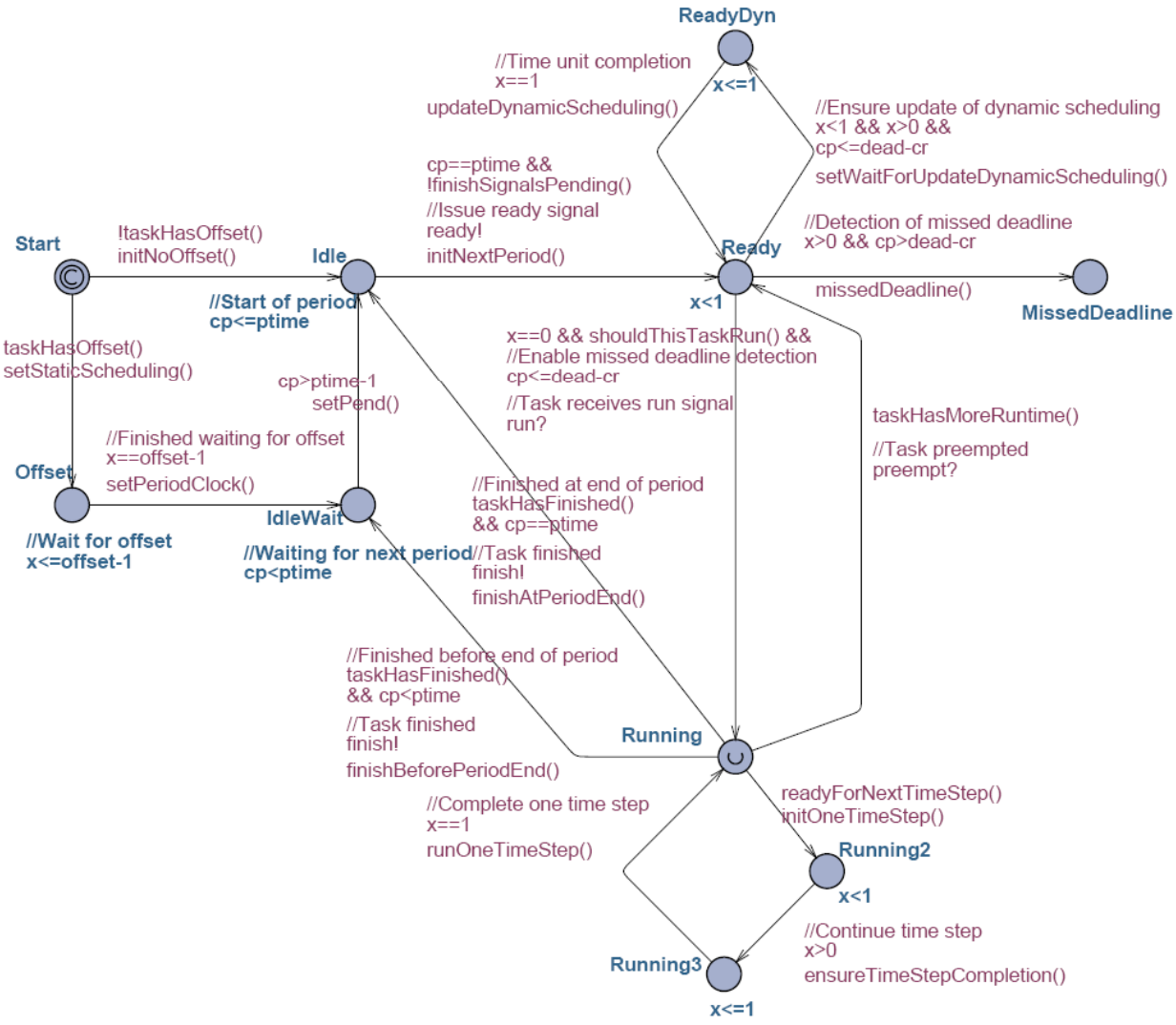


Smart phone:

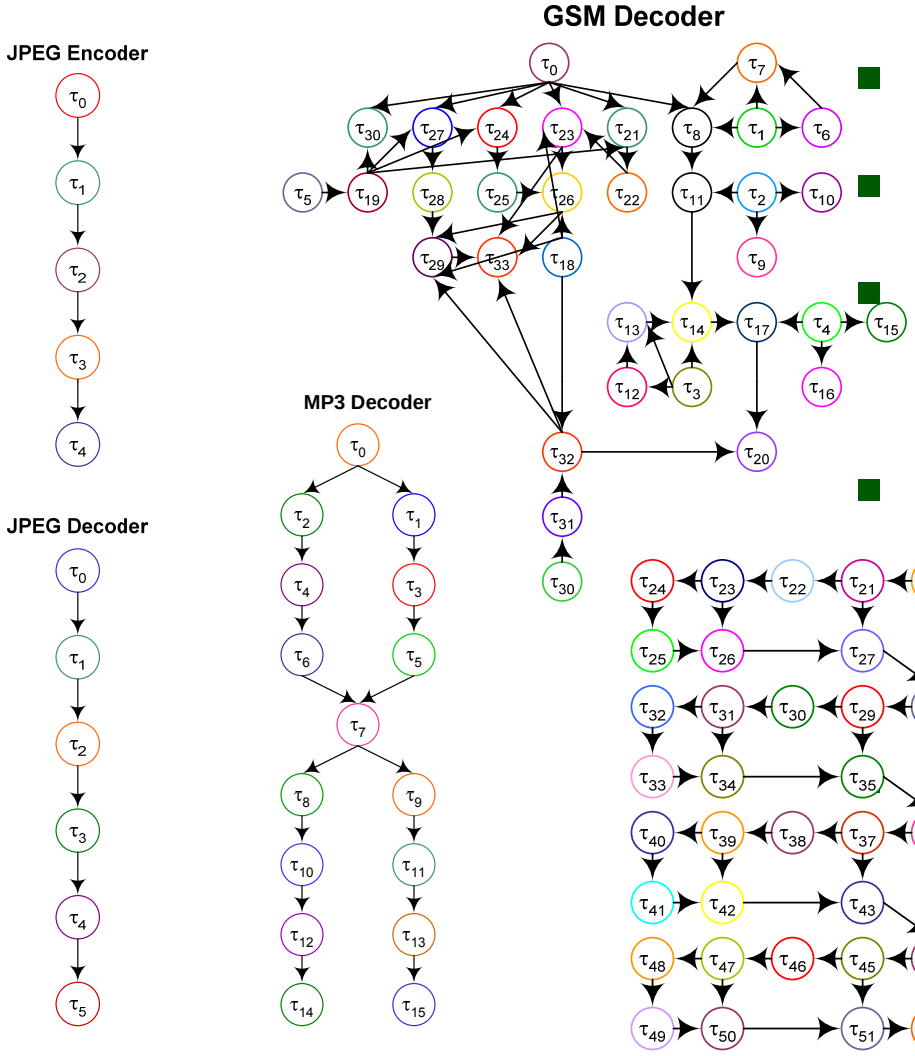
Jan Madsen
Aske Brekling
Michael R. Hansen/ DTU

[Application from Marcus Schmitz, TU Linkoping]

Timed Automata for a task



Smart phone

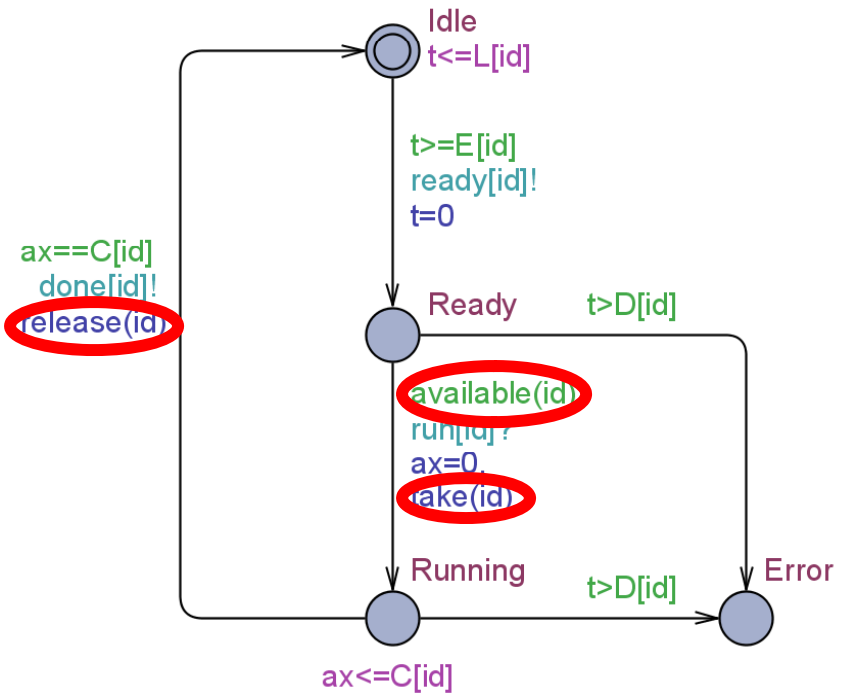


- Tasks: 114
- Deadlines: [0.02: 0.5] sec
- Execution: [52 : 266.687] cycles
- Platform:
  - 6 processors, 25 MHz
  - 1 bus

Verified in 1.5 hours!

Dealing with Resources

```
bool resource[N];

bool available(id_t id)
{
    return !resource[need[id]];
}

void take(id_t id)
{
    assert(!resource[need[id]]);
    resource[need[id]] = true;
}

void release(id_t id)
{
    assert(resource[need[id]]);
    resource[need[id]] = false;
}
```

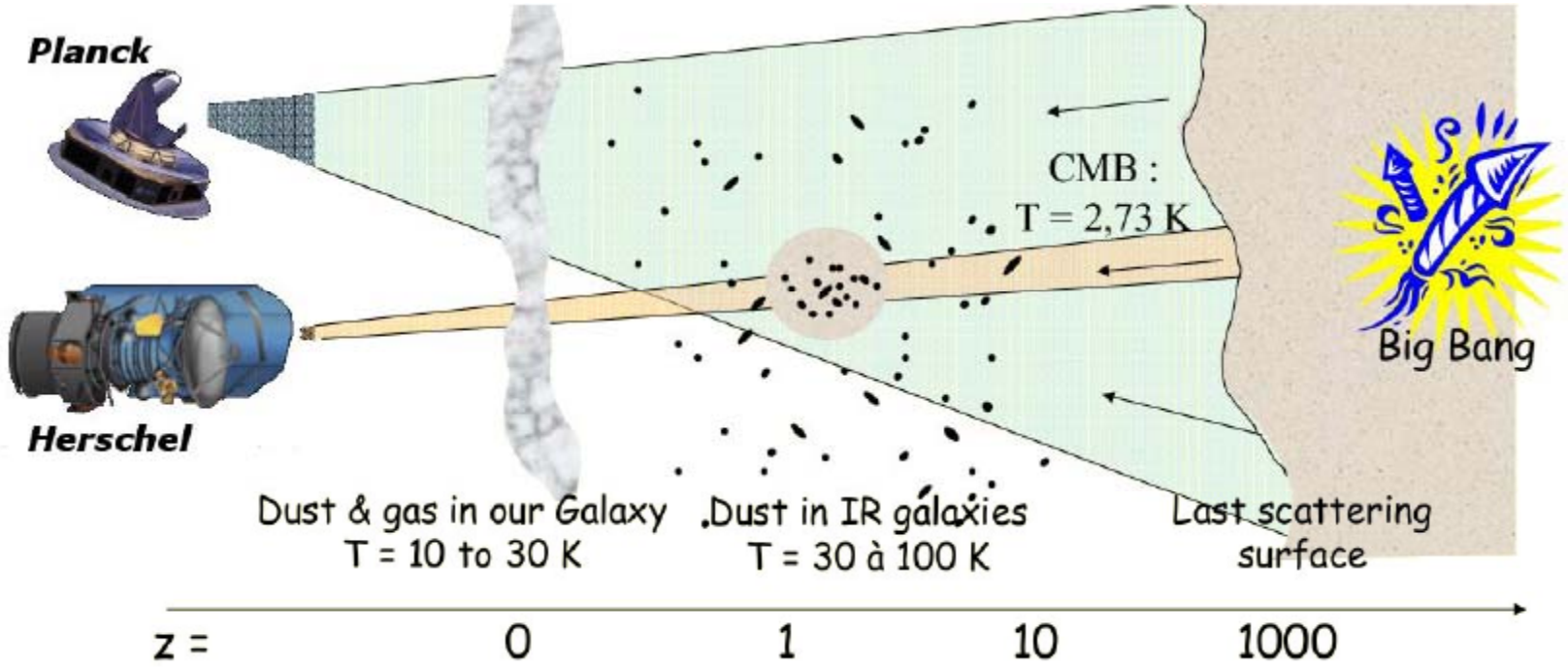


ESA Missions

TERMA

Quasiomodo

- Solar System, cold dust clouds and cores, star and galaxy formations, cataloging galaxies, gravitational lensing, cosmic microwave background, topology of the universe...

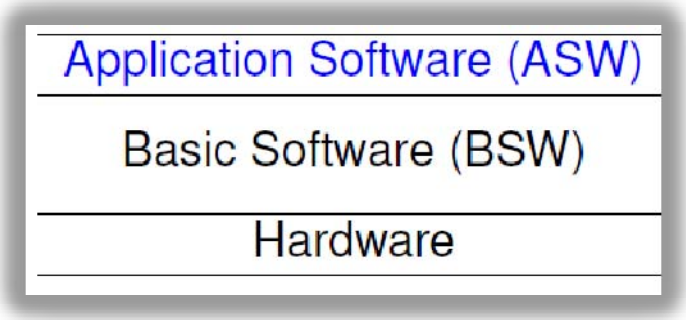


- Terma: Develop software for Attitude and Orbit Control System

Herschel & Planck Satelites

TERMA

- Application software (ASW)
  - built and tested by Terma:
  - does attitude and orbit control, tele-commanding, fault detection isolation and recovery.
- Basic software (BSW)
  - low level communication and scheduling periodic events.
- Real-time operating system (RTEMS)
  - Priority Ceiling for ASW,
  - Priority Inheritance for BSW
- Hardware
  - single processor, a few buses, sensors and act



Requirements:

Software tasks should be schedulable.
CPU utilization should not exceed 50% load

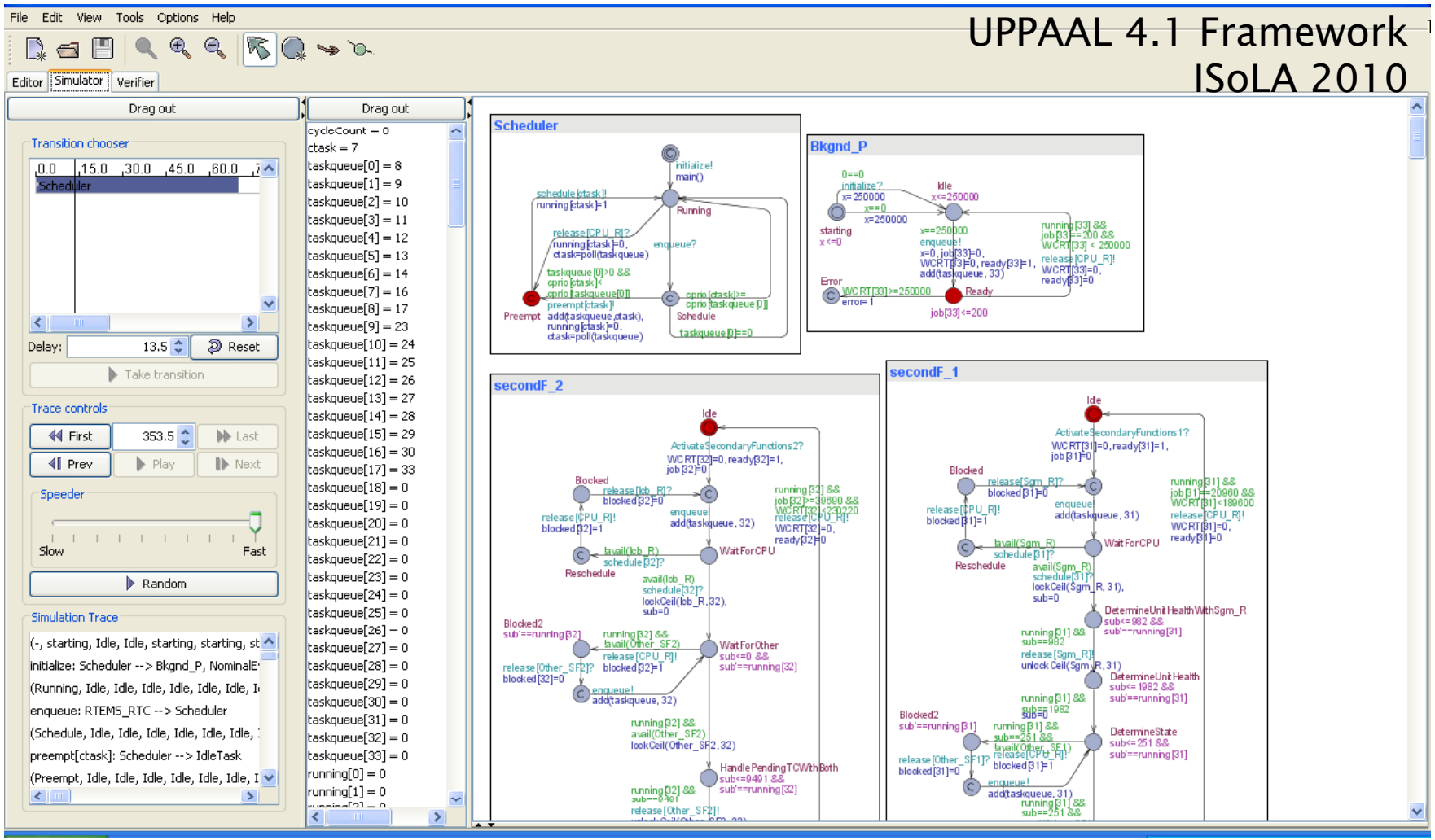
UPPAAL Model

TERMA

- One template for CPU scheduler:
  - maintains a queue of ready tasks
  - schedules tasks with highest priority in the queue
  - reschedule if higher priority task arrives to the queue
- One template per **each** ASW task.
- Two templates for BSW tasks: 1 plain, 1 using resource.
- One template for "idle" task to count CPU utilization.
- WCET is modeled by stopwatches and lower bound.
- WCRT is modeled by stopwatches.
- Deadline is enforced as guard on WCRT.
- System is schedulable if no deadline violated.
- CPU load is $\frac{\text{used time}}{\text{total time}}$.

Modeling in UPPAAL

TERMA



UPPAAL 4.1 Framework
ISoLA 2010

Gantt Chart 1. cycle

TERMA

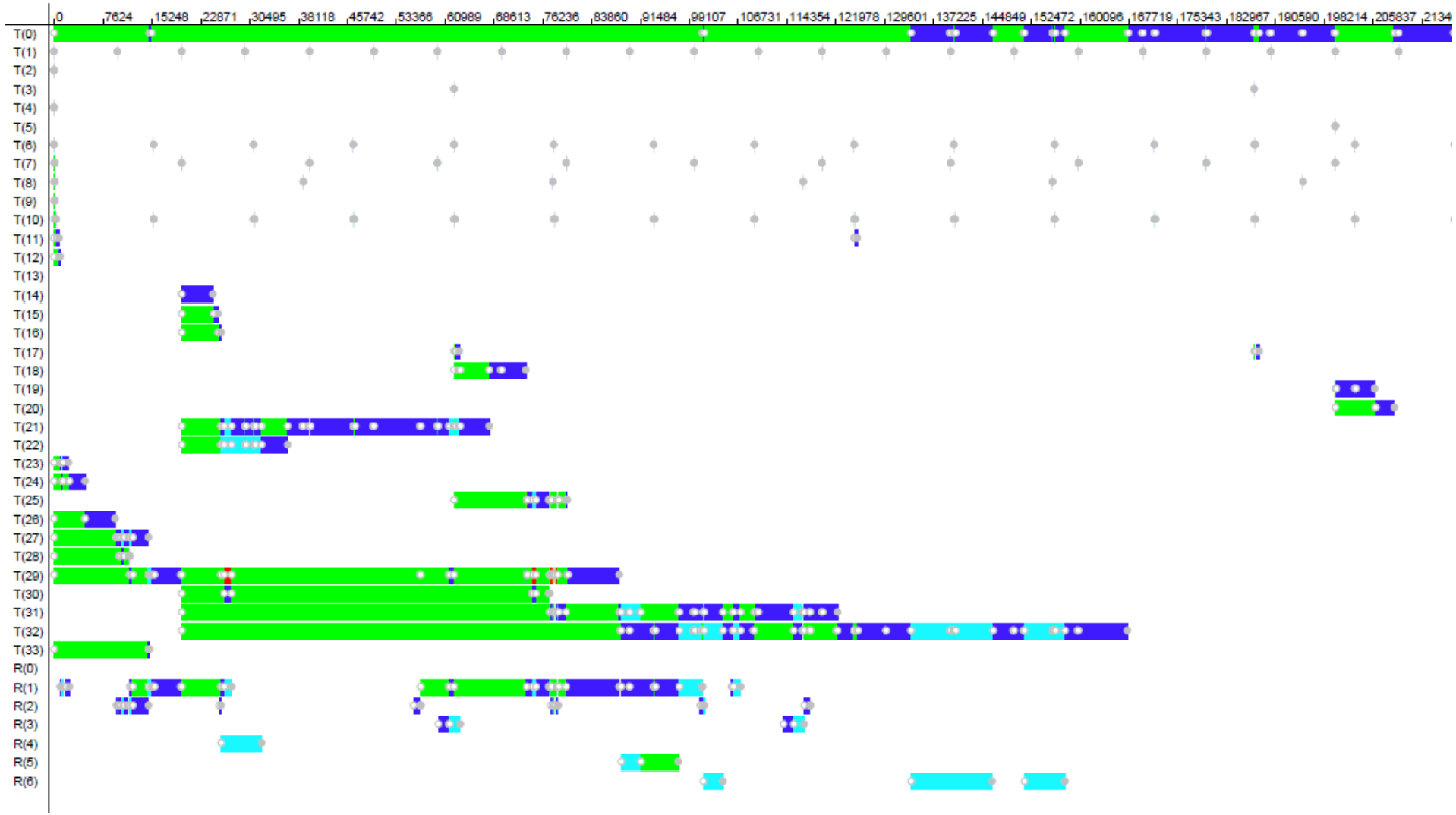


Fig. 11. Gantt chart of a schedule from the first cycle: green means ready, blue means running, cyan means suspended, red means blocked. R stand for resources: CPU_R=0, Icb_R=1, Sgm_R=2, PmReq_R=3, Other_RCS=4, Other_SF1=5, Other_SF2=6.

Blocking & WCRT

TERMA

ID	Task	Specification			Blocking times			WCRT		
		Period	WCET	Deadline	Terma	UPPAAL	Diff	Terma	UPPAAL	Diff
1	RTEMS_RTC	10.000	0.013	1.000	0.035	0	0.035	0.050	0.013	0.037
2	AswSync_SyncPulseIsr	250.000	0.070	1.000	0.035	0	0.035	0.120	0.083	0.037
3	Hk_SamplerIsr	125.000	0.070	1.000	0.035	0	0.035	0.120	0.070	0.050
4	SwCyc_CycStartIsr	250.000	0.200	1.000	0.035	0	0.035	0.320	0.103	0.217
5	SwCyc_CycEndIsr	250.000	0.100	1.000	0.035	0	0.035	0.220	0.113	0.107
6	Rt1553_Isr	15.625	0.070	1.000	0.035	0	0.035	0.290	0.173	0.117
7	Bc1553_Isr	20.000	0.070	1.000	0.035	0	0.035	0.360	0.243	0.117
8	Spw_Isr	39.000	0.070	2.000	0.035	0	0.035	0.430	0.313	0.117
9	Obdh_Isr	250.000	0.070	2.000	0.035	0	0.035	0.500	0.383	0.117
10	RtSdb_P_1	15.625	0.150	15.625	3.650	0	3.650	4.330	0.533	3.797
11	RtSdb_P_2	125.000	0.400	15.625	3.650	0	3.650	4.870	0.933	3.937
12	RtSdb_P_3	250.000	0.170	15.625	3.650	0	3.650	5.110	1.103	4.007
14	**FdirEvents**	250.000	5.000	230.220	0.720	0	0.720	7.180	5.153	2.027
15	**NominalEvents_1**	250.000	0.720	230.220	0.720	0	0.720	7.900	5.873	2.027
16	**MainCycle**	250.000	0.400	230.220	0.720	0	0.720	8.370	6.273	2.097
17	HkSampler_P_2	125.000	0.500	62.500	3.650	0	3.650	11.960	5.380	6.580
18	HkSampler_P_1	250.000	6.000	62.500	3.650	0	3.650	18.460	11.615	6.845
19	Acb_P	250.000	6.000	50.000	3.650	0	3.650	24.680	6.473	18.207
20	IoCyc_P	250.000	3.000	50.000	3.650	0	3.650	27.820	9.473	18.347
21	**PrimaryF**	250.000	34.050	59.600	5.770	0.966	4.804	65.470	54.115	11.355
22	**RCSControlF**	250.000	4.070	239.600	12.120	0	12.120	76.040	53.994	22.046
23	Obt_P	1000.000	1.100	100.000	9.630	0	9.630	74.720	2.503	72.217
24	Hk_P	250.000	2.750	250.000	1.035	0	1.035	6.800	4.953	1.847
25	StsMon_P	250.000	3.300	125.000	16.070	0.822	15.248	85.050	17.863	67.187
26	TmGen_P	250.000	4.860	250.000	4.260	0	4.260	77.650	9.813	67.837
27	Sgm_P	250.000	4.020	250.000	1.040	0	1.040	18.680	14.796	3.884
28	TcRouter_P	250.000	0.500	250.000	1.035	0	1.035	19.310	11.896	7.414
29	Cmd_P	250.000	14.000	250.000	26.110	1.262	24.848	114.920	94.346	20.574
30	**NominalEvents_2**	250.000	1.780	230.220	12.480	0	12.480	102.760	65.177	37.583
31	**SecondaryF_1**	250.000	20.960	189.600	27.650	0	27.650	141.550	110.666	30.884
32	**SecondaryF_2**	250.000	39.690	230.220	48.450	0	48.450	204.050	154.556	49.494
33	Bkgnd_P	250.000	0.200	250.000	0.000	0	0.000	154.090	15.046	139.044

Marius Micusionis

Effort and Utilization

TERMA

cycle limit	Uppaal resources CPU, s	Mem, KB	States, #	Herschel CPU utilization Idle, μs	Used, μs	Global, μs	Sum, μs	Used, %
1	465.2	60288	173456	91225	160015	250000	251240	0.640060
2	470.1	59536	174234	182380	318790	500000	501170	0.637580
3	461.0	58656	175228	273535	477705	750000	751240	0.636940
4	474.5	58792	176266	363590	636480	1000000	1000070	0.636480
6	474.6	58796	178432	545900	955270	1500000	1501170	0.636847
8	912.3	58856	352365	727110	1272960	2000000	2000070	0.636480
13	507.7	58796	186091	1181855	2069385	3250000	3251240	0.636734
16	1759.0	58728	704551	1454220	2545850	4000000	4000070	0.636463
26	541.9	58112	200364	2363640	4137530	6500000	6501170	0.636543
32	3484.0	75520	1408943	2908370	5091700	8000000	8000070	0.636463
39	583.5	74568	214657	3545425	6205745	9750000	9751170	0.636487
64	7030.0	91776	2817704	5816740	10183330	16000000	16000070	0.636458
78	652.2	74768	257582	7089680	12411420	19500000	19501100	0.636483
128	14149.4	141448	5635227	11633480	20366590	32000000	32000070	0.636456
156	789.4	91204	343402	14178260	24821740	39000000	39000000	0.636455
256	23219.4	224440	11270279	23266890	40733180	64000000	64000070	0.636456
312	1824.6	124892	686788	28356520	49643480	78000000	78000000	0.636455
512	49202.2	390428	22540388	46533780	81466290	128000000	128000070	0.636455
624	3734.7	207728	1373560	56713040	99286960	156000000	156000000	0.636455

Marius Micusionis

TERMA Case Conclusion

- Schedulability analysis using UPPAAL:
  - Reusable and customizable task templates.
  - *Blocking* times and WCRTs can be derived from the model.
  - WCRTs of all tasks are more optimistic than in RTA.
  - There are very few blocking times and they are short.
  - PrimaryF meets deadline (59.6ms) with WCRT=54.1ms (65.5ms in RTA).
  - Herschel event mode is **schedulable**.
- UPPAAL verification for schedulability:
  - can be **scaled** using sweep-line method,
  - takes up to **2min** to verify schedulability of 32 task system,
  - takes up to **8min** to find all WCRTs and CPU utilization.
- In addition, it is possible to:
  - simulate the system model and examine details,
  - render a Gantt chart, validate and inspect visually.

TERMA Case Follow-Up

% : difference In BCET and

limit: no of 250ms cycles

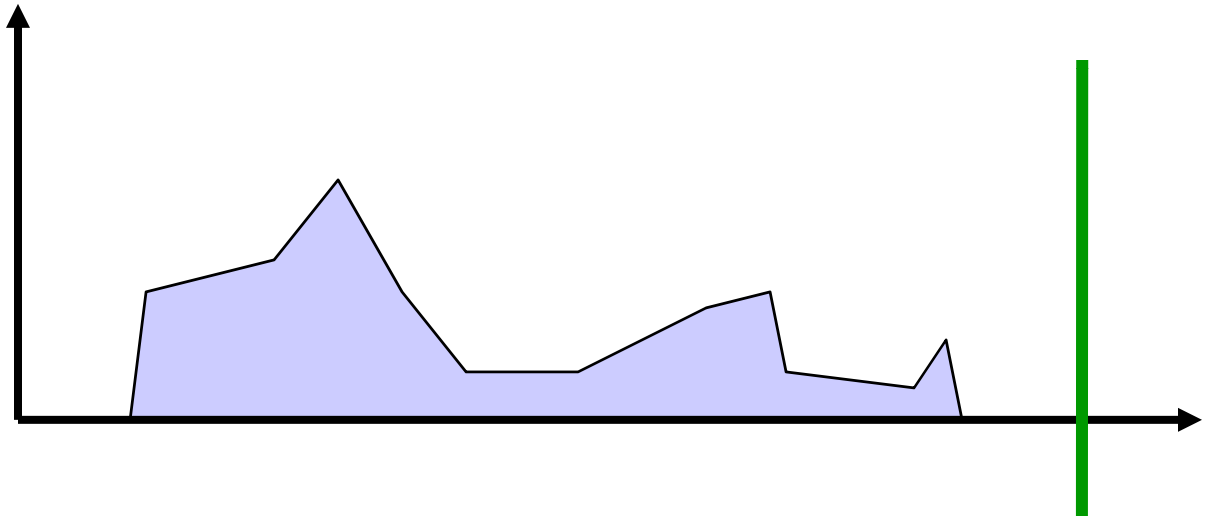
1 Day

6 Days

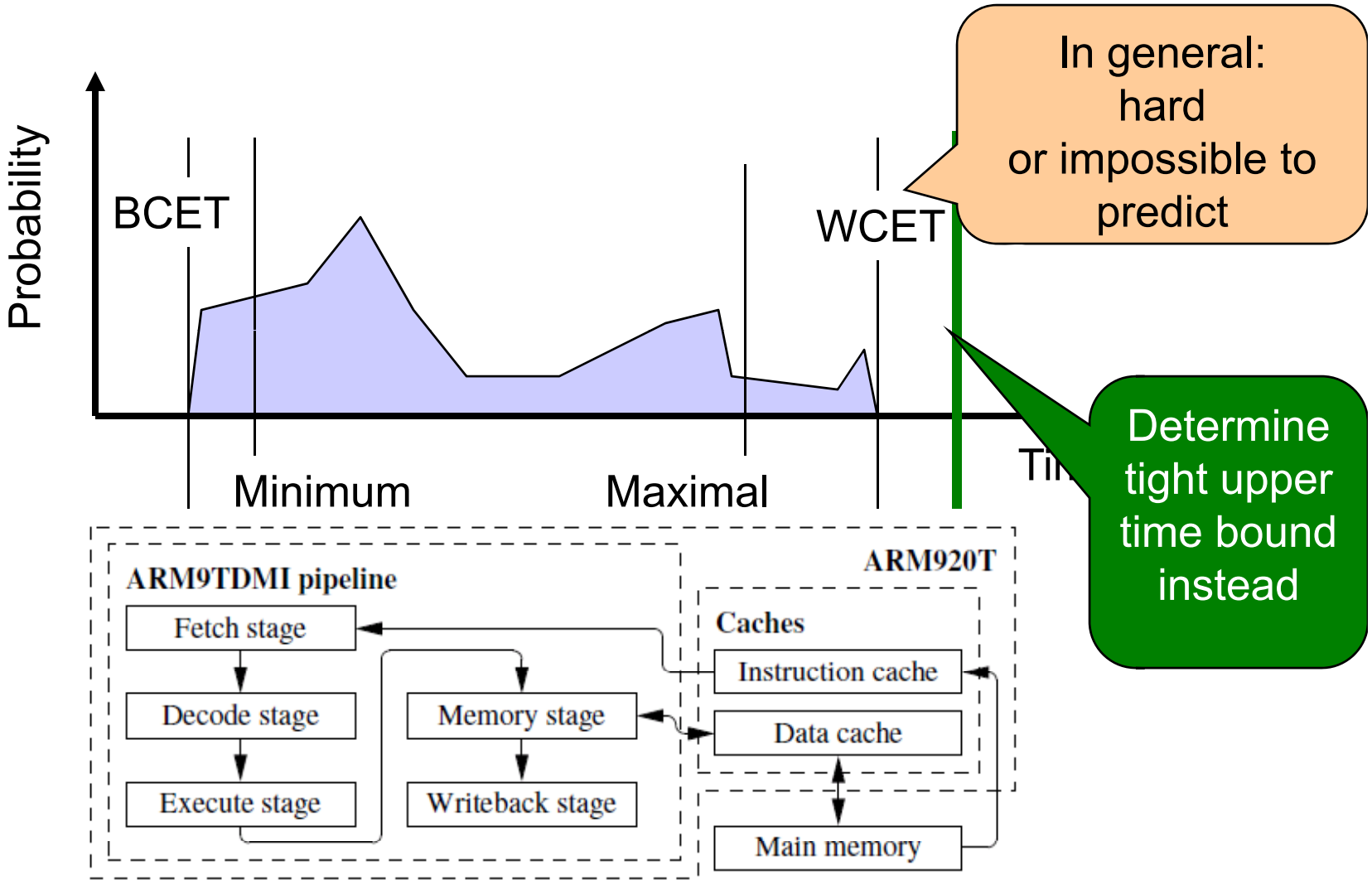
limit	0%			5%		
	states	mem	time	states	mem	ti
1	1300	51.2	1.47	485077	83.0	90
2	2522	53.7	2.45	806914		
4	4981	54.5	4.62	1499700		.8
8						
16						
∞	1					

10%			14%		
states	mem	time, s	states	mem	time
1481162	124.1	4962.8	3348246	186.9	23986.5
2414679	139.7	7755	5253778	198.7	33299.2
4421630	138.3	13720	9231399	274.6	51176.6
9093562	156.5	3112.3	18240030	364.6	102932.4
17798572	176.0	6012.5	35432003	520.4	158816.7
181869652	1682.2	530604.9	error may be reachable		

WCET Analysis



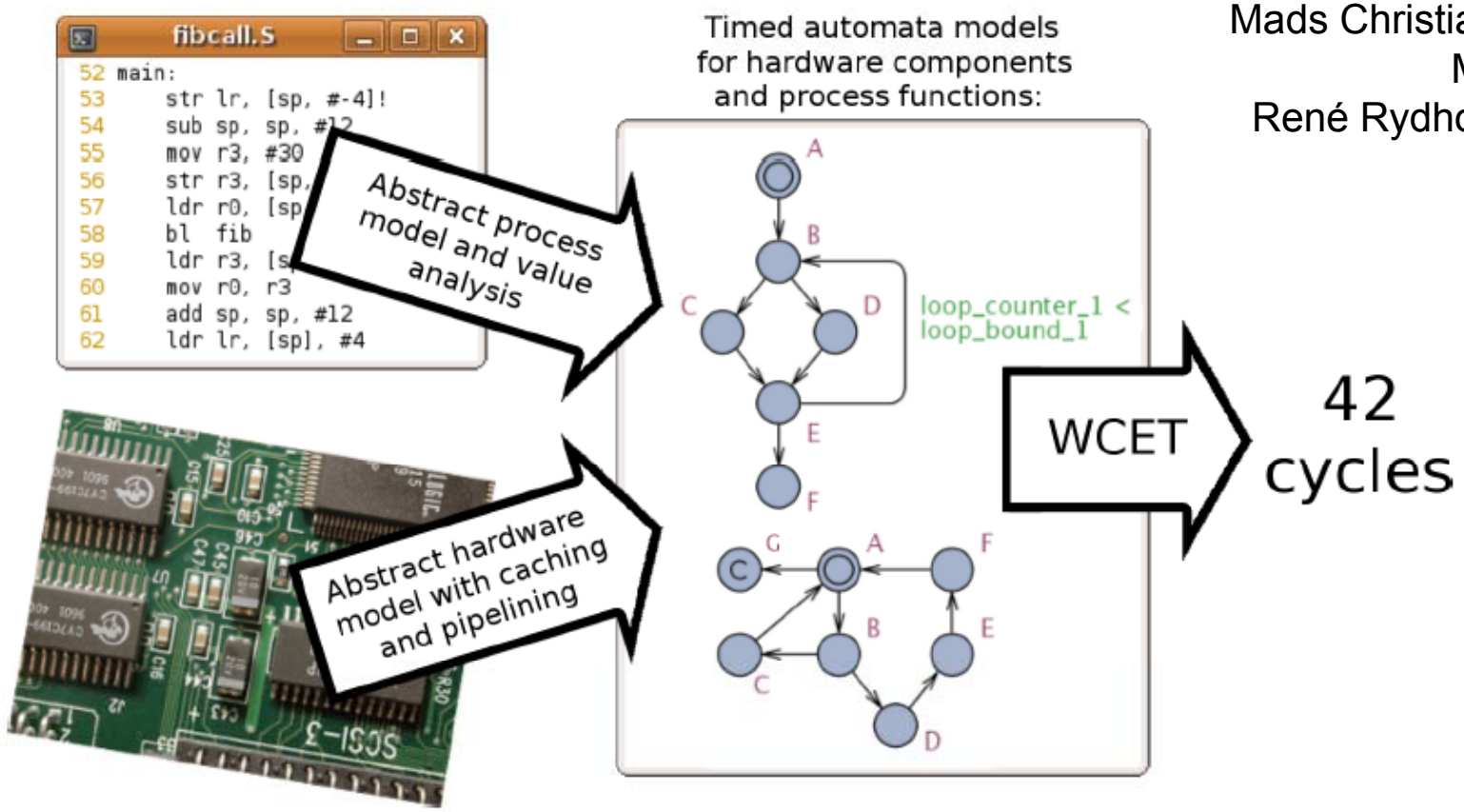
WCET: Worst Case Execution Time



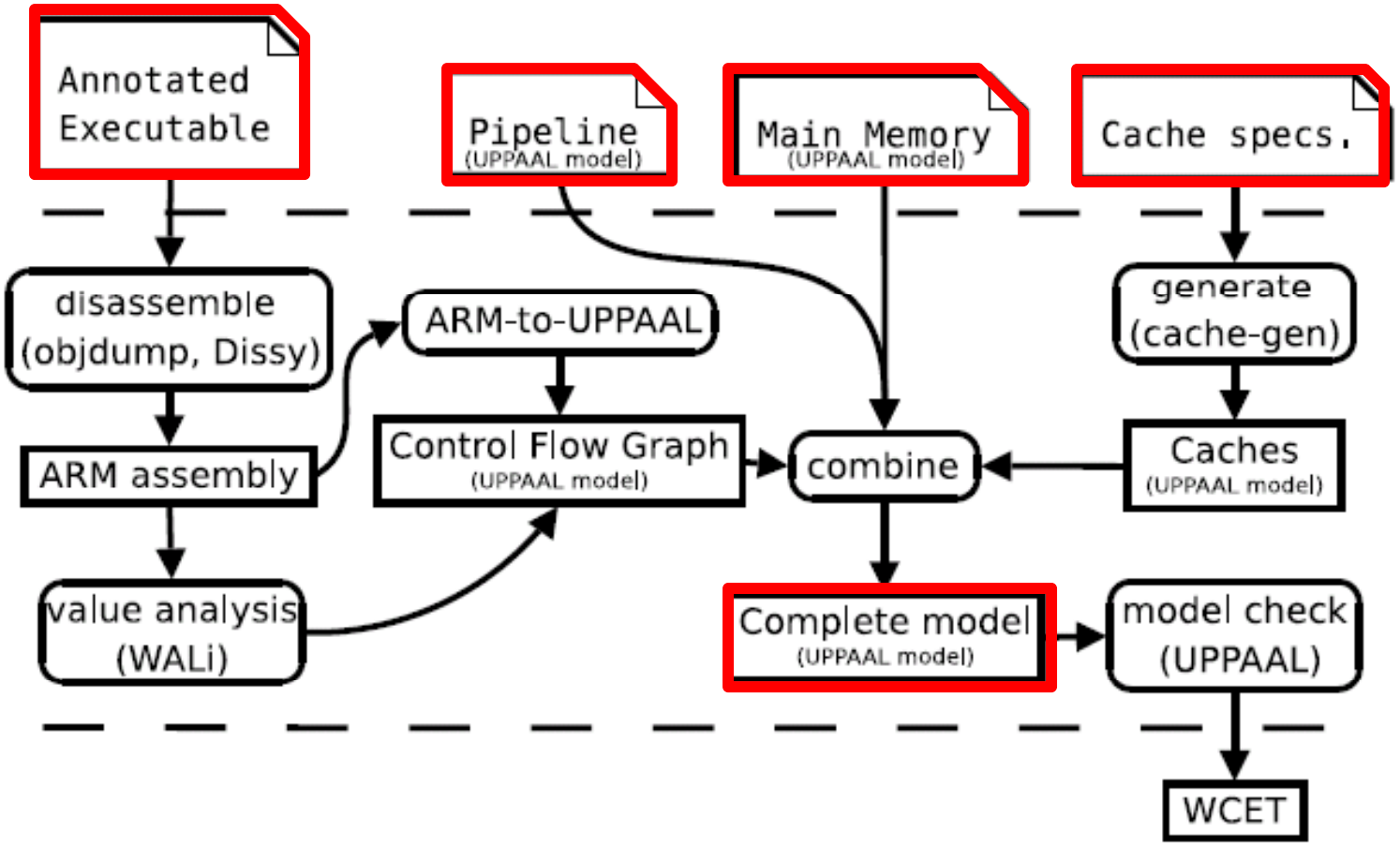
METAMOC

Modular Execution Time Analysis using MOdel Checking

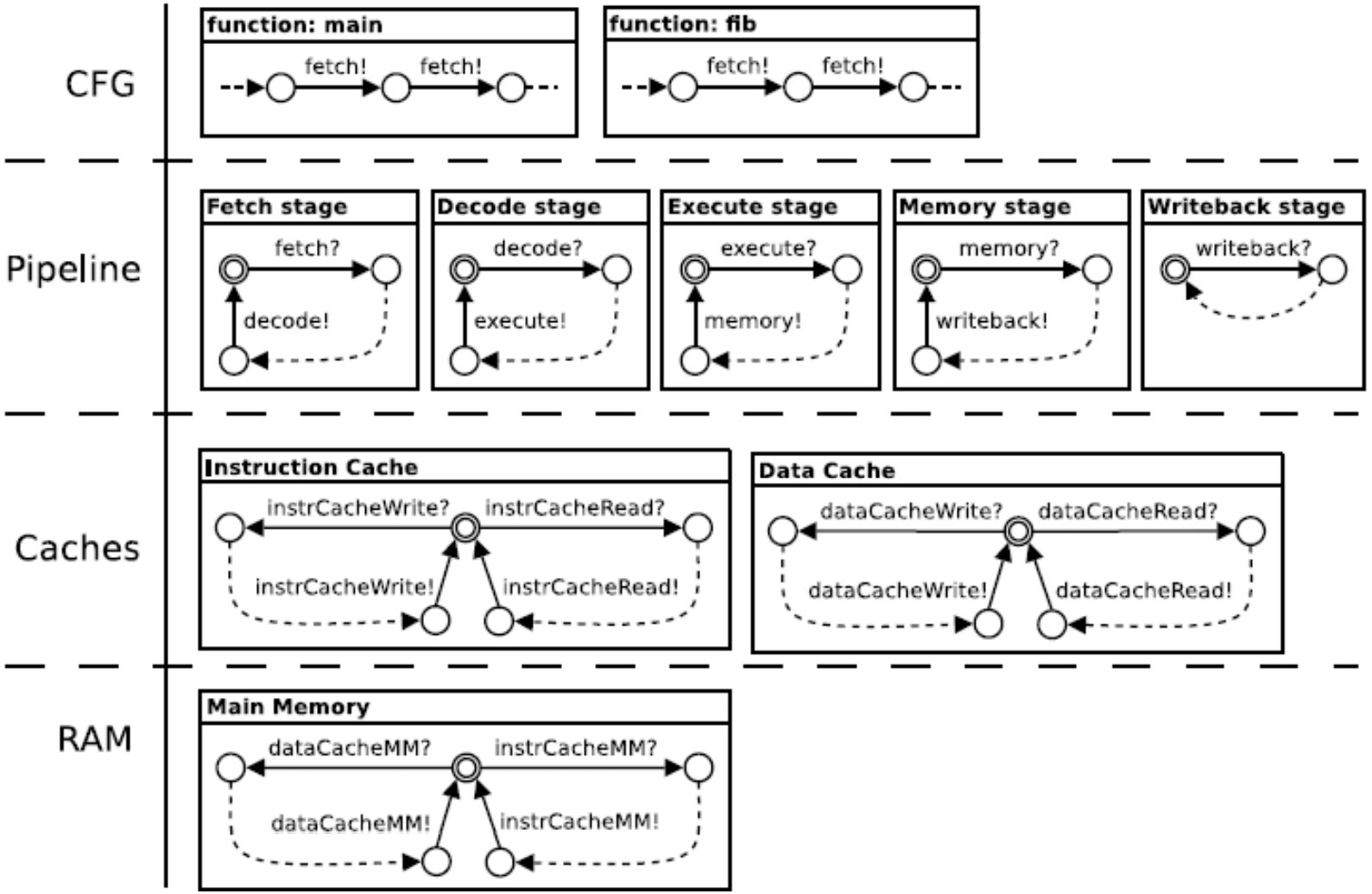
with
Andreas Dalsgaard
Mads Christian Olesen
Martin Toft
René Rydhof Hansen



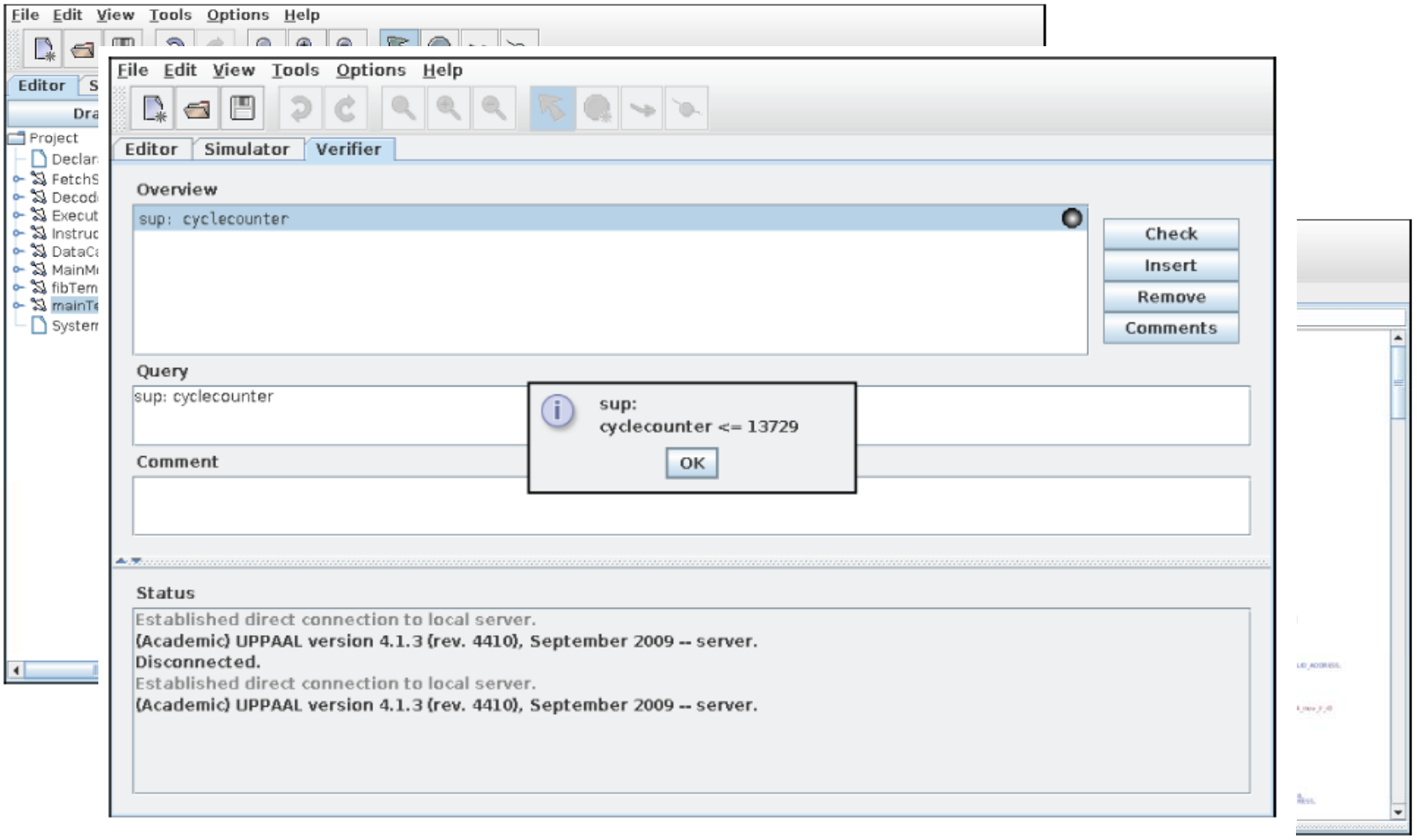
Overview of METAMOC



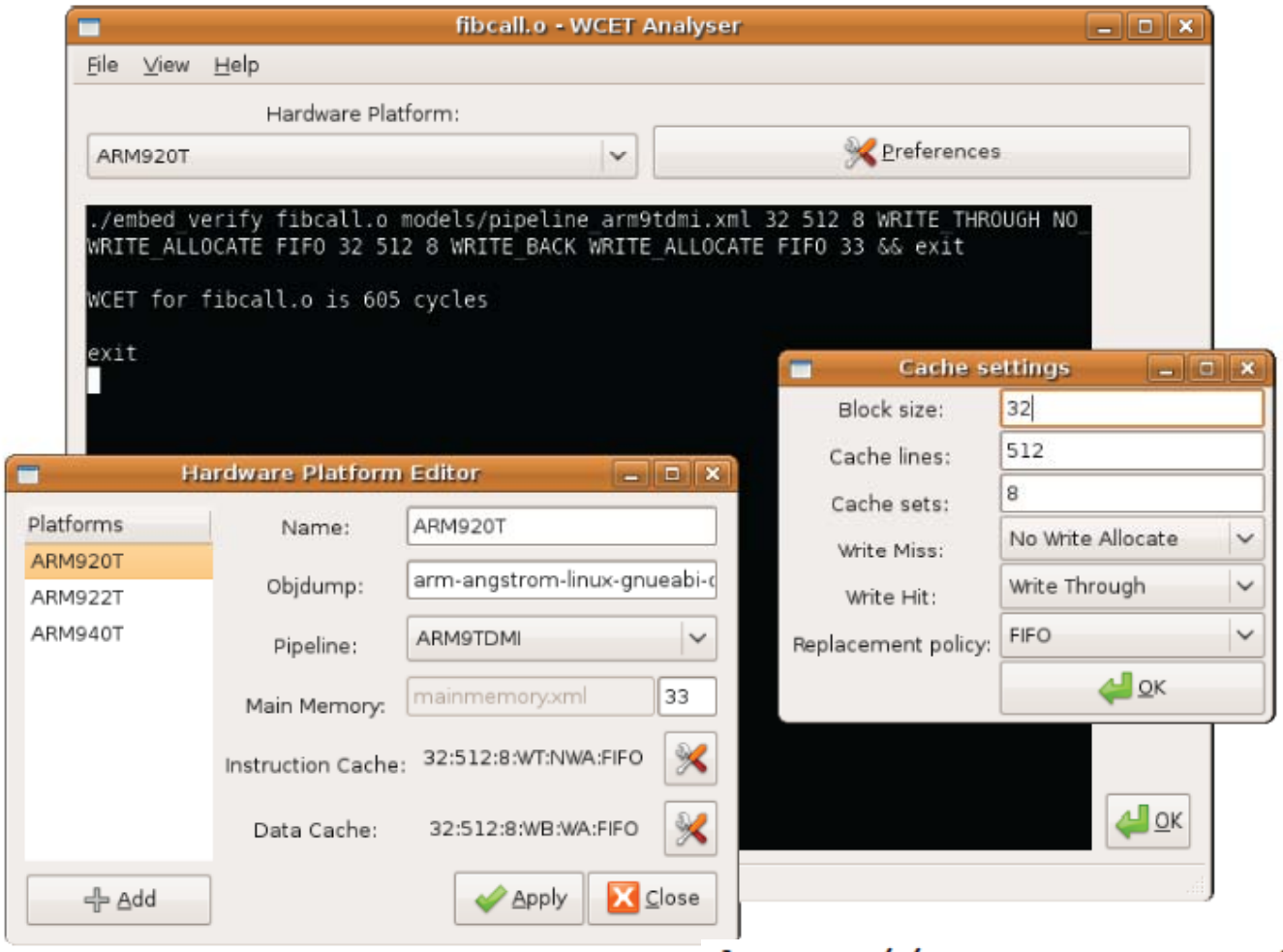
Modeling using Timed Automata



Analysis in UPPAAL



GUI for METAMOC



http://metamoc.martintoft.dk

Status

- Started out with ARM9 support
  - Five stage pipeline, instruction cache, data caches, simple main memory
- Now
  - .. support for ARM7, ARM9 and ATMEL AVR 8-bit
  - .. with modest effort

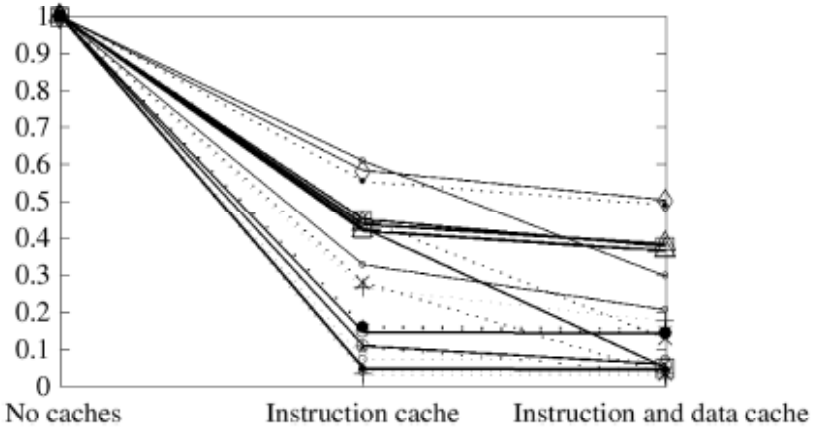
Experiments

- Evaluation using WCET benchmark programs from Mälardalen Real-Time Research Centre[2]
  - Applicability
  - Performance
- Discarded a number of programs
  - Floating point operations handled by software routines
  - Dynamic jumps
  - Some programs do not compile
- 21 programs for ARM and 19 programs for AVR
- Manually annotated loop bounds

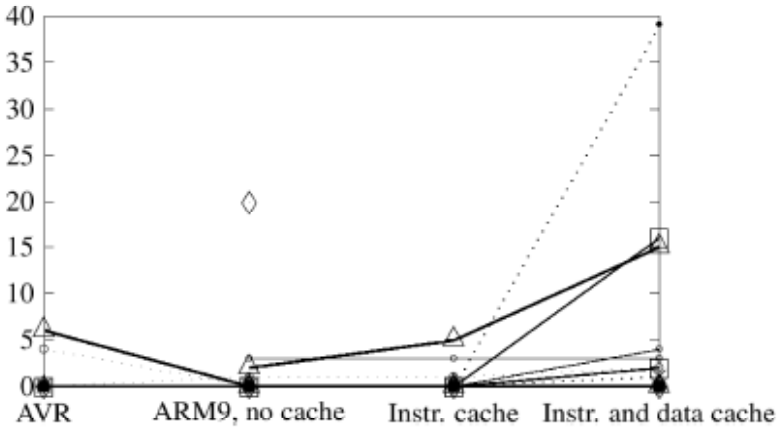
Experiments

ARM9, 21 benchmarks	
Analysable without caches	21
Analysable with instruction cache	20
Unanalysable, state space explosion	1
Analysable with data and instruction cache	20
Unanalysable, state space explosion	1
Manual modification of e.g. data cache size	4

ATMEL AVR 8-bit, 19 benchmarks	
Analysable	16
Unanalysable, state space explosion	3



Relative improvement in WCET for ARM9.

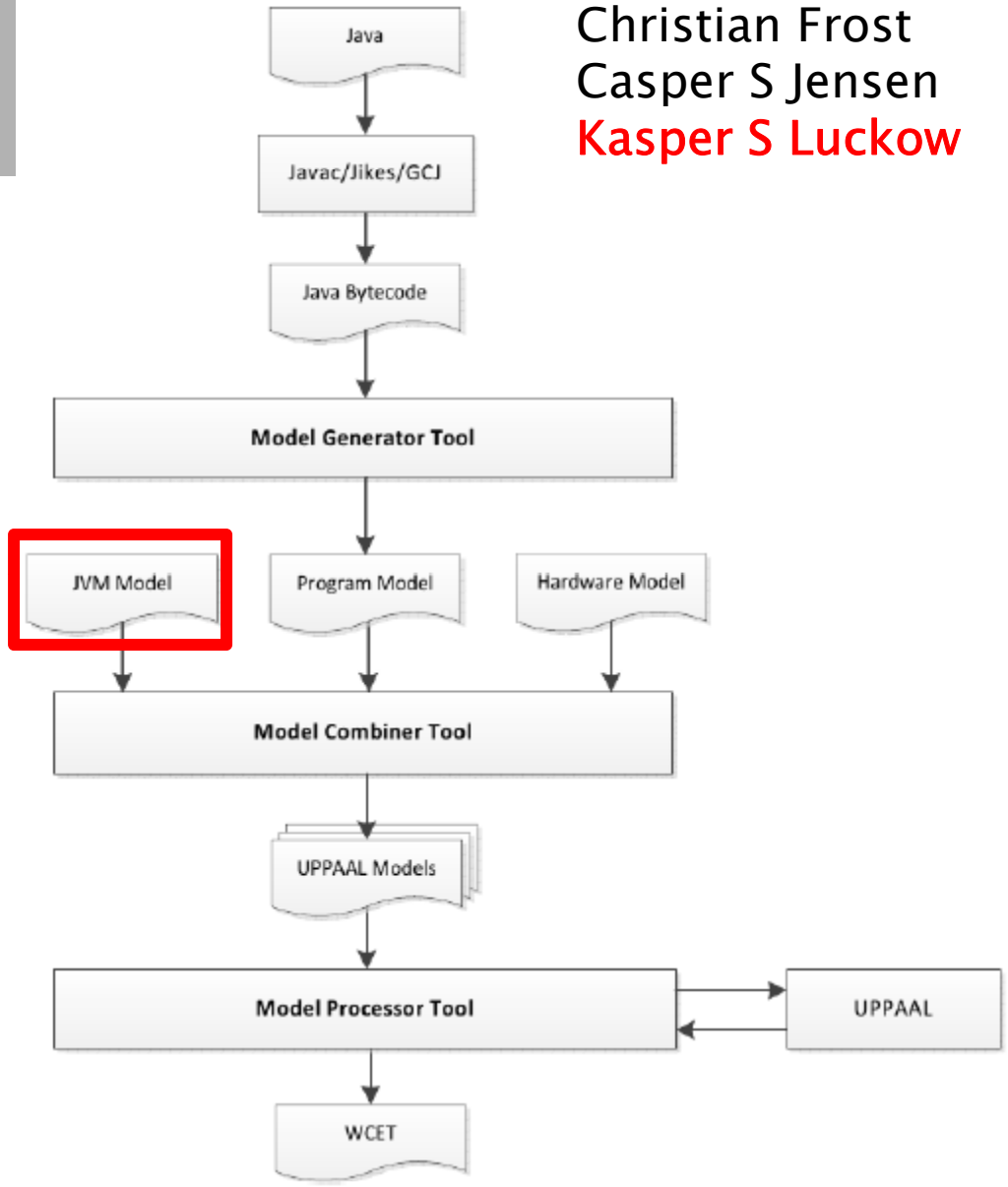


Analysis times in minutes for AVR and ARM9.

TetaJ [2011]

Christian Frost
Casper S Jensen
Kasper S Luckow

- Constructing UPPAAL models
- TetaJ Control Flow Graphs (TCFGs)
  - Forms the interface for model construction
  - Achieves reusability:
    - Java Bytecode to TCFG
    - AVR to TCFG
- CFG analyses are applied yielding annotated TCFGs
  - Loop detection
  - Condition optimisation
  - Progress measures in UPPAAL
- TCFGs are transformed to models
- The models are combined to one model
- UPPAAL conducts the WCET analysis on the final model



Evaluation of TetaJ

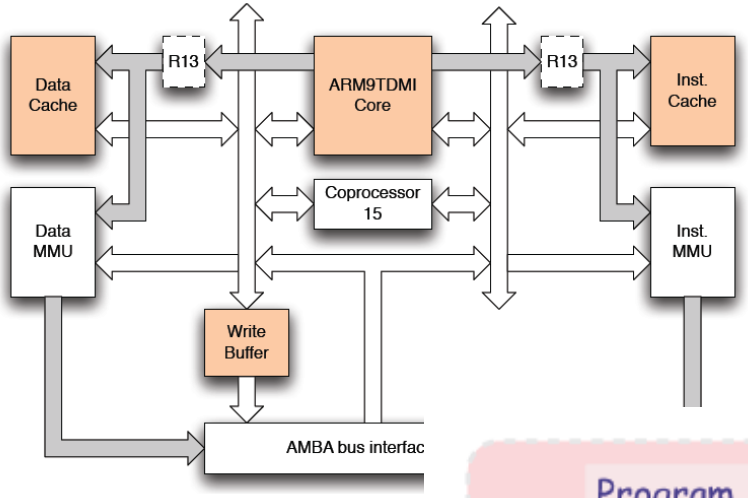
PERFORMANCE

Optimisation	Analysis time	States explored	Max memory usage
No optimisations	14h 51m 17s	41,854,143	3,905 MB
Only progress measures	4d 12h 7m 8s	408,223,029	589 MB
Only state space reduction	13h 33m 21s	41,854,143	2,426 MB
Only condition optimisation	1m 16s	53,732	294 MB
Only template reduction	4h 46m 41s	41,854,143	3,851 MB
All			

Algorithm	Measured WCET	TetaJ WCET	Pessimism
Iterative fibonacci	46,642 clock cycles	46,933 clock cycles	0.6%
Factorial	39,726 clock cycles	40,939 clock clycles	3.1%
Reverse ordering	64,436 clock cycles	81,919 clock cycles	27.1%
Bubble sort	907,103 clock cycles	2,270,401 clock cycles	150.3%
Binary Search	54,430 clock cycles	99,301 clock cycles	82.4%
Insertion Sort	849,353 clock cycles	3,740,769 clock cycles	440.4%

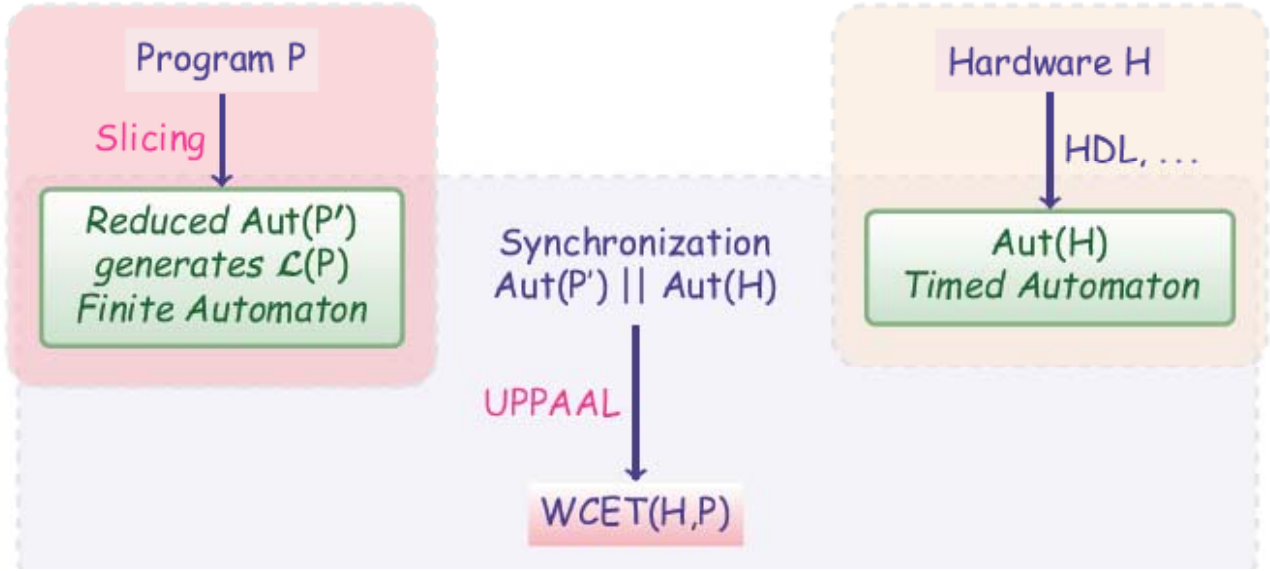
ACCURACY

Program Slicing & Model-Checking



ARM920T

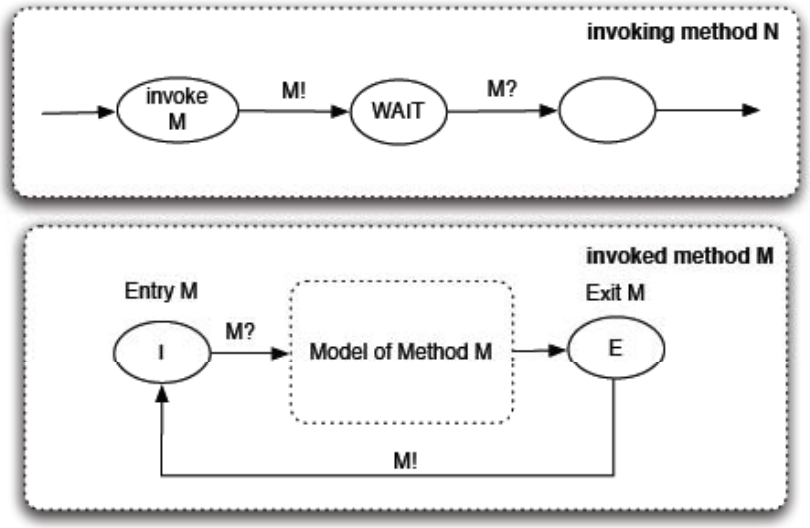
Jean-Luc Béchenec
Franck Cassez
IRCCyN



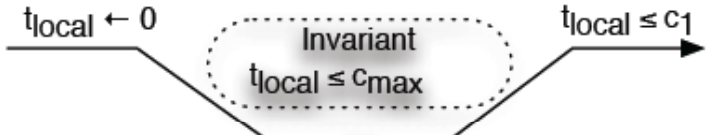
Program	loc	UPPAAL Time States Explored	Computed WCET (C)	Measured WCET (M)	$\frac{(C-M)}{M} \times 100$	Slice
Single-Path Programs						
fib-O0	74	1.74s/74181	8098	8064	**0.42%**	47/131
fib-O1	74	0.61s/22332	2597	2544	**2.0%**	18/72
fib-O2	74	0.3s/9710	1209	1164	**3.8%**	22/71
janne-complex-O0*	65	1.15s/38014	4264	4164	**2.4%**	78/173
janne-complex-O1*	65	0.48s/14600	1715	1680	**2.0%**	30/89
janne-complex-O2*	65	0.46s/13004	1557	1536	**1.3%**	32/78
fdct-O1	238	1.67s/60418	4245	4092	**3.7%**	100/363
fdct-O2	238	3.24s/55285	19231	18984	**1.3%**	166/3543
Single-Path Programs‡ with MUL/MLA/SMULL instructions (instructions durations depend on data)						
fdct-O0	238	2.41s/85007	[11242,11800]	11448	**3.0%**	253/831
matmult-O0*	162	5m9s/10531230	[502850,529250]	511584 528684	**0.1%**	158/314
matmult-O2*	162	43.78s/1780548	[122046,148299]	116844 140664	**5.4%**	75/288
jfdcint-O0	374	2.79s/100784	[12699,12699]	12588	**0.8%**	159/792
jfdcint-O1	374	1.02s/35518	[4897,4899]	4668	**7.0%**	25/325
jfdcint-O2	374	5.38s/175661	[16746,16938]	16380	**3.4%**	56/2512
Multiple-Path Programs						
bs-O0	174	42.6s/1421474	1068	1056	**1.1%**	75/151
bs-O1	174	28s/1214673	738	720	**2.5%**	28/82
bs-O2	174	15s/655870	628	600	**4.6%**	28/65
cnt-O0*	115	2.3s/76238	9028	8836	**2.1%**	99/235
cnt-O1*	115	1s/27279	4123	3996	**3.1%**	42/129
cnt-O2*	115	0.5s/11540	3065	2928	**4.6%**	39/263
insertsort-O0*	91	10m35s/24250737	3133	3108	**0.8%**	79/175
insertsort-O1*	91	7m2s/11455293	1533	1500	**2.2%**	40/115
insertsort-O2*	91	11.5s/387292	1371	1344	**2.0%**	43/108
ns-O0*	497	83.4s/3064315	30968	30732	**0.8%**	132/215
ns-O1*	497	11.3s/368719	11701	11568	**1.1%**	61/124
ns-O2*	497	29s/1030746	7343	7236	**1.4%**	566/863

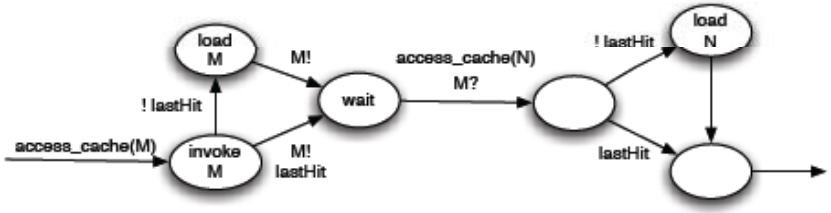
WCA: IPET versus MC

- Benedikt Huber, Martin Schoeberl



(a) Method Invocations





(b) Cache Simulation

Checking

(b) Modeling loops

WCA: IPET versus MC

Problem	IPET	UPPAAL Breadth First		UPPAAL Progress	
		Verify	Search	Verify	Search
DCT	0.00	0.09	1.21	0.07	0.84
GCD	0.00	3.10	47.65	0.20	2.75
MatrixMult	0.01	0.21	3.52	0.23	4.58
CRC	0.01	1.21	16.32	0.52	9.46
BubbleSort	0.00	7.63	197.91	1.33	268.43
LineFollower	0.00	0.11	1.07	0.15	1.10
Lift	0.01	0.1	2.07	0.18	1.38
UdpIp	0.03	8.3	84.69	1.78	30.28
UdpIp simplified		0.64	7.28	0.44	7.07
Kfl (no cache)	0.04	92.19	1229.42	0.57	9.23
Kfl simplified (no cache)		33.81	444.73	0.45	7.23
Kfl (8 blocks)	0.13	—	—	31.77	428.24
Kfl simplified (8 blocks)		—	—	17.72	263.18

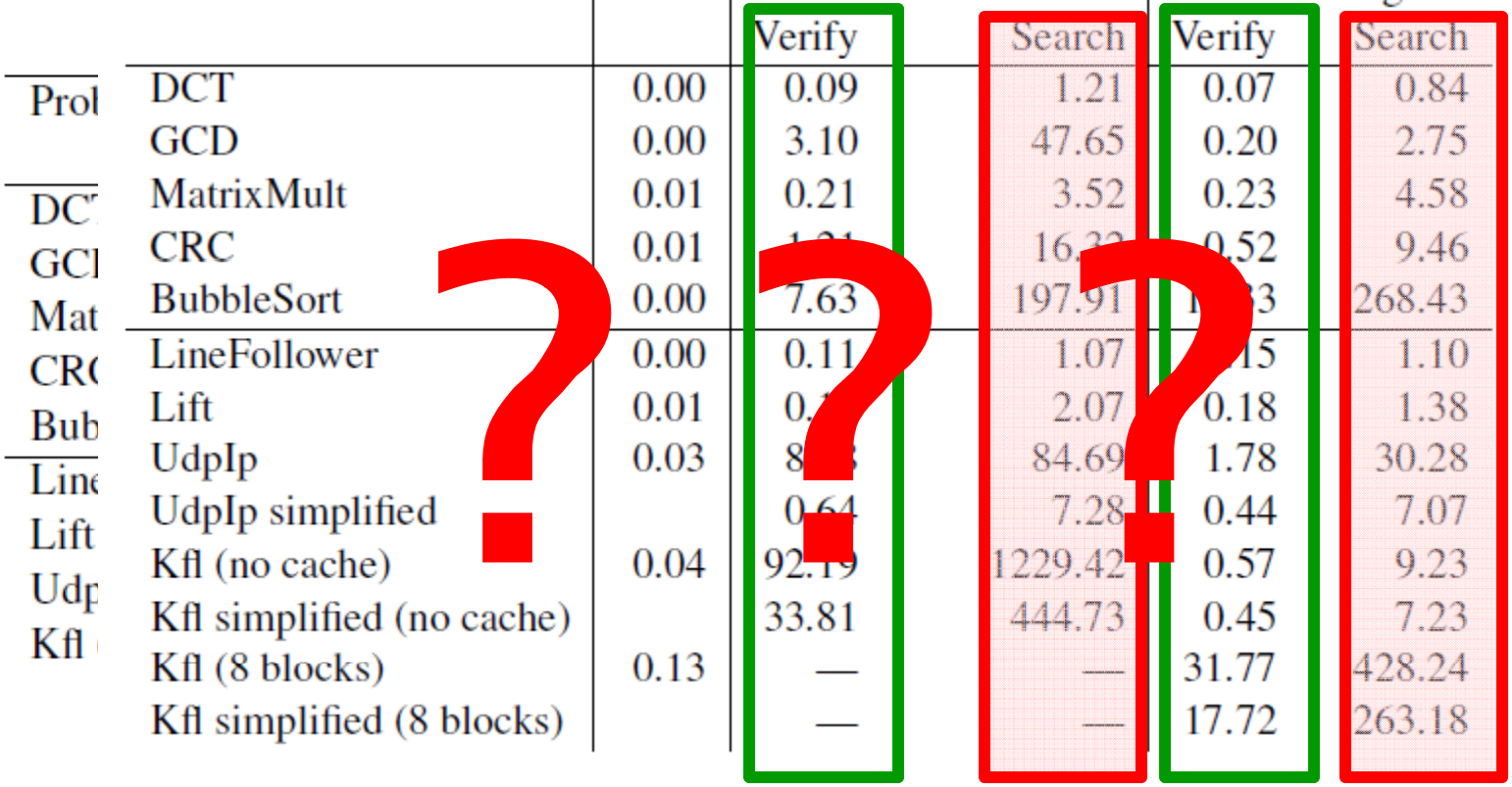
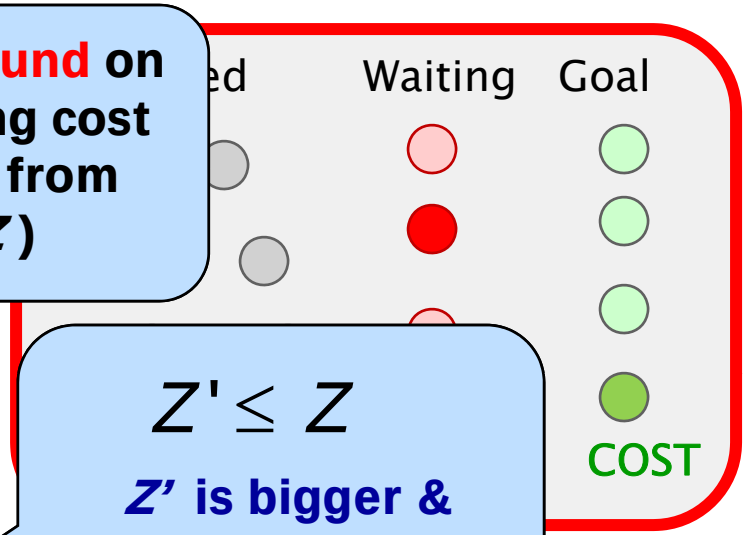


Table 3. Analysis exe

SUP: EXPR in UPPAAL

Symbolic B & B Algorithm

??????



Cost := 0
Passed := ∅
Waiting := $\{(l_0, Z_0)\}$
while Waiting ≠ ∅ **do**
  select (l, Z) from Waiting
  if $l = l_g$ and maxCost(Z) < Cost **then**
    Cost := maxCost(Z)
  if maxCost$(Z) + \text{Rem}_{(l,Z)} \leq$ Cost **then** break
  if for all (l, Z') in Passed: $Z' \not\leq Z$ **then**
    add (l, Z) to Passed
    add all (l', Z') with $(l, Z) \rightarrow (l'$
return Cost

Upper bound on remaining cost to goal from (*l,Z*)

$Z' \leq Z$

***Z'* is bigger & more costly than *Z* (=> prog msr)**

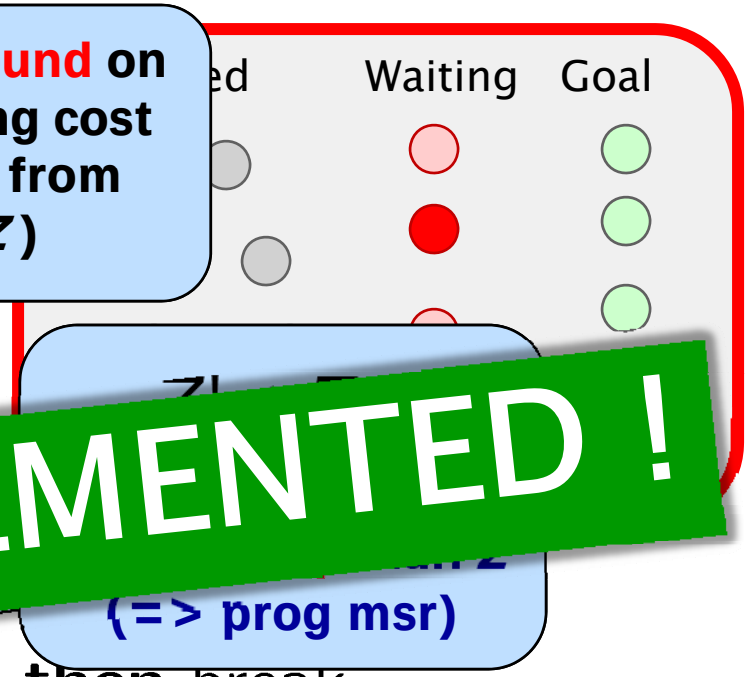
All states reaches eventually goal guarantees termination!

Symbolic B & B Algorithm

??????

Cost := 0
Passed := ∅
Waiting := $\{(l_0, Z_0)\}$
while Waiting $\neq \emptyset$ **do**
  select (l, Z) from Waiting
  if
  if $(Z) + \text{Rem}_{(l,Z)} \leq$ Cost **then** break
  if for all (l, Z') in Passed: $Z' \not\subseteq Z$ **then**
    add (l, Z) to Passed
    add all (l', Z') with $(l, Z) \rightarrow (l'$
return Cost

Upper bound on remaining cost to goal from (*l,Z*)



(=> prog msr)

TO BE IMPLEMENTED !

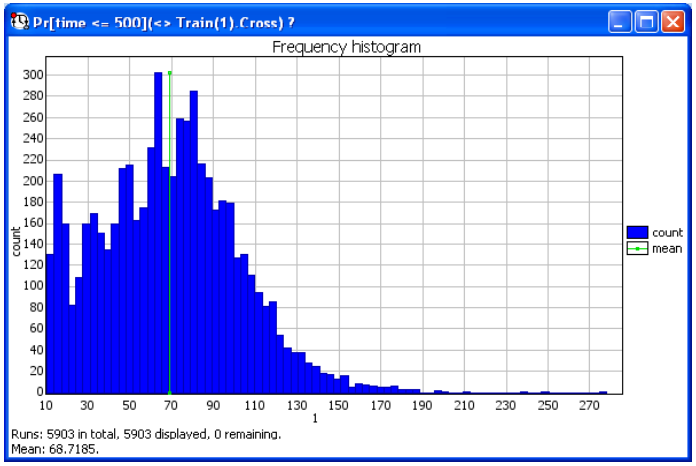
All states reaches eventually goal guarantees termination!

More ..

- Schedulability Analysis
  - TIMES tool [TACAS 2002]
  - Multitasking applications under OSEK [RTS 2008]
  - CREOL Modular schedulability [FSEN09]
  - SARTS Java byte code on FPGA [JTRES08]
  - Schedulability Analysis Using UPPAAL 4.1 [Model-Based Design for ES, CRC Press 2010]
  - ARTS: MPSoC Schedulability [Model-Based Design for ES, CRC Press 2010]
- Worst Case Execution Time Analysis
  - WCA [Schoeberl 2010]
  - METAMOC [WCET10,NSF11]
  - TetaJ [AAU 2011}
  - Combining AI & MC for Timing Analysis of MultiCore [Yi et al, RTSS10]
  - WCET analysis of Multicore using UPPAAL [Petterson et al]

sarts.boegholm.dk
metamoc.martintoft.dk
tetaj.dk
www.irccyn.fr/franck/wcet/

Performance Analysis
using
Statistical Model Checking

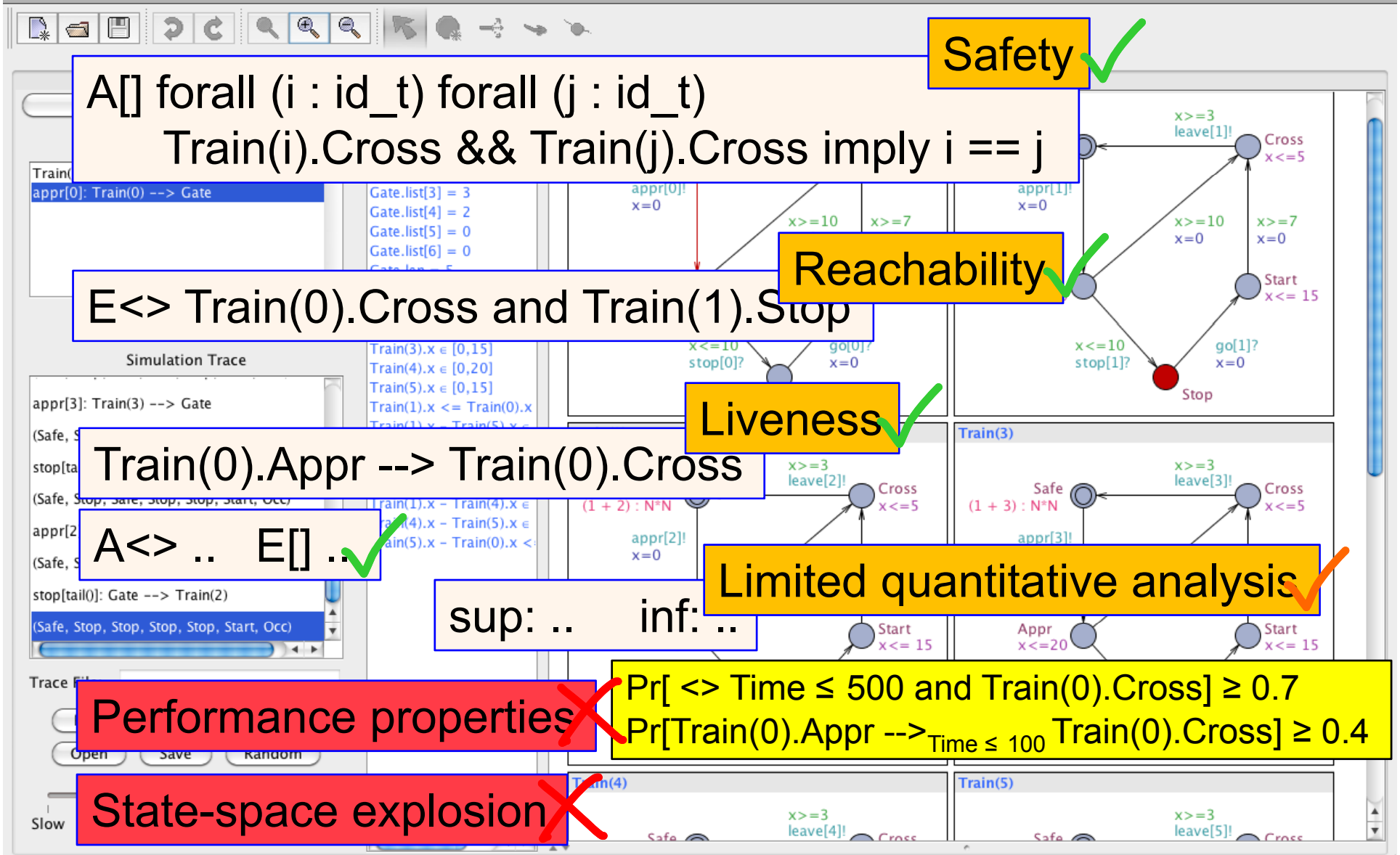


Collaborators:

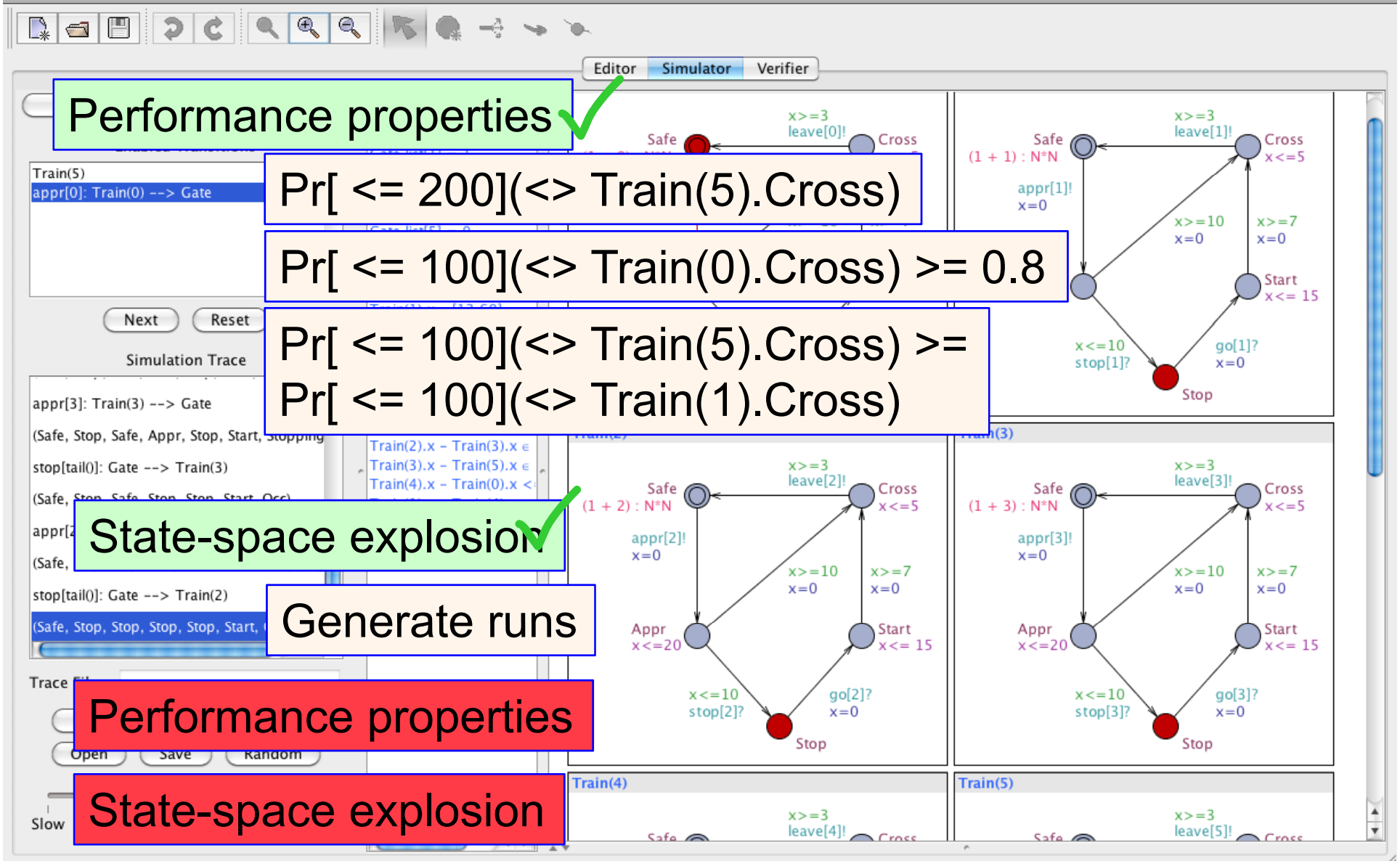
Peter Bulychev, Alexandre David
Axel Legay, Marius Mikucionis
Wang Zheng
Jonas van Vliet, Danny Poulsen

CAV 2011, PDMC 2011,
FORMATS 2011

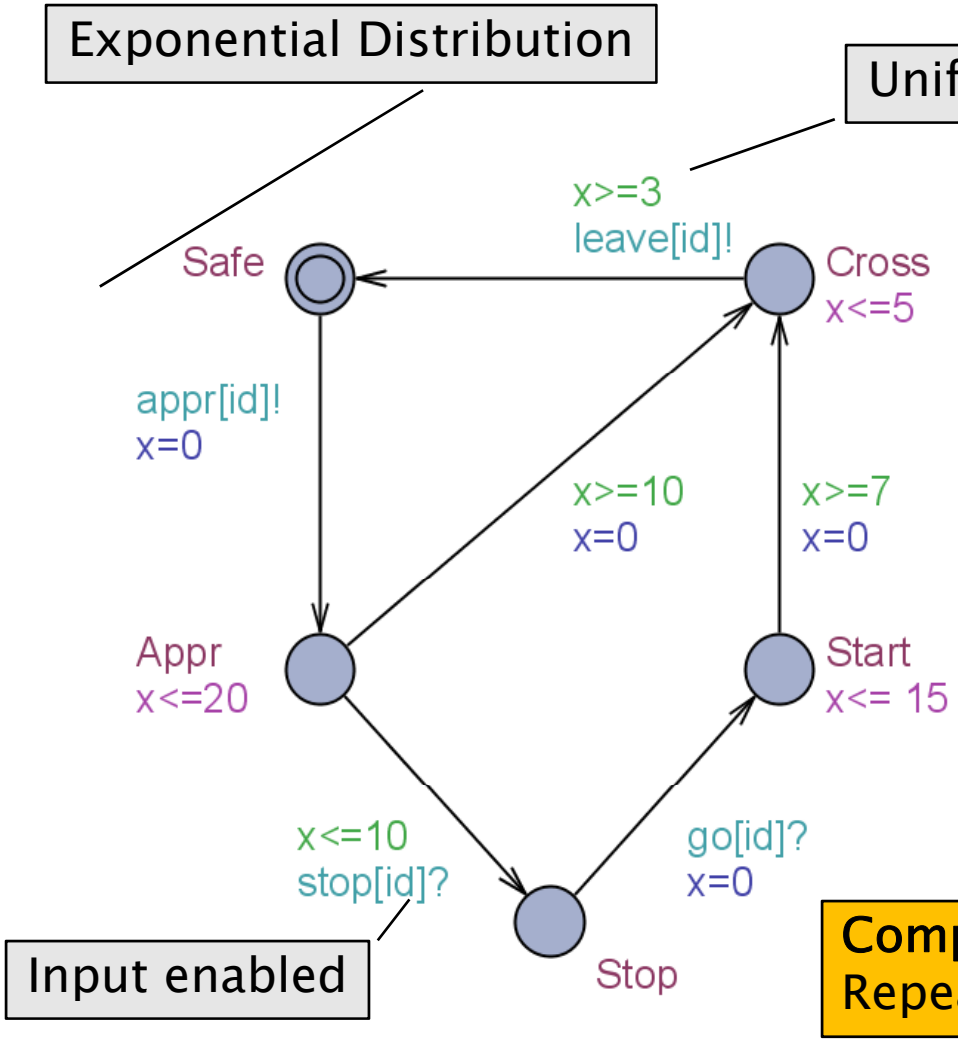
UPPAAL

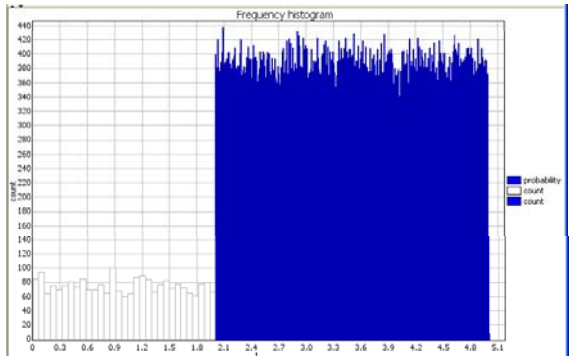

A[] forall (i : id_t) forall (j : id_t)
Train(i).Cross && Train(j).Cross imply i == j
Safety
E<> Train(0).Cross and Train(1).Stop
Reachability
Train(0).Appr --> Train(0).Cross
Liveness
A<> .. E[] ..
sup: .. inf: ..
Limited quantitative analysis
Performance properties
Pr[<> Time ≤ 500 and Train(0).Cross] ≥ 0.7
Pr[Train(0).Appr -->Time ≤ 100 Train(0).Cross] ≥ 0.4
State-space explosion
Simulation Trace
Train(3)
Train(4)
Train(5)
Cross
Start
Stop
Appr
Safe
Open
Save
Random
Slow

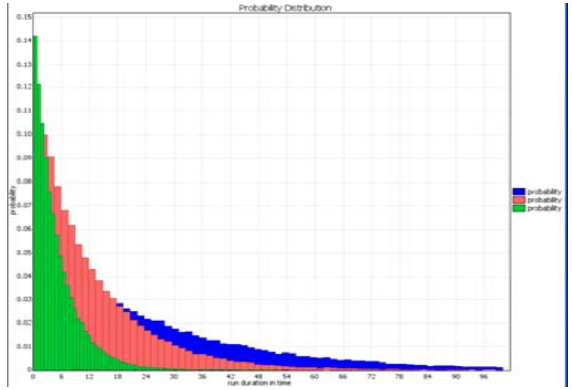
UPPAAL SMC


Editor
Simulator
Verifier
Performance properties
Pr[<= 200](<> Train(5).Cross)
Pr[<= 100](<> Train(0).Cross) >= 0.8
Pr[<= 100](<> Train(5).Cross) >=
Pr[<= 100](<> Train(1).Cross)
State-space explosion
Generate runs
Performance properties
State-space explosion
Train(5)
appr[0]: Train(0) --> Gate
Next
Reset
Simulation Trace
appr[3]: Train(3) --> Gate
stop[tail()]: Gate --> Train(3)
stop[tail()]: Gate --> Train(2)
Open
Save
Random
Slow
Safe
Cross
Appr
Start
Stop
x>=3
leave[0]!
leave[1]!
leave[2]!
leave[3]!
leave[4]!
leave[5]!
x>=10
x>=7
x<=10
x<=5
x<= 15
go[1]?
go[2]?
go[3]?
stop[1]?
stop[2]?
stop[3]?
Train(4)
Train(5)

Stochastic Semantics of TA



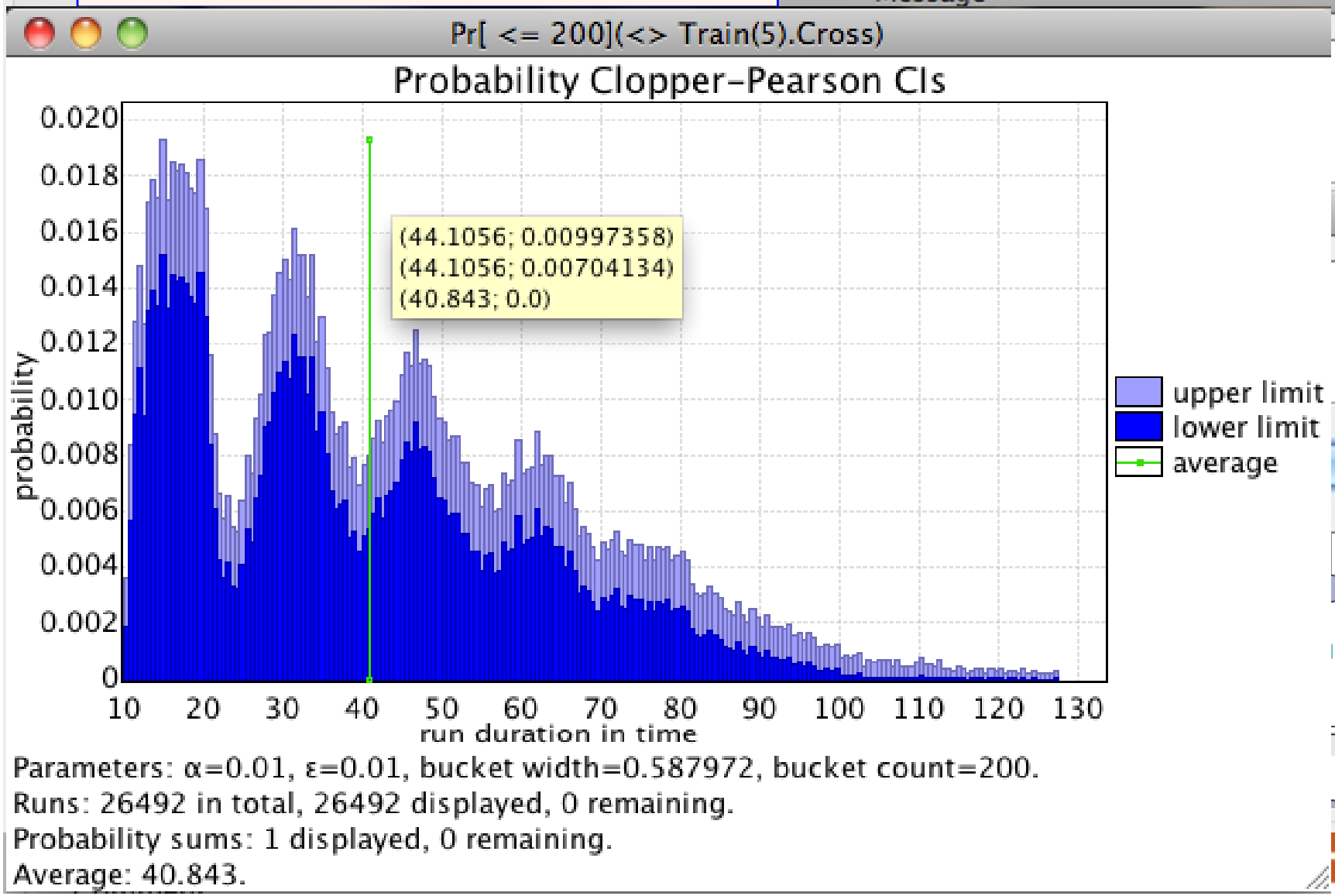




Composition =
Repeated races between components

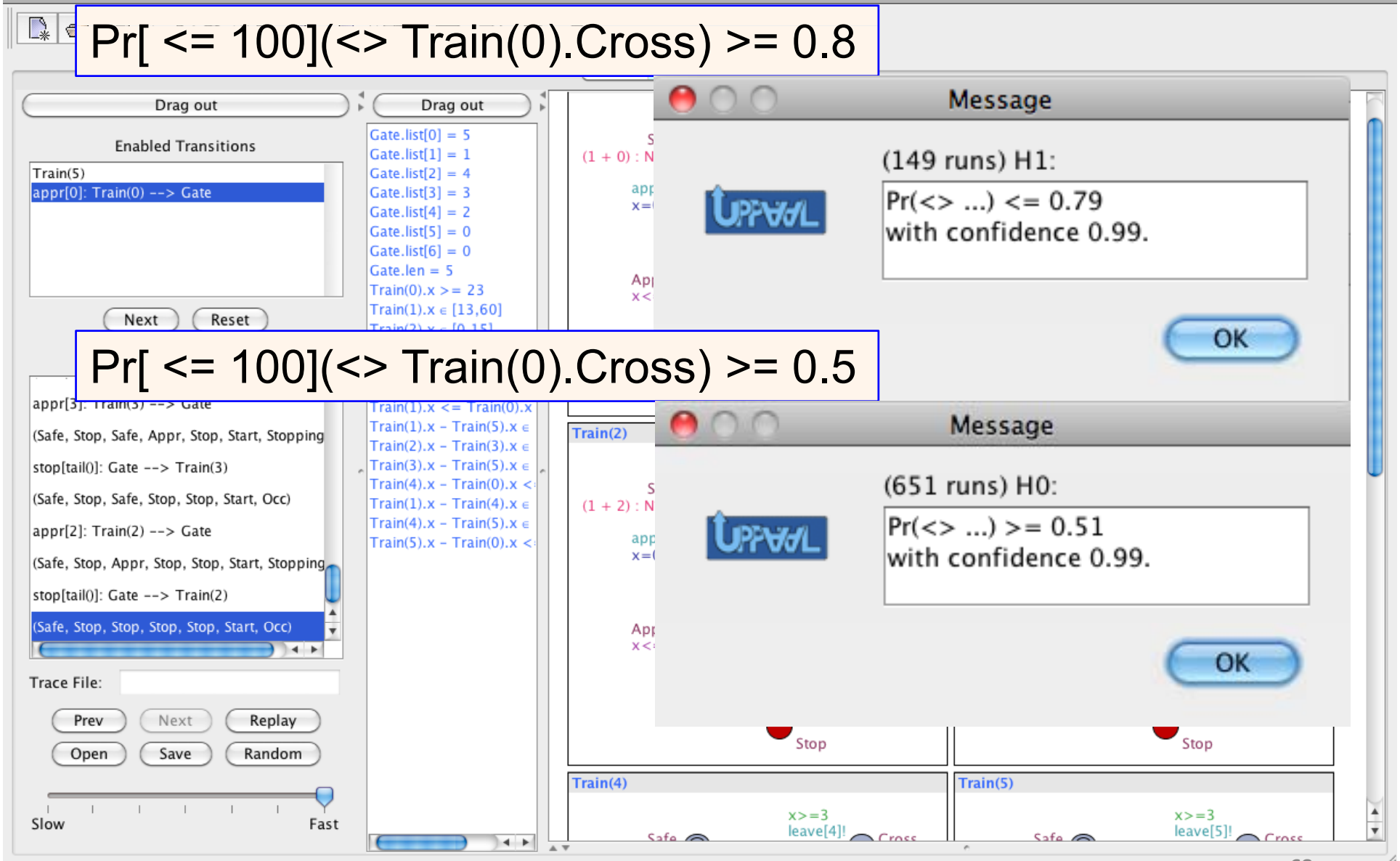
Queries in UPPAAL SMC

Pr[<= 200](<> Train(5).Cross)



Queries in UPPAAL SMC

Pr[<= 100](<> Train(0).Cross) >= 0.8

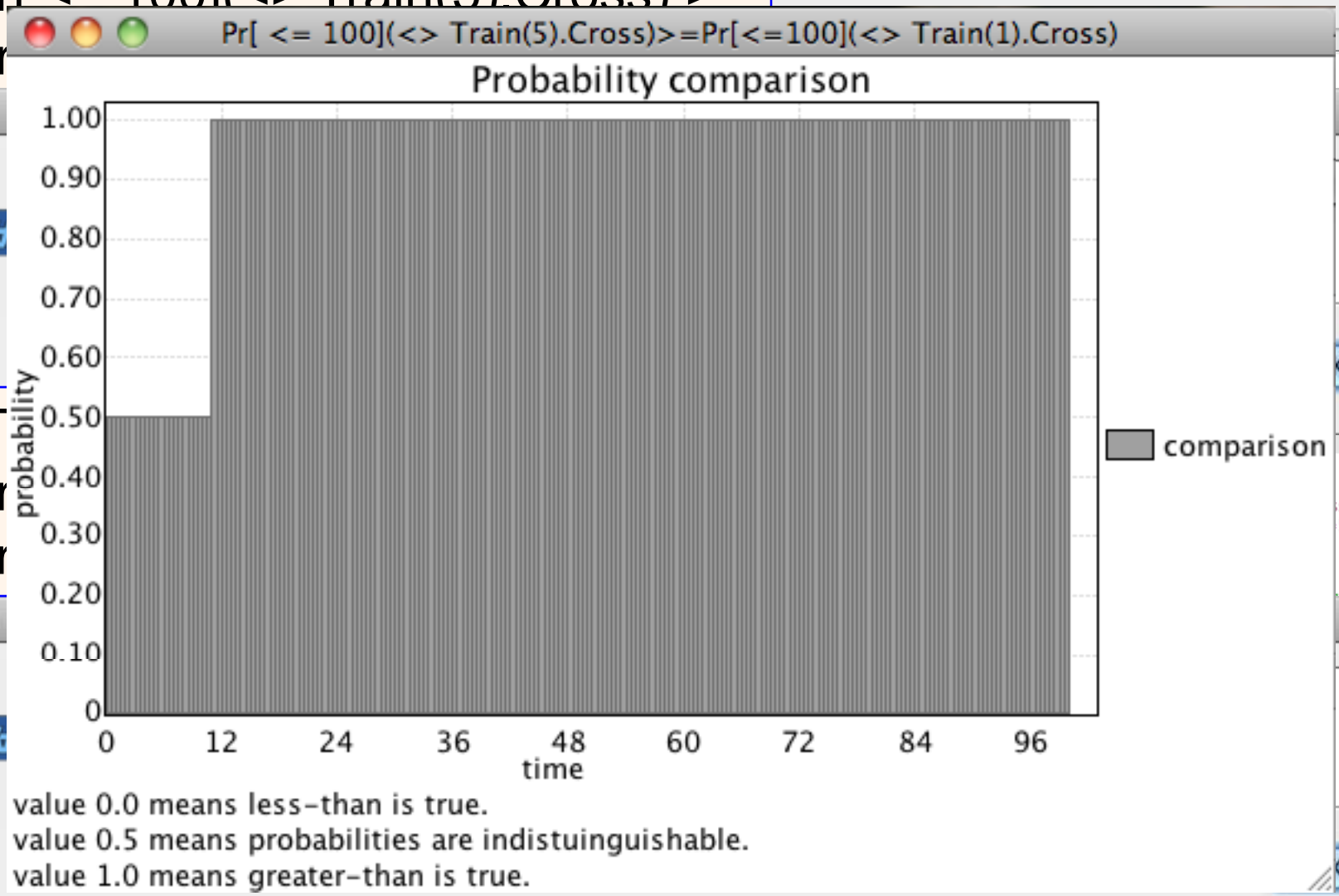


Pr[<= 100](<> Train(0).Cross) >= 0.5

Queries in UPPAAL SMC

Pr[<= 100](<> Train(5).Cross) >=

Pr

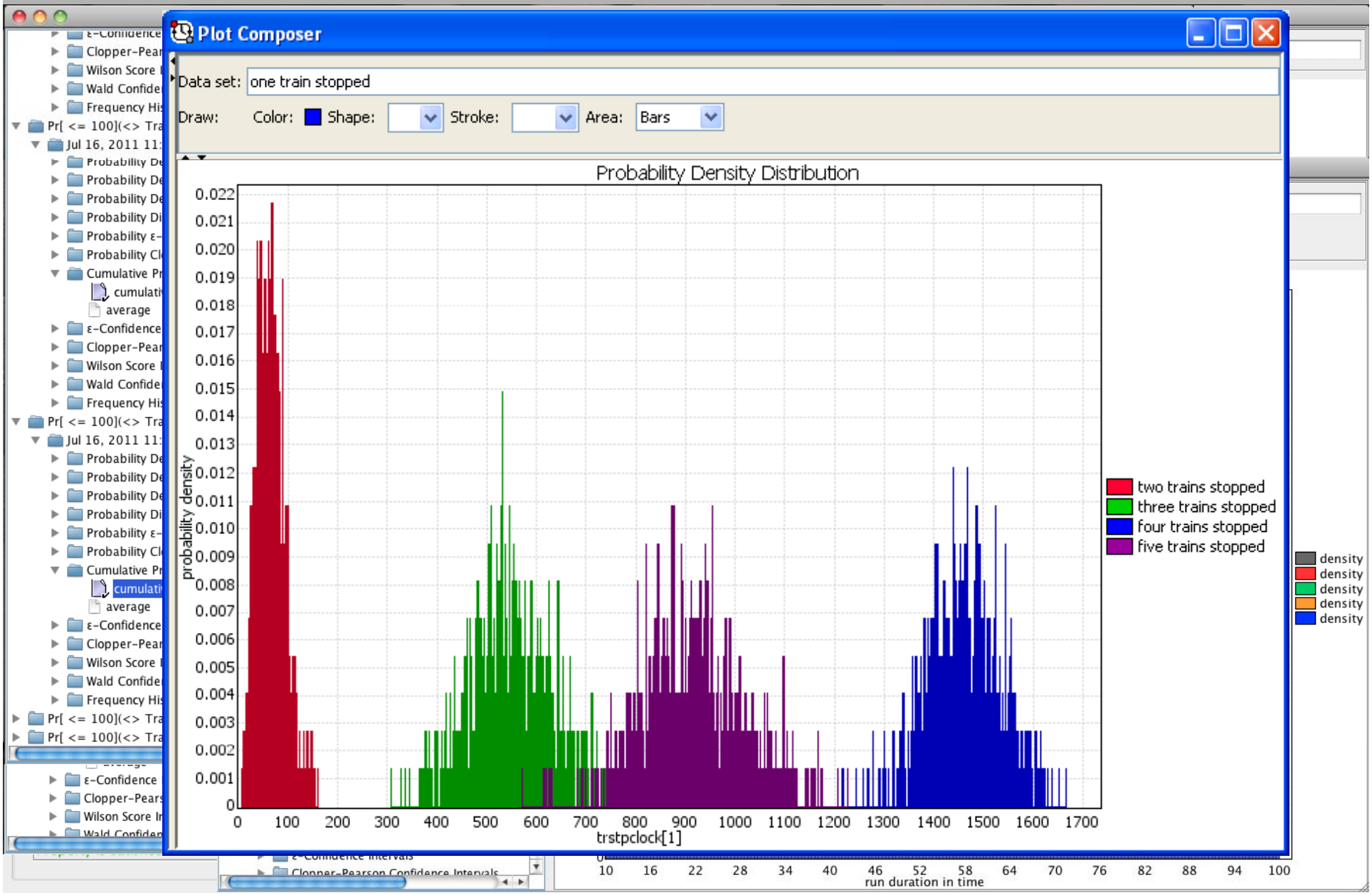


∀

Pr

Pr

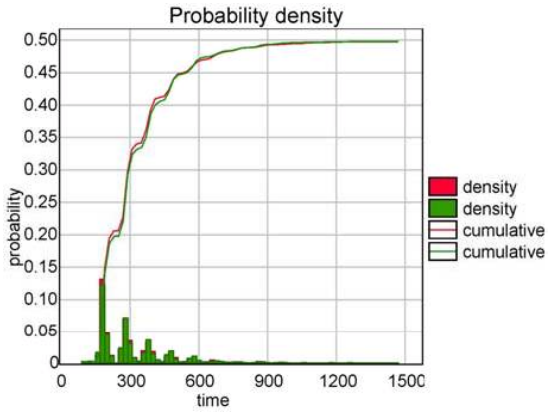
Analysis Tool: Plot Composer



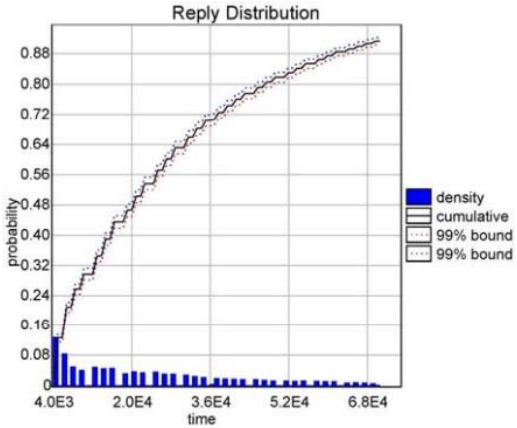
SMC in UPPAAL 4.1.4

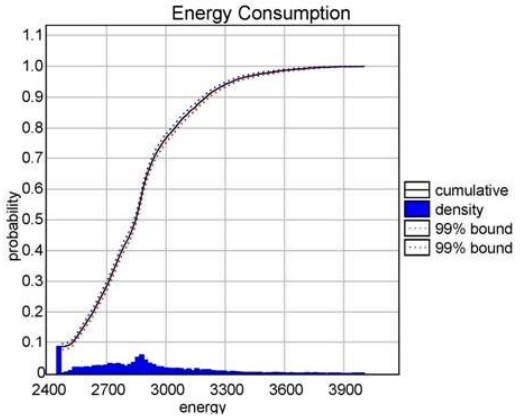
- Constant Slope Timed Automata
  - Clocks may have different (integer) slope in different locations.
  - Branching edges with discrete probabilities (weights).
  - Beyond Priced TA, Energy TA. Equal LHA in (non-stochastic) expressive power.
  - Beyond DTMC, beyond CTMC (with multiple rewards)
- All features of UPPAAL supported
  - User defined functions and types
  - Expressions in guards, invariants, clock-rates, delay-rates (rationals), and weights.
- New GUI for plot-composing and exporting.
- Distributed SMC, 64bits.

Case Studies

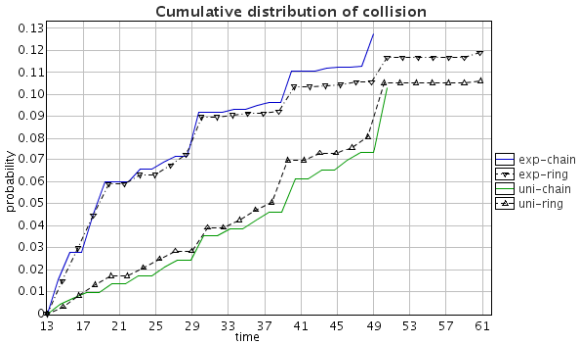


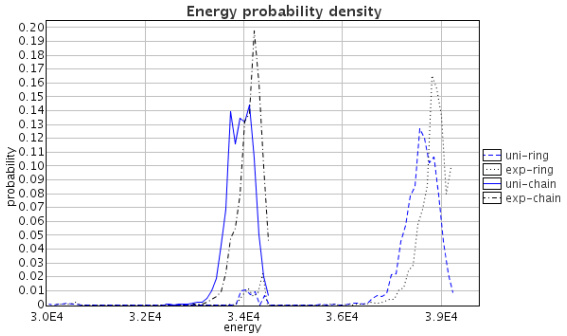
FIREWIRE



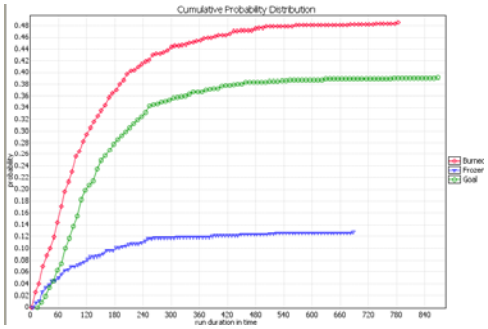


BLUETOOTH





10 node LMAC



100 x 100 ROBOT

Conclusion & Future Work

- TA Model Checking provides highly modular, flexible and accurate timing analysis.
- Using static analysis, slicing, optimized models and verification condition yields significant performance improvements.

- Implementation of B&B for maximum cost reachability.
- Abstraction-Refinenment
- Generation of concrete traces
- Use of abstract caches in model checking (UPPAAL with lattice-types.
- Support of Distributed Model Checking
- Support for 64 bit.

Thank You !