Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Computer Engineering and Networks Laboratory

Thermal-Aware Design of Real-Time Multi-Core Embedded Systems

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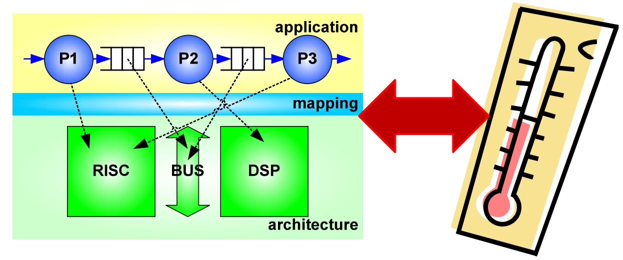
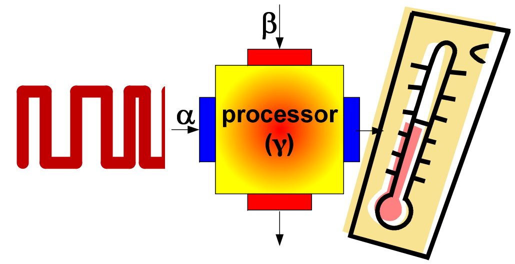
How Hot Can It Get?

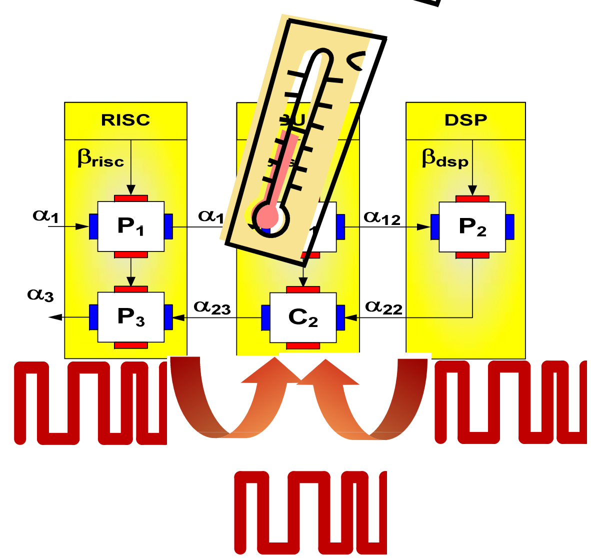
CAN WE PREDICT *WORST CASE (PEAK) TEMPERATURES* OF AN EMBEDDED SYSTEM?

Outline

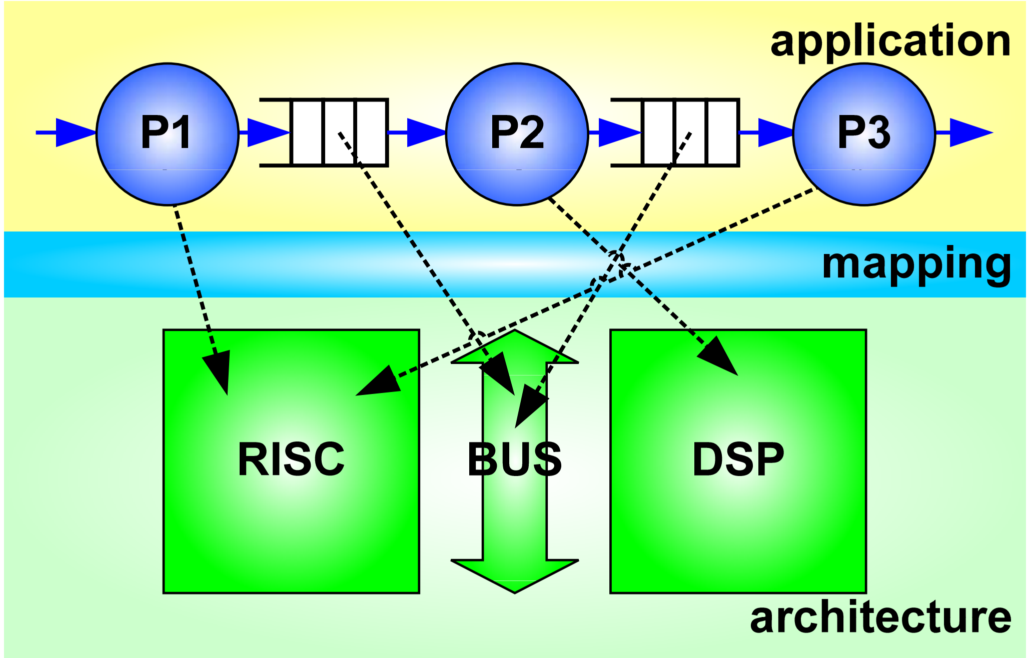
- introduction
  - system model
  - time, power, and temperature models
- worst-case temperature analysis
  - critical instance in terms of temperature
  - worst-case peak temperature
  - computational aspects
- how about multi-cores?
- experiments & conclusions





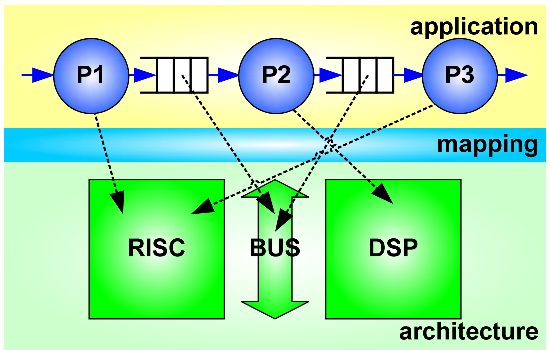


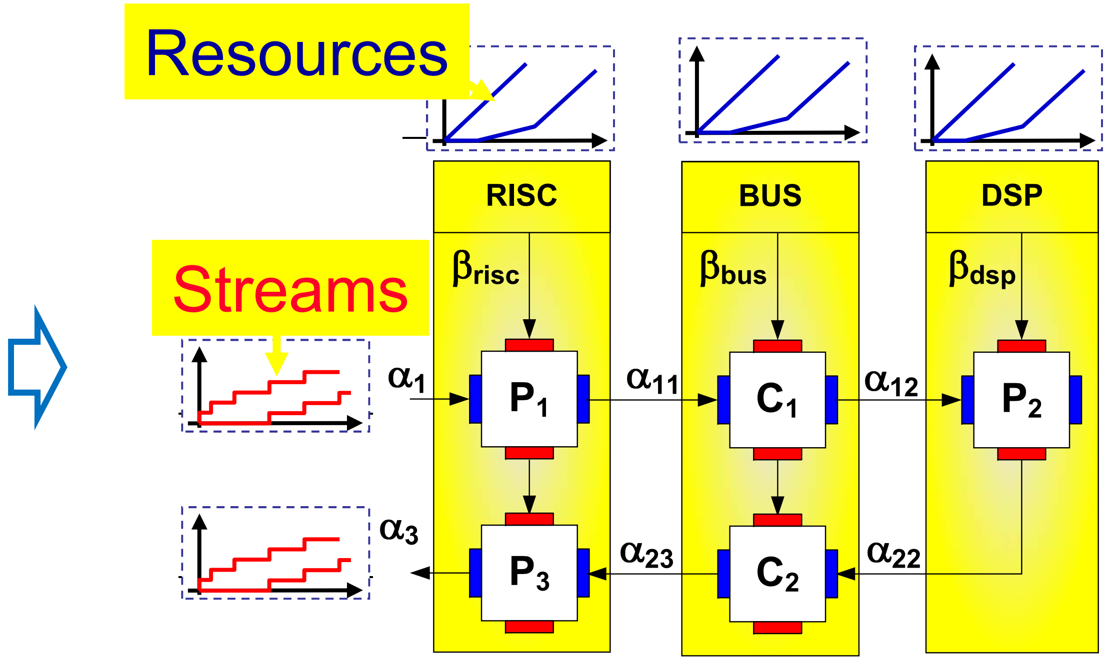
System



- **embedded system specification**
  - **process network – parallel applications**
  - **multi-core/3D architecture**
  - **mapping (binding, scheduling)**

System and Analysis Model

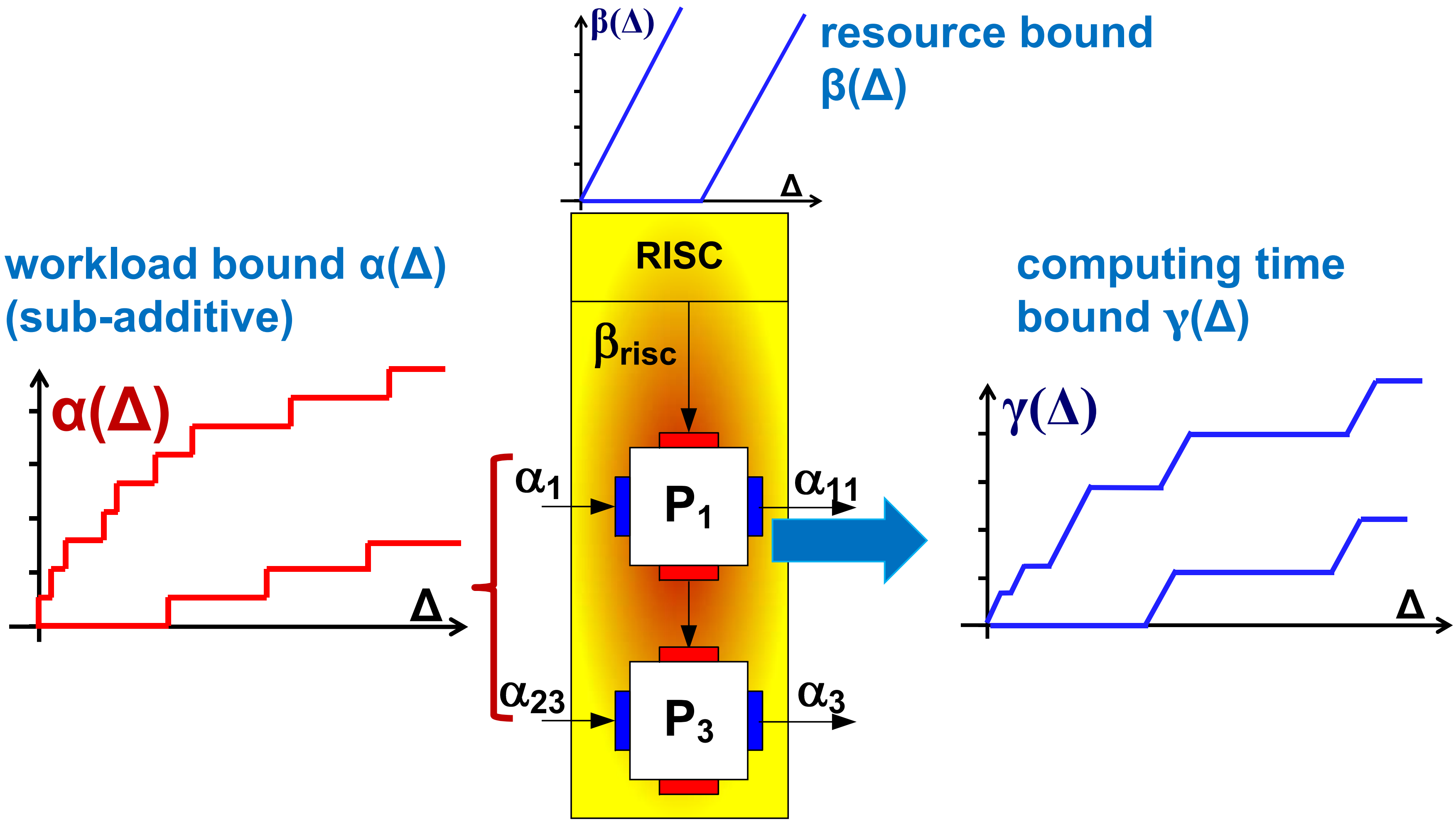




- **real-time analysis via Modular Performance Analysis (MPA)***
  - streams and resources represented by ***arrival/service curves***
  - **output:** ***worst-case bounds*** on system timing properties

***Modular Performance Analysis (MPA) http://www.mpa.ethz.ch**

MPA Component

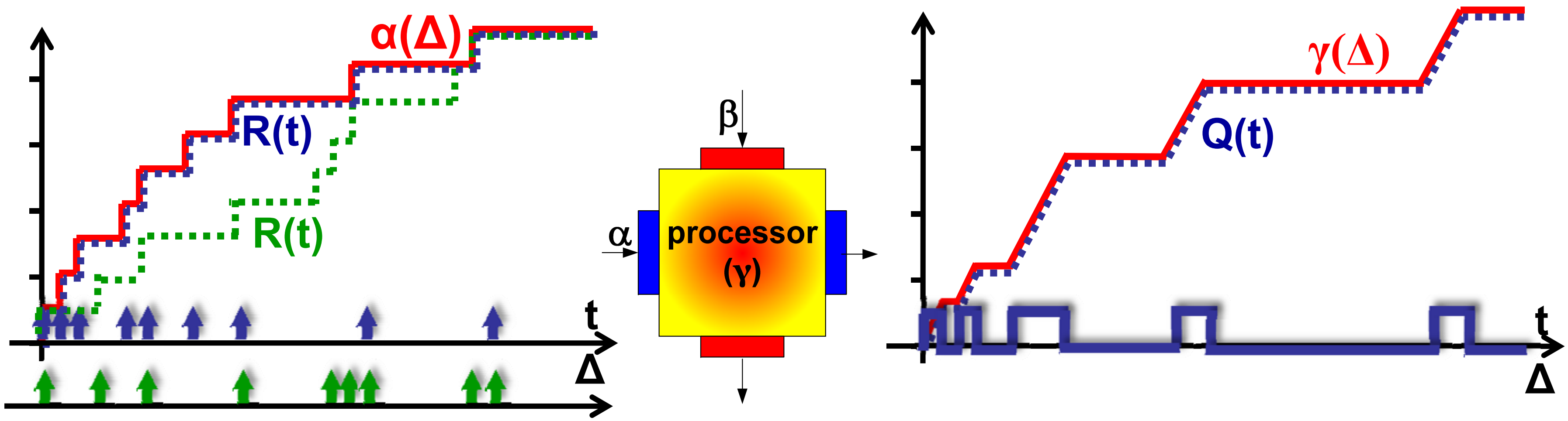


*Modular Performance Analysis (MPA) http://www.mpa.ethz.ch

Workload/Computing Time Bounds

cumulative workload R(t) and bound α(Δ)

accumulated computing time Q(t) and bound γ(Δ)



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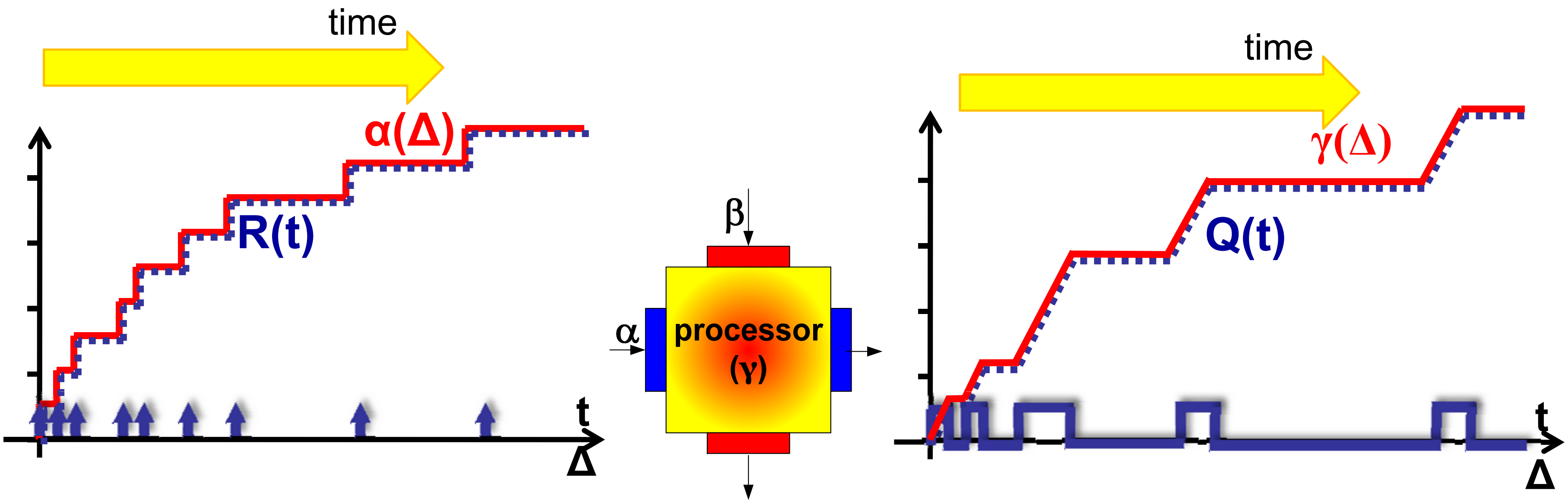
Workload/Computing Time Bounds

α(Δ) corresponds to **time-critical instance**, leading to ***worst-case execution time***

accumulated computing time Q(t) and bound γ(Δ)



***Modular Performance Analysis (MPA) http://www.mpa.ethz.ch**

Power and Temperature Models

- **power model**
  - **active** and **idle** task modes

$$P_a = \phi_a T + \psi_a \qquad P_i = \phi_i T + \psi_i$$

temperature-dependent leakage

- **temperature model**

$$C\frac{dT}{dt} = P - G(T - T_{amb})$$

active/idle power params $\phi_{a/i}$, $\psi_{a/i}$

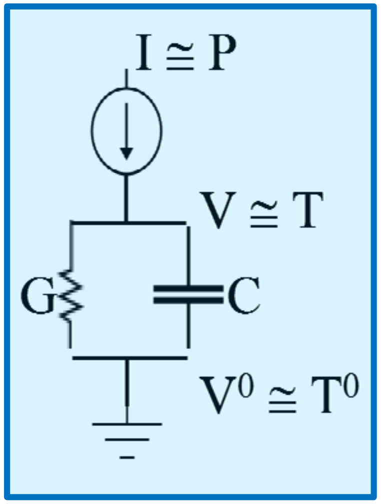
$$\frac{dT}{dt} = -gT + h \text{ with } g = \frac{G-\phi}{C}, \; h = \frac{\psi + GT_{amb}}{C}$$

thermal conductance

thermal capacity

environment temperature

… in analogy with electrical circuits

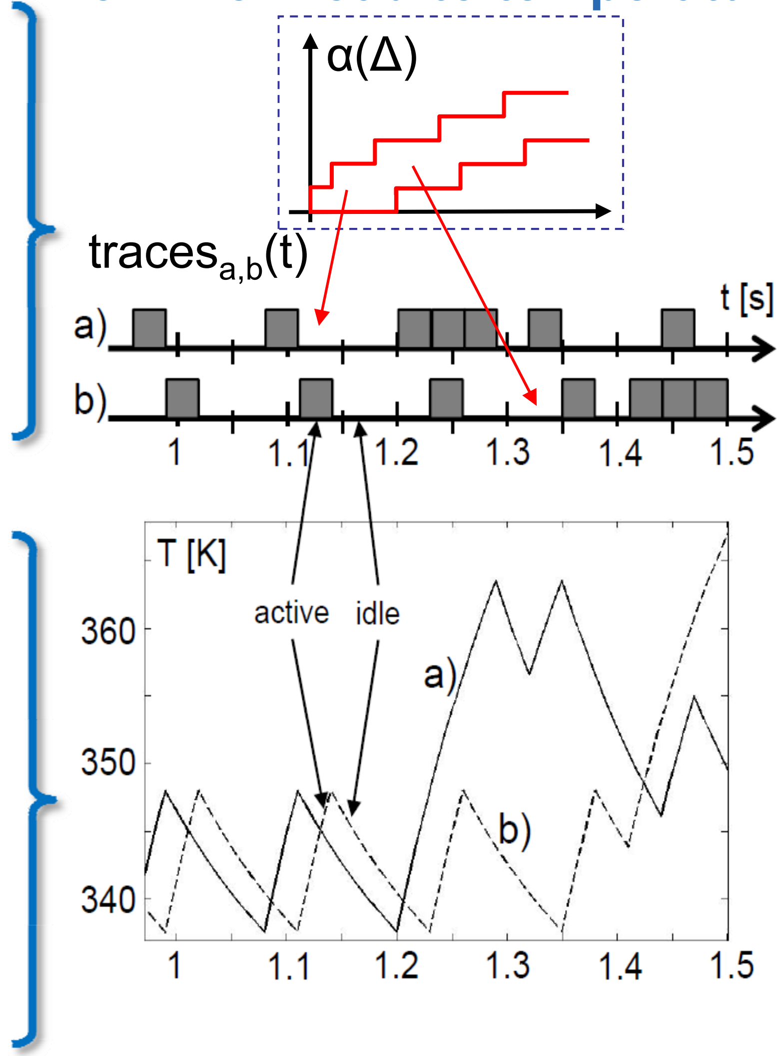


Embedded System – Thermal Model

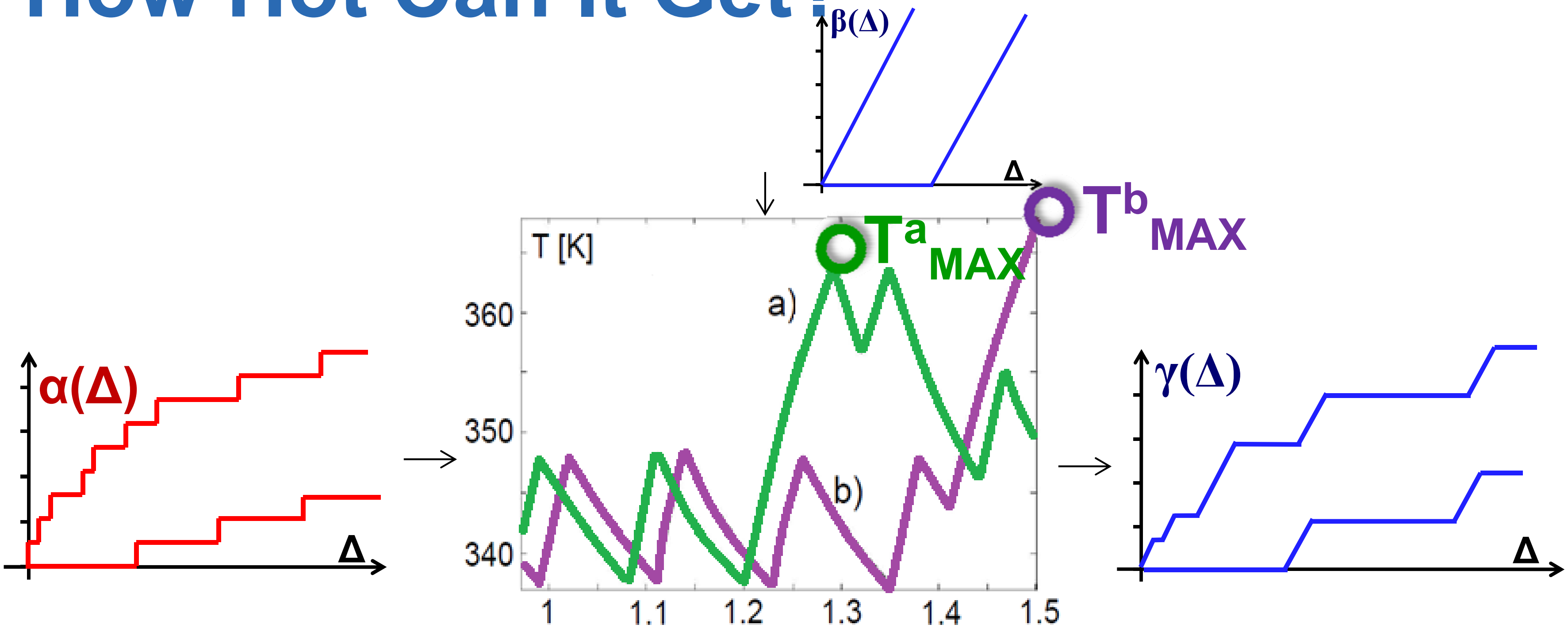
- **bounds on workload arrivals**
  - …arrival curves **$\alpha(\Delta)$**
- **computation model**
  - …from arrival curves to task execution traces **[$tr_a(t)$, $tr_b(t)$, …]**
- **power model**
  - …from task executions to **active/idle power modes**
- **temperature model**
  - …from power to temperature

$$C\frac{dT}{dt} = P - G(T - T_{amb})$$

from workload to temperature



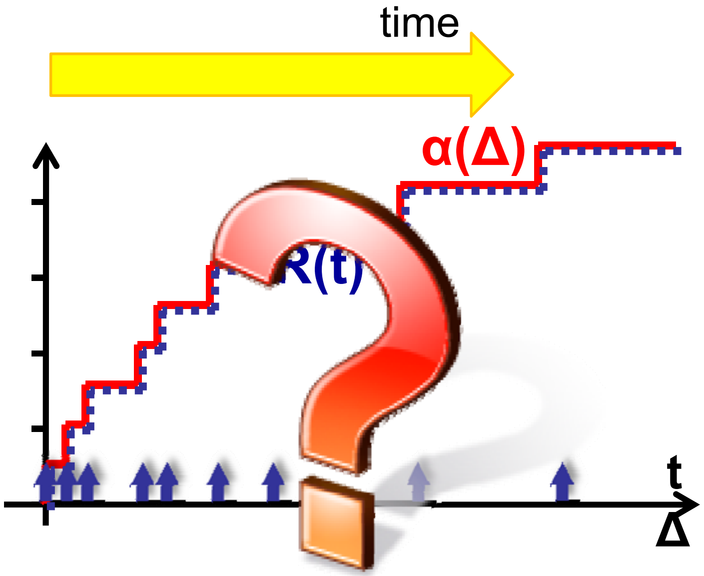
How Hot Can It Get?



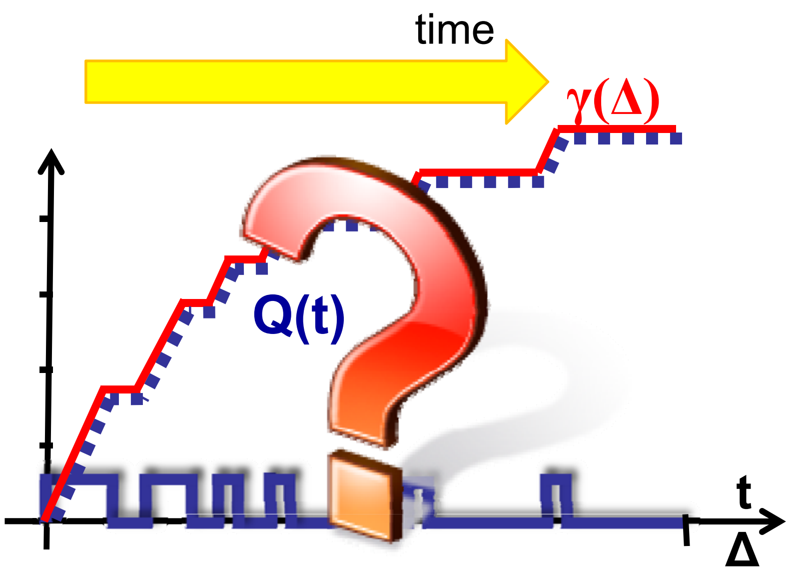
CAN WE DETERMINE
WORST CASE (PEAK) TEMPERATURES
IN MPA COMPOSITIONAL FRAMEWORK?
(AT SYSTEM LEVEL – DESIGN TIME)

Critical Instance for Temperature Analysis?

α(Δ) corresponds to time-critical instance, leading to *worst-case execution time*



γ(Δ) is the upper bound on accumulated computing time, due to α(Δ)



Critical Instance for Temperature Analysis?

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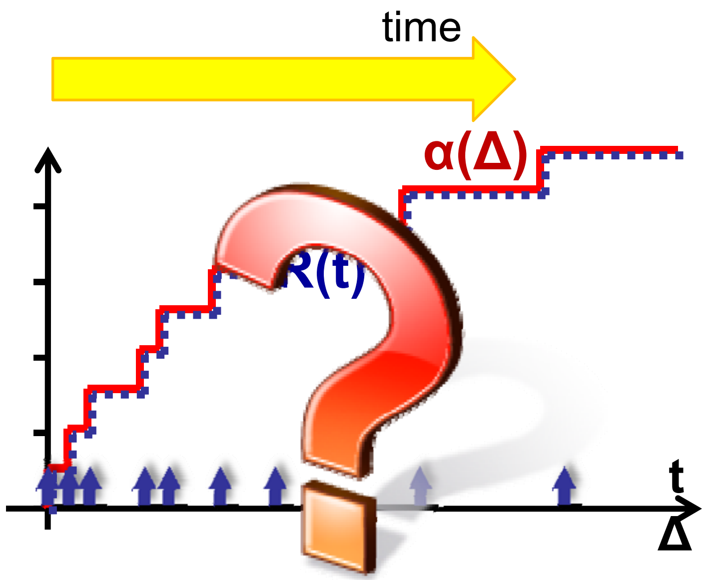
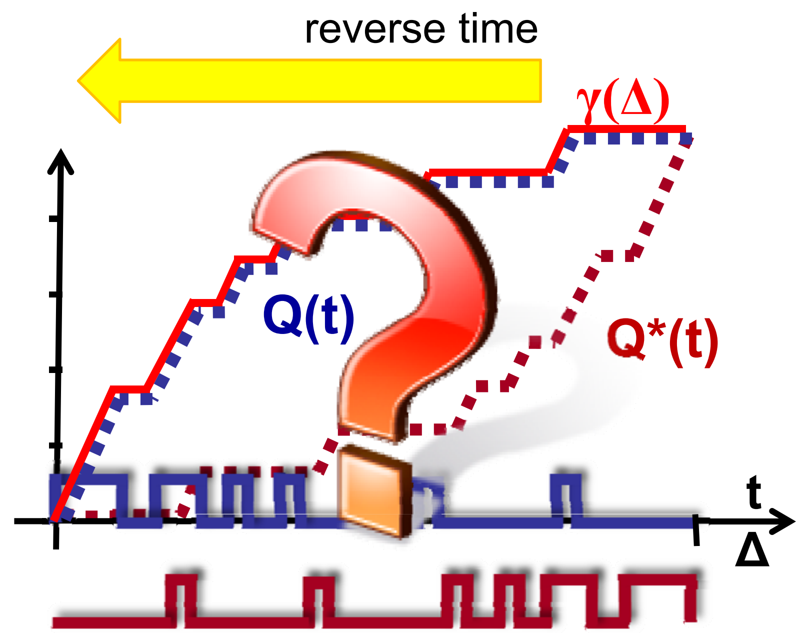
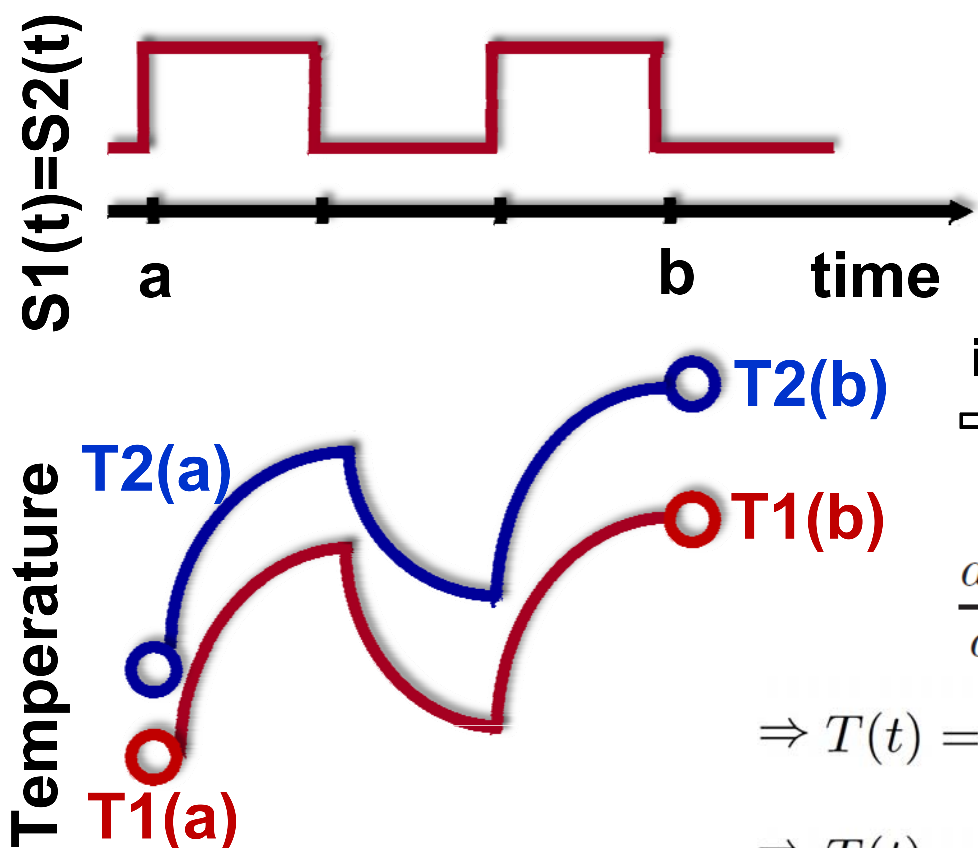


**Q*(t) leads to MAX T*(t)!
(see DATE2011 paper)**



Basics: Thermal Monotonicity

- For 2 equal *idle/active* sequences in [a,b], the sequence with higher initial temperature *T2(a)>T1(a)*, leads to a higher final temperature *T2(b)>T1(b)*.



if T2(a) >T1(a)
⇨ T2(b) >T1(b)

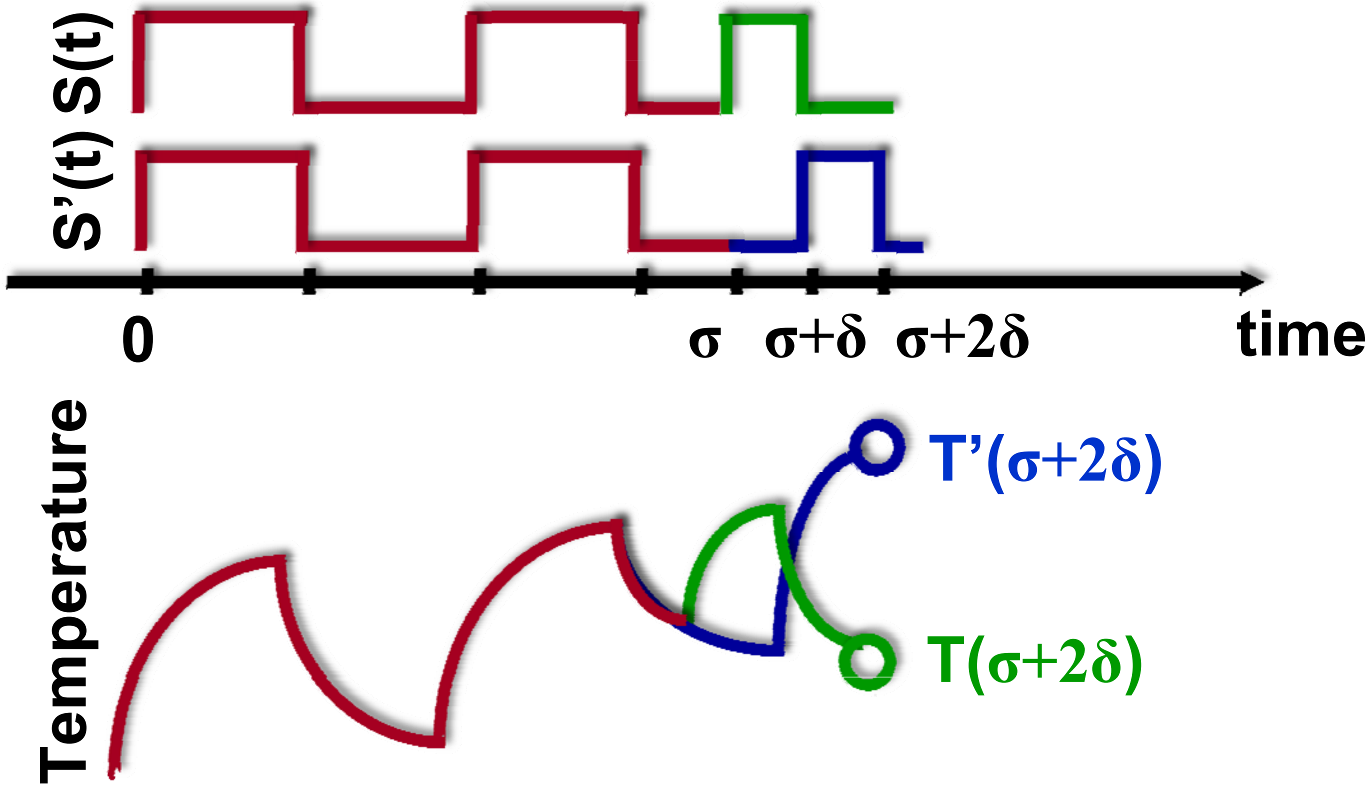
$$\frac{dT}{dt} = -gT + h$$

$$\Rightarrow T(t) = T(t_0) \cdot e^{-g(t-t_0)} + \int_{t_0}^{t} h \cdot e^{g\tau} d\tau$$

$$\Rightarrow T(t) = T_\infty + (T(t_0) - T_\infty) \cdot e^{-g \cdot (t-t_0)}$$

Basics: Exchange Theorem

- Given sequences S(t) and S'(t), differing in [σ, σ+2δ], s.t., ***S(t)=[active, idle]*** and ***S'(t)=[idle, active]***, for the same initial temperature ⇨ **T(τ)≤T'(τ)**



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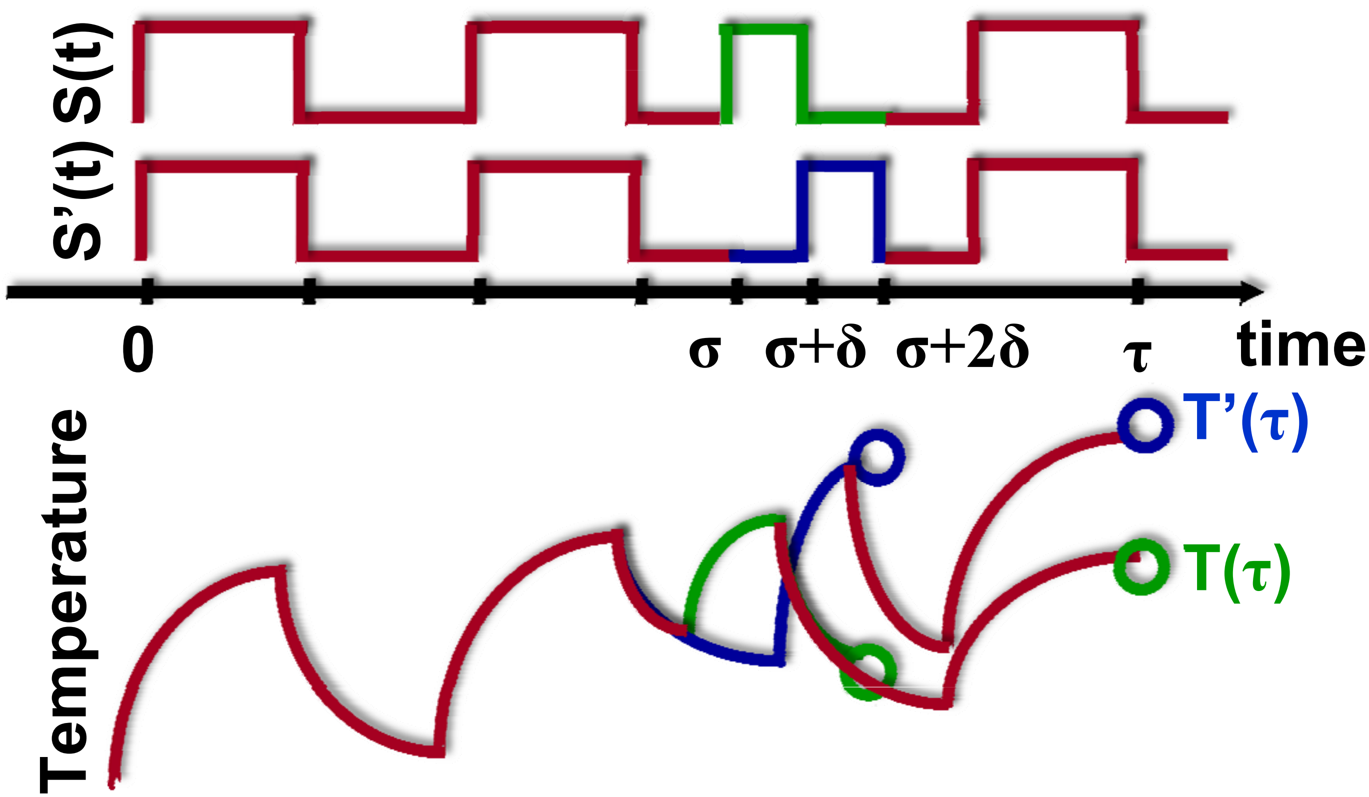
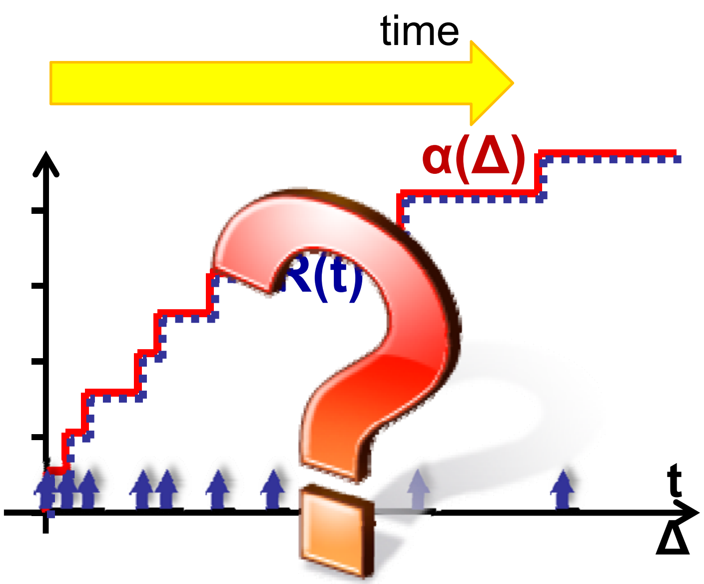
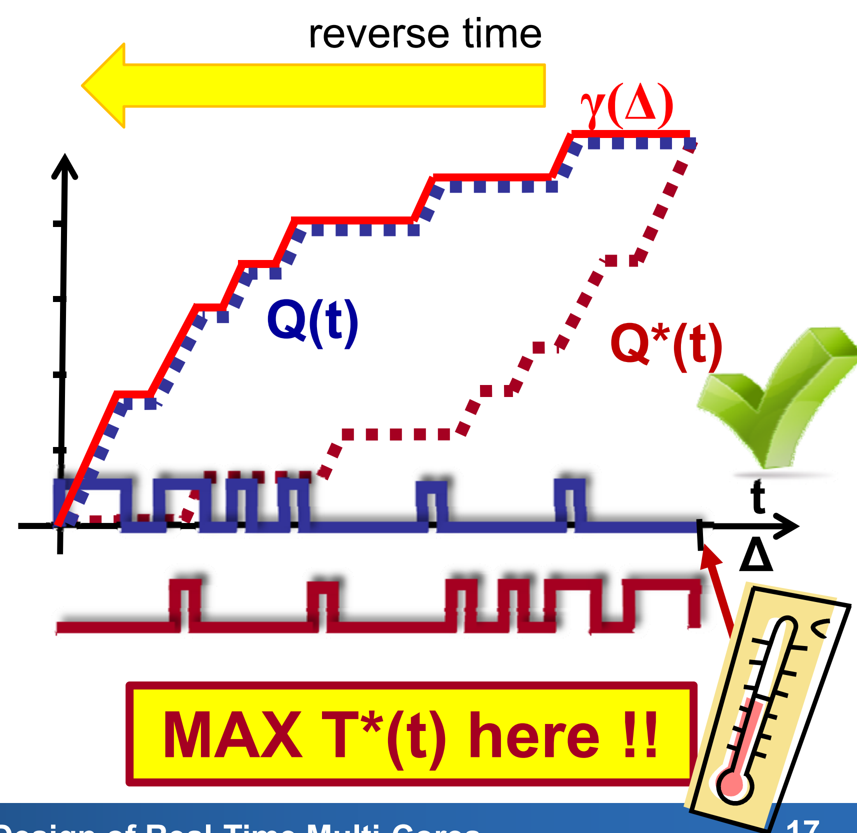


Critical Instance for Temperature Analysis?

does there exist a
feasible input trace
that leads to MAX. peak T°?

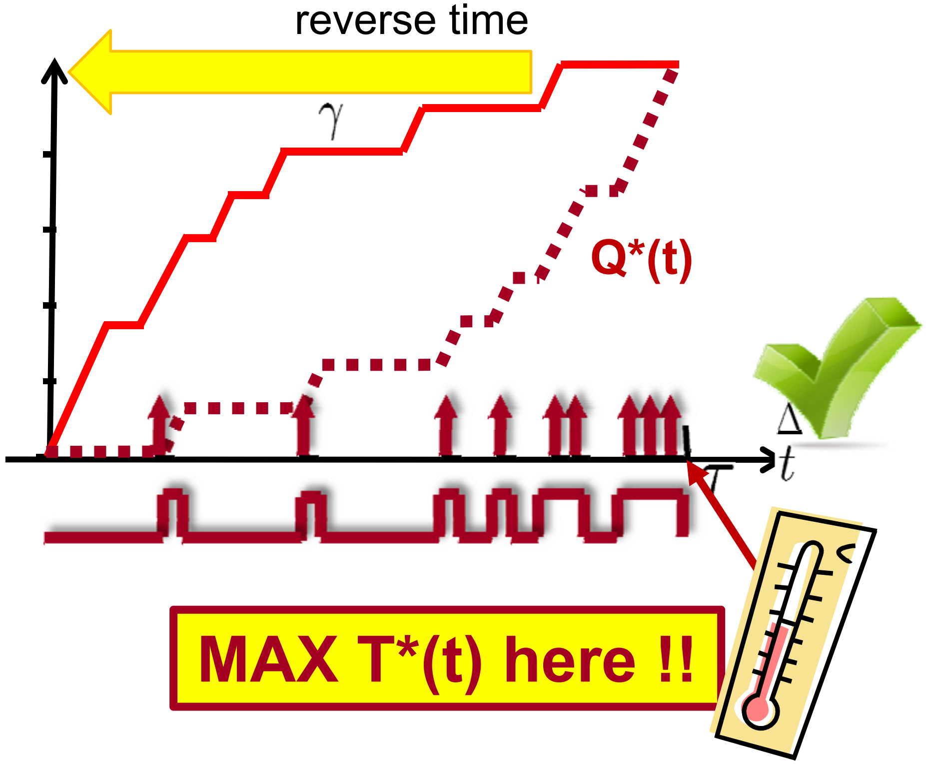
Q*(t) leads to MAX T*(t)!
(see DATE2011 paper)



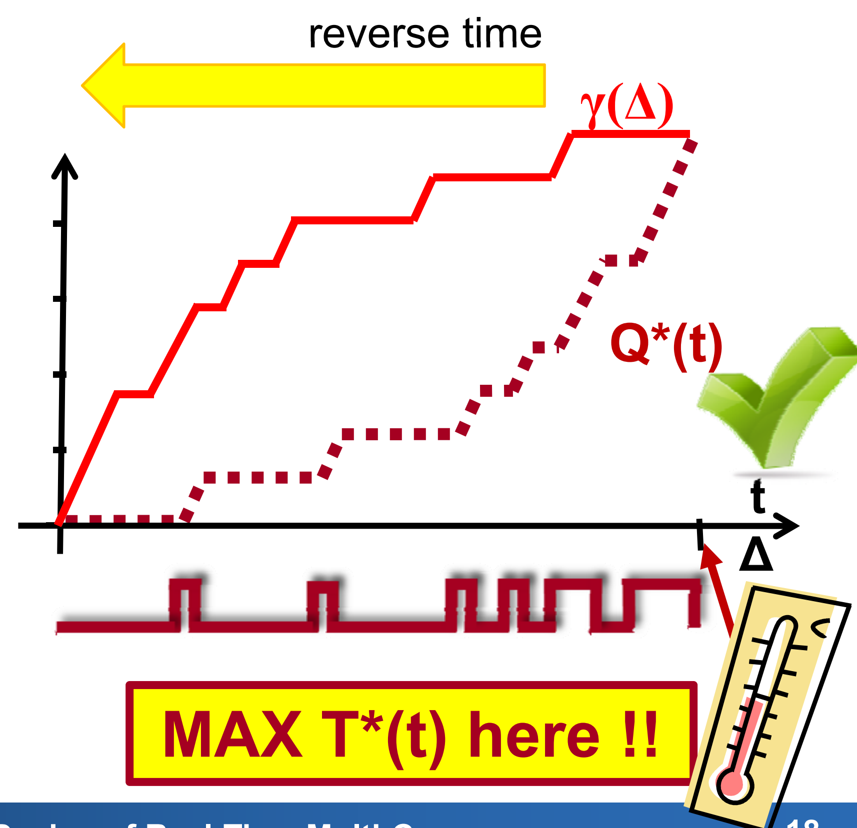


Critical Instance for Temperature Analysis?

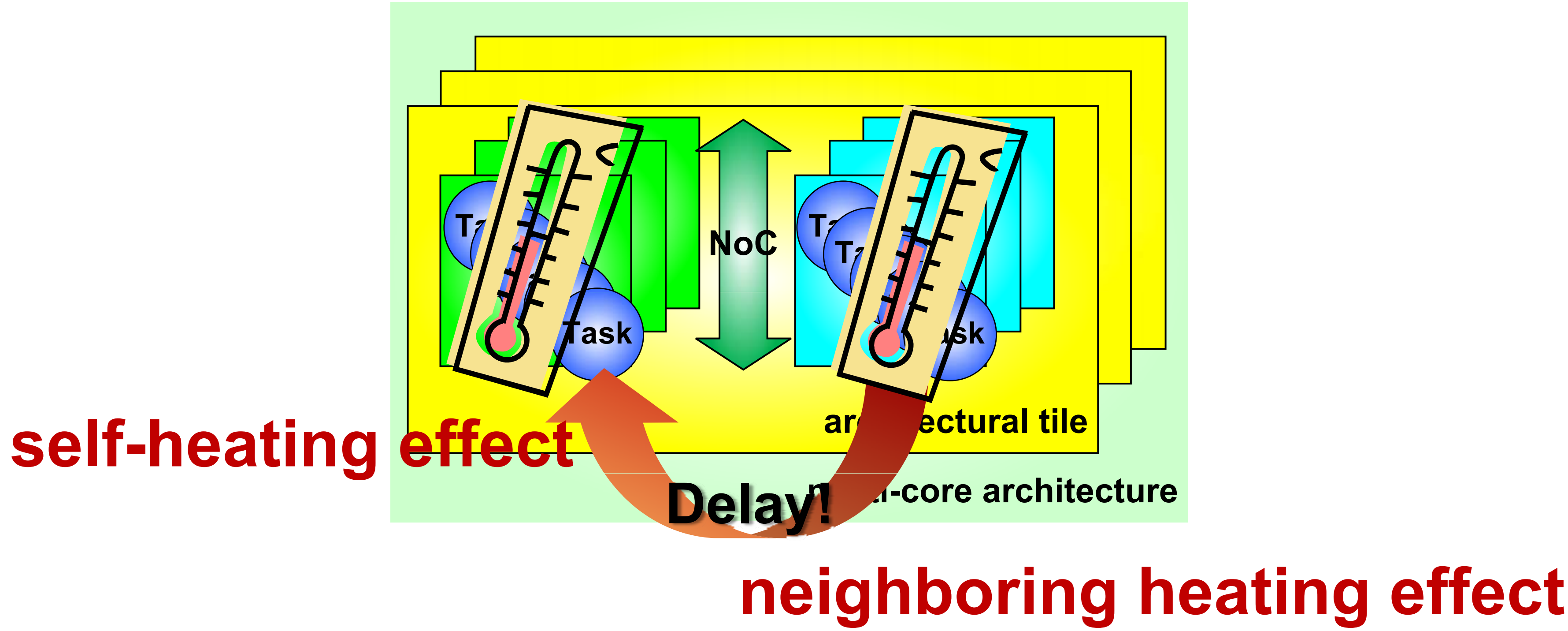
R*(t) = Q*(t) leads to MAX T*(t)!



Q*(t) leads to MAX T*(t)! (see DATE2011 paper)



How about Peak Temperature in Multi-Cores?

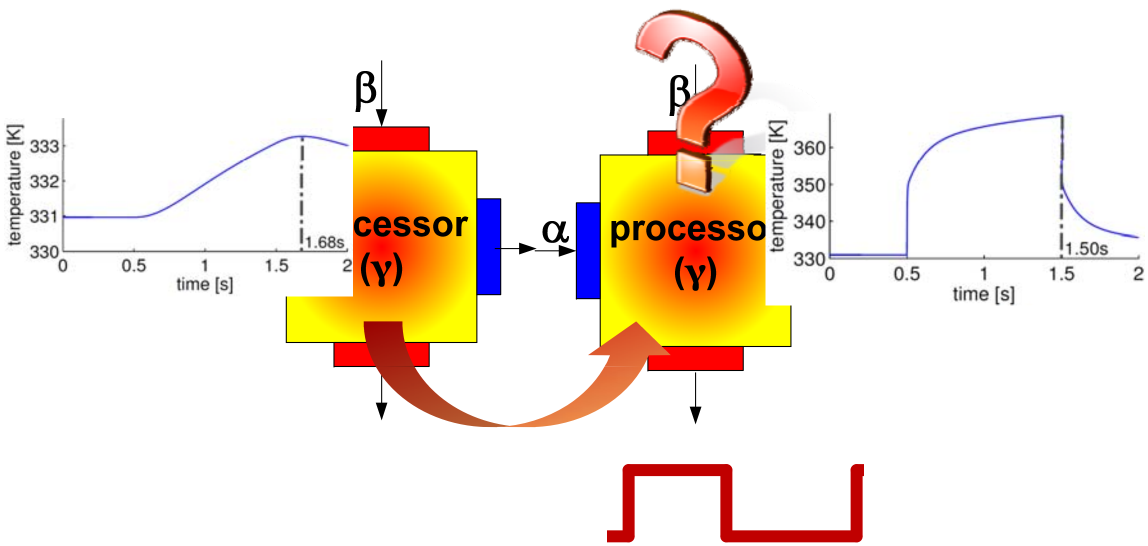


- $T_{MAX}\{SYSTEM\} = \max \{T_{MAX}\{SYSTEM_{\{COMPONENTi\}}\}\}$
- $T_{MAX}\{SYSTEM_{\{COMPONENTi\}}\} =$

  $Tself\_heating_{\{COMPONENTi\}} + \Sigma\ [Tneighboring\_heating_{\{COMPONENTk\}}]$

How about Temperature Critical Instances of Multi-Cores?

1. Reduction to One Input – One Output relation
2. $T_{MAX}\{SYSTEM\} = \max\{T_{MAX}\{SYSTEM_{\{COMPONENTi\}}\}\}$



$T^*_{2,2}$	304 K
$T^*_{2,1}$	41 K
T^*_2	345 K

Thermal Optimization Problem

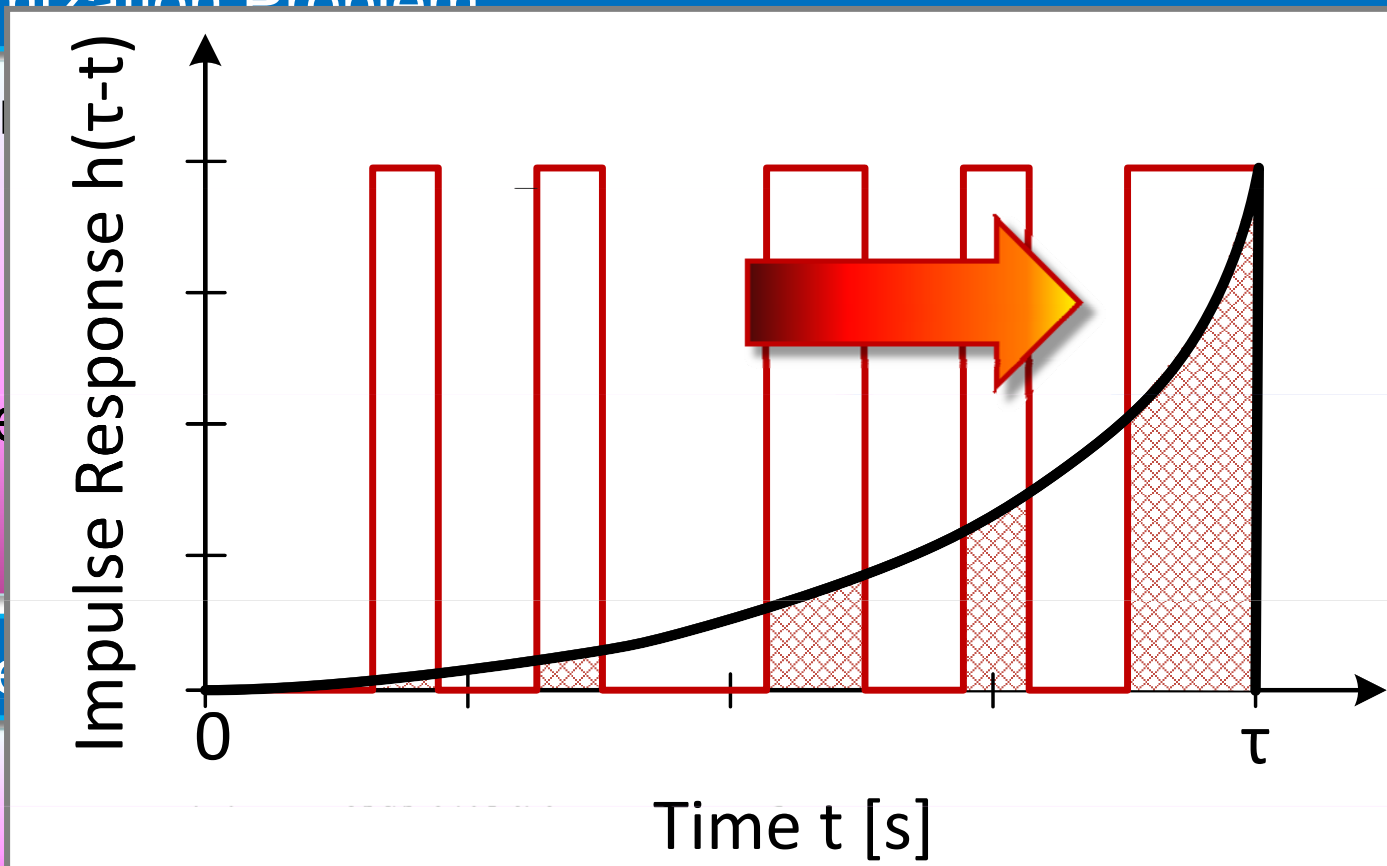
Optimization Problem

Maxi

Subje

e

Mode



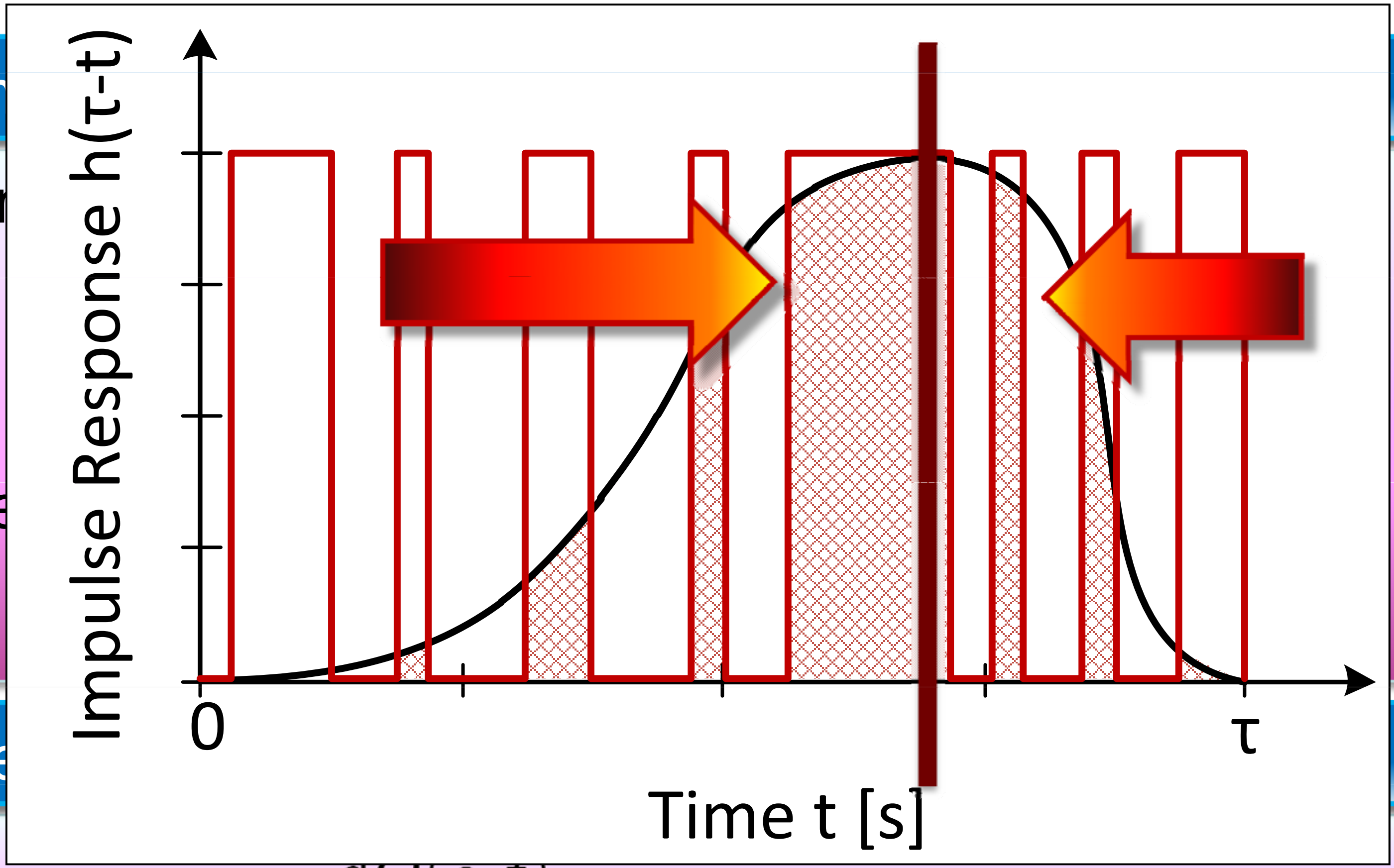
Thermal Optimization Problem

Optir

Maxir

Subje

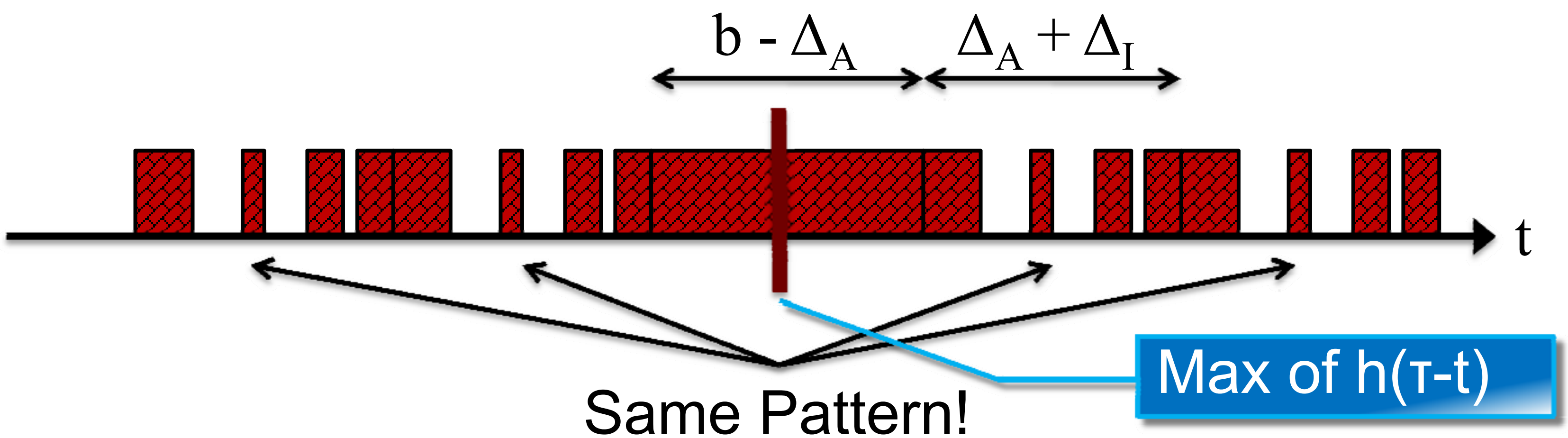
Mode



$$S(t) = \frac{dQ(s,t)}{dt} \in \{0,1\}$$

Critical Instance for Multi-Cores – Exact Sol.

Exact Solution

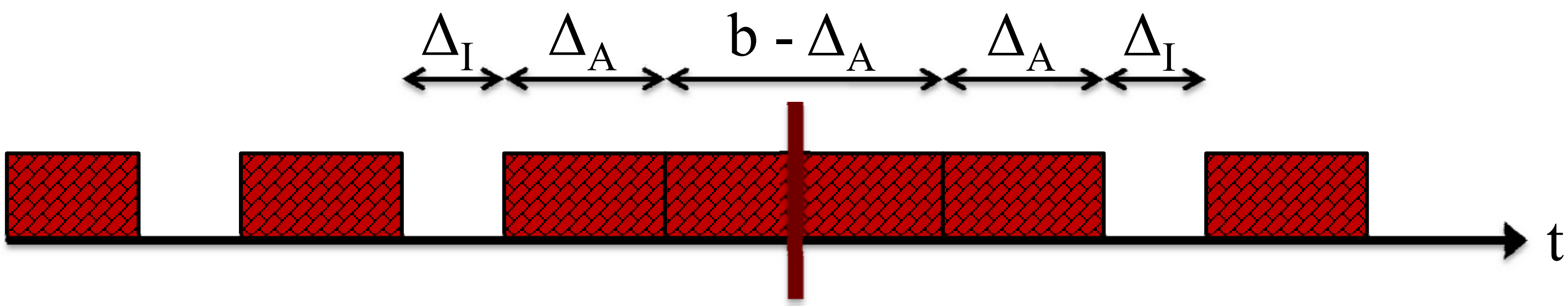


Exhaustive search:

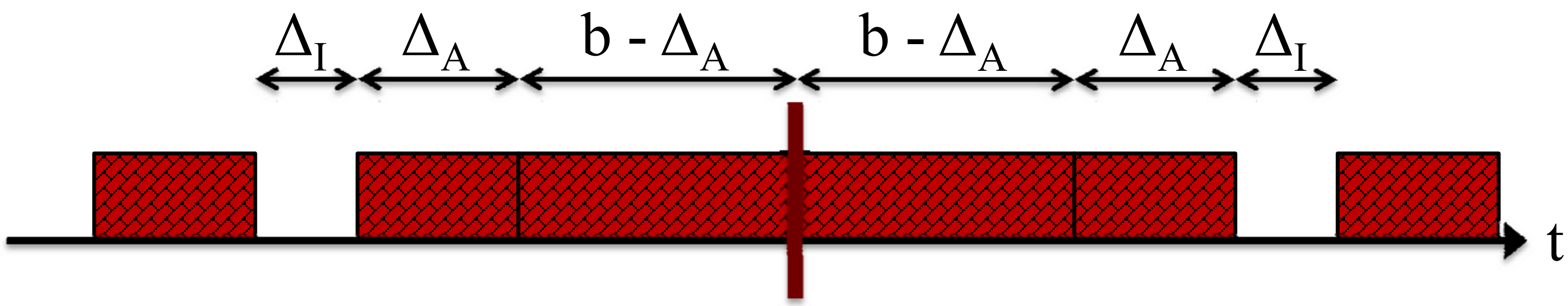
- Position of the first block?
- Pattern?

Critical Instance for Multi-Cores – Approx.

Approximation 1



Approximation 2



How large should τ be?

- All observation times **t ≤ τ** guarantee peak-temperature precision of **$T^*_a(\tau)$-$T^*_i(\tau)$** for estimating **T*** with upper bound **$T^*_a(\tau)$**

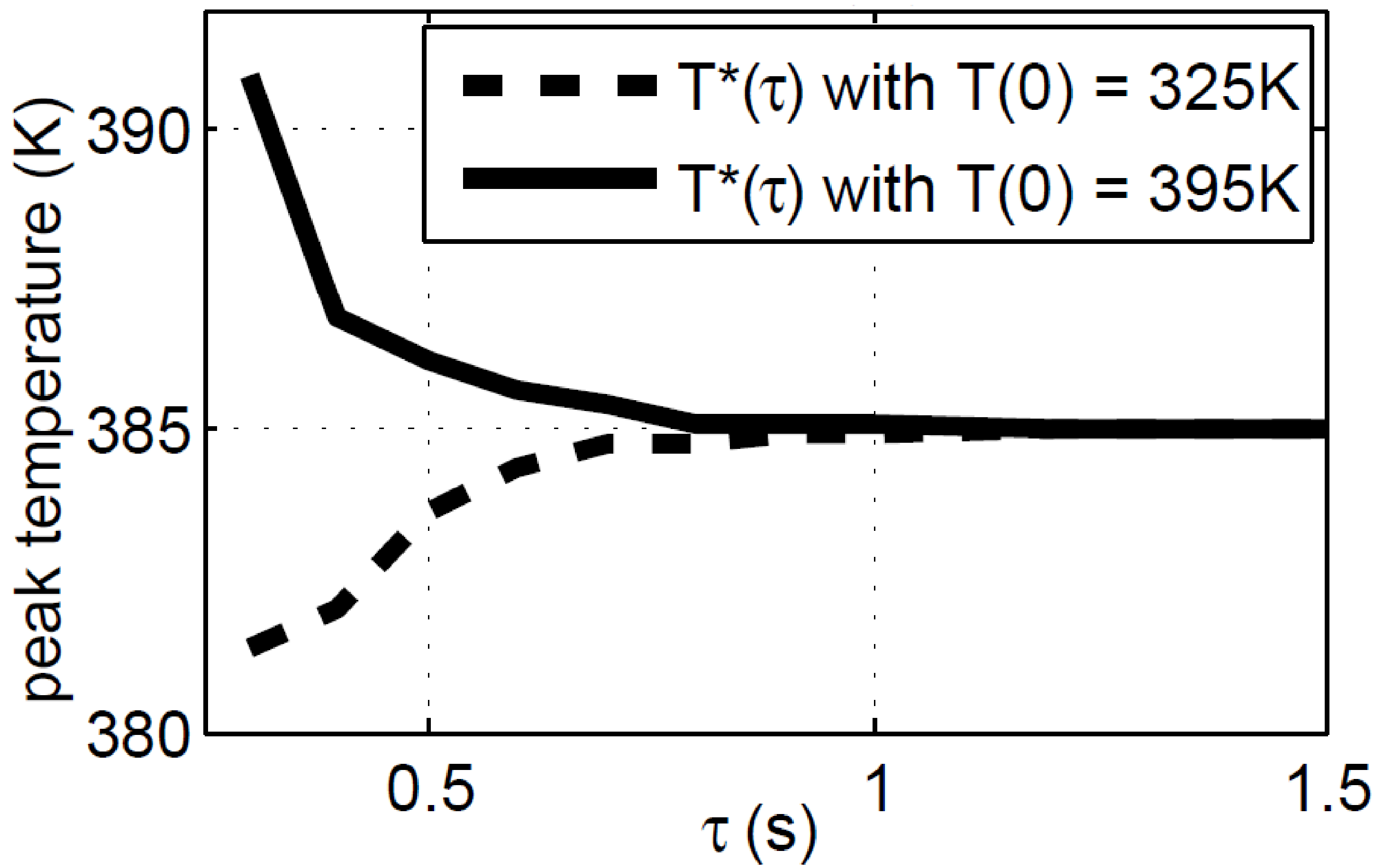
$$\tau \geq \frac{1}{\min\{g_i, g_a\}} \cdot \log \frac{(T_\infty)_a - (T_\infty)_i}{T^*_a(\tau) - T^*_i(\tau)}$$

thermal coefficients for *active/idle* power modes

steady-state temperatures for *active/idle* modes

temperatures for *active/idle* modes at τ, with initial $(T\infty)_a/(T\infty)_i$

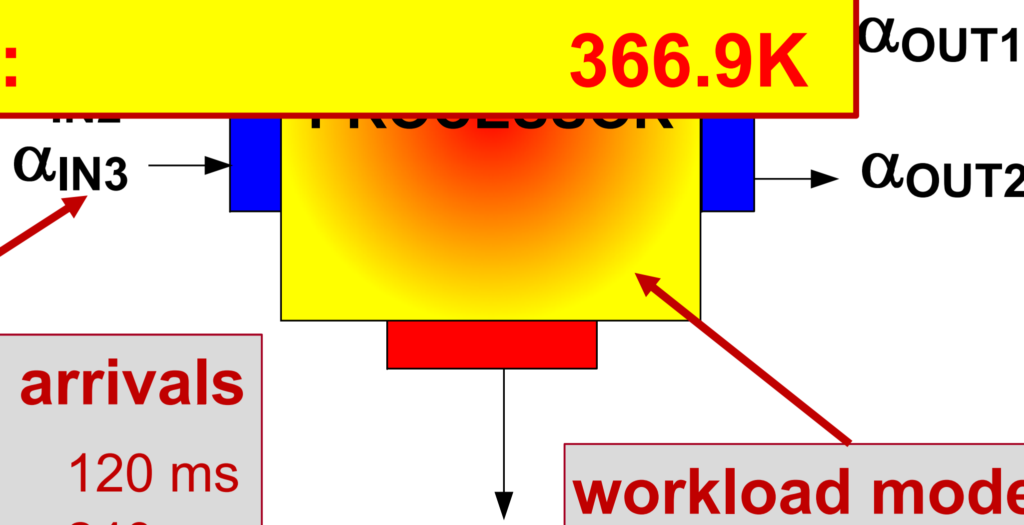
How Large Should τ Be?



Simple Example

peak temperatures

- average workload (25%): **342.5K**
- random traces (500 s): **362.2K**
- reasonable heuristic: **363.5K**
- **worst case: 366.9K**



bounds on event arrivals

- period:	120 ms
- jitter:	240 ms
- inter-arrival time:	30 ms

workload model

- execution time: 30ms

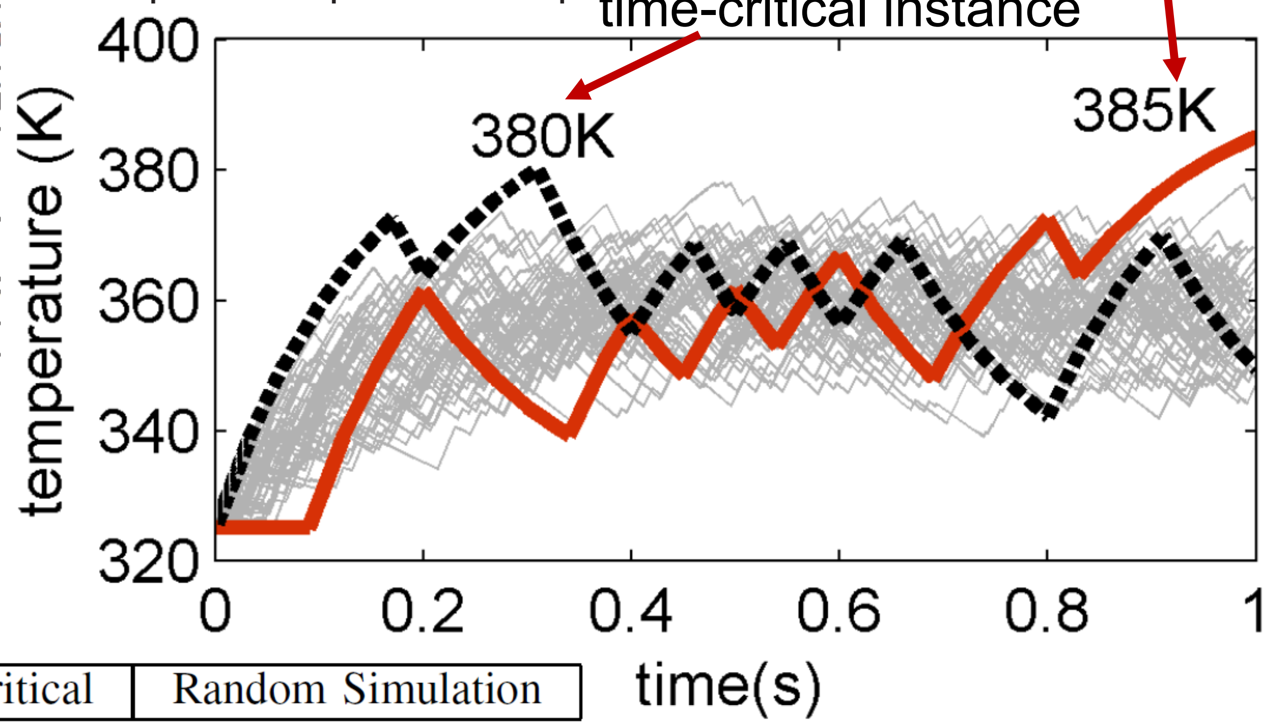
Example 2: 3-Multi-Media Applications

	Video	Audio	Network
period (p)	[20, 90]ms	30ms	30ms
jitter	[20, 90]ms	10ms	10ms
min. inter-arrival	1ms	1ms	1ms
execution demand	6		
deadline	peri		

G	C	$\phi_i =$
$0.3\frac{W}{K}$	$0.03\frac{J}{K}$	0.1

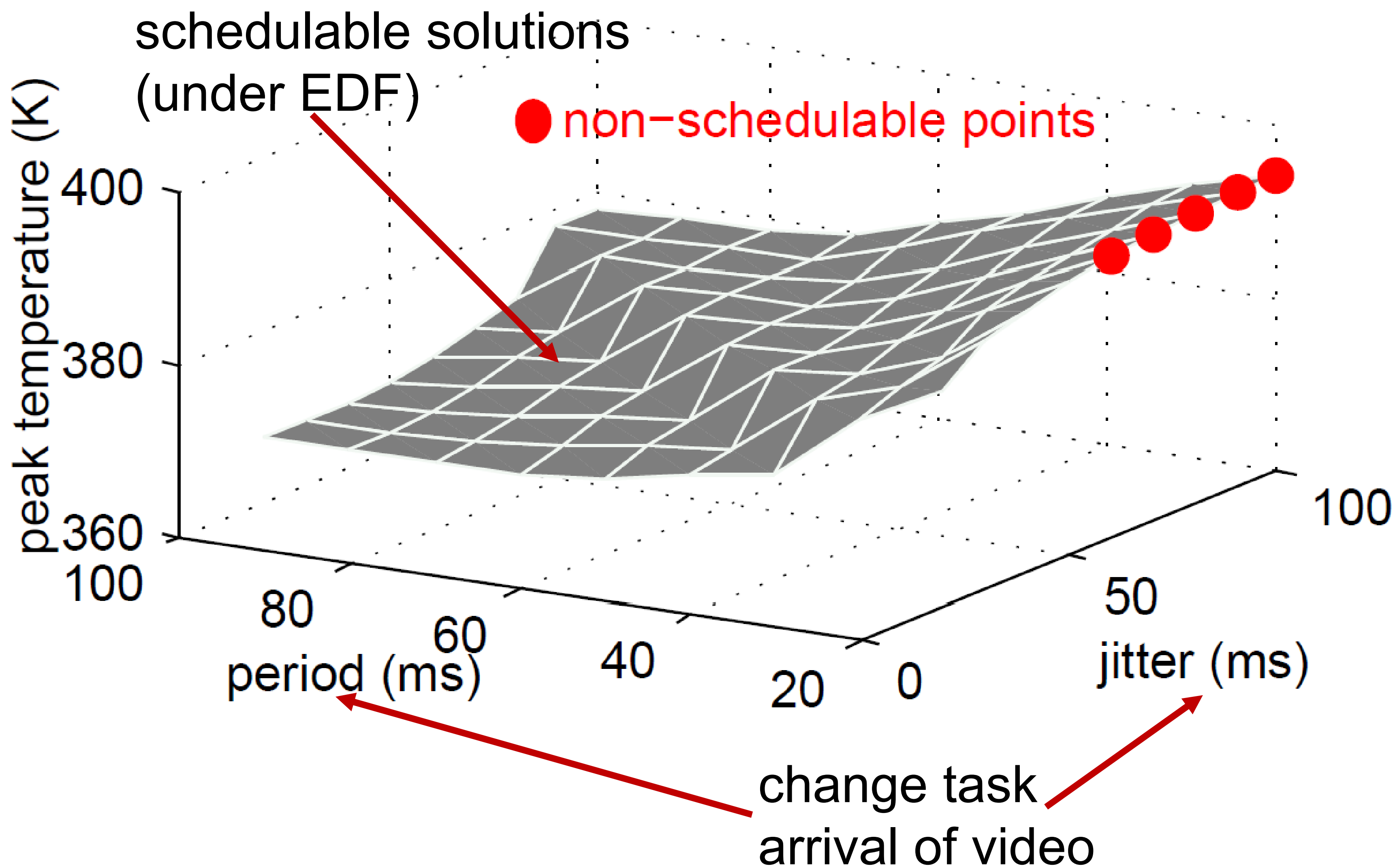
peak temperature for temperature-critical instance

peak temperature for time-critical instance



Thermal critical	Timing critical	Random Simulation
$385.00K$	$380.00K$	$378.00K$

Example 2: Design Space Exploration

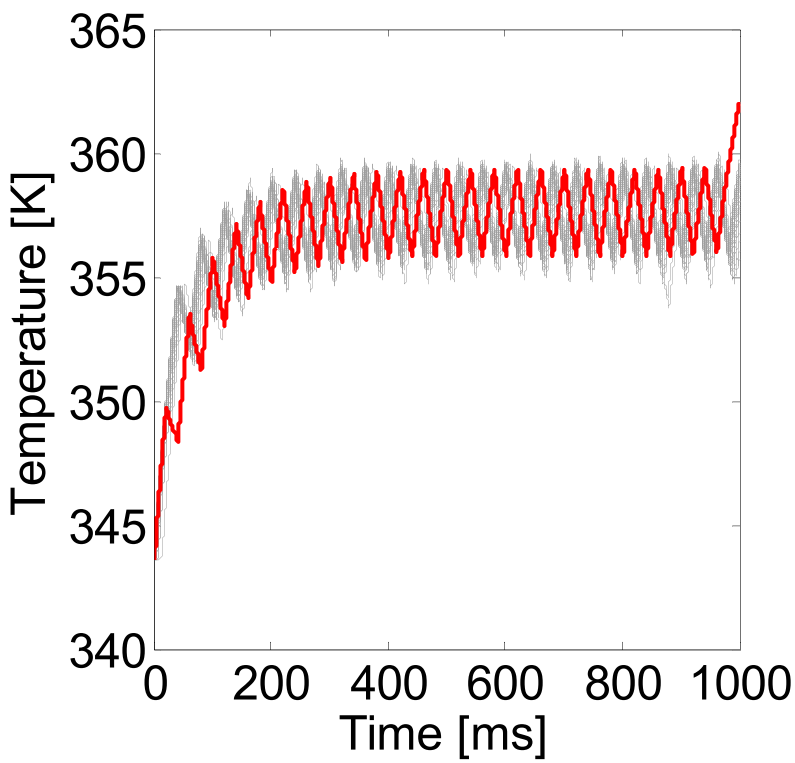


Multi-Core Evaluation: Setup

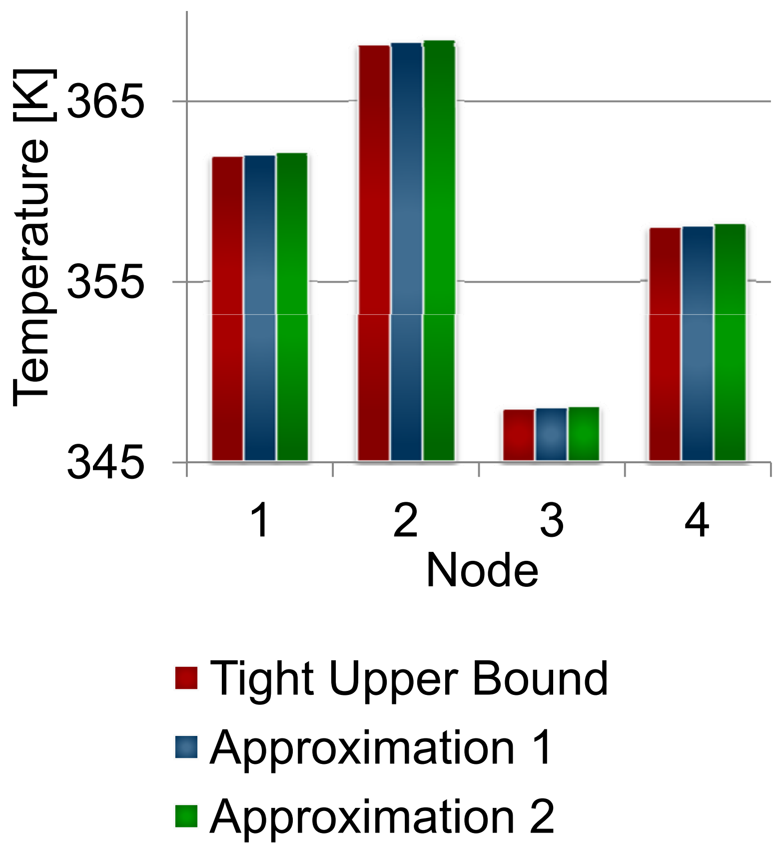
	Processing Component 1	Processing Component 2	Processing Component 3	Processing Component 4
Period p	40ms	44ms	24ms	36ms
Jitter j	20ms	22ms	48ms	36ms
Min. inter-arrival a	1ms	1ms	1ms	1ms
Execution demand d	20ms	22ms	12ms	18ms

Multi-Core Evaluation: Result

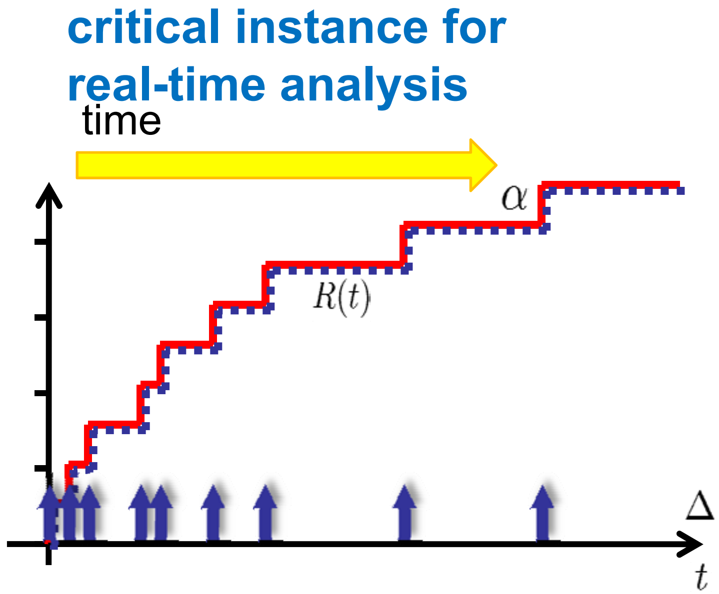
Random Trace

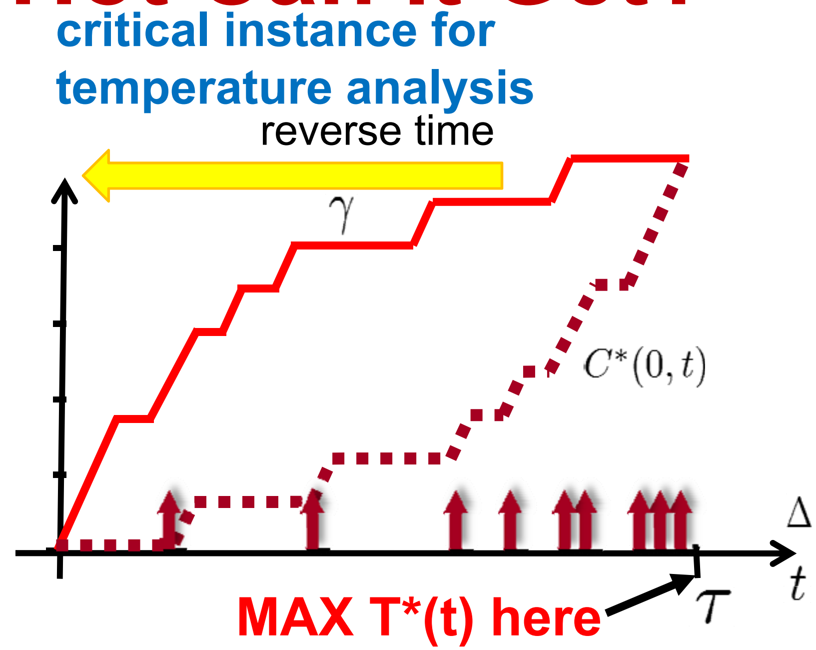


Approximation



In Conclusion: How Hot Can It Get?





- Analytic framework **guaranteeing max temperature** on-chip, at system-level and at design time
- Optimize mappings w.r.t. **time AND temperature**
- Results integrated in **MPA toolbox (http://www.mpa.ethz.ch)**