

# Schedulability analysis of Ravenscar systems with MAST+



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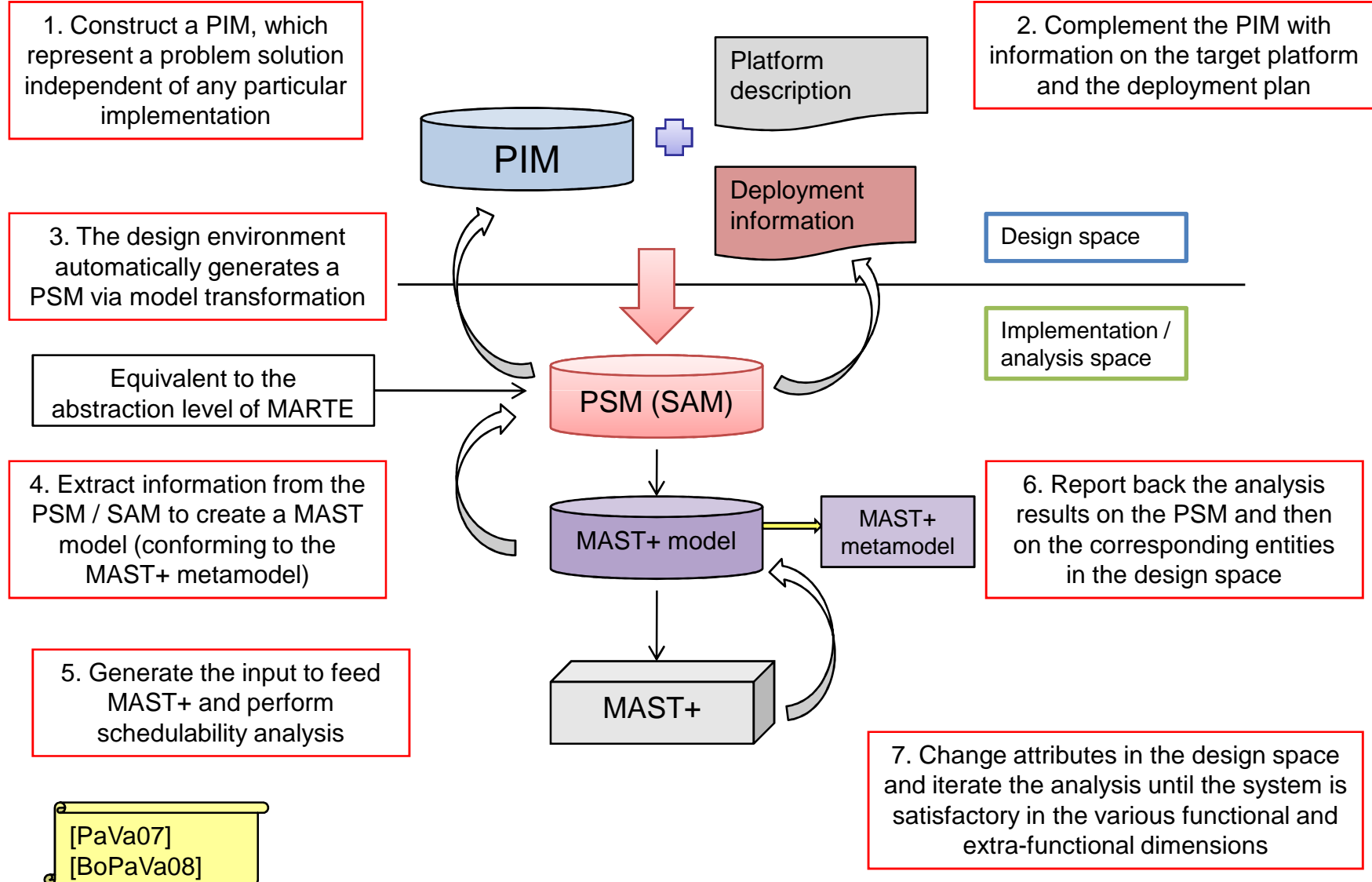
# Outline

- **Overview on MAST+**
  - Use of MAST+ in the ASSERT project
- **Overview on the Ravenscar Profile**
- **Ravenscar-aware schedulability analysis**
- **Implementation in MAST+**
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  - MAST+
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# Overview on MAST+

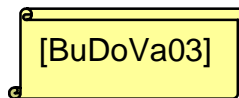
- **Developed in the scope of the ASSERT project**
  - ❑ FP6 [2004-2008]
  - ❑ Model-based process for the development of on-board software
- **Support for**
  - ❑ Modeling of systems abiding by the priority-band architecture
    - ❑ Hierarchical architecture of interest for the project
  - ❑ Modeling of Ravenscar systems
  - ❑ Ravenscar-aware scheduling analysis
    - ❑ Holistic analysis
  - ❑ XML output [missing in MAST at that time]
- **Realized as an extension to MAST 1.3.6**
  - ❑ Developed in the period August 2006-December 2007

# Use of MAST+ in the ASSERT project



# Overview on the Ravenscar profile

- **Restricted tasking model for the Ada programming language**
  - ❑ Removes all sources of non-determinism and unbounded execution cost
  - ❑ Can be implemented in a small and efficient real-time kernel
  - ❑ Can be conceptually mirrored in other languages (e.g. RTSJ)
- **Ravenscar programs are amenable to static analysis**
  - ❑ Static existence model
    - ❑ Fixed set of tasks and interrupts, fixed priorities, no task termination
  - ❑ Static synchronization and communication model
    - ❑ No task synchronization (rendezvous)
    - ❑ Asynchronous one-way communication mediated by protected objects
  - ❑ Deterministic execution model
    - ❑ Max 1 PO Entry, Max 1 Task per PO Entry, No Relative Delay, No Asynchronous Control, use of high-precision notion of time (e.g. Ada.Real\_Time)
  - ❑ Deterministic memory usage
    - ❑ No\_Implicit\_Heap\_Allocations



# Ravenscar-aware schedulability analysis

Classical uniprocessor response time equation

$$w_i^n = B_i + C_i + \sum_{j \in hp(i)} \left\lceil \frac{w_i^{n-1} + J_i}{T_j} \right\rceil C_j$$

Validity condition

$$D_i \leq T_i$$

Termination condition

$$w_i^{n+1} = w_i^n$$

Ravenscar uniprocessor equations

$$w_i^n = \max(B_{ker}, B_i) + CS1 + C_i + \sum_{j \in hp(i)} \left\lceil \frac{w_i^{n-1} + J_i}{T_j} \right\rceil (CS1 + C_j + TS + CS2) + I_{clock}^{w_i^{n-1}} + I_{extint}^{w_i^{n-1}}$$

Kernel blocking time
“In” Context switch
“In” Context switch
Suspension overhead
“Out” Context switch
Clock overhead
Interrupt management

$$I_{clock}^{w_i^n} = I_{periodic}^{w_i^n} + I_{demanded}^{w_i^n} = \left\lceil \frac{w_i^n}{T_{periodic}} \right\rceil CH_{periodic} +$$

$$\sum_{j \in hp_{periodic}(i)} \left\lceil \frac{w_i^n}{T_j} \right\rceil CH_{demanded} + \sum_{k \in lp_{periodic}(i)} CH_{demanded}$$

CS1=Ready+Select+Switch

CS2=Select+Switch

TS<sub>periodic</sub>=Delay\_until

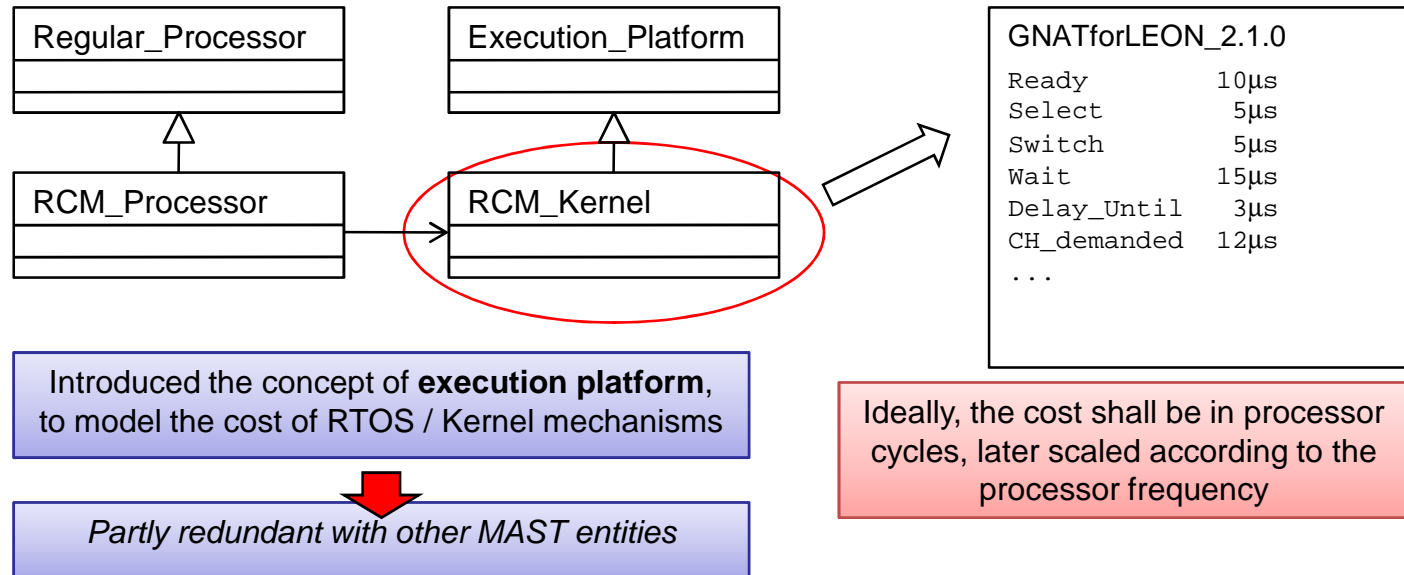
TS<sub>sporadic</sub>=Delay\_until+Wait(Enter)

Knowledge of *which* kernel mechanisms (and *how many times*) are used in a busy interval

[VaZaPu05]

# Implementation in MAST+

## 1) System modeling



## 2) Analysis tools

- **Implemented a Ravenscar-aware holistic analysis**
  - ❑ The analysis tool can access the kernel metrics and use them as terms in the equations
  - ❑ Considerable as a “feasibility study” for the implementation of Ravenscar-aware offset-based analysis

# Conclusions

- **MAST+**
  - ❑ Created as part of a MDE process
    - ❑ Supported also by the “follow-up” of the ASSERT project, named CHESS
  - ❑ Responds to important modeling and analysis needs
    - ❑ Ravenscar systems
    - ❑ The implementation was not optimal
      - ❑ Constrained by other project- and maintenance-related aspects
  - ❑ Support is discontinued
    - ❑ Too costly to backport the changes of newer versions of MAST
      - ❑ Easier to re-start directly from MAST 1.3.8



# Evolution of MAST

- **Relationship with the UML MARTE profile**
  - Development of standard converters to and from MAST
- **Easy of extensibility to support additional analysis tools and platforms**
- **How to promote a third-party extension to the mainstream version of MAST?**

# Bibliography

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