

AFDX networks

By: J. Javier Gutiérrez (gutierjj@unican.es)

Computers and Real-Time Group, University of Cantabria

**ArtistDesign Workshop on Real-Time System Models for
Schedulability Analysis**

Santander, 7-8 February 2011

Introduction to AFDX networks

AFDX (Avionics Full Duplex Switched Ethernet) is a communications network defined in the ARINC-664, Part 7 standard:

- point to point full duplex Ethernet links (redundant)
- special purpose switches with preconfigured routing
- two main types of communication ports:
 - *Sampling Port*: the arriving message overwrites the current message stored in the buffer
 - *Queueing Port*: the arriving message is appended to a FIFO queue
- UDP/IP protocol is used for transmission
- traffic regulation is made in transmission via *Virtual Links*

Traffic regulation in AFDX

Each virtual link (VL) is characterized by two parameters:

- the largest Ethernet frame (**Lmax**): a value in bytes that can be transmitted on the VL
- the Bandwidth Allocation Gap (**BAG**):
 - the minimum interval in milliseconds between Ethernet frames transmitted on the VL
 - a power of 2 value in the range [1,128]

Each virtual link has a FIFO queue for all the fragmented packets:

- the same VL can be shared by several ports, tasks or partitions
 - It can cause a poor schedulability of the system
- there is no way to prioritize messages on a VL

Maximum jitter

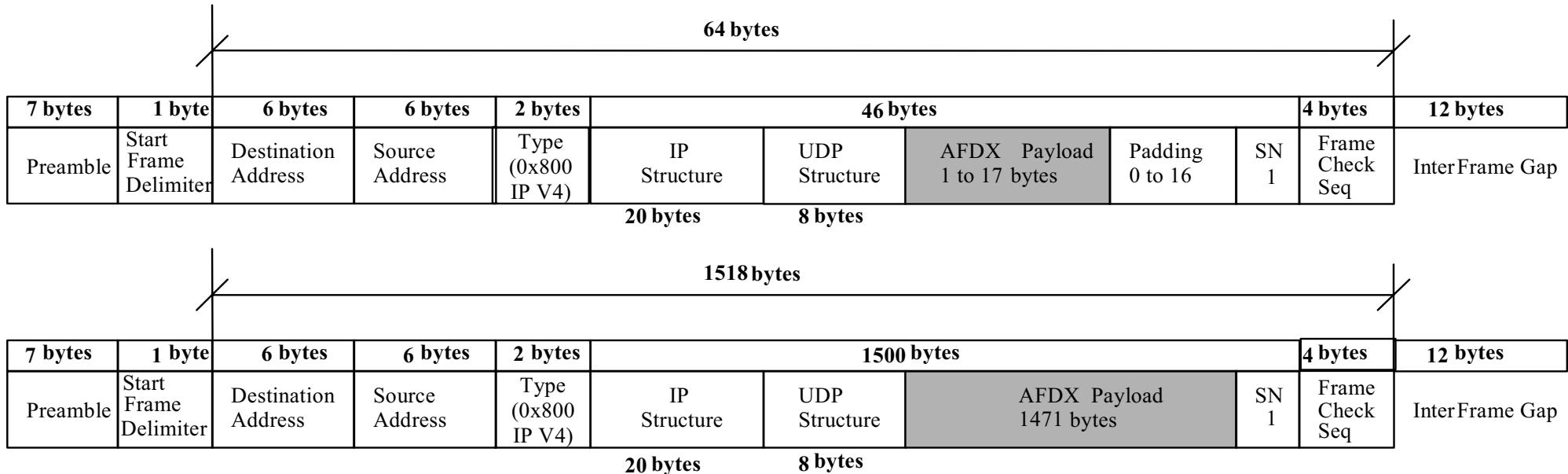
The maximum allowed jitter on each VL at the output of the end system should comply with both of the following formulas:

$$MaxJitter \leq 40\mu s + \frac{\sum_{i \in \{setofVLs\}} ((20 + Lmax_i) \cdot 8)}{N_{bw}}$$

$$MaxJitter \leq 500\mu s$$

- N_{bw} is the speed of the Ethernet link in bits per second
- 40 μs is the typical minimum fixed technological jitter

Ethernet frame



- L_{max} should be in the interval [64,1518]

Sub-Virtual Links

A virtual link can be composed of a number of Sub-Virtual Links

Each Sub-VL has:

- a dedicated FIFO queue
- a round robin algorithm working over IP fragmented packets

Latency in the transmission

If fragmentation is not required and the messages are produced at a frequency that is equal to or lower than the *BAG* of the VL:

$$\text{MaxLatency} \leq \text{BAG} + \text{MaxJitter} + L_T$$

- L_T is the technological latency in the transmission (it should be lower than $150\mu\text{s}$).

If fragmentation is required or messages are produced in bursts, the latency for packet p (with $p-1$ packets waiting in the VL FIFO queue):

$$\text{MaxLatency}(p) \leq p \cdot \text{BAG} + \text{MaxJitter} + L_T$$

AFDX switch

Transmissions to or from the switch are made using the full capacity of the physical link

Packets are delivered in a store and forward way:

- **the hardware latency of the switch should be taken into account**

A new source of jitter appears in the FIFO queue where packets should wait to be sent to the destination end system

Latency in the reception

Once a message is completely received, it is enqueued at the corresponding AFDX port

- it could potentially overflow

The technological latency of the end system in reception, L_R , should be lower than $150\mu\text{s}$

Modelling

The model is similar to the one for the analysis of tasks

We consider two types of messages:

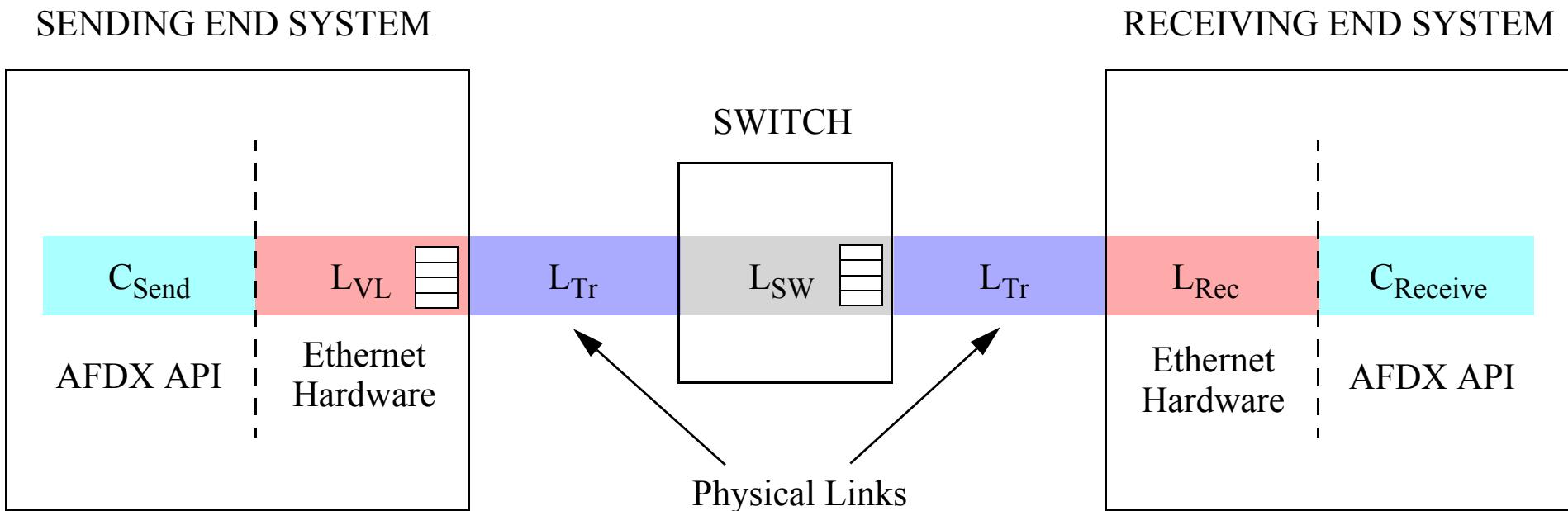
- **Synchronized:**
 - the release times of these messages are relative to a general and *common reference of time*
 - an *offset* to represent the interval between the start of the MAF (Major Frame) and the earliest release of the message
- **Non-synchronized:** messages can be released at any time

Modelling (cont'd)

Different types of parameters to model AFDX communication:

- message stream parameters
 - M_i , p_i , Np_i , N_i , M_i^b , p_i^b , Np_i^b , N_i^b , T_i , Φ_i , J_i , $\text{Source}(\sigma_i)$, L_i , L_i^b
- VL parameters
 - BAG_j , L_{max_j} , $\text{SourcePorts}(VL_j)$, $\text{DestinationPorts}(VL_j)$
- hardware parameters
 - N_{bw} , L_T , L_{Tmin} , J_{Tech} , L_R , L_R^b , L_S^b
- Ethernet frame and protocol parameters
 - O_{Eth} , O_{Prot} , N_{min}

Latency Model

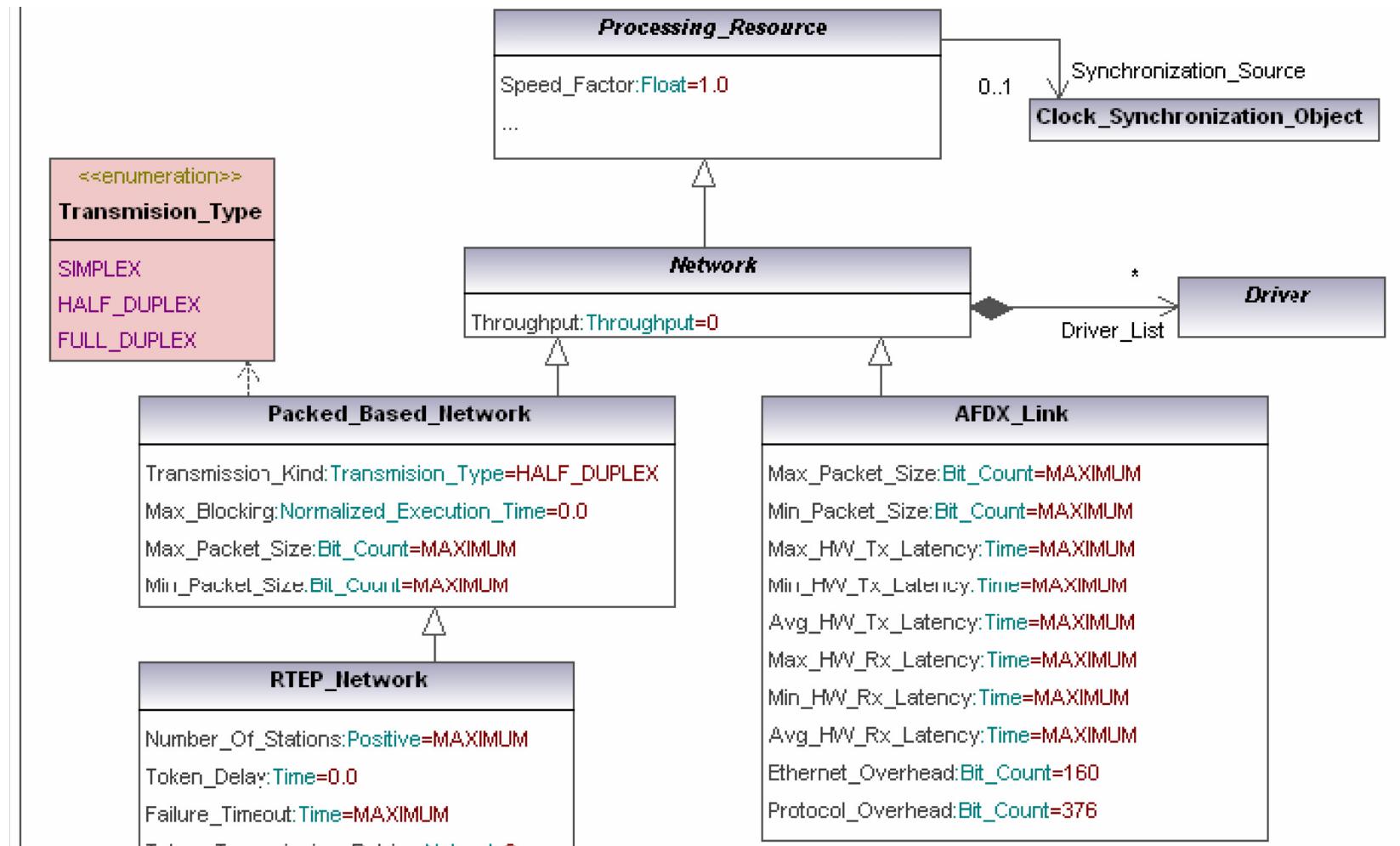


- **5 steps in the communication process**
- **2 contention points: queueing in the sending end system (L_{VL}) and queueing in the switch (L_{Sw})**

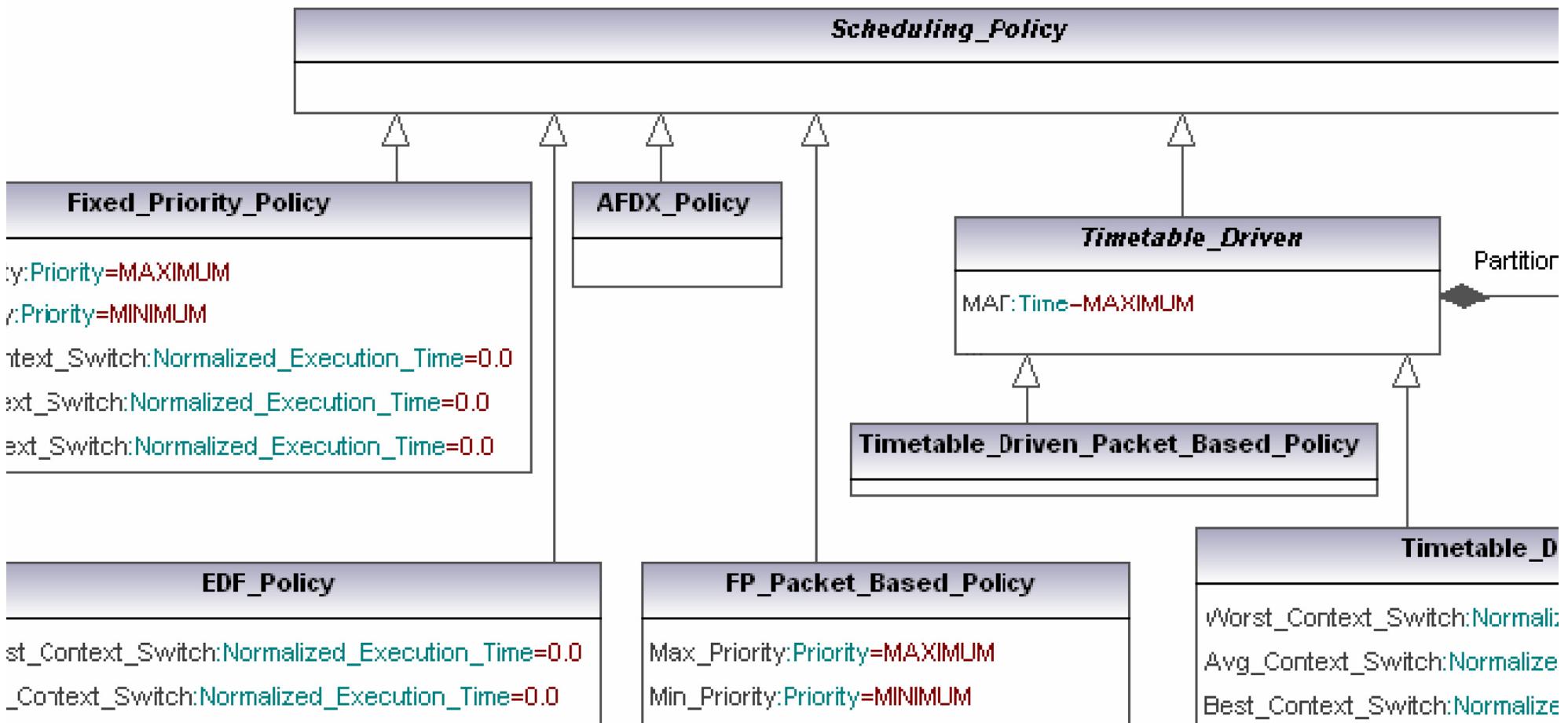
AFDX in MAST-2

- Processing Resources
 - Network: AFDX_Link
 - Network_Switch: AFDX_Switch
- Scheduling Policy
 - AFDX_Policy
- Scheduling Parameter
 - AFDX_Virtual_Link
- Schedulable Resource
 - Communication_Channel
- Event Handler
 - Message_Event_Handler: Message_Delivery, Message_Fork

AFDX in MAST-2: Network



AFDX in MAST-2: Scheduling Policy



AFDX in MAST-2: Scheduling Policy (cont'd)

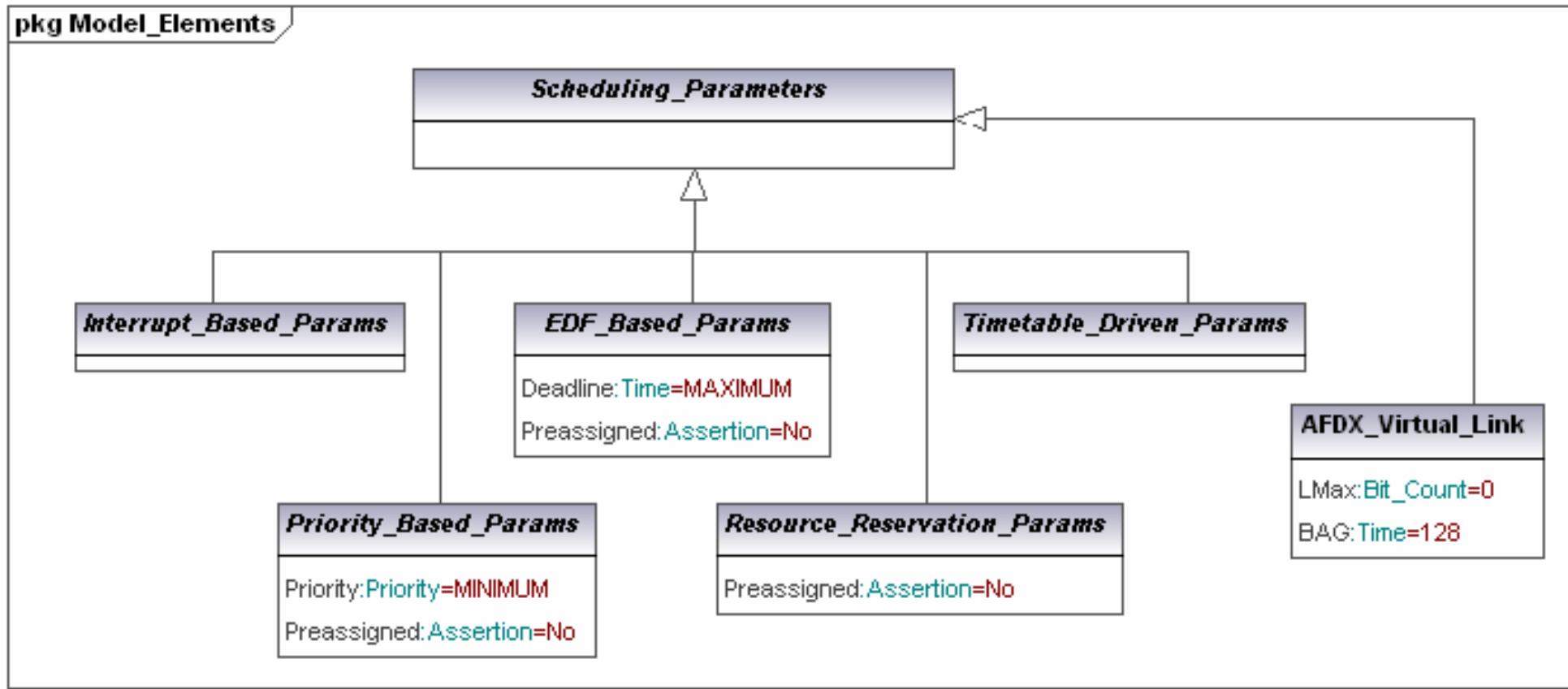


AFDX_Policy:

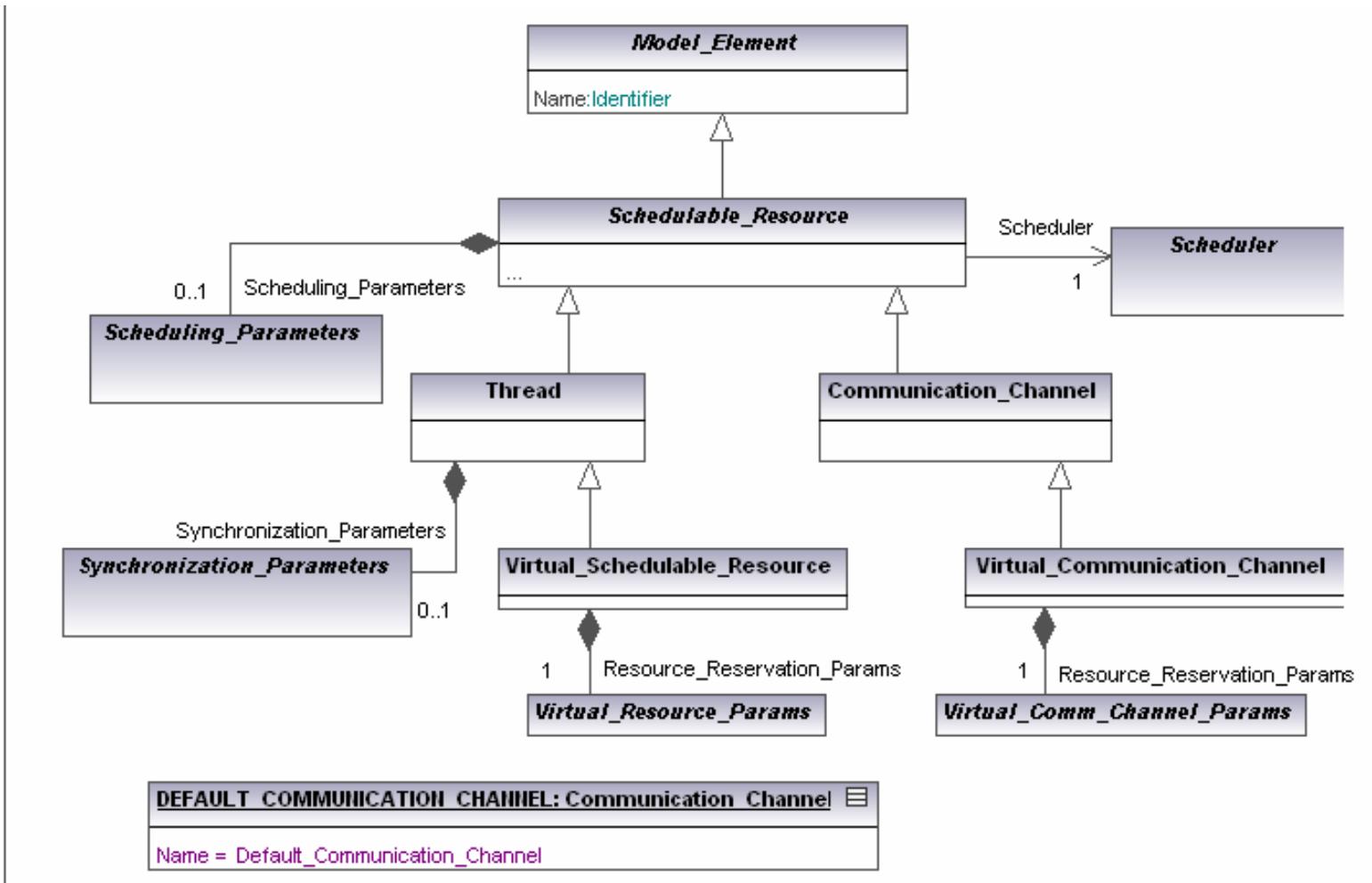
- messages are scheduled through virtual links
- messages are scheduled in FIFO order when they are originated at an AFDX switch

This policy may only be assigned to a scheduler that has an AFDX_Link as its host

AFDX in MAST-2: Scheduling Parameters



AFDX in MAST-2: Schedulable Resource



AFDX in MAST-2: Schedulable Resource (cont'd)

DEFAULT_COMMUNICATION_CHANNEL:

- used for communications through AFDX links when the message is originated at an AFDX switch
- the implicit scheduling policy is FIFO ordering for the messages

AFDX in MAST-2: Switch

It is capable of delivering messages arriving at an input port to one or more output ports

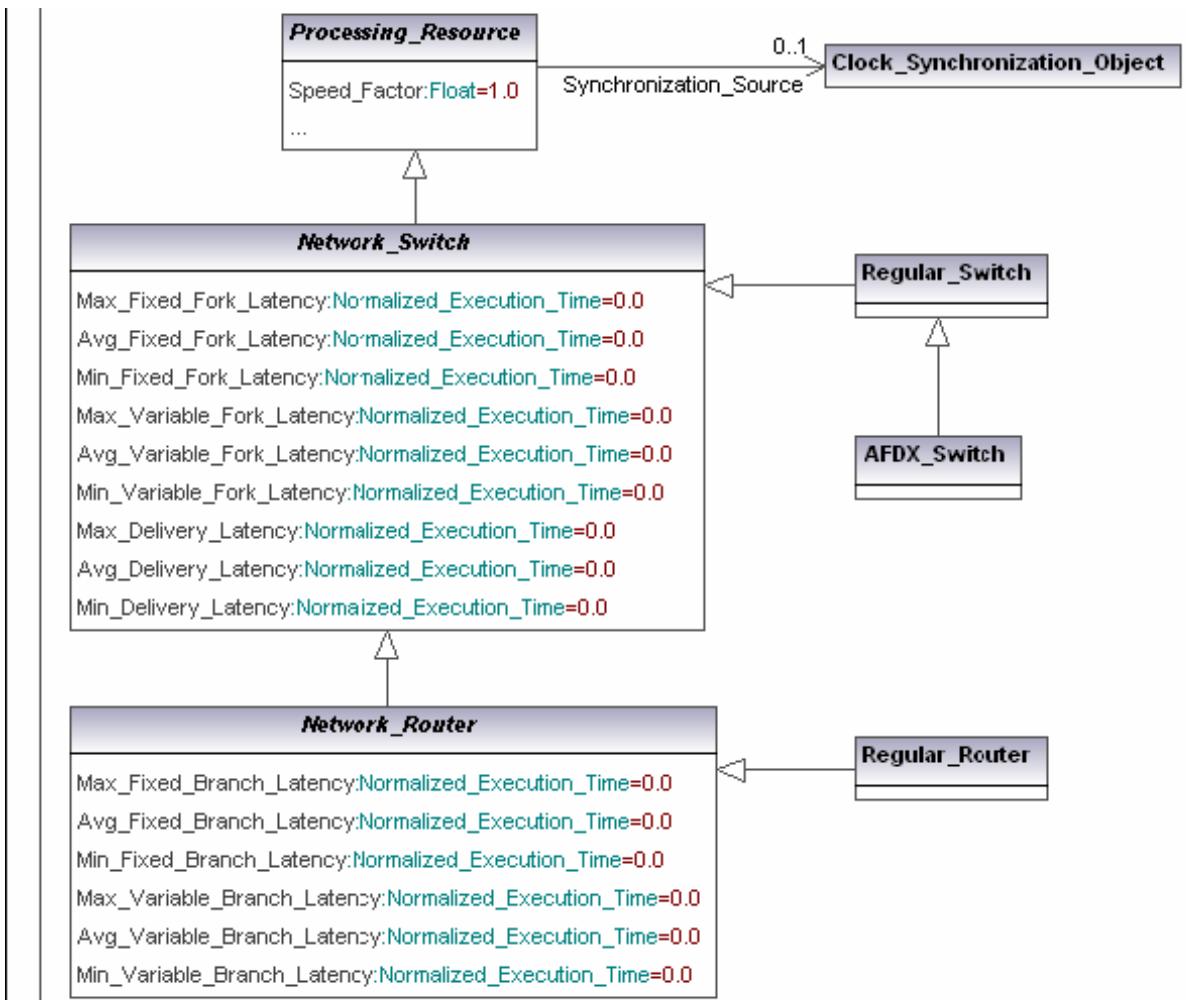
The delivery operations are specified through special-purpose *message event handlers*

MAST does not require to define the network topology (it is implicit in the end-to-end-flow)

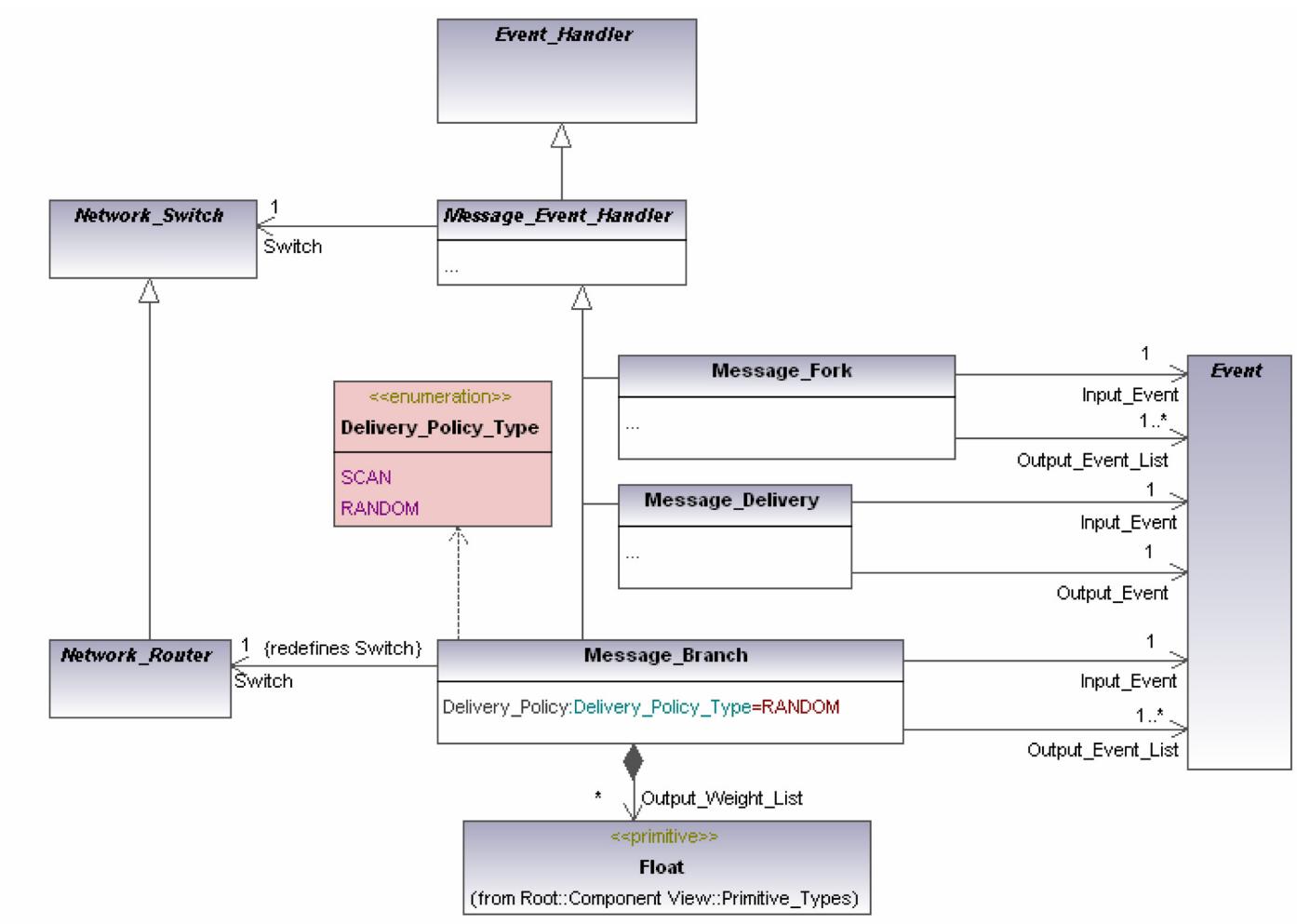
It is assumed a shared memory switch in which messages do not need to be copied

Contention occurs when several messages need to be sent to the same output port, in which case a queue is used at the output port

AFDX in MAST-2: Switch (cont'd)



AFDX in MAST-2: Message_Event_Handler



Example: sending a message through a switch

