MADES

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MADES

- EU FP7 STREP project – April 2010 for 30 months
- Model-driven Code Generation for Embedded Systems
  - UML + MARTE to Real-Time Java / C++

The University of York
A World Top 100 University

Politecnico di Milano

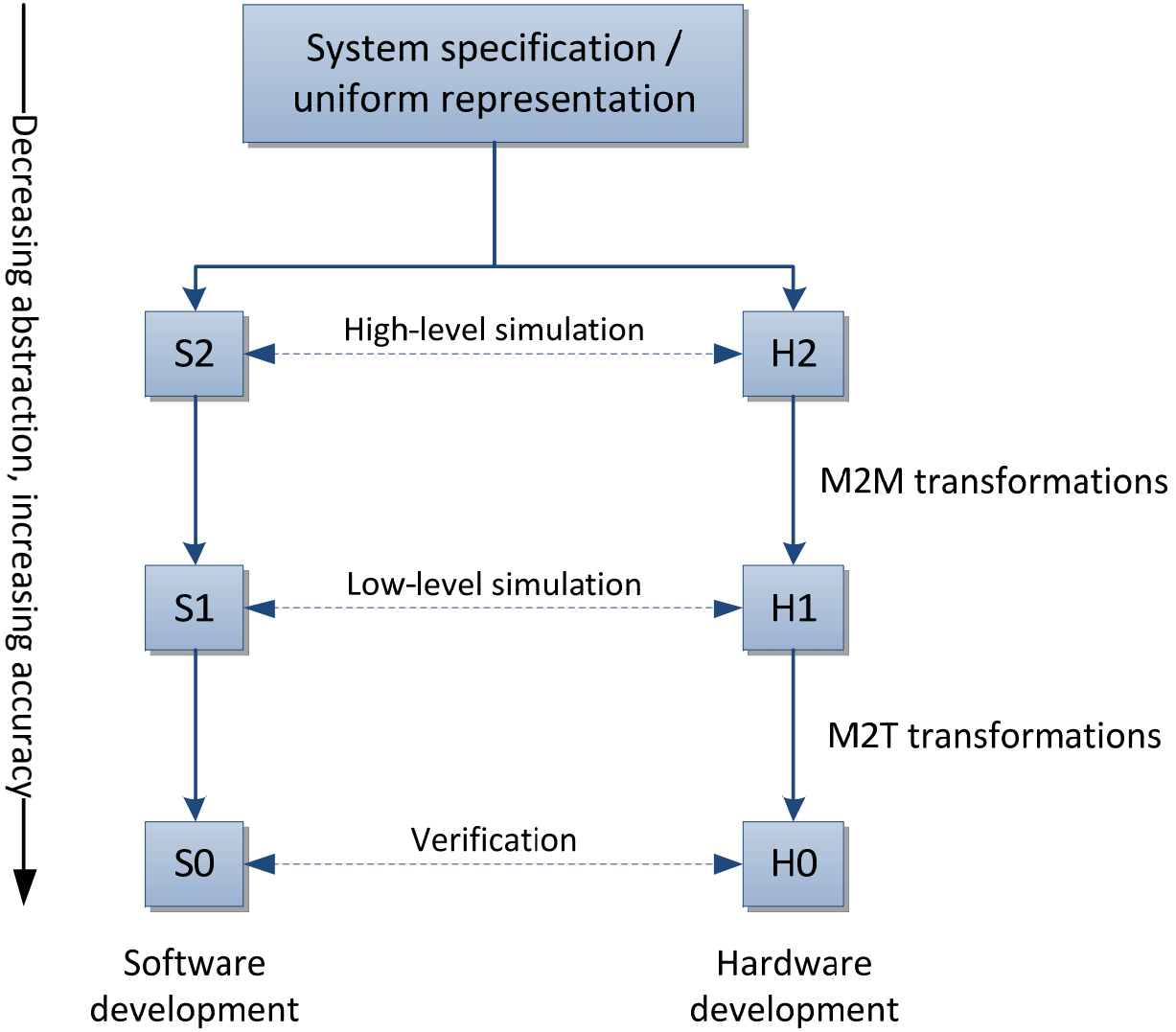
The Open Group

CASSIDIAN
An EADS Company

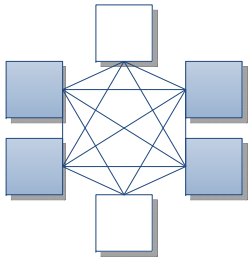
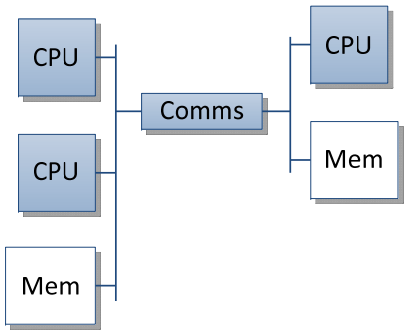
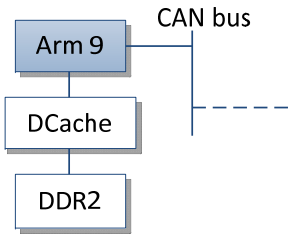
TXT e-solutions

SOFTEAM
Think Object

Modelling overview



Hardware models

Model	Modelling level	System C simulation level
H2	 Topology not modelled, totally-connected network assumed	Functional
H1	 Topology modelled, untimed, simple functional model reduces accuracy of simulation	Transaction-level modelling (TLM)
H0	 Complete hardware model, allows verification	Cycle-accurate

Model Verification and Code Generation