

SymTA/S - Roadmap

Future of standards and tools for schedulability analysis

ArtistDesign Workshop on Real-Time System Models for Schedulability Analysis

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Santander, February 7-8, 2011

Solutions for Complex
Real-Time Systems

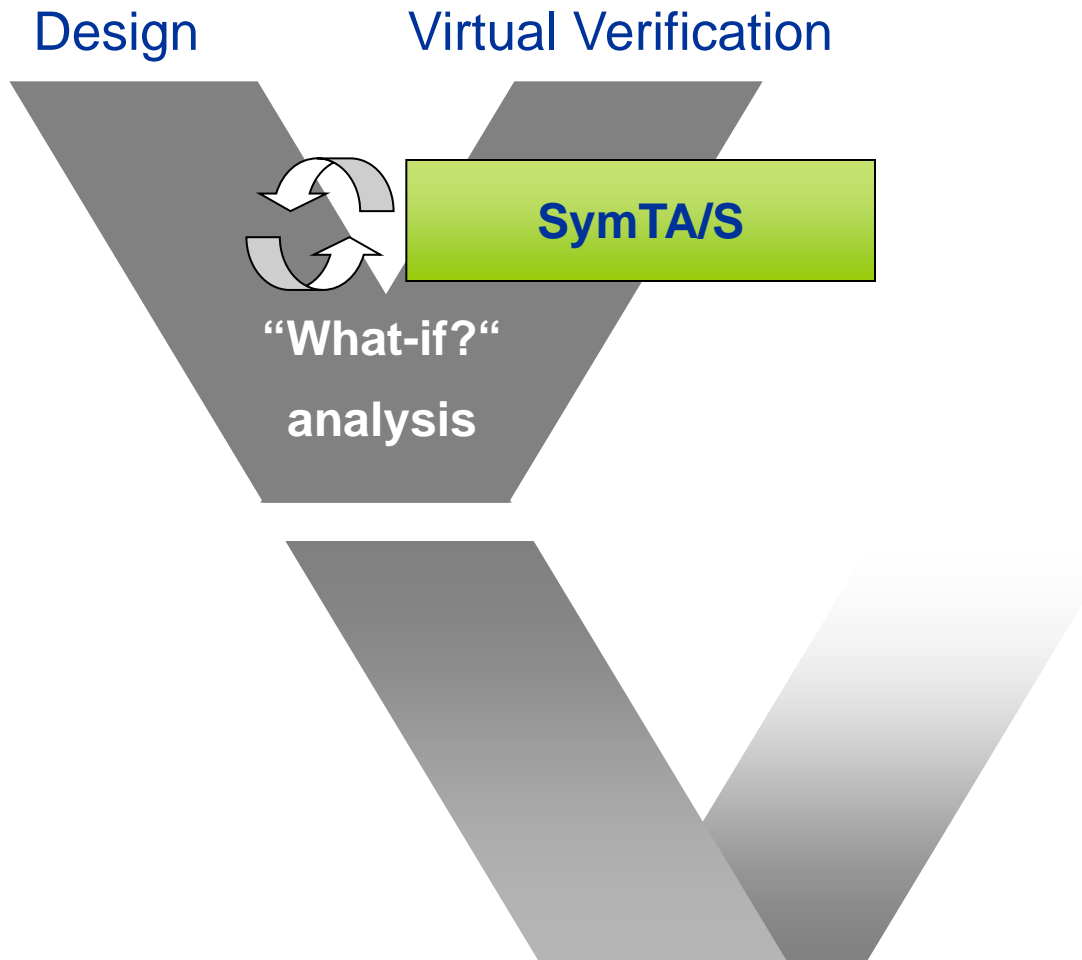


Future work

- ❑ Full integration of SymTA/S in design and development processes in automotive
 - ❑ Interfaces, tool chains, etc.

- ❑ Upcoming analysis topics:
 - ❑ Gateway analysis
 - ❑ Multi-Core
 - ❑ Aerospace
 - ❑ Ethernet

Early-Phase: Virtual Timing Verification



Network:

- ❑ network topology options
- ❑ bus configuration rules

ECU:

- ❑ initial task layout & software architecture
- ❑ execution time budgets / estimates
- ❑ virtual timing verification
- ❑ avoid late timing problems
- ❑ system optimization

Late-Stage: Integration Verification

Network:

- ❑ fixed topology
- ❑ detailed network configuration

ECU:

- ❑ detailed OS configuration
- ❑ measured execution times

- ❑ “real” timing verification
- ❑ system fine-tuning
- ❑ safety guarantees

Test & Integration Verification



SymTA/S

TraceAnalyzer

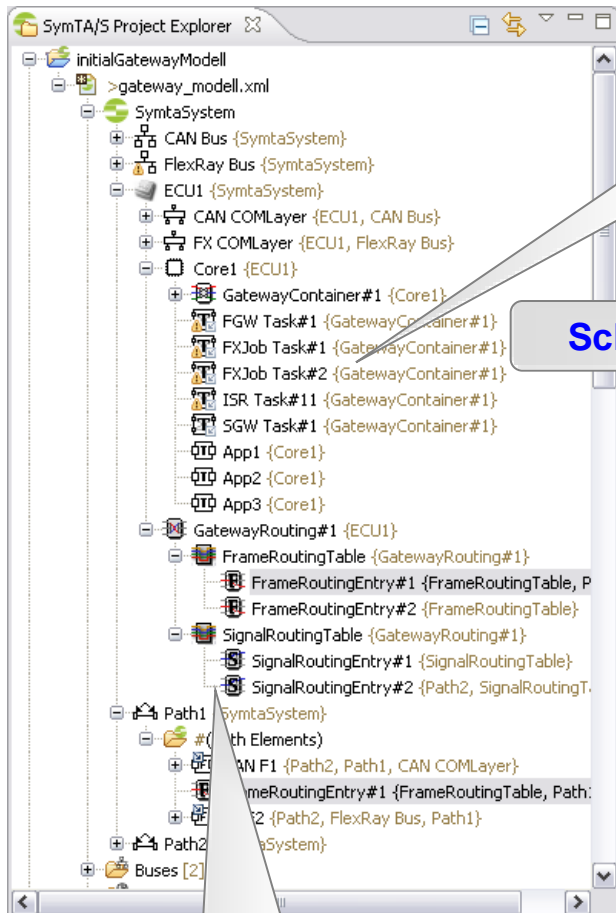
Gateway Analysis Library

- ❑ Modeling of gateway timing:
 - ❑ COM BSW components: CAN ISRs, FlexRay jobs, gateway tasks
 - ❑ configuration data: signal & frame routing tables
 - ❑ combination with application software tasks
 - ❑ scheduling analysis of BSW execution & routing delay

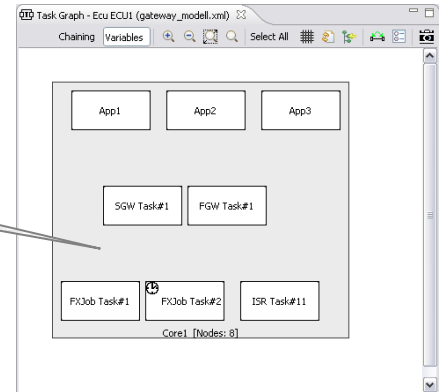
- ❑ Design support:
 - ❑ GW SW architecture optimization
 - ❑ GW delay minimization
 - ❑ avoidance of critical ASW disturbance

- ❑ interface: ARXML and SymTA/S XML

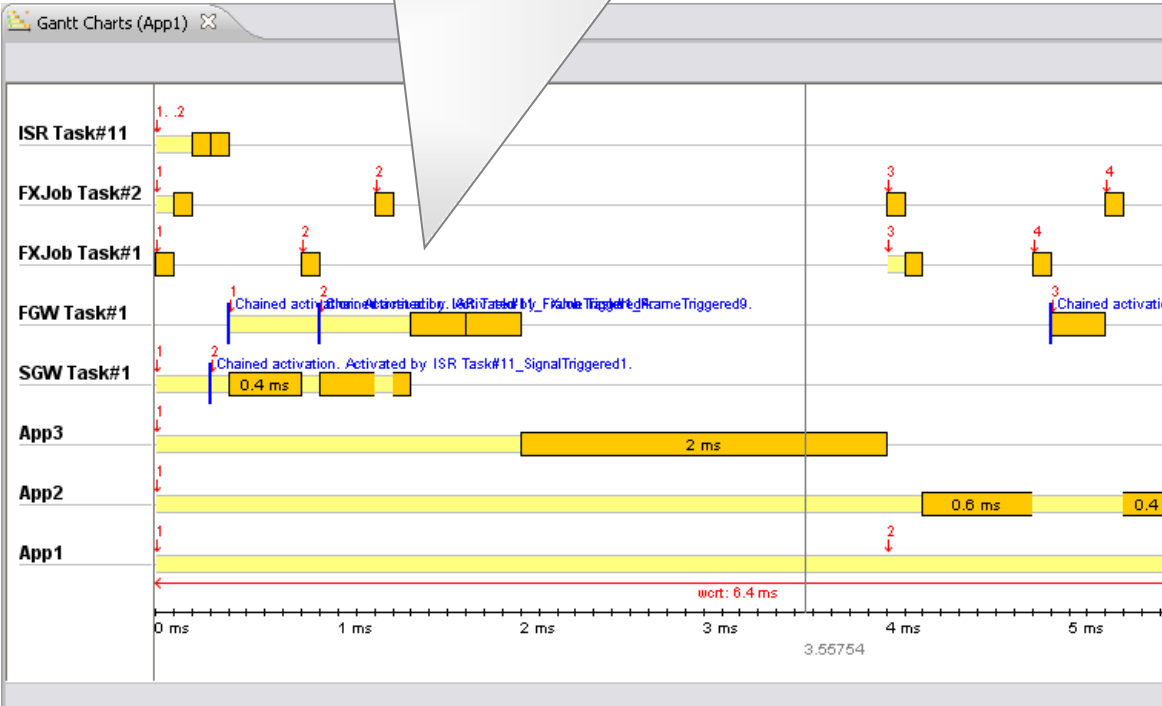
Gateway Analysis Prototype Preview



COM BSW Elements



Scheduling Analysis of COM BSW and user Tasks



Routing Tables for Signals and Frames

Multicore Feature Roadmap in SymTA/S

- ❑ waiting effects due to runnable chains across cores
- ❑ Communication cost analysis
 - ❑ different memory imply different data access time
 - ❑ work done at Symtavisision (together with Infineon, publication imminent)
 - ❑ prototype exists
- ❑ Consideration of timing implication of locking semaphore across cores
 - ❑ critical sections can contain also memory accesses
 - ❑ work performed at TUBS
 - ❑ current goal is to enable prototype in SymTA/S
- ❑ Automatic SW-mapping in multicore environment
 - ❑ Runnable remapping and task schedule synthesis

Symtavisision Aerospace Roadmap

- ❑ Status: Available prototypes for
 - ❑ ARINC 653 (IMA)
 - ❑ CAN
 - ❑ ARINC 664 (AFDX)
 - ❑ TTP

- ❑ Next:
 - ❑ Productization of ARINC 653 (IMA) and CAN for aerospace
 - ❑ Collaboration with lead customers

Thank You !

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