



IST-214373 ArtistDesign  
Network of Excellence  
on Design for Embedded Systems

Activity Progress Report for Year 4

## Platform and MPSoC Analysis

Cluster:

**Hardware Platforms and MPSoC**

Activity Leader:

**Prof. Jan Madsen (DTU)**  
<http://www.imm.dtu.dk>

*Policy Objective (abstract)*

The main objective of the activity is to build a common research environment, which integrates performance analysis algorithms and tools for hardware platforms and Multi-Processor System-on-Chip (MPSoC). The main challenge is the introduction of new aspects such as robustness, adaptivity and power consumption, which need to be addressed at run-time. The teams involved in the activity aim at developing and integrating modeling and analysis techniques for scalable performance analysis of applications executing on embedded hardware platforms.

## Versions

number	comment	date
1.0	First version delivered to the reviewers	January 15 <sup>th</sup> 2010

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# 1. Overview of the Activity

## 1.1 ArtistDesign participants and their role within the Activity

Activity leader: Prof. Jan Madsen – Technical University of Denmark, DTU (Denmark)  
*System-level modeling and analysis of MPSoC and networked embedded systems. Architectures and programming models for multi-core embedded systems. Analysis and Optimization of real-time and fault-tolerant applications implemented on distributed Platforms and MPSoC. Reconfigurable platforms and run-time resource management.*

Team leader: Prof. Petru Eles – Linköping University, LiU (Sweden)

(i) *Timing Analysis.*

(ii) *Analysis and Optimization of real-time and fault-tolerant applications implemented on distributed Platforms and MPSoC.*

(iii) *Analysis and Optimization of energy efficient, time constrained embedded systems.*

Team leader: Prof. Lothar Thiele – TIK, ETH Zürich, ETHZ (Switzerland)

*Developing a calculus to describe the performance of communication-centric systems, unifying the models for computation, combining tools for component-based performance analysis of MPSoC. Our role in this activity will be on component-based analytic methods to analyze the performance properties and memory requirements of distributed embedded systems.*

Team leader: Prof. Rolf Ernst – TU Braunschweig, TUBS (Germany)

*TU Braunschweig contributes formal performance analysis methods for MpSoCs, with a focus on the timing implications of inter-task synchronization.*

Team Leader: Prof. Maja D'Hondt – Interuniversity Microelectronics Centre, IMEC vzw. (Belgium) This team will introduce novel design-time and run-time resource management optimizations for MPSoC platforms.

Team leader: Prof. Luca Benini – University of Bologna, UNIBO (Italy)

(i) *Development of power modeling and estimation framework for systems-on-chip.*

(ii) *Development of optimal allocation and scheduling techniques for energy-efficient mapping of multi-task applications onto multi-processor systems-on-chips.*

(iii) *Development of energy-scavenging techniques for ultra-low power sensor network platforms.*

Professor, Prof. Axel Jantsch and Hannu Tenhunen, Royal Institute of Technology, KTH (Sweden)

*The contribution from KTH focuses on various design aspects, architectures, run-time reconfigurability and adaptivity.*

Team Leader : Dr. Raphaël David – CEA LIST (France)

(i) *Development of exploration framework for multi- and many-core architectures*

(ii) *Development of advance strategies for the deployment and the management of multi-task applications onto multi- and many-core devices*

(iii) *Design of multi-core architectures for dynamic multi-task applications*

Team Leader: Prof. Giovanni De Micheli – Swiss Institute of Technology, EPFL (Switzerland)

(i) *Development of process-induced skew variability for clock distribution networks in 3-D ICS*

(ii) *Development of analytic thermal models for vertically integrated systems*

(iii) *Design automation tools for MPSoC and NoC*

(iv) *Optimization techniques for thermal management of MPSoC and NoC*

**-- Changes wrt Y3 deliverable --**

*No changes with respect to year 3.*

## **1.2 Affiliated participants and their role within the Activity**

Dr. Daniel Karlsson, Volvo Technology Corporation

*Architecture and Design of Automotive Embedded Systems*

Dr. Kai Richter – Symtavision (Germany)

*Symtavision contributes industrial methodologies.*

Dr. Arne Hamann – Robert Bosch GmbH (Germany)

*Contributes on important embedded systems related research problems in the automotive industry.*

Prof. Dimitrios Soudris – Democritus Uni. of Thrace, DUTH (Greece)

*This team will introduce novel dynamic data type and data allocation optimizations for MPSoC platforms.*

Prof. David Atienza – Uni. Complutense de Madrid, UCM (Spain)

*This team will introduce novel run-time memory management optimizations for MPSoC platforms.*

Prof. Per Gunnar Kjeldsberg - Norges Teknisk-Naturvitenskapelige Uni., NTNU (Norway)

*This team will introduce novel task migration methodologies for MPSoC platforms utilizing hardware accelerators.*

Bjørn Sand Jensen – Bang & Olufsen ICEpower (Denmark)

*Areas of his team's expertise: chip design for audio signal processing*

CTO Rune Domsteen – Prevas (Denmark)

*Areas of his team's expertise: platform design for embedded systems*

Dr. Patrick Schaumont – Virginia Tech (USA)

*Design methods and architectures for secure embedded systems. Hardware/software codesign tool.*

**-- Changes wrt Y3 deliverable --**

*No changes with respect to Year 3.*

## **1.3 Starting Date, and Expected Ending Date**

**Starting date:** January 2008.

**Ending date:** Modeling and analysis is a long term effort and is expected to continue after the end of the project due to the lasting integration achieved by the NoE.

**-- Changes wrt Y3 deliverable --**

*No changes with respect to Year 3.*

## 1.4 Policy Objective

With growing maturity of scalable performance analysis algorithms and tools, new aspects such as the platform robustness can be included in analysis. Robustness to changes is particularly important for systems on chip since the cost of a redesign is high. At the same time robustness to faults is becoming a concern with shrinking feature sizes. In most practical cases, power consumption must be considered. There is currently no team in Europe that addresses all aspects. So integration of methods and tools will be needed to be able to (1) define meaningful robustness metrics that reflect design tradeoffs (2) assess the robustness of a design based on such metrics. This integration will extend the world leading position of Europe in the field of scalable formal performance analysis to hardware platform and MPSoC design.

**-- Changes wrt Y3 deliverable --**

*No changes with respect to Year 3.*

## 1.5 Background

The activity will be based on the complementary expertise of the participating partners in terms of Hardware Platform and MPSoC Analysis. In particular, the following areas are covered: Power modeling and analysis, power robustness assessment (University Bologna), platform performance modeling (University Braunschweig), analytical methods for reliability, performance and adaptability analysis of execution platforms (University of Denmark), reliability modeling, analysis and optimization (University Linköping), interfaces that communicate at run-time, aspects that are relevant for the efficiency of the run-time mapping components (IMEC, Belgium), simulation techniques and tools for NoC performance estimation and validation, interconnect and communication centric performance estimation techniques (KTH Sweden).

In addition, there have been already joint work and publications by some of the members of this activity, which will be used as a valuable starting point.

In more details, the above mentioned group has been working intensively on Power Modeling for SoC Platforms. In particular, they developed a virtual platform for power modeling of complex multi-core systems on chip. This platform can facilitate further integration among partners and associates, thanks to its flexibility and generality. In terms of "scheduling based energy optimization for energy-scavenging wireless sensor networks", a novel scheduling strategy (called lazy scheduling) that is well suited to energy-harvesting systems operating under real-time constraints has been developed by ETHZ and University Bologna. It is the first result of this kind in this quickly growing research area and received a lot of attention in the scientific community.

At ETHZ, an open tool set is available that allows the performance analysis of distributed embedded systems and MPSoC. It is based on the concept of Modular Performance Analysis (MPA). In addition, there are first results available that connect this system to the MPAARM simulation framework from University Bologna and the Symta/S analysis system from University Braunschweig/Symtavision.

**-- Changes wrt Y3 deliverable --**

*No changes with respect to Year 3.*

## **1.6 Technical Description: Joint Research**

The major focus of the activity on Platform Analysis is to establish a set of models and analysis methods that (a) scales to massively parallel and heterogeneous multiprocessor architectures, (b) is applicable to distributed embedded systems as well, (b) allows for the analysis of global predictability and efficiency system properties and (c) takes the available hardware resources and the corresponding sharing strategies into account. Promising approaches are based on composable frameworks and treating resources as first class citizens in the analysis. Both, simulation-based and analytic methods will be combined. In addition, methods that focus on worst-case/best-case results as well as those based on stochastic models will be combined.

As a central ingredient of any analysis model, synchronization & communication abstractions are required for successfully deploying MPSoC hardware in embedded application domains. Efficiency is inherently related to both power and performance; hence it is an energy metric. In embedded systems, abstractions are acceptable only if they do not compromise efficiency. It also extremely important to take into account variabilities of both hardware fabrics and application workloads, which are deemed to rapidly increase. In particular, the above abstractions need to be embedded into a framework that allows to analyze the performance properties and memory requirements of distributed systems. In particular, we will focus on methods that satisfy composability properties and to lift the component-based methods as known from software design to interfaces that talk about resource interaction. In addition, we are interested in adding run-time adaptivity to systems while using efficient run-time estimation methods combined with distributed finite horizon control methods. Again, the focus is on predictability AND efficiency. Here, we will use the expertise that is available at ETH Zurich (Lothar Thiele) and University Bologna (Luca Benini), Hannu Tenhunen (KTH), Stylianos Mamagkakis (IMEC), Jan Madsen (DTU), TU Braunschweig (Rolf Ernst) are involved in this activity.

Another major challenge is to provide analysis tools and techniques to support the transitions between different abstraction levels in the design flow. Constraints should be communicated at design-time from one step to the next, taking into account the global effect that they will introduce in the system. Also, in order to ensure adaptivity of the system an interface should communicate at run-time the changes in the resource requests and the changes in the actual resource availability.

**-- Changes wrt Y3 deliverable --**

*No changes with respect to Year 3.*

## 2. Work Achieved in the NoE

### 2.1 *Synthesis View of the Main Overall Achievements*

During the four years of ArtistDesign significant results have been achieved within the activity of analysis. This covers both research result achieved in collaboration among the partners and in a large number of events where the results have been disseminated.

A major activity has been on performance analysis methods. Over the last years, the intense activity on developing performance analysis methods for multi- and many-core systems led to valuable solutions that have been published in different international journals and conference proceedings. Collaborations and discussions with members of the Timing Analysis Cluster helped to address challenges in the analysis of multi-core systems with shared resources. Some of the developed analysis methods were prototypically implemented (in the tool SymTA/S) and used in collaboration with industrial partners for the analysis of realistic use cases (e.g. in the automotive domain). This has increased the acceptance of formal analysis methods and triggered the integration of the research solutions in the commercially available version of the tool SymTA/S. Another aspect of performance analysis has been that of analysing energy and temperature in multi-core systems. This is a particular important topic when dealing with the new 3-D chip topologies and how to map applications onto these as well as how to design the communication infrastructure. For the communication infrastructure analysis has developed from bus-based over Ethernet-based to fully 3-D Network-on-Chip topologies. Several of the analysis tools have been interfaced, allowing the analysis to be based on mixed models as well as a mix of analytical and simulated methods. In particular the tools SymTA/S and MPA have been coupled. Relying on different analysis techniques each of the two tools can be individually used to evaluate the performance of embedded real-time systems. The interface developed for tool coupling now allows combining the strengths of the two tools. Evaluations have been jointly performed and the work resulted in joint publications.

A particular feature of performance analysis, which has been studied, is that of reliability. This had lead to an emphasis on analyzing fault tolerant embedded systems, covering both single systems and distributed systems. In particular, fault tolerance has been studied related to automotive systems. The work covers approaches to handle both processor and communication faults in distributed real-time systems based on CAN or FlexRay communication. Several timing analysis and cost optimisation methods have been proposed. The work resulted in highly referenced publications, a DATE best paper award, and invited talks at major conferences. Another related aspect has been analysis for runtime resource management and its implementation as software runtime management. Besides dealing with aspects of fault tolerance, this has resulted in several analysis techniques to be used for dynamic load balancing for energy and temperature, as well as for memory usage, and ultimately for making systems adaptive and self-organizing.

During ArtistDesign, the analysis activity has created:

- 5 modeling and analysis tools.
- 42 joint publications and 119 individual publications.

The collaborations leading to these results have been partly funded by:

- 10 national projects, 5 EU FP7 projects and 1 Advanced ERC grant.
- 6 Artemis JU projects on embedded systems.

The partners will continue their collaborations after ArtistDesign through these and new joint projects.



-- The above is new material, not present in the Y3 deliverable --

## 2.2 Work achieved in Year 1 (Jan-Dec 2008)

A number of problems were tackled in Year 1, through several cooperations involving two or more partners. In the following paragraphs, we briefly summarize the problems tackled and the partners involved.

The Linköping group has addressed two major issues: *Timing analysis of distributed real-time systems*. In this context, the emphasis was on heterogeneous systems using various task scheduling policies and heterogeneous communication protocols with static and dynamic phases. Both formal and simulation based approaches were developed. *Analysis of fault tolerant real time systems considering various reliability requirements and fault tolerance mechanisms has been done*. In particular, the issue of transient faults has been considered. The basic effort was toward development of adequate scheduling algorithms. This work has been performed in cooperation with the DTU group.

As a central ingredient of any analysis model, synchronization & communication abstractions are required for successfully deploying MPSoC hardware in embedded application domains. Efficiency is inherently related to both power and performance; hence it is an energy metric. In embedded systems, abstractions are acceptable only if they do not compromise efficiency. It is also extremely important to take into account variability of both hardware fabrics and application workloads, which are deemed to rapidly increase. In particular, the above abstractions need to be embedded into a framework that allows to analyze the performance properties and memory requirements of distributed systems. In particular, ETHZ had its focus on methods that satisfy composability properties and to lift the component-based methods as known from software design to interfaces that talk about resource interaction. In the past year, ETHZ followed the following research directions: Together with University Bologna, ETHZ worked on combining the MPARM simulation framework with the performance analysis framework MPA (modular performance analysis). In particular, we attempted to set up the simulation environment in a way, that it follows the semantics of the analytic models and a comparison is possible. Together with University Braunschweig, ETHZ worked on the combination of the Symta/S symbolic analysis tool with the MPA (modular performance analysis framework). In particular, a tool coupling has been established that allows a seamless integration of both analysis methodologies. In addition, both research groups worked on a proper modeling of hierarchical event stream concepts.

To provide a formal performance analysis that captures the timing implications of multiprocessor systems on chip, the applicability of concepts from the analysis distributed systems is limited. A major difference lies in the use of common resources, either physically, such as a shared coprocessor or memory, or logically, such as a semaphore or a shared data structure in the memory. In ARTIST2 already first steps were taken towards addressing implications of a shared memory, which need to be extended in order to achieve the goals of this activity. We have taken steps towards generalization of the concepts from shared memory modeling to cover arbitrary shared resources. The approach chosen promises a higher accuracy than traditional approaches, due to more sophisticated modeling of shared resource load, and a better composability of designs, as the analysis of the shared resource delay is decoupled from the response time analysis of the requesting tasks.

The main problem tackled by IMEC and its affiliated partners (ie, DUTH, NTNU and UCM) was the definition of a specific software metadata format, which can be linked to each embedded software application or downloadable software service. This software metadata information can



be used to configure and self-adapt the run time resource management software for dynamic data transfer and storage on MPSoC platforms. Additionally, IMEC has developed profiling and analysis tools that extract and post-process these software metadata, in order to be used for both memory hierarchy assignment (ie, MH tool) and source code parallelization tools (ie, MPA tool).

University of Bologna has addressed, in cooperation with DTU, the issue of prolonging the system life-time. Even though systems that harvest energy from the environment are adopted, such an environmental energy is not distributed uniformly and there is a lot of parameters that influence the efficiency and the schedulability of tasks. In particular we tackled the problem of routing messages in a sensor network with energy awareness and real-time responsiveness together with scheduling policies, which guarantee to execute tasks under unpredictable profile of the harvested energy.

**-- No changes wrt Y3 deliverable --**

*This section was already presented in the Y3 deliverable, in section 1.7.*

### **2.3 Work achieved in Year 2** (Jan-Dec 2009)

Many of the problems tackled in Year 2 are continuations of the problems and cooperations initiated in Year 1.

Linköping and DTU have continued their work regarding analysis and optimization of distributed embedded real-time systems, with application in automotive electronics. The issue of average response time (as a complement to the previous work, regarding worst case response times) of FlexRay-based distributed systems has been addressed.

At Linköping, in cooperation with Lund, analysis and optimisation techniques for control-scheduling co-design have been developed. It integrates a controller design with both static and priority-based scheduling of the tasks and messages, and in which the overall control performance is optimized. The technique has also been extended to cover the case of multimode control systems.

As a main result during the second year, the groups at Linköping and DTU have developed an analysis approach that determines the system failure probability, based on the number of re-executions introduced in software and the process failure probability of the computation node with a given hardening level. Based on this analysis, an optimisation technique has been proposed in which hardware and software fault tolerance techniques are combined.

TU Braunschweig and GM Labs have collaborated in the COMBEST project on the definition of methods and tools for the timing analysis of automotive systems based on a mix of complex communication protocols/software scheduling techniques. Within this area, ETHERNET (and its different implementations, e.g., AFDX and TT-ETHERNET) was of special interest, because increasing bandwidth, low latency/jitter, and time determinism requirements make an Ethernet based solution for in-vehicle networking attractive. In this scope, the partners examined the application of methods and tools to possible future use cases from the automotive domain. To examine the accuracy of the conservative performance bounds obtained by the formal worst case analysis, a comparison between results of formal analysis and results obtained by simulation was performed. A joint publication containing the results of the comparison has been submitted for publication.

UNIBO and Linköping have tested Basic Scheduling Alternative (BSA) in a Multi-Processor System-on-Chip shared bus. A RTL-level cycle accurate TDMA bus arbiter model has been developed and plugged in MPARM simulator. Many exhaustive sets of experiments have been done in order to validate the BSA framework and during each step of the exploration, a hardware synthesis has been performed to keep under control the underlying logic complexity.

DTU has continued the work on analytical performance models. In particular, the formalisation of the ARTS model has been extended to capture more aspects of both the application and the platform. Another important issue to be addressed is the scalability of the model such that larger and more complex systems can be modelled.

During the annual Meeting of the ArtistDesign Cluster on Hardware Platforms and MpSoC in Braunschweig, the partners of this activity have identified common goals and similarities in their approaches to address shared resources in multiprocessor systems. Shared resources generally complicate the timing verification, because they introduce timing inter-dependencies between the tasks on different cores. To address this challenge, Linköping University, ETH Zürich, TU Braunschweig are working on formal approaches to increase the predictability of such systems: Linköping University's focus is finding static bus schedules that minimize the overhead from a worst-case perspective. At the ETH Zürich, work is being done on finding the worst-case timing interference within assigned time-slots. The TU Braunschweig is working on an approach that allows to bound the interference in the absence of static schedules.

In the collaboration between ETHZ and University of Bologna, further investigation of energy harvesting systems was performed. In particular, this concerned both hardware and software aspects of sensor nodes which are powered solar energy. The main goal was to merge the different approaches and illuminate several application scenarios that are of practical relevance.

Concerning the integration of SymTA/S and MPA as well as unifying approaches for hierarchical scheduling, hierarchical event streams have been in the focus of research in the second year. The major issue here is to also allow an extraction of single event streams from previously merged and transformed event streams. The transformation is hereby due to the fact that incoming streams can be combined via OR-operation and may pass different system components, which may buffer these streams due to scheduling policies.

CEA LIST has been involved in a new cooperation with university of Bologna for the definition of a Software Runtime Architecture for the management of many-cores components. CEA LIST has proposed with University of Bologna a framework supporting the development of various services, ranging from dynamic application deployment, task scheduling, resources allocation to fault and power management.

IMEC focused its research closer to the hardware platform and more specifically regarding variability and reliability issues arising from the usage of sub 45nm technology nodes. To this end Variability Aware Modeling focused on analysis of SRAM designs and the Knobs and Monitors framework extensions focused on RTL2RTL transformations for latency monitors.

Finally, KTH and DTU have started an collaboration within the SYSMODEL project on the development of a multi-MoC modeling framework for heterogeneous systems integrated with performance analysis and design space exploration tools.

**-- No changes wrt Y3 deliverable --**

*This section was already presented in the Y3 deliverable, in sections 1.8 and 3.1.*

## 2.4 Work achieved in Year 3 (Jan-Dec 2010)

**University of Bologna (UNIBO)** tackled the scheduling problem on multicore systems. An effective multicore computing is not only a technology issue, as we need to be able to make efficient usage of the large amount of computational resources that can be integrated on a chip. This has a cross-cutting impact on architecture design, resource allocation strategies, programming models. The objective of our work is the development of a predictable and efficient non-preemptive scheduling of multi-task applications with inter-task dependencies.

Moreover **UNIBO** addressed the thermal and reliability management for multicore platforms together with **Intel Labs**. (Braunschweig). The goal is to mitigate the onchip temperature hotspots, which can cause non-uniform ageing, by online tuning of system performance and adopting closed-loop controls.

**ETHZ** has been investigating various component-based approaches to the analysis of MPSoC. In particular, new interface-based approaches have been proposed that allow for an end-to-end analysis based on a novel interface algebra. The work is described in [SCT10].

**ETHZ** and **UNIBO** have been pushing forward the adaptive strategies for power management in case of environmentally powered systems. This joint work has been published in [MTBB10].

Furthermore, **ETHZ** has been investigating various methods to analyse the performance of multiprocessor systems under power and temperature constraints, e.g. involving leakage power. Finally, the component-based approach has been extended towards combining various models of computation, i.e. state-based component descriptions and analytic functional models, see [LPT10]. There has been substantial progress in understanding the influence of memory buses on the performance of multicore systems, see [SPCTC10].

The collaboration between **TU Braunschweig** and GM Labs in the COMBEST project started in 2009 was focused on the application of methods and tools developed in COMBEST on possible future test use cases from the automotive domain. The results of this collaboration have been published at SAE 2010 [RE10]. As a follow up to the successful collaboration in 2009, in 2010, two separate R&D projects between iTUBS and GM Labs have been initiated to further exploit the COMBEST research results. The focus of these projects was on the development of methods and tools for the analysis (i) of Ethernet based architectures and (ii) of multi-core platforms. Both projects, which are currently still ongoing, have a strong focus on applying formal scheduling theory to realistic foreseeable automotive architectures. In particular, the collaboration with GM Labs shows that the techniques developed in COMBEST (e.g. formal performance analysis of Ethernet based communication networks) help to obtain formal analysis results for realistic use cases of GM and give much tighter analysis results than the formal techniques previously available. This generally increases the user acceptance of formal analysis methods and it also increases the user value of the tool SymTA/S.

**TU Braunschweig** has continued the work on the performance analysis for multiprocessor systems with shared resources. Timing implications of using shared resources in multi-core systems have been investigated for different setups and, key components of a safe inter-task and inter-core synchronization algorithm for shared resources have been identified. Also, in a joint meeting **TU Braunschweig** and **ETHZ** have discussed open issues and identified possible improvements on the modelling and analysis approaches of multi-core systems with shared resources. Results have been presented jointly by **TU Braunschweig** and **ETHZ** at the annual ArtistDesign Cluster Meeting in Leuven. During this meeting, further ideas regarding approaches addressing shared resources in multiprocessor systems have been exchanged with partners of this activity, e.g. **Linköping University**.

Concerning contract based architecture dimensioning, **KTH** has formulated flow based traffic shaping optimization problem for minimizing buffers in the communication network, while meeting the throughput and delay requirements for each flow. In a case study we observed

62.8% reduction of total buffers, 84.3% reduction of total latency, and 94.4% reduction on the sum of variances of buffers. Likewise, the experimental results demonstrate similar improvements in the case of synthetic traffic patterns. The optimization algorithm has low runtime complexity, enabling quick exploration of large design spaces. From those experiment it can be concluded that flow regulation can be a valuable instrument for buffer optimization in NoC designs.

The memory organization and the management of the memory space is a critical part of every NoC based system. **KTH** has developed a Data Management Engine (DME), that is a block of programmable hardware and part of every processing element. It off-loads the processing element (CPU, DSP, etc.) by managing the memory space, memory access and the communication over the on-chip network. The DME's main functions are virtual address translation, private and shared memory management, cache coherence protocol, support for memory consistency models, synchronization and protection mechanisms for shared memory communication. The DME is fully programmable and configurable thus allowing for customized support for high level data management functions such as dynamic memory allocation and abstract data types.

A system modelling framework for modelling, analysis and refinement of heterogeneous MPSoCs is being developed by **KTH** in cooperation with **DTU** and Tampere University. The framework rests on the formal basis of ForSyDe and is extended for modelling of both the functionality and platform architecture. Also, a SystemC implementation has been defined and is under development. To allow the modeling of abstract heterogeneous system models we have specified the System Functionality Framework (SFF), which defines the modeling of functionality at a high-level of abstraction. The SFF comprises several models of computation, which are formally defined using the ForSyDe framework. SystemC has been selected as the main modeling language for the SFF. The Platform Architecture Framework (PAF) is a library of platform components modeled at different levels of abstraction. PAF includes processor cores, memory models, interconnection structures, and instruction set simulators and other components. The system level models serve as behavioral references (or executable specifications) for the lower level components. Therefore, the system level models alleviate the design validation and design space exploration.

The **CEA LIST** and **UNIBO** focused during year 2010 on the exploration and the development of dynamic management strategies for the deployment and the execution of multi-tasks application on many-cores architectures. Special attention has been paid on load-balancing and power management. Also, smart deployment of application, taking care of potential hardware defaults in the device, has been explored.

Temperature aware system level design methods rely on the availability of temperature modeling and analysis tools. The **Linköping** group has developed new, fast, and accurate temperature analysis techniques that are sufficiently fast to be and used inside a temperature aware system level optimization loop.

**Linköping** and **Lund** has worked together on QoS optimization of real-time control applications. Time-triggered periodic control implementations are over provisioned for many execution scenarios in which the states of the controlled plants are close to equilibrium. To address this inefficient use of computation resources, researchers have proposed self-triggered control approaches in which the control task computes its execution deadline at runtime based on the state and dynamical properties of the controlled plant. The potential advantages of this control approach cannot, however, be achieved without adequate online resource-management policies. The groups at Linköping and Lund have addressed the issue of performance modelling and resource scheduling for multiple self-triggered control tasks that execute on a uniprocessor platform.

**DTU** has continued the work on analytical performance models. In particular, the formalisation of the ARTS model has been extended to capture more aspects of both the application and the platform. Another important issue to be addressed is the scalability of the model such that larger and more complex systems can be modelled.

An important part of the work implemented by **EPFL** is concerned with the synthesis of application specific Network-on-Chip (NoC) topologies for 3D integrated systems [SMBM10]. The work presents a complete algorithm with two underlining approaches that is capable to explore the tradeoffs between topology performance (power consumption, network delay) and the number of required vertical links that use Through Silicon Vias (TSVs). The synthesis algorithm is extended with a custom floorplanning routine that preserves the relative positions of the core blocks. The work also presents a comparison between application specific NoC for 2D and 3D Integrated circuits (ICs) and presents the benefits of the topologies for the 3D ICs.

A further study makes a comparison between NoC topologies for 2D and 3D IC in the presence of Voltage and Frequency Islands (VFI) [SMBM10b]. The study shows the advantages of 3D topologies for different VFI assignments of the System-on-Chip (SoC) cores. The work also shows the need for synthesis tools for the exploration and design of custom topologies for 3D ICs.

Deadlock freedom is a necessity for NoC. Traditional deadlock avoidance techniques that restrict the synthesis tools can lead to the impossibility of the synthesis algorithm to find paths in the presence of additional constraints (e.g. restricted number of vertical links that require TSVs) [SMBM10c]. We presented an algorithm to remove possible deadlocks after synthesis. The algorithm can be applied to any topology and removes the deadlocks by minimally adding parallel physical links or virtual channels. This work was done in cooperation with **UNIBO**. The goal of the collaboration is to provide tools for application specific NoCs for realistic systems that use VFIs (since most SoCs do today) and for 3D IC (which is a promising technology for future SoCs).

Thermal management management policies for MPSoCs have also been another focus within **EPFL**. This project was a partly joint effort with **ETHZ**. Three-Dimensional integrated circuits and systems are expected to be present in electronic products in the short term. Specifically 3-D multi-processor systems-on-chip (MPSoCs), realized by stacking silicon CMOS chips and interconnecting them by means of through silicon vias has been considered. Because of the high volumetric density of devices and interconnect, thermal issues pose critical challenges, such as hot-spot avoidance and thermal gradient reduction. Thermal management is achieved by a combination of active control of on-chip switching rates as well as active interlayer cooling with pressurized fluids.

**-- No changes wrt Y3 deliverable --**

*This section was already presented in the Y3 deliverable, in sections 1.9 and 3.1.*

## **2.5 Work achieved in Year 4** (Jan-Dec 2011)

**Linköping** has continued the work on temperature modelling and extended the earlier elaborated temperature models to multicore systems. The particular focus was on dynamic steady state thermal analysis and its potential application to reliability optimisation of multicore embedded systems.

**Linköping** has also continued the cooperation with **DTU** on fault tolerant distributed systems. The focus has been fault modelling of the communication infrastructure aiming at the synthesis of fault tolerant communication over FlexRay buses for automotive applications. In conjunction



with **Lund**, the work on control quality optimisation has continued. The particular focus, this year, has been on modelling and optimisation of the FlexRay-based communication platform.

The follow up R&D projects which started in 2010 between **ITUBS** and GM for further exploitation of the COMBEST results have been finished in 2011 to the complete satisfaction of both partners. The focus of these projects was on the development of methods and tools for the analysis (i) of Ethernet based architectures and (ii) of multi-core platforms. Some of the results were submitted to DATE 2012 [RGE12] and have been accepted for publication.

New R&D projects between **ITUBS** and Daimler AG have been initialized to investigate the applicability and the performance (i.e. how useful are the obtainable results) of compositional system level timing analysis when applied to current and future automotive E/E architectures. In this context, two problems of the existing formal approach have been identified. First, for the dynamic segment of FlexRay as it is used in some of the investigated automotive use cases, no suitable analysis exists, making systems containing such components not analyzable. Second, when the compositional analysis was applicable, the obtained system level results, i.e. end-to-end latencies, often overestimated the timing behavior of the real system by such a large amount that the results were deemed unusable by Daimler. Therefore, we developed a new response time analysis for the dynamic segment of FlexRay covering the most recent FlexRay specification and an improved end-to-end latency analysis technique. The results of this cooperation are currently under submission.

During the fourth year **TU Braunschweig** has continued the work on performance analysis methods for multiprocessor systems with shared resources. The focus was on extending existing analysis solutions to consider more complex multiprocessor applications. The applicability of the proposed methods to realistic foreseeable industrial (e.g. automotive) applications has been investigated. Furthermore, new analysis methods have been developed and are currently submitted for publication.

**TU Braunschweig** has also investigated the timing behaviour of multi-mode applications, i.e. applications that can switch between different operational modes at runtime. Real-time applications that can change their functionality over time and execute in different operational modes can be found in several applications domains from safety-critical avionic and automotive control systems to multimedia smart devices. In case of applications distributed over multiple processors, the initiation of a mode change has not only a local effect on only one processor, but also impacts the timing of tasks executing on other processors. In order to provide real-time guarantees for multiprocessor systems that accommodate multi-mode applications, the systems' timing behaviour has to be verified in each individual mode and during every transition between two modes. In addition the duration of the transition phases between different modes has to be computed in order to avoid the violation of the timing constraints at runtime. An analysis method for deriving transition latencies in multi-mode systems was published in [NNSSE11].

**CEA LIST** work in 2011 consisted mainly in taking the work done with the collaboration with **UNIBO** in 2010 to the next level by proposing a portable runtime software for the dynamic deployment and the execution of multi-task applications on many-cores architectures. This software was tested on a complete application in the context of the COBRA CATRENE project as well as on multiple instances of platform P2012. Also, **CEA LIST** has started benchmarking different multicore architectures, aiming to provide a knowledge database as well as formal methods to help choosing the right architecture for a given application.

During 2011 **KTH** and **DTU** have continued to develop the SystemC based modeling framework. Progress has been made in a systematic step-wise refinement by replacement methodology and by a general co-simulation technique. Both results are based on formal properties of the framework but are very pragmatic in allowing for reuse of existing IPs and



models to cater for industrial needs. Industrial partners from the SYSMODEL project have contributing to this development with requirements, feed-back and applications.

**DTU** has in the fourth year put an effort into the establishment of a formal framework that is intended for supporting the analysis of wireless sensor networks with focus on energy harvesting and routing protocols. Furthermore, emphasis has been placed on techniques and tools aiming at improving the efficiency of analysis conducted by the Duration Calculus model checker.

**KTH** has further developed the performance analysis and dimension techniques for MPSoC communication infrastructure. To that end detailed and formal delay analysis techniques for both worst case and average case have been developed. They are based on Network calculus and queuing theory. The derived worst case delay bound for on-chip communication in mesh based wormhole switching, deterministic routing networks have been shown to be tight and can thus be the bases for guaranteeing communication services with specified delay, throughput bounds. The average case analysis based on queuing theory has a demonstrated accuracy of 10% delay deviation in non-saturated networks with execution times 4-5 orders of magnitude lower than simulation. Hence it is suitable to analyse and compare a large number of architecture and mapping alternatives in design space exploration.

Fault tolerant and reliable communication in MPSoCs has been an emerging but important activity at **KTH**. Various fault tolerant routing schemes for various topologies and under different fault scenarios have been studied. Among other techniques, Fault-on-Neighbor and Q-learning based routing schemes have been identified to constitute useful trade-off points. Fault-on-neighbor is a very low overhead technique that can tolerate a large number but not all kinds of fault patterns. Q-Based learning routing is more expensive but allows to deal with all kinds of fault patterns up to the point when the network is completely split.

As a new activity, **KTH** is initiating work on fault-tolerant and reliable MPSoC communication architectures. Further technology scaling will increase the need for an ability to tolerate faults and errors. **KTH** will focus on techniques to identify, correct, and tolerate faults on the link layer, the network layer and the transport layer of the MPSoC communication fabric.

**UNIBO** will continue on the research activity about many-core simulation using GPGPUs. The main goal will be the interfacing with other simulators like QEMU in order to simulate host plus accelerator scenarios.

Next generation of 3-D systems will integrate more processor and memories by means of Through-Silicon Vias (TSV) in the 3D stack. As a consequence, it is mandatory, especially in complex 3-D MPSoCs architectures, to support efficient on-chip control thermal management. **EPFL** continued their activities partly joined in the past with ETHZ regarding the development of DVFS techniques for 2-D MPSoC [ZABM11]. In this year, further work was performed to combine an active control of on-chip switching rates with an interlayer cooling with pressurized fluids [ZMAM11][ZAM11]

From a technology perspective, **EPFL** has been active on the design of analytical models to study the effect of Thermal Through-Silicon Vias (TTSV) on decreasing the temperature of the circuit [XPM11, X11], and statistical models to analyze the effect of the process variations and power supply noise in 3-D clock distribution networks (CDN) [XPM11b][XPM11c][XPMB11].

**ETH Zurich (ETHZ)** has been mainly concentrating on the analysis of thermal behaviour. Here, we had substantial progress in the compositional analysis including heat transfer between the various computing elements. Part of this work has been done in close cooperation with EPF Lausanne in the context of the European Project Pro3D. In addition, we have been cooperating

with Intel Laboratories Braunschweig in using their 48-core platform INTEL SCC. Finally, there has been a close cooperation with Univ. Trento for the parametric analysis of MPSoC architectures and with Univ. Pisa in terms of the analysis of server structures. In summary, we have been working on the following items:

- Parametric feasibility analysis [SRLPPT11]
- Worst-case temperature analysis [RYBCT11], [SYBT11], [KT11]
- Compositional heterogeneous analysis of complex parallel and distributed systems [PLT11]
- Analysis of server structures [KCTSB11]

**-- The above is new material, not present in the Y3 deliverable --**

## 3. Summary of Activity Progress in Year 4 *(Jan-Dec 2011)*

### 3.1 *Technical Achievements*

#### **System Level Temperature Modeling and Analysis (Linköping)**

During year four the Linköping group has continued the work on temperature modelling and extended the earlier elaborated temperature models to multicore systems. The particular focus was on dynamic steady state thermal analysis and its potential application to reliability optimisation of multicore embedded systems.

We have considered multiprocessor systems running applications exhibiting a power profile that can be considered periodic. We have developed an approach that is both accurate and fast, for Steady State Dynamic Temperature Profile (SSDTP) calculation. Based on our SSDTP calculation technique, we have proposed an approach to efficiently perform reliability optimization, based on the thermal cycling (TC) failure mechanism. More exactly, we have proposed a temperature-aware task mapping and scheduling technique that addresses the TC ageing effect.

#### **Modelling and Synthesis for Efficient and Fault Tolerant Communication over FlexRay Buses (Linköping, DTU, Lund)**

The emerging popularity of FlexRay has sparked much interest in techniques for scheduling signals on the FlexRay bus. Signals are, essentially, elementary units of communication data that need to be transmitted from one ECU to another. In practice, signals are first packed together into frames at the application-level and the frames are then transmitted over the bus. The frames must be scheduled such that the hard real-time deadlines, as demanded by automotive applications, are satisfied. However, apart from realtime issues, frames on the bus may become corrupt due to transient faults, thereby posing reliability issues. Electronic devices, including communication buses, are becoming increasingly vulnerable to transient faults. Transient faults occur for a short duration of time and cause a bit flip, without causing any permanent damage to the logic. They are caused by factors like electromagnetic radiation and temperature variations. In contrast to permanent faults (e.g., those caused by physical damage) which cause long term malfunctioning, transient faults occur much more frequently.

In spite of such reliability concerns, existing frame packing techniques have assumed a fault-free transmission of frames over the bus. In this work, we propose a technique for frame packing for the FlexRay bus that guarantees to achieve reliability against transient faults while satisfying the timing constraints. To achieve fault tolerance, our technique relies on temporal redundancy, i.e., our proposed scheme relies on frame retransmissions. However, this increases the bandwidth utilization cost. Our proposed scheme is constructed to minimize the bandwidth utilization required to guarantee the fault-tolerance of frames transmitted on the FlexRay bus.

Modern automotive systems with several computation nodes and communication units exhibit a complex temporal behaviour which depends highly on the FlexRay configuration and influences the performance of running control applications. We have developed a design framework for integrated scheduling and design of embedded control applications, where control quality is the optimization objective. Currently we have extended the framework to handle FlexRay-based embedded control systems and have proposed a method for the decision of FlexRay parameters aiming at the optimization of control quality.

### **Analysis of communication networks (TU Braunschweig)**

In year 4, the cooperation between iTUBS and GM for further exploitation of the COMBEST results on analysis methods for Ethernet-based communication networks have been finished to the complete satisfaction of both partners. Some of the results were submitted to DATE 2012 [RGE12] and have been accepted for publication. In the cooperation with Daimler started in 2011, a new response time analysis for the dynamic segment of FlexRay and a new approach for determine tighter system level end-to-end latencies have been developed. Results have been submitted for publication and are currently under review.

### **Modelling and Analysis of Multiprocessor Systems with Shared Resources (TU Braunschweig)**

TU Braunschweig has further worked on performance analysis methods for multiprocessor systems with shared resources. New analysis methods have been developed for automotive specific setups, e.g. for the foreseeable automotive multi-core ECUs (Electronic Control Units). For this purpose, automotive specific processor scheduling (according to the OSEK/VDX specification) and shared resource arbitration strategies (specified in the current AUTOSAR R4.0 release) have been considered. The modelling and analysis framework developed in the previous years was extended with the new analysis methods. Results in this direction have been submitted for publication and are currently under review.

### **Modelling and Analysis of Multi-Mode Applications (TU Braunschweig)**

TU Braunschweig has also investigated the timing behaviour of multi-mode applications, i.e. of applications that can switch between different operational modes at runtime. Previous research related to multi-mode systems indicate that computing worst-case response times for multi-mode applications is required for each individual mode and also for the transition phases between two modes. However, as multiprocessor systems will accommodate multi-mode applications distributed among different processors the timing behaviour of the entire system is much more complex and requires additional solutions. In [NNSSE11] we showed that in case of distributed applications, computing only worst-case response times in each individual mode and during every transition between two modes is not enough. The duration of the transition phases has to be computed and considered at design time in order to avoid the overlap of multiple mode changes that can cause violation of the timing constraints. A solution for deriving transition latencies in multi-mode systems was published in [NNSSE11]. The new analysis for multi-mode systems was integrated in the modelling and analysis framework previously developed for multiprocessor systems with shared resources. This integration permits the implementation of new analysis solutions for multi-mode applications which share resources in multiprocessor systems.

### **Runtime layer design for many-cores architectures (CEA LIST)**

In 2011, **CEA LIST** has evolved its programming model for fine-grain parallel tasks. By introducing asynchronous fork-join primitives to its tasks scheduling engine developed with the collaboration of **UNIBO**, it achieved better results in load balancing and reactivity in tasks scheduling. In fact, simulations conducted on the VC-1 decoding application, showed 43% reduction of the task scheduling overhead with respect to the synchronous version developed in 2010 with **UNIBO**. A pedestrian detection application was ported on a cluster of 16 xP70 processors using the multi programming models capability of the **CEA LIST** runtime layer. Actually, the parallelization was done using a threads based model to exploit the TLP in this application as well as the tasks based model to take advantage of DLP.

Moreover, **CEA LIST** has extended its runtime layer scope to cover a two-level control infrastructure based on a global and centralized programmable controller and local cluster-level controllers taking advantage of the acceleration provided by its hardware synchronizing component.

Finally, in the context of the SMECY project, **CEA LIST** has worked on optimizations of the dynamic memory allocator in the runtime layer using dynamic code generation. It resulted in a flexible dynamic memory allocator which is able to match the constraints of embedded systems, such as the P2012 platform (limited and fragmented memory space). Using dynamic code generation, a flexible, and yet performing, implementation was delivered by regenerating at runtime some of its critical functions according to runtime profiling.

### **Benchmarking of multicore architectures (CEA LIST)**

**CEA LIST** has started in 2011 a benchmarking activity with dual goals. The first one is to constitute a knowledge database of performances of multiple parallelization techniques on different multicore architectures. The second is to formally define correlations between these architectures and the applications. From these correlations, it will be possible to estimate a gain of parallelization depending on the technique and the architecture.

### **GPGPU-Accelerated Parallel and Fast Simulation of Thousand-core Platforms (University of Bologna, EPFL)**

Modern system design and application development methodologies in almost every computing domain are largely based on simulation. Virtual platforms are indeed extensively used both to do early software development before the real hardware is available, and to optimize the parallelization and the hardware resources utilization of the application itself when the real hardware is already there.

During the last decade the design of integrated architectures has been characterized by a paradigm shift. Boosting clock frequencies of monolithic processor cores has clearly reached its limits, and designers are turning to multicore architectures to satisfy the growing computational needs of applications within a reasonable power envelope. Multicores are thus becoming ubiquitous in every computing domain, from High Performance Computing (HPC) to embedded systems. To meet the ever-increasing demand for peak performance while fitting tight power budgets there is a clear trend towards simplifying the core microarchitecture design. Future manycore processors will thus embed thousands of simple cores and on-chip memories connected through a network-on-chip, more than hundred times faster than traditional off-chip interconnections.

Simulation and virtual prototyping technology must obviously evolve to tackle the numerous challenges inherent in simulating such complex and highly-parallel future architectures. Simulating a parallel system is an inherently parallel task, since individual processor simulation may independently proceed until the point where communication or synchronization with other processors is required. This is the key idea behind parallel simulation technology, which distributes the simulation workload over parallel hardware resources. In parallel simulation, each simulated processor works on its own by selecting the earliest event available to it and processing it without knowing what happens on other simulated processors. Parallel simulators leverage the availability of multiple physical processing nodes to increase the simulation rate. However, this requirement may turn out to be much too costly if server clusters or computing farms are adopted as a target to run the simulation. Moreover, the high cost – in terms of increasing latency and decreasing bandwidth – for inter-node communication over traditional interconnection systems (i.e. Ethernet) typically leads to poor scalability due to the synchronization overhead when increasing the number of processing nodes.



The development of computer technology has recently led to an unprecedented performance increase of General-Purpose Graphical Processing Units (GPGPU). Modern GPGPUs integrate hundreds of processors on the same device, communicating through low-latency and high bandwidth on-chip networks and memory hierarchies. This allows cutting inter-processor communication costs by orders of magnitude with respect to server clusters. Even more important, such a scalable computation power and flexibility is delivered at a rather low cost by commodity GPU hardware. As a last positive remark, besides hardware performance improvement, the programmability of GPUs also has been significantly increased in the last five years. This has lately led to the diffusion of computing clusters based on such manycores leading to inexpensive solutions in HPC for a wide community.

This scenario motivated **UNIBO** and **EPFL** in developing a novel parallel simulation technology that leverages the computational power of widely-available and low-cost GPUs. **UNIBO** and **EPFL** developed a new simulation technology to deploy a parallel simulator for 1000-core systems on top of GPGPUs. The simulated architecture is composed by several cores (i.e. ARM ISA based), with instruction and data caches, connected through a Network-on-Chip (NoC). The GPU-based simulator is not intended to be cycle-accurate, but instruction accurate. Its simulation engine and models provide accurate estimates of performance and various statistics. Experiments confirm the feasibility and goodness of the idea and approach, as the simulator can model architectures composed of thousands of cores while providing fast simulation time and good scalability.

### **A Simulation Based Buffer Sizing Algorithm for Network on Chips (University of Bologna, EPFL)**

Scalable on-chip networks have evolved as the communication medium to connect the increasing number of cores and to handle the communication complexity. In a NoC, a packet may be broken down into multiple flow control units called flits and NoC architectures have the ability to buffer flits inside the network to handle contention among packets for the same resource link or switch port. The buffers at the source Network Interfaces (NIs) are used to queue up flits when the network operating frequency is different from that of the cores or when there is congestion inside the network that reaches the source. NoCs also employ some flow control strategy that ensures flits are sent from the switch (NI) to another switch (NI) only when there are enough buffers available to store them in the downstream component.

The network buffers account for a major part of the power and area overhead of the NoC in many architectures. Thus, reducing the buffering overhead of the NoC is an important problem.

**UNIBO** and **EPFL** present a simulation-based algorithm for sizing NoC buffers for application traffic patterns. **UNIBO** and **EPFL** present a two-phase approach: in the first phase, mathematical models are used based on static bandwidth and latency constraints of the application traffic flows to minimize the buffers used in the different components based on utilization. In the second phase, an iterative simulation based strategy is used, where the buffers are increased from the ideal minimal values in the different components, until the bandwidth and latency constraints of all the traffic flows are met during simulations. While in some application domains, such as in Chip Multi-Processors (CMPs), it is difficult to characterize the actual traffic patterns that occur during operation at design time, there are several application domains (such as mobile, wireless) where the traffic pattern is well-behaved. This work targets such domains where the traffic patterns can be pre-characterized at design time and a simulation based mechanism can be effective.

Results show that there is 42% reduction in the buffer budgets for the switches, on an average. This translates to around 35% reduction in the overall power consumption of the NoC switches.



### **Analysis of Clock Distribution Networks in 3-D ICs (EPFL)**

Clock and power distribution are expected to be predominant problems in the 3-D design process. Furthermore, EPFL has been focus on the analysis of the effect of different sources of variation in 3-D clock distribution networks (CDN), including (a) process variations and (b) power supply noise.

Through a statistical model and SPICE-based simulations, 2-D and 3-D clock trees have been compared in terms of the process-induced. In addition, multi-domain and different skew of 3-D CDNs have been studied and contrasted in order to give a set of guidelines to facilitate the design of robust 3-D CDNs [XPM11b][XPM11c]. Finally, a co-modeling of process variations and power supply noise have been developed showing that simultaneously modeling different sources of variations is necessary to obtain the correct distribution of clock skew and jitter [XPMB11].

### **Thermal Issues and Thermal Management Policies for 3-D ICs (EPFL)**

Due to the high power densities and the trend to increase higher number of cores in 3-D SoCs to improve performance, thermal issues pose critical challenges, such as hot-spot avoidance, thermal gradient reduction, etc. In order to address and investigate these challenges, two analytical models of Thermal TSVs (TTSVs) are used to describe the effect of TTSVs on decreasing the temperature of the 3-D system, with different tradeoffs between computational time and accuracy [XPM11][X11].

On the other hand, we propose novel online thermal management policies for high-performance 3-D systems with liquid cooling. Our proposed controllers use centralized [ZAM11] and hierarchical [ZMAM11] approaches with global and local controllers regulating the active cooling and performing dynamic voltage and frequency scaling (DVFS). The on-line control is achieved by policies solving an optimization problem that considers the thermal profile of 3D-MPSoCs, its evolution over time and current time-varying workload requirements. Experiments have been performed on a 3D-MPSoC case study with different interlayer cooling structures, using benchmarks ranging from web-accessing to playing multimedia. Results show significant advantages in terms of energy savings that reaches values up to 50% versus state-of-the-art thermal control techniques for liquid cooling.

### **Parametric Analysis of Heterogeneous MPSoC Systems (ETH Zurich, Univ. Trento)**

Trento and ETH Zurich developed a hybrid design and analysis methodology for distributed real-time systems. The proposed approach integrates Modular Performance Analysis (MPA-RTC) with Parametric Feasibility Analysis (PFA). It uses a simplified representation of arrival curves to interface heterogeneous modeling components. More specifically, the method automatically converts arrival curves as used by MPA-RTC to Timed Automata models, and uses these models to trigger a state-based and parameterized model of a processing or communication component. In a similar fashion, the output of the component is characterized by appropriate observer automata and automatically converted to arrival curves. The novelty of our approach consists in deriving feasible regions for various component parameters such as tolerable data rates or bursts for the input or the output of the component, and tolerable fill levels for its activation buffer. Our results extend previous analysis methods which permitted the evaluation of single design points only. For automatically deriving the region of feasible parameters for a component, we implemented a dedicated tool-chain which employs Uppaal and NuSMV. The resulting tool permits us to efficiently explore large design spaces and hence directly supports the design of complex distributed systems, see [SRLPPT11].

### **Worst-case Temperature Analysis of MPSoC (ETH Zurich)**

With the evolution of today's semiconductor technology, chip temperature increases rapidly mainly due to the growth in power density. For modern embedded real-time systems, it is crucial to estimate maximal temperatures in order to take mapping or other design decisions to avoid burnout, and still be able to guarantee meeting real-time constraints. This work provides answers to the question: When work-conserving scheduling algorithms, such as earliest-deadlinefirst (EDF), rate-monotonic (RM), deadline-monotonic (DM), are applied, what is the worst-case peak temperature of a real-time embedded system under all possible scenarios of task executions? We proposed an analytic framework, which considers a general event model based on network and real-time calculus. This analysis framework has the capability to handle a broad range of uncertainties in terms of task execution times, task invocation periods, and jitter in task arrivals. Simulations show that our framework is a cornerstone to design real-time systems that have guarantees on both schedulability and maximal temperatures, see [RYBCT11], [SYBT11], [KT11].

### **Analysis of Servers for MPSoC Systems (SSSA Pisa, ETH Zurich)**

Several servers have been proposed to schedule streams of aperiodic jobs in the presence of other periodic tasks. Standard schedulability analysis has been extended to consider such servers. However, not much attention has been laid on computing the worst-case delay suffered by a given stream of jobs when scheduled via a server. Such analysis is essential for using servers to schedule hard real-time tasks. In this joint work, we illustrate, with examples, that well established resource models, such as supply bound function and models from Real-Time Calculus, do not tightly characterize servers. In this work, we analyze the server algorithm of the Constant Bandwidth Server and compute a provably tight resource model of the server. The approach used enables us to differentiate between the soft and hard variants of the server. A similar approach can be used to characterize other servers; the final results for which are presented.

### **Contract based architecture dimensioning (KTH)**

Defining and constraining traffic in the on-chip network can be a means to achieve predictable performance at low cost. Based on traffic contracts between IPs and the communication infrastructure the network can be optimized to meet all performance constraints at minimum cost. In earlier years a flow regulation technique has been developed. In 2011 the focus was on developing improved delay models for the complex, contention heavy scenarios of on-chip communication traffic. A worst case delay model, based on network calculus, has been developed which provides tight bounds. Based on queuing theory an average delay model has been derived which is 4-5 orders of magnitude faster than simulation with less than 10% accuracy loss in non-saturated networks. These techniques give better means in dimensioning the network, studying and comparing large number of design alternatives during design space exploration.

### **Integration of the communication architecture with the memory architecture (KTH)**

KTH has developed a Data Management Engine (DME) that manages all communication and a distributed, shared memory space in an MPSoC. The DME is fully programmable and offers a range of functionalities from virtual memory space managing to dynamic memory allocation. Conceptually the work has been completed and its performance has been studied in various experiments with different applications. The work is evaluated by industrial partners and options for commercialization are investigated.

### **Modeling and analysis of heterogeneous systems (KTH, DTU)**

As part of the ARTEMIS project SYSMODEL KTH, DTU and Tampere University are developing a complete system-level modelling framework for analysis and refinement of heterogeneous MPSoCs. During 2011 a systematic methodology for refinement-by-replacement has been developed and a cosimulation environment has been built. Both techniques are based on the formal composability properties of the modelling framework but are driven by pragmatic requirements and needs of the industrial partners. These tools have been built into the SystemC based model based design framework.

DTU has focused on energy and reliability analysis. With regard to energy minimization, the most common approach that allows energy/performance trade-offs during run-time of the application is dynamic voltage and frequency scaling (DVFS). DVFS aims at reducing the dynamic power consumption by scaling down operational frequency and circuit supply voltage. Addressing energy and reliability simultaneously is especially challenging because lowering the voltage to reduce energy consumption has been shown to increase the number of transient faults exponentially. DTU has extended the state-of-the-art by providing models, methods and tools that can take into account the interplay between the energy and reliability.

Tasks are divided into two categories: critical and non-critical. To prevent the application failure, critical tasks have to tolerate transient faults. A critical task and its replicas could be mapped on the same PE and run at different modes, or mapped on different PEs. Each processing element has a real-time operating system. Tasks are started in accordance with the fixed-priority preemptive scheduling. A PE could be run at different operating modes, and thus could take different amounts of time to execute the same task. The typical approach for energy minimization is to decide the mapping and the operating mode for each task such that the energy consumed is minimized and the deadlines are satisfied. The analysis technique developed by DTU allows to reduce the negative impact on reliability without a significant loss of energy savings, by carefully deciding the mapping and operating modes.

Another important issue is that of risk management during the design flow. Flexibility, the ability to adapt to change, is very important for embedded systems design. It is widely acknowledged that the early estimation might be inaccurate, as well as the early requirements might be changed, while the initial system configuration is not entirely or finally specified, variations of system properties may occur at any step during the design process. Therefore, the designer must be supplied with additional information concerning the uncertainties of different system configurations.

In practice, a designer adds some slack to the system parameters, e.g. maximum system utilization limitation both for processing element and bus communication. Adding slack used to work reasonably, but with growing system complexity, the prediction becomes more difficult and the unknown coupling effects or limitations increase design risks. Also, it can lead to over-design. In this context, uncertainties need to be investigated in order to guarantee high system flexibility.

DTU has identified a flexibility model that will be integrated into the design space exploration, such that risk management will be possible.

### **Modeling and analysis of fault tolerant distributed embedded systems (DTU, Linköping)**

DTU has started to consider also other communication protocols, besides FlexRay, such as Time-Triggered Ethernet (TTEthernet). TTEthernet implements three traffic classes: (1) Time-Triggered (TT) traffic is used for applications with tight latency, jitter and determinism requirements. (2) Rate-Constrained (RC) messages ensure that bandwidth is predefined for each application, and that delays are bounded. Best-Effort (BE) messages are the classical Ethernet messages, without any guarantees regarding the transmission, delivery and delay of

this class of messages. These messages have no priority and are transmitted when there is no TT or RC traffic.

For this protocol, DTU has surveyed the existing analysis techniques and has completed a MSc project on implementing the “trajectory approach”, which is an analysis that can determine the worst-case end-to-end delay of a RC message. This analysis will be used as part of an optimization approach to determine the static schedules of the TT messages.

### **Modeling and Verification of Embedded Systems (DTU, AAU)**

The verification technique we currently are exploring for Duration Calculus reduces the model-checking problem to checking a formula of quantified linear arithmetic (of integers), i.e. to Presburger Arithmetic. This technique has been developed in collaboration with a group from Oldenburg University. There are several challenges in using this technique: one is the high complexity of the decision problem of Presburger Arithmetic, another is that huge Presburger formulas are generated by the model-checking algorithm. The size of the generated formulas was, in fact, the main problem in the first prototypes. Therefore, emphasis has been put on the development and implementation of a normal form for Presburger formulas that support simplification, including some “cheap” quantifier-elimination techniques. Experiments with this normal form showed encouraging results with respect to the size of problems that we are now able to handle.

In the fourth year we have started up activities exploring the paradigm: program declaratively and execute efficiently on a multi-core platform using the decision problem for quantified linear arithmetic as a case study. We have achieved a speed-up on approximately 6 on a 8-core processor for the exact shadow of the Omega test (corresponding directly to the Fourier-Motzkin elimination procedure for the theory of real numbers) and a speed-up of approximately 4 for other quantifier elimination techniques. The implementations have been based on the function programming language F# and .Net libraries for parallelization.

In the case studies considered focus has been on wireless sensor networks, where a modeling framework has been established for modeling and analyzing networks with energy harvesting capabilities, where a particular emphasis has been on energy-harvesting aware routing algorithms. The established framework captures in a natural manner existing routing protocols like Distributed Energy Harvesting Aware Routing and Directed Diffusion.

Furthermore, in the area of on-line, model-based testing a collaboration has been established with Tallinn Technical University (TTU), and Marko Käärmees from TTU has visited DTU twice, in the form of a 3 month visit and a shorter 4 days visit in 2011. During these visits focus has been on establishing theories for on-line testing.

**-- The above is new material, not present in the Y3 deliverable --**

## **3.2 Individual Publications Resulting from these Achievements**

### **ETHZ**

1. [RYBCT11] Devendra Rai, Hoeseok Yang, Iuliana Bacivarov, Jian-Jia Chen, Lothar Thiele: Worst-case temperature analysis for real-time systems. DATE 2011: 631-636.
2. [SYBT11] Lars Schor, Hoeseok Yang, Iuliana Bacivarov, Lothar Thiele: Worst-Case Temperature Analysis for Different Resource Availabilities: A Case Study. PATMOS 2011: 288-297.

3. [PLT11] Simon Perathoner, Kai Lampka, Lothar Thiele: Composing heterogeneous components for system-wide performance analysis. DATE 2011: 842-847.
4. [KT11] Pratyush Kumar, Lothar Thiele: System-Level Power and Timing Variability Characterization to Compute Thermal Guarantees. In Proc. of the 9th International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS 2011, ACM, Taipei, Taiwan, October, 2011.

### TU Braunschweig

5. [NNSSE11] Mircea Negrean, Moritz Neukirchner, Steffen Stein, Simon Schliecker, und Rolf Ernst, "Bounding Mode Change Transition Latencies for Multi-Mode Real-Time Distributed Applications," in *16th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA'11)*, (Toulouse, France), September 2011
6. [REG12] Jonas Rox, Rolf Ernst, Paolo Giusto, "Using Timing Analysis for the Design of Future Switched Based Ethernet Automotive Networks", in Proceedings Design, Automation and Test in Europe (DATE 12) (to appear).

### Linköping

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**-- The above are new references, not present in the Y3 deliverable --**

### **3.3 Interaction and Building Excellence between Partners**

#### **Modelling and Synthesis for Efficient and Fault Tolerant Communication over FlexRay Buses (Linköping, DTU, Lund)**

The interaction in this activity has been between Linköping, Lund, DTU.

- Joint work to develop control performance models, scheduling, and optimisation algorithms.
- Soheil Samii and Anton Cervin have done several visits at Lund and Linköping, respectively.

- Petru Eles has visited DTU in June 2011.
- One joint paper has been published.

#### **Analysis of Servers in MPSoC (Univ. PISA SSSA, ETH Zurich)**

The interaction in this activity was on new methods to analyse servers as used in complex distributed and parallel real-time systems. The results have been published in [KCTSB11]:

- Collaboration and information exchange in the area of servers for real-time systems.
- Development of a new methodology to analyse them.

#### **Scalable heterogeneous analysis of MPSoC (Univ. Trento, ETH Zurich)**

We have been advocating a rigorously formal and compositional style for obtaining key performance and/or interface metrics of systems with real-time constraints. In this joint work we combine the analysis methods developed in the two groups towards a hierarchical approach that couples the independent and different by nature frameworks of Modular Performance Analysis with Real-time Calculus (MPA-RTC) and Parametric Feasibility Analysis (PFA):

- Joint discussions on the coupling of the methods.
- Joint publication that shows the results, including the corresponding software implementation [SRLPPT11].

#### **Modeling and analysis of heterogeneous systems (KTH, DTU)**

The interaction in this activity has been between KTH and DTU, and has been supported by the Artemis project SYSMODEL.

- Joint work to develop the System Functionality Framework (SFF) based on the ForSyDe model.
- Joint development of SystemC templates to ease the creation of SFF models for SMEs.
- Mikkel Koefoed Jakobsen and Seyed Hosein Attarzadeh Niaki have done several visits at KTH and DTU respectively.
- Two joint 1-day workshops have been held.
- A tutorial on Model based Design has been organized jointly with Tampere University of Technology, DTU and KTH at the International Symposium on Systems on Chip, November 2011.
- A first joint paper is accepted for Embedded World.

**-- Changes wrt Y3 deliverable --**

*This is new text reflecting the interactions of Y4.*

### **3.4 Joint Publications Resulting from these Achievements**

1. [SEP 11] Soheil Samii, Petru Eles, Zebo Peng, Anton Cervin, Design Optimization and Synthesis of FlexRay Parameters for Embedded Control Applications, 6th International Symposium on Electronic Design, Test and Applications (DELTA 2011), Queenstown, New Zealand, 2011.
2. [KCTSB11] Pratyush Kumar, Jian-Jia Chen, Lothar Thiele, Andreas Schranzhofer, Giorgio C. Buttazzo: Real-Time Analysis of Servers for General Job Arrivals Proc. of

17th IEEE Intl. Conf. on Embedded and Real-Time Computing Systems and Applications (RTCSA 2011), IEEE, Toyoma, Japan, August, 2011.

3. [SRLPPT11] Alena Simalatsar, Yusi Ramadian, Kai Lampka, Simon Perathoner, Roberto Passerone, Lothar Thiele: Enabling parametric feasibility analysis in real-time calculus driven performance evaluation. CASES 2011: 155-164.
4. M. K. Jakobsen, J. Madsen, S. H. A. Niaki, I. Sander, J. Hansen, "System level modeling with open source tools", to appear in proceedings of Embedded World 2012.

-- The above are new references, not present in the Y3 deliverable --

### 3.5 Keynotes, Workshops, Tutorials

#### **Lothar Thiele ETH Zurich: Temperature-aware Scheduling ARTIST Summer School September 4-9, 2011**

*Aix-les-Bains (near Grenoble), France*

Power density has been continuously increasing in modern processors, leading to high on-chip temperatures. A system could fail if the operating temperature exceeds a certain threshold, leading to low reliability and even chip burnout. There have been many results in recent years about thermal management, including (1) thermal-constrained scheduling to maximize performance or determine the schedulability of real-time systems under given temperature constraints, (2) peak temperature reduction to meet performance constraints, and (3) thermal control by applying control theory for system adaption. The presentation will cover challenges, problems and approaches to real-time scheduling under temperature constraints for single- as well as multi-processors.

#### **Invited Talk, Petru Eles, Scheduling and Optimization of Fault-Tolerant Embedded Systems**

**ACM SIGPLAN/SIGBED Conference on Languages, Compilers, Tools and Theory for Embedded Systems (LCTES 2011), Chicago, IL, USA, 12-14 April 2011 (in conjunction with CPS Week 2011)**

Abstract: This work addresses the issue of design optimization for fault-tolerant hard real-time systems. In particular, our focus is on the handling of transient faults using both checkpointing with rollback recovery and active replication. Fault tolerant schedules are generated based on a conditional process graph representation. The formulated system synthesis approaches decide the assignment of fault-tolerance policies to processes, the optimal placement of checkpoints and the mapping of processes to processors, such that multiple transient faults are tolerated and the timing constraints of the application are satisfied. We propose a fine-grained transparent recovery, where the property of transparency can be selectively applied to processes and messages. Transparency hides the recovery actions in a selected part of the application so that they do not affect the schedule of other processes and messages. While leading to longer schedules, transparent recovery has the advantage of both improved debuggability and less memory needed to store the fault-tolerant schedules.

#### **Invited Talk: Using Compositional Performance Analysis for Obtaining Viable End-to-End Latencies in Distributed Embedded Systems**

**(Jonas Rox, Rolf Ernst, TU Braunschweig)**

**Rigorous Embedded Design 2011 - organized and funded by ARTIST**

*Salzburg, Austria – April 10<sup>th</sup>, 2011*

The objective of the workshop was to discuss new methodologies for the rigorous design of embedded systems. Through a series of invited talks, the workshop surveyed some of the challenges and emerging approaches in the area. A series of design flows were presented. The workshop mainly discussed performance analysis, correctness (high confidence and security), code generation, and modeling aspects (including timed scheduling and software/hardware interactions). Those concepts were illustrated with examples coming from the aeronautic, automotive, and robotic areas. Interactions between industrial and academic researchers were also facilitated through a series of open discussion sessions.

**Invited Talk: Formal Performance Analysis in Automotive Systems Design – A Rocky Ride to New Grounds**

**(Rolf Ernst, TU Braunschweig)**

**23rd IEEE Conference on Computer Aided Verification (CAV) Symposium**

*Snowbird, Utah, USA – July 20, 2011*

CAV 2011 was the 23<sup>rd</sup> in a series dedicated to the advancement of the theory and practice of computer-aided formal analysis methods for hardware and software systems. The conference covered the spectrum from theoretical results to concrete applications, with an emphasis on practical verification tools and the algorithms and techniques that are needed for their implementation. The talk given by Prof. Ernst focused on performance challenges in automotive design. Formal performance analysis methods for automotive design were presented and major obstacles from theory to industrial application were highlighted.

<http://www.cs.utah.edu/events/conferences/cav2011/>

**Invited Talk: Mixed safety critical system design and analysis**

**(Rolf Ernst, TU Braunschweig)**

**ARTIST Summer School Europe 2011**

*Aix-les-Bains (near Grenoble), France – September 4-9, 2011*

The lecture gave an introduction to mixed criticality system design and the related safety standards using the IEC 61508 as a prominent example. Focusing on systems which are both time and safety critical, such as in automotive and avionics, the lecture further elaborated on the impact of fault tolerance and fail safe mechanisms on real-time properties. Formal models and analysis methods were presented that support the efficient design of mixed critical systems.

<http://www.artist-embedded.org/artist/Technical-Programme>

**Invited Talk: Multicore Architectures for Mixed Safety Critical Applications – Challenges and Opportunities**

**(Rolf Ernst, TU Braunschweig)**

**SafeTRANS Industrial Day**

*Hamburg, Germany – November 08, 2011*

**SafeTRANS** ("Safety in Transportation Systems") is a Competence Cluster combining research and development expertise in the area of complex embedded systems in transportation systems. SafeTRANS drives research in human centred design, in system and software development methods for embedded systems, as well as in safety analysis and - for avionics and rail - its integration in certification processes, driven by a harmonised strategy addressing the need of the transportation sector. The topic of the 11<sup>th</sup> SafeTRANS Industrial Day was "**Development processes for Multicore**".

Sharing embedded system resources among functions of different safety criticality usually leads to mixed safety and time critical embedded systems. Such mixed critical systems must

combine conflicting safety and efficiency requirements and related design processes. The talk gave an overview on mixed critical system design challenges and explained how different criticalities can be properly separated in function and timing. In multicore architectures, separation is more difficult than in networks due to low level resource sharing. The talk showed the effects and provided solutions addressing multicore and manycore systems.

[http://www.safetrans-de.org/en\\_11\\_Industrial\\_Day.php](http://www.safetrans-de.org/en_11_Industrial_Day.php)

### **Tutorial / Invited Talk: Multi-Core and Many-Core for Mixed-Critical Systems - Denial of Service and other Performance Challenges**

**(Mircea Negrean, Rolf Ernst, TU Braunschweig)**

**BoCSE (Bosch Conference on Systems and Software Engineering)**

*Ludwigsburg, Germany – November 15 – 17, 2011*

The talk was part of a tutorial at the 4<sup>th</sup> BoCSE-Conference. The conference organized by Bosch brings together engineers, managers, technology experts from different departments of the company, from other companies and from academia. In 2011 the event had over 600 participants. The focus of the given presentation was on challenges which arise in case of integrating applications with different criticalities/different safety requirements on multi-core and many-core systems.

### **Seminar: Timing Analysis Workshop (Paul Pop, DTU)**

**Safety-Critical Systems Interest Group, Infnit innovation network on ICT**

*Lyngby, Denmark – 15.2.2011*

Timing analysis plays an important role in the certification of safety-critical systems. The workshop is intended to present the main approaches and uses of timing analysis during the development of such systems. Timing analysis can also be used in systems which are not safety-critical, but where performance guarantees are important. The event had 80 participants, more than half were from the industry.

<http://scsig15022011.eventbrite.com/>

### **Tutorial: Digital Microfluidic Biochips: Functional Diversity, More than Moore, and Cyberphysical Systems (Krishnendu Chakrabarty, Duke University, USA; Paul Pop, DTU; Tsung-Yi Ho, National Cheng Kung University Tainan, Taiwan)**

*Taipei, Taiwan - 9.11.2011*

Advances in droplet-based "digital" microfluidics have led to the emergence of biochip devices for automating laboratory procedures in biochemistry and molecular biology. These devices enable the precise control of nanoliter-volume droplets of biochemical samples and reagents. As a result, non-traditional biomedical applications and markets (e.g., high-throughput DNA sequencing, portable and point-of-care clinical diagnostics, protein crystallization for drug discovery), and fundamentally new uses are opening up for ICs and systems. However, continued growth (and larger revenues resulting from technology adoption by pharmaceutical and healthcare companies) depends on advances in chip integration and design-automation tools.

<http://www2.imm.dtu.dk/~pop/codes+iss02tu-chakrabarty.html>

### **Presentation: "Hardware support for online resources management" (Raphaël David, CEA LIST) + Program Co-Chair**

**International Forum on Embedded MPSoC and Multicore, MPSoC'2011**

*Beaune, France, July 4-8, 2011*

Presentation dedicated to the Hardware Synchronizer resource and its usefulness for dynamically managing computing resources.

**Tutorial: “Dynamic management of Embedded Multi-core architectures” (Raphaël David, CEA LIST)**

**Asia South Pacific Design Automation Conference, ASP-DAC’2011**

*Yokohama, Japan, January 25-28, 2011*

Tutorial dedicated to present solutions for dynamically managing computing resources in MPSoC architectures as well as hardware supports for accelerating this management. Focus on CEA LIST experience (SCMP, Platform 2012 architectures and the related acceleration modules).

**Keynote: Computational limits in 3-d integrated systems (Axel Jantsch)**

**International Symposium on Systems on Chip**

*Tampere Finland, November 2011*

Abstract: The intrinsic computational efficiency (ICE) of silicon defines the upper limit of the amount of computation within a given technology and power envelope. The effective computational efficiency (ECE) and the effective computational density (ECD) of silicon, by taking computation, memory and communication into account, offer a more realistic upper bound for computation of a given technology. Among other factors, they consider how distributed the memory is, how much area is occupied by computation, memory and interconnect, and the geometric properties of 3-D stacked technology with through silicon vias (TSV) as vertical links. We use ECE and ECD to study the limits of performance under different memory distribution constraints of various 2-D and 3-D topologies, in current and future technology nodes. Among other results, our model shows that in a 35 nm technology a 16 stack 3-D system can, as a theoretical upper limit, obtain 3.4 times the performance of a 2-D system (8.8 Tera OPS vs 2.6 TOPS) at 70% reduced frequency (2.1 GHz vs 3.7 GHz) on 1/8 the total area (50 mm<sup>2</sup> vs 400 mm<sup>2</sup>).

Web site: <http://web.it.kth.se/~axel/presentations/2011/3DLimits-SoCTampere.pdf>

**Tutorial : System Level Modeling**

**International Symposium on System-on-Chip**

*Tampere, Finland, October 31 - November 2, 2011*

The tutorial course describes the system-level modeling concepts, gives an overview of existing open-source tools, presents languages for high-level modeling, and gives examples on practical modeling cases. Talks given by DTU, KTH, UC Berkeley, University of York, UK, TUT, Finland, DA Design, Finland.

**Tutorial: Memory architecture and management in a NoC platform.**

*Design Automation and Test Conference (DATE), March 2011.*

Presentation given by Axel Jantsch, KTH

**Tutorial: Shared memories in multiprocessors.**

*Lecture at the Shenzhen Summer School on Embedded Systems, July 2011.*

Presentation given by Axel Jantsch, KTH.

**Invited seminar: Predictable communication performance in on-chip networks.**

University of Technology Vienna, June 2011

Presentation given by Axel Jantsch, KTH

**Invited Talk: Many-core Interconnection Networks Trends: Fast, Vertical, Asynchronous (Luca Benini, UNIBO)**



**System Level Interconnect Prediction (SLIP)**

*San Diego Convention Center, San Diego, California on June 5, 2011*

The 2011 System Level Interconnect Prediction (SLIP) workshop has been co-located with the 48th IEEE/ACM Design Automation Conference. The general technical scope of the workshop is the design, analysis and prediction of intercommunication fabrics in electronic systems.

<http://www.sliponline.org/>

**Invited Talk: Going up: 3D integration and many-core SoCs (Luca Benini, UNIBO)  
3D Integration Workshop For High Performance Computing System**

*Abu Dhabi, April 18-19, 2011*

The presentation focused on many-core SoC design and 3D integration.

<http://eeweb.poly.edu/hli/3D-Workshop/Home.htm>

**Keynote: G. De Micheli – Nanosystems: sensors and electronics for rational health monitoring.****4th International Workshop on Advances in Sensors and Interfaces (IWASI)**

*Savelletri di Fasaro, Brindisi, Italy, June 28-29, 2011.*

Abstract: Smart micro/nano systems will foster a revolution in health and environmental management, with the final objective of improving security and quality of life. At the same time, they will create a large market of components and systems, and a renewed perspective for electronic design and manufacturing companies. Such systems will be the fundamental building blocks of wearable and ambient systems, to gather and integrate heterogeneous data in real time and to operate and communicate in a wireless and ultra low power mode.

The design of these systems will be enabled by the hybridization of manufacturing technologies which enables us to attain unprecedented levels performance as well as to integrate electronic and fluidic circuits with sensors and actuators. To accomplish this ambitious goal, new technologies and architectures must be matched and tailored to the operational environment by solving novel and challenging design and optimization problems, through the creation of novel design methodologies and tools.

<http://iwasi2011.poliba.it/key4.html>

**-- The above is new material, not present in the Y3 deliverable --**

## 4. Milestones, and Future Evolution

### 4.1 Current Milestones

#### Integration of Symta/S - MPA and unifying approaches for hierarchical scheduling

More recent versions of SymTA/S employ more general event models (denoted here as delta-functions) which can be considered as the pseudo-inverses of arrival curves. The conversion of arrival curves to delta-functions has been completed. The conversion of delta-functions to arrival curves is still open and will be tackled in the next year.

*This milestone has been fulfilled. When converting event models from the SymTA/S to the MPA representation an issue with the interface SymTA/S → MPA is that it is not always tight, i.e., it can introduce pessimism for the analysis results. ETHZ and TUBS invested efforts to find a solution for reducing the pessimism. The conclusion is that a lossless interface for converting event models from SymTA/S to MPA seems not realizable. It is, however, possible to control the precision of the conversion.*

**In Year 4 the tool coupling with the ability of adjusting the conversion precision will be used to study the trade-off between accuracy and runtime.**

*The above milestone has been fulfilled.*

#### Performance analysis of inter-task synchronization in multiprocessor systems (TU Braunschweig)

In the 3rd year, the work on unifying the methodologies to capture shared resource synchronization and shared memory accesses shall be continued. The framework shall be applied to new applications.

*This milestone has been fulfilled. A method that captures more accurately the interference between different cores that share common resources has been published in [SNE10]. The framework has been applied to investigate the impact of the shared resource usage on the systems' timing for different multiprocessor design options [NSE+10]. Further work was performed to investigate the applicability of the analysis methods to particular problems in the industry, e.g. in the automotive domain.*

In the 4<sup>th</sup> year, the work on the methodology to capture the shared resource synchronization in multiprocessor systems will continue. The framework developed in the previous years will be extended to consider new system setups. Further on, effort will be devoted to provide analysis approaches for multi-mode systems.

*This milestone has been fulfilled. The framework developed in the previous years was updated. Extensions of the previously available analyses as well as new analysis solutions were implemented. Results related to the analysis of multiprocessor systems with shared resources are submitted for publication. Furthermore, research on the timing behaviour of multi-mode systems was performed. A solution for deriving transition latencies in multi-mode systems was published in [NNSSE11].*

#### Hybrid approach combining Real-Time Analysis and Timed Automata

Concerning the hybrid approach combining Real-Time Analysis (RTC) and Timed Automata, CEA will try to extend the schedulability analysis of RTC to state-based schedulers by applying the event generator approach. For example, we are working on

the feasibility analysis for adaptive DVS scheduling, to optimistically minimize the energy when the system is lightly loaded by executing at low speeds, and to pessimistically meet the timing constraints when the system is heavily loaded by executing at the maximum speed of the system. ETHZ will extend its framework for coupling timed automata with MPA and attempt to improve its scalability to large distributed embedded systems.

In the third year, we have been able to couple the RTC Analysis framework of ETHZ with state-based performance analysis methods. Therefore, this milestone has been reached, see [LDT10].

**The focus in the fourth year will be the extension of this hybrid approach to the analysis of bus-based multicore systems, i.e. systems with several interacting resources. New methods of interference analysis of task executions on joint resources developed in cooperation with other partners in this activity.**

### Contract based architecture dimensioning

Based on the definition of performance contracts between IPs and the SoC infrastructure (done in year 1), in year 2 KTH will work on formulating the problem of dimensioning the infrastructure, given a set of contracted flows and proposing methods for solving it.

*The above milestone has been fulfilled partially. The regulation spectrum has been defined, which defines the space of possible contract parameters and the optimization opportunities for traffic shaping. An optimization algorithm has been developed and implemented and will hopefully be published in year 3.*

During the third year we will further study different aspects of infrastructure dimensioning based on contracted flows, and develop optimization methods and algorithms.

*The above milestone has been fulfilled. The basic concepts have been built and a static resource dimensioning method has been developed.*

**The focus in year 4 will be to formulate the problem for dynamic renegotiation of traffic contracts between IPs and infrastructure, develop a solution and conduct experiments.**

*This milestone has been partially achieved. The problem of dynamic traffic regulation has been formulated and one part, the development of a dynamic delay and performance model, has been completed. It has been published in ICCD 2011 and DATE 2012. The second part, the development of a dynamic regulation algorithm is targeted for 2012.*

### Integration of the communication architecture with the memory architecture

KTH will develop a scalable, distributed memory architecture for MPSoCs. It will facilitate efficient handling of a virtual address space, cache coherence and memory consistency.

*The above milestone has been fulfilled. During the second year Data Management Engine has been developed and implemented, that is programmable and can in principle support all types of MPSoC memory management functions and algorithm.*

**During year 3 we will develop and implement a programmable memory management handler that realizes many memory management functions efficiently. Emphasis will be put on scalable performance for distributed memory system in MPSoCs.**

*The above milestone has been fulfilled. In the third year, cache coherence protocols, memory consistency models, dynamic memory allocation algorithms have been developed.*

**Focus in year 4 will be on developing a scalable cache coherence solution, improve the memory consistency models and their implementations, and conduct more realistic experiments.**

*The above milestone has been completed and results have been published in ASPDAC 2011, a chapter of the Springer book "Scalable Multi-core Architectures", IEICE Electronics Express no 22 2011, and DSD 2011.*

### **Modeling and analysis of heterogeneous systems:**

In this new activity, started during year 2, KTH and DTU will develop a SystemC based modeling framework for heterogeneous systems including untimed, synchronous time, discrete time and continuous time models of computation.

*The above milestone has been fulfilled partially. The SystemC based models have been created for the synchronous time and discrete time (event driven) MoCs.*

**KTH and DTU will continue their development of a comprehensive SystemC based modelling framework for heterogeneous systems. Focus in year 4 is on integrating performance analysis tools into the modeling framework, and to implement the framework in SystemC to allow for broader industrial use.**

*The SystemC based framework has been further developed to a state where industrial users perform case studies (within the Artemis SYSMODEL project).*

### **System Level Temperature Modelling and Analysis**

During the third year, the Linköping group will work on the elaboration of fast and sufficiently accurate analytical temperature models for the system level. Such an efficient approach to temperature analysis is extremely important as a component in a temperature aware optimisation framework for the design of energy efficient embedded systems.

*The above milestone has been fulfilled.*

**In year 4, LiU will extend the elaborated temperature models to multicore systems.**

*The above milestone has been fulfilled.*

### **Simulation-based and analytical methods for performance estimation of distributed real-time systems for control applications**

During the third year the groups at Linköping, DTU, and Lund will continue their work on modelling and quality optimisation for control applications implemented on distributed embedded systems. Special emphasis will be placed on the issue of event based control and the related quality vs. resource utilisation tradeoffs.

*The above milestone has been fulfilled.*

**This activity is considered done and will not be continued in year 4.**

*The above milestone has been fulfilled.*

### **Modeling and analysis of fault tolerant distributed embedded systems**

During the second year Linköping and DTU will develop a reliability analysis approach for distributed and MPSoC systems considering various hardening degrees of the underlying hardware platform.

*The above milestone has been fulfilled.*

During the third year, DTU will investigate "design for adaptivity". The question is how can a system be designed offline such that runtime adaptation is facilitated. We will identify a relevant case-study that can be used to motivate such an approach and propose design methods for adaptivity.

*The above milestone has been fulfilled. The research performed has been reported in the DTU technical report "Fault-Tolerant Design of Mixed-Criticality Adaptive Embedded Systems", by P. K. Saraswat, P. Pop and J. Madsen.*

**In year 4, DTU will focus on the modelling and analysis of certification costs for mixed-criticality embedded systems. Using such an analysis model, DTU will extend their temporal optimization tool to incorporate trade-offs related to certification costs.**

*The above milestone has been fulfilled.*

## Modeling and Verification of Embedded Systems

In year 1 DTU will continue to formalize the ARTS system-level simulation model using timed automata based on UPPAAL. This work was started in ARTIST2. The aim is to make it usable for designers early in the design process. In order to support designers of industrial applications, the timed-automata model will be hidden for the user, allowing the designer to work directly with the abstract system-level model of embedded systems. The work will be carried out in cooperation with AAU.

*The above milestone has been fulfilled, resulting in a prototype framework called MoVES, which allows to experiment with different models-of-computation.*

During the second year this work will be continued with the aim to capture more aspects of both the application and the platform. A goal is to make a stronger link between the system-level model and a more detailed hardware platform model. DTU will refine its formal model to address modeling and verification issues closer to the hardware layer of the execution platform.

*The above milestone has been fulfilled,*

In the third year, DTU will extend the MoVES Framework in various ways, e.g. to incorporate more resource aspects and more advanced bus structures. Furthermore, the issue of scalability will be addressed.

*The above milestone has been fulfilled,*

**In the fourth year, the availability of the MoVES tool will be improved.**

*In connection with the completion of the PhD project of Aske Brekling (around New Year 2010-2011), the webpage [www.imm.dtu.dk/moves](http://www.imm.dtu.dk/moves) was established so support easy experimentation.*

*The above milestone has been (partially) fulfilled.*

## Analysis tools for embedded systems

In year 1 DTU has established efficient methods for verification of resource constraints. One activity will focus on the real-time logic durations calculus.



*The above milestone has been fulfilled. A model-checking result was established which has the potential of verifying strong timing constraints as well as other kinds of resource constraints. The work has been done in collaboration with University of Oldenburg.*

Based on the encouraging results from a first prototype implementation, the plan for next year is to extend the theory and to advance the development of the tool.

*The above milestone has been fulfilled.*

In the third year, DTU will continue the Improvement of the Duration Calculus model checker with respect to both the theoretical aspects and the practical improvements of the prototype.

*The above milestone has been fulfilled.*

**In the fourth year, DTU will continue this activity. Furthermore, investigations concerning implementations exploiting multi-core platforms will be initiated.**

*The theories and tools for Duration Calculus model checking has been further developed in 2011 and we have established the first results on the exploitation of multi-core platforms.*

*The above milestone has been fulfilled.*

### **Reliability extensions for Variability Aware Modeling (IMEC)**

In the 3rd year a research effort will start for the integration of reliability issues like Negative Bias Temperature Instability (NBTI), Hot Carrier Degradation (HCD), Soft Break Down (SBD in oxide) and Soft Errors in the VAM framework.

*The above milestone has been fulfilled within the IWT funded Project ELIXIR.*

*In addition, within the European project SYNAPTIC, regarding lithography evaluation, Imec defined the litho process variability aware methodology for the target technology TSMC40LP to characterize SRAM sensitivity to variability and litho issues.*

*Within the European project TRAMS, we report a method and its implementation in a prototype tool hereafter called Memory Variability Aware Modeling based on a novel technique that predicts the correct memory wide statistics of any parameter that can be measured in a SPICE/SPECTRE testbench, such as access time, power, stability checks such as read margin, and so on. The method relies on a mix of critical path sensitivities to process variations in its building blocks. Such sensitivity analysis is done at a larger granularity than the transistor level proposed so far for analog circuits, hence leading to a more efficient amount of simulation runs needed hence much less CPU time, and it provides a holistic treatment of all interactions.*

**In the 4<sup>th</sup> year, the focus within SYNAPTIC will be on the tool flow and benchmarking while in TRAMS the focus will be on FinFET technology.**

- Within the IWT project ELIXIR, about self-repairing electronic systems: (1) the initial requirements, the definition and the development of a method for a self-monitored system were performed; (2) a controller for experimental demo setup of a self-monitored system has been characterized.
- Within the European project TRAMS, about terascale reliable adaptive memory systems: a method for variability modeling for FinFET SRAM blocks has been reported, including a comparison between planar and FinFET SRAM cell technologies at 10nm node.
- Within the European project SYNAPTIC, about SYNthesis using Advanced Process Technology Integrated in regular Cells, IPs, architectures, and design platforms: (1) a test vehicle has been defined for benchmarking purposes based on SRAM layout in

40nm planar CMOS technology; (2) a tool flow has been implemented for sub-wavelength lithography and variability aware SRAM characterization; (3) the vehicle using the implemented characterization flow has been benchmarked.

*The above milestone has been fulfilled.*

### Runtime layer design for many-cores architectures (CEA, UNIBO)

**During Year 3 CEA LIST** has implemented a SW runtime for the management of resources in a multi-core architecture where computing processors are sharing a single memory space with uniform access time properties.

*The above milestone has been fulfilled.*

**In year 4, CEA LIST will tackle the challenge of managing resources of manycores architecture by extending actual framework to support clustered architectures with a non uniform memory space.**

*The above milestone has been fulfilled.*

### 3-D Systems (EPFL)

Since EPFL has only recently joined the cluster, solely future milestones are mentioned

#### **Analysis of multi-clock domain for 3-D systems**

**Models that include process variability both random and systematic will be developed for different clock distribution networks. Note that the models need to be adapted to the traits of each investigated network.**

#### **IR drop analysis for 3-D systems**

**Effort will be placed to develop a power grid analysis tool that can handle 3-D power distribution network including the vertical interconnect (a new structure as compared to planar power grids).**

*Both of the above milestones have been fulfilled.*

## 4.2 Main Funding

The ArtistDesign NoE funds integration and building excellence with the partners, and with the European research landscape as a whole. Beyond this “glue” for integration and excellence, during Year 3 this activity has benefited from direct funding from:

#### **Linköping University:**

- Swedish Foundation for Strategic Research (SSF)  
Project name: “Fault-Tolerant and Secure Automotive Embedded Systems.”
- Swedish research Council  
Project name: “Adaptive Resource Allocation for Distributed Embedded Systems.”

#### **DTU**

- SYSMODEL (ARTEMIS JU). Period 2009-2011.
- DaNES (Danish Network for Embedded Systems, funded by the Danish Advanced Technology Foundation), Denmark. Period 2007-2010.
- ProCell (project on programmable cell chip: culturing and manipulation of living cells with real-time reaction monitoring funded by the Danish Strategic Research Council),

- RECOMP funded by ARTEMIS JU. Period 20010-2013.
- SMECY funded by ARTEMIS JU. Period 20010-2013.
- ASAM funded by ARTEMIS JU. Period 20010-2013.

#### CEA LIST

- MC2H (ManyCore for Computing and Healing). French R&D cooperation program (Nano 2012), focusing on the design of multi-core component and on the development of the SW layer allowing to manage it. In this project CEA LIST mainly focus on the SW runtime development in this project.
- SCALOPES (SCAlable LOw Power Embedded platformS). ARTEMIS project. The project focus technology and tool developments for multi-core architectures for communication infrastructure, surveillance systems, smart mobile terminals and stationary video systems.
- SMECY (Smart Multicore Embedded SYstems). ARTEMIS project. The mission of the SMECY project is to develop new programming technologies enabling the exploitation of manycore architectures

#### UNIBO

- ICT-Project PREDATOR
- ICT-Project GALAXY
- ICT-Project Scalopes (Artemis JU)
- Industrial funding on Sensor Networks from Telecom Italia spa

#### TUBS

- COMBEST (IST STREP 215543)  
This IST STREP project COMBEST provides a formal framework for component based design of complex embedded systems.  
<http://www.combest.eu/home/>
- DFG (Deutsche Forschungsgemeinschaft / German Research Foundation  
[www.dfg.de](http://www.dfg.de))

#### ETH Zurich

- PROD3D Programming for Future 3D Architecture with Many Cores (EU FP7)
- EURETILE Mapping Algorithms onto Tiled Multirocessor Arrays (EU, FP7)
- PREDATOR Predictable and Efficient Embedded Systems (EU, FP7)
- COMBEST Component Based Design of Embedded Systems (EU FP7)
- MICS Mobile Information and Communication Systems (Swiss National Science Foundation)

#### KTH

- SYSMODEL (ARTEMIS JU). Period 2009-2011.
- Swedish national funding VR for a NoC performance analysis project. Period 2009-2011.
- iFest (ARTEMIST JU). Period 2010-2013.

#### EPFL

- PROD3D Programming for Future 3D Architecture with Many Cores (EU FP7)
- Guaranteeing Power and Signal Integrity for 3-D ICs (Swiss National Science Foundation)
- Nanosystems (Advanced ERC grant)

**-- Changes wrt Y3 deliverable --**

*The list of projects funding the activities in the activity, has been updated*

## **5. Internal Reviewers for this Deliverable**

- **Dr. Raphaël DAVID** (CEA LIST)
- **Associate Professor Paul Pop** (DTU)