IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Transversal Activity Progress Report for Year 4

Transversal Activity:
Industrial Integration

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Policy Objective (abstract)
Each of the ArtistDesign Thematic Clusters (WP3-WP6) is important *per se* for advancing the state-of-the-art in embedded system design. However, if we wish to have a strong impact on industry and society at large, the results of the thematic clusters have to be harmonized in an overall design flow that can sustain the industrial embedded design chain from conception of the product to its implementation.This transversal activity is intended to define design flows and methodologies for two or three industrial segments leveraging the research carried out in the Thematic Clusters. This deliverable summarizes the achievements of the activity during Y3 of ArtistDesign.

Versions

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1. Overview

1.1 High-Level Objectives

Each of the ArtistDesign Thematic Clusters (WP3-WP6) is important *per se* for advancing the state-of-the-art in embedded system design. However, if we wish to have a strong impact on industry and society at large, the results of the thematic clusters have to be harmonized in an overall design flow that can sustain the industrial embedded design chain from conception of the product to its implementation.

The chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics).

Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, the system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company. The benefits of these flows and methods are obvious as they provide shorter time to market and better quality designs but require a will of the industrial segment to work together towards this goal. In the automotive domain, Autosar is an excellent step in that direction. Other industrial segments are less cohesive in searching for a unified approach to design. In addition, society concerns such as energy, health and environment conservation, are offering new business opportunities for emerging technologies such as wireless sensor networks. The difficulty in these new opportunities resides in lack of standards and of experience with new communication concepts and, last but not least, in security.

We believe that all the thematic clusters bring something important to all industrial segments, but we need to pay attention to the way the results obtained by the clusters are formulated. Integration is a matter of modelling and providing interfaces that guarantee that the properties of the components are maintained after integration. Integration takes two forms: an horizontal one where different IPs coming from different companies or from different design groups in the same company have to be assembled; a vertical one, where the requirements are clearly and possibly formally communicated from a higher level player to a lower level one and where the information about the capabilities and limitations of the IPs are unambiguously communicated from the lower level to the higher level. The ultimate goal of this activity is to provide the “meta rules” according to which the design transformations are carried out and interfaces are built and hence to provide strong guidance to the clusters to make their results more relevant and applicable. Understanding the roles and dynamics of an existing, well-established, vertical industrial segment is a complex task. We could only imagine the complexity of industrial segments that are coming together in these years. While we do target some industrial domain to be the driver for this activity, we understand that our research is going to be more relevant

and better quality if we can distil some common traits of these domains and work with those to choose at a later date which particular chains to address.

The transversal activity hence has two prongs:

- to dive into particular vertical industrial segments and package design methods out of the thematic cluster results for the segments;
- to identify some important common features among verticals and work towards developing methods to address these topics.

We note that the two concerns that are also part of the Transversal JPRAs (**predictability** and **adaptability**) are common to almost all industrial concerns: For this reason, they provide a framework to start the work on integration driven by industrial applications. Predictability has been a goal since the beginning of the modern industry: predicting the capabilities of existing components allows companies to come to market faster with new products and prevents taking dead ends; predicting the effort needed to develop parts of the design and their correct integration prevents early recalls and associated costs. The faster is the dynamics of the industry, the more important is to have predictability in design.

Adaptability is the property of a design to be adapted to changing environments and working conditions. Reconfigurability, programmability, dynamic restructuring are all facets of adaptability. Novel approaches to communication could benefit greatly from adaptability. In fact, much research is being carried out to design devices that could sense available bandwidth and adapt the communication protocol to the most convenient band at the time.

We believe that it will be eventually easier to compose the vertical design industrial flows once these two sub-flows have been examined and results obtained. In addition, being generic concerns they do not require effort from the academic partners to understand the *modus operandi* of entire industrial segments and offer a shorter time to results.

The vertical industrial segment motivated prong will begin *by bringing up-to-speed the largest possible number of participants to the logic of the design chain by organizing workshops for discussion with the participants to the chain.*

We proposed at the onset of the activity to target Automotive, Nomadic and Health Applications as potential vertical segments where we have a range of maturity from well-established (automotive) to emerging (health). At the 2008 meeting in Rome of the ArtistDesign partners, the three vertical markets of interest were identified as:

1. Automotive/avionics since we noted a strong similarity in the overarching issues faced by these two industrial segments that are driven by safety concerns and have to consider distributed implementations;
2. Health applications with particular emphasis on equipment design and manufacturing and a new thrust in the use of emebedded system design methodologies to synthetic biology;
3. Energy efficient buildings, a novel field of great interest to the European Community as well as to the rest of the world as 30% of energy consumption is considered to be in commercial buildings.

These applications address an established area of excellence of European Industry where international competition is fierce, an area of growth where again European Industry has a strong position but where the dynamics are fast and new applications are envisioned in strategic areas such as elderly care, and a new area with great potential where energy

conservation concerns are going to place a great political emphasis. In addition, we believe that synthetic biology is going to have a fundamental role for the foreseeable future in the definition of new organisms to foster the creation of new drugs as well as new materials. Given the nature of this work, the main participants in the cluster are the groups that have industrial vocation such as ESI, OFFIS, and IMEC.

-- Changes wrt Y3 deliverable --

No changes with respect to Y3 except for the new extension to synthetic biology.

1.2 Industrial Sectors

This transversal activity is intended to funnel the results of the thematic clusters and of the other two transversal activities towards industry, thus maximizing the impact of ArtistDesign findings. We expect the impact to be above and beyond the industrial segments identified above (automotive/avionics, health care and energy efficient buildings). In particular, we expect that the nomadic and consumer sectors be also impacted albeit some of the issues typical of these two vertical domains are substantially different from the others.

-- Changes wrt Y3 deliverable --

No changes with respect to Y3.

1.3 Main Research Trends

The advancement of the embedded system research activities in Academia and research institutions has been gaining momentum over the past few years. Some industrial segments, typically avionics and automotive, have been also progressing in the use of tools and methodologies that have improved productivity and design quality albeit the advancements have not been uniform across companies and divisions inside the same company. In particular, *model-driven design* is becoming a standard. In this methodology, the design is captured and analyzed at the functional level with simulation tools and in some limited cases, with formal analysis techniques. The most used flow especially in the avionics/automotive domain is the Simulink Mathworks flow that uses Real Time Workshop (or dSpace, TargetLink) to generate implementation code on the most used single-processor platforms. Other industrial approaches are based on UML and the associated tools provided by IBM (Telelogic and Rational). There has been strong interest in defining UML profiles that are dedicated to real time embedded systems: in particular, SysML is gaining a broad attention. However, in both cases (but more visibly in the UML design flow), the semantics of the design has not been captured well enough to allow for formal analysis. Although domain specific modelling languages are being harmonized with the UML through its profiling mechanism, the wide variety of (non compatible) UML profiles together with a lack of well defined interoperability for the UML (encompassing also profiles and graphical representing) is limiting the industrial applicability. The SPEEDS IP aims at improving substantially the quality of the embedded system design process by providing formal contract-based models that capture not only the functional aspects of the design but also the non functional ones such as power and timing with the Hierarchical Rich Component modelling approach. In this approach, the model can be mapped into the format accepted by advanced academic tools such as BIP so that formal analysis and simulation of the design can be carried out in a rigorous way. To capture the non functional aspects of the design novel timing analysis tools that are commercially available and that have been originally

developed by ArtistDesign partners such as SymTA (Rolf Ernst) and AbsInt (Rheinhard Wilhelm), are being integrated into tool chains comprising model-based design tools, compilers, timing-analysis and schedulability tools. This tool integration will guarantee highest precision and thus avoid the need for over-commissioning. Similar approaches have also been developed in the automotive industry through European and national projects such as ATESST, ATESST2, TIMMO and EDONA. The results from several of these projects are currently being integrated within the CESAR project (http://www.cesarproject.eu/).

We believe that the main issue is not one of modelling and tool usage but one of adopting and enforcing an appropriate methodology that could embrace advanced modelling and could use new generation tools. The aim of the transversal activity is indeed to study and propose to our industrial partners this approach. We do not expect to have an immediate success in having industry adapt the design flows since the tools and approaches are fairly sophisticated and require a quantum leap in the technical background of the designers.

The research trends in this domain is then to identify common layers of abstraction that favor the communication along the supply chain across company boundaries and the design chain inside each company. In addition, industry is pushing towards a better design capture methodology and formal model to allow for stronger verification and validation. In the case of the transportation and military industry, there is increased activity in design for certification. Certification is about design processes and not about the behavior of the artifact. We believe there will be a trend towards making the actual behavior of the artifact be certified which will in turn force companies to adopt rigorous methodologies for modeling and analysis.

Another important research trend to consider is how to accommodate the increased attention to energy efficiency. On October 21st, the US National Science and Technology Council (NSTC) released a report describing R&D activities that could decrease use of natural resources and improve indoor environments while reducing greenhouse gas emissions and other harmful pollutants from the building sector. The report, *Federal R&D Agenda for Net-Zero Energy, High-Performance Green Buildings*, was produced by the NSTC's Buildings Technology Research and Development Subcommittee under the auspices of the Office of Science and Technology Policy (OSTP) in the Executive Office of the President. Commercial and residential buildings consume about one-third of the world's energy. In particular, U.S. buildings account for more than 40 percent of total U.S. energy consumption, including 72 percent of electricity generation. If current trends continue, by 2025, buildings worldwide will be the largest consumer of global energy, consuming as much energy as the transportation and industry sectors combined. Building systems are characterized by uncertain process dynamics; time-varying behavior; multiple objectives (cost functions) that change over time (water usage for evaporative cooling, peak electrical power); and environmental effects (disturbances) such as ambient temperature and humidity, solar radiation, and user behavior. The challenges posed to the research community are large. The actual situation in bulding management is worrisome. The level of sophistication of building managers, of commissioning personnel and of building management companies is very low. Simple minded control laws are implemented on information systems that are under dimensioned with respect to the needs of a comprehensive design approach. The research agenda here is to tie together the various aspects of building management, e;g., Heating, Ventilation and Air Conditions (HVAC), lighting and safety (fire and intrusion alarms, egress systems) into an integrated monitoring and control system. This action must include research on hierarchical multi-objective control, distributed system design, sensor and actuator selection and positioning. The systems must be adaptive, predictable and fault tolerant. The research agenda in the design and operation of energy efficient buildings is fully consistent with the thematic clusters and with the transversal integration activities. The role of industry here is very relevant as the important aspects to take into consideration when developing algorithms and methodology cut across multiple domains and company boundaries. The industrial landscape is moving at an interesting pace: players are repositioning to take advantage of the concerns dictated by the political climate on energy

issues. For example, equipment companies are now setting up new system divisions to address the integration problems. This situation offers this transversal activity a unique opportunity to influence the way industry is looking at the problem. There is a new term being used in the research community interested in this area: systems of systems, meaning that the level of integration needed here is one or more levels above what has been done today in other industrial sectors such as automotive. In the 2010 GREEMBED Workshop, the activities in energy efficiency by the leading industrial concerns and by selected academic groups were reviewed and potential for future collaboration identified. The Workshop was a follow on of the activity of SEEC 2009 that was considered to be a success by the participants where we had a strong mandate to continue organizing similar workshops in the future.

Synthetic biology is a dynamic, innovative and highly promising blend of science and engineering which aims to construct novel biological entities and to redesign existing ones. It is a new field, but one that has already stimulated substantial discussion regarding its technical possibilities, its role in addressing global challenges, and its use in increasing our understanding of biology. New applications may be found in medicine, energy, environment and materials. Synthetic biology also aims to increase our understanding of biological systems; in particular, it may offer an approach to managing their complexity. Indeed, Synthetic Biology offers *the possibility of developing novel biological functions and tools by modifying or integrating well-characterized biological components into higher-order systems using mathematical modeling to direct the construction towards the desired end product*[1]. This approach is squarely in the domain of interest of ArtistDesign and extends ArtistDesign reach to new communities that are gaining tremendous popularity both in Academia and industry.

In 2010 a report on opportunities and challenges for Synthetic Biology[2] was published under the auspices of the National Academie, OECD and the Royal Society. ‘’[The main findings of the report are]:

- It is crucial to invest in underpinning technologies, science, education and policy in order to ensure the safe and efficient development of synthetic biology. Investments in automated technologies such as DNA synthesisers and combinatorial technologies are important to enhance research and optimise the use of researchers’ time. Rewarding and publishing advances in synthetic biology would also be a strong stimulus for the field.
- ***The gap between applications and tools and techniques must be bridged. This calls for investments to develop tools and techniques***.
- The degree to which experience and knowledge gained from other emerging technologies are being drawn upon and used is not clear.
- Issues raised during the symposium that would benefit from further investigation and, in some cases, policy interventions at multiple levels, include:
  - *Standardisation, for example of biological parts;*
  - *The shaping of an intellectual property model;*
  - *International collaboration and co-operation in the regulation and governance of synthetic biology, as well as scientific and technical development.*

[1] Jay Keasling, Building life from the ground up, Keynote presentation, *World Congress on Industrial Biotechnology and Bioprocessing*, March 2007.

[2] SYMPOSIUM ON OPPORTUNITIES AND CHALLENGES IN THE EMERGING FIELD OF SYNTHETIC BIOLOGY: Synthesis Report, copyright of the NAS, OECD, and RS, May 2010.

- Opportunities for public debate and discussion of synthetic biology need to be created. Part of the challenge will be to develop a common, widely understood language for discussing ethical and social, as well as technical aspects of synthetic biology. The public should be involved in a healthy and open dialogue. What is needed is real dialogue and engagement with the public rather than a simple communication strategy.
- Communication between the many stakeholders involved in novel technologies and science depends on a variety of complex factors and is context-dependent.''

The paragraph in bold points out once more how important is the development of methodologies and tools and mathematical models to advance the state of the art. We venture to say that the Artist Design Community is the appropriate group to help in this endeavour.

-- Changes wrt Y3 deliverable --

The topics of energy efficiency, cyber-physical systems and synthetic biology are coming rapidly to the center stage of the international research agenda and this is reflected in the activity that we have chosen to invest on.

2. State of the Integration in Europe

2.1 Brief State of the Art

As in the other transversal activities, it is almost impossible to provide a BRIEF state of the art of integration in Europe since this activity involves many different aspects in many different industrial segments. This transversal activity not only feeds from the thematic clusters but also from the other two transversal activities. Hence, the state of the art in each of the thematic clusters and transversal activities are propedeutic to this section and will not be repeated here.

In general, research activities tend to focus on specific problems and to develop techniques that are aimed at solving well defined aspects of these problems. This transversal activity is about integration at the industrial segment level transcending companies' boundaries and actually helping to integrate better the activities across the supply chain. In addition, the activity aims at providing inputs to the ArtistDesign community on how to interface methods and tools so that an overall methodology can be assembled. Today, integration at this level is vigorously pursued in Europe in some industrial segments (most notably the automotive domain) but it still needs years to come up with an agreed upon solution. In the energy efficient building domain achieving integration even inside single company boundaries is a difficult proposition. The potential impact of a research aimed at developing this overarching vision cannot be overemphasized. The objective is ambitious and it needs attention at the community level: a single research group does not have the breadth or the muscles to develop this vision.

The automotive industrial segment with the Autosar initiative has an important message about the integration of the design chain and advocates the adoption of standards in interfaces and operating systems. We actually believe that much more work needs to be done at the semantics level and at the non functional aspects of design. The work carried out in SPEEDS is an example of how to address these problems not only in the automotive domain but also in the avionics domain albeit limited to higher levels of abstraction. The CESAR Artemis project is about taking the work of SPEEDS to a new level of sophistication and to extend its reach to implementation issues. The large participation of industrial concerns in CESAR and SPEEDS that involve OEMs, Tier 1 suppliers and tool providers bodes well for the activity of this transversal activity.

The solidification of the Artemis JTI has been instrumental in driving the industrial interest in embedded systems. In particular, as quoted by the Artemis Web-site: "*The European Union recognises the strategic importance of Embedded Computing Systems and has launched the Artemis Joint Technology Initiative (JTI). The ARTEMIS JTI is implemented as a Joint Undertaking (JU) which is a public-private partnership between:*

- *The European Commission*
- *Member States*
- *ARTEMISIA, a non-profit Industrial Association*

ARTEMISIA is the ARTEMIS Industrial Association which represents the research commmunity including Industry (large, small and medium sized companies), universities and research institutes. The ARTEMIS JU is an organisation based in Brussels that was legally established in February 2008 and it is managed by an Executive Director."

Hence the links of the ArtistDesign community to Artemis and Artemisia are of paramount importance for the development of the deliverables of the Industrial Integration Transversal Activity. In particular, the steering Board of Artemisia counts three of the ArtistDesign Partners (Joseph Sifakis (CEA), Luca Benini (U. Bologna) and Rudi Lauwereins (IMEC)) among the 5 research representatives. Alberto Sangiovanni Vincentelli is a member of the Public Authority

Board and the Governing Board of Artemis and he was a member of the expert panel (7 members) for the ''First interim evaluation of the ARTEMIS and ENIAC Joint Technology Initiatives'' released in December 2010. We expect the ties with Artemis and Artemisia to grow stronger in the future

The German competence cluster SafeTRANS (Safety in Transportation Systems,) including ArtistDesign members TU Braunschweig and OFFIS, concentrates research and development expertise in Germany in the area of the design of complex embedded systems for transport systems, to develop in cooperation with leading companies in the transport industry methodologies and processes for the development of safety critical embedded systems within the framework of a mutual research strategy. SafeTRANS and the French Pôles de Compétitivité SYSTEM@TIC-PARIS-REGION and Aerospace Valley allied to form the European institute EICOSE (European Institute for Complex and Safety Critical Embedded Systems Engineering). In the meantime EICOSE has become the first »Innovation Cluster« within the technology platform ARTEMIS.

In September 2008, the new KTH Centre in Embedded systems - ICES, joining forces from several research groups at KTH and industry (ABB, Enea, Ericsson, Scania, Stoneridge and ÅF) was founded. Key goals of the centre include acting as a catalyst for improved interactions between academia and industry, and between the member companies. The centre has a focus on embedded systems engineering and science, emphasizing system design, architecture and methodology. For this reason, KTH has been added to the core team for the Transversal Activity. During 2011 the networking activities of ICES have continued with a number of successful industrial events and a main conference on Sept. 1st. ICES roles as a catalyst has worked well and in 2011 manifested itself in several ways:

- Several new partners joined the ICES network including Atlas Copco and Maquet.
- The autumn 2011 a new masters program in embedded systems started at KTH. This program was initiated by ICES industrial members and four of the schools at KTH. The program was very successful in recruiting students and features selected courses provided by the different schools at KTH. It will be interesting to see how the program can evolve. The industrial partners are very keen in supporting the program.
- During 2011 so called thematic groups were launched with the idea to stimulate interactions between industrial and academic experts in different fields. Two of the first groups to kick off include an "architectural team"[3] and a group on safety and reliability. The first meetings were very positive and we believe that this form of meetings can yield various types of spin-offs: white papers and research projects are being discussed.

In May 2006, the European Embedded Control Institute was created in the framework of the HYCON Network of Excellence (FP6-IST-511368). EECI has the intent to:

- Become a long-term world-wide renowned focal point by stimulating new collaborative (multi-national and multi-disciplinary) research on networked and embedded control,
- Break down the barriers between the traditional disciplines,
- Be a motor for the dissemination of methods and tools,
- Promote the education of students and researchers
- Encourage the transfer of methodologies to industry,

[3]http://www.kth.se/itm/centra/ices/previous-events/ices-workshop-autonomous-systems-the-architectural-perspective-1.198374?l=en_UK

- Seek financial support from both industry (through industrial projects and teaching) and European and national research foundations

EECI is member of ARTEMISIA B Chamber. Its participants formed the HYCON2 NOE that was approved in April 2010. The charter of HYCON2 is to stimulate and establish the long-term integration of the European research community, leading institutions and industry in the strategic field of control of complex, large-scale, and networked dynamical systems. Several members of the ArtistDesign NOE are also members of the HYCON2 NOE (e.g., INRIA, Trento, ETH, and Lund).

Recently the EU launched a research initiative in the area of Systems of Systems (SoS). This domain is clearly of great industrial interest encompassing important topics such as smart cities, traffic and water management, air traffic control, UAVs and large scale environment control. The Smarter Planet initiative by IBM is squarely in the core of this domain. SoS have been investigated for years especially in the US for defense applications but with little science foundations. The concepts developed by the traditional SoS community are mostly heuristics and have not touched the hard core problems involving independent agent integration and coordination. We believe that the rigorous approach fostered by ArtistDesign can have a great impact in this domain. Several participants of Artist Design (Trento, Offis, and INRIA with their industrial partners, such as ALES, IBM, IAI and EADS) have teamed to try to bring a formal analysis approach to the domain with the DANSE IP. We do hope that the activities of the Artist Design partners in the DANSE IP will advance the state of the art and contribute to make SoS a research and industrial success.

-- Changes wrt Y3 deliverable --

No changes with respect to Y3.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

This transversal activity is intrinsically about integration. Integration is across the various partners who are active in it as well as across the different thematic clusters and other transversal activities. Since our aim is about integration of other groups in ArtistDesign we are depending on the delivery of their findings to build an effective approach to the design integration across industrial segments. We also aim at integrating our work with the work in other industrial and academic communities. The interaction with US companies and research organizations is documented in the activity report about the Forum on CyberPhysical Systems where industry, academia, and government agencies came together to discuss how to approach the new generation challenges posed by the closer interaction between the physical world and computing. Also the topical event in Trento (SEEC09) saw the participation of companies that are not (yet) in the ArtistDesign community as well as US companies who are interested in exchanging notes and results with our community. The green energy and intelligent building work continued with the GreenEmbed Workshop held during CPS Week and with the Trento School held in the summer of 2011.

The industrial integration activity is intented to last beyond the period in which ArtistDesign will be funded. It does have important links with large European projects (IP EU projects SPEEDS and DANSE, and Artemis project CESAR) and with industry independently. Partners OFFIS, ESI, IMEC and Trento are directly connected with industry in deep ways. They provided the backbone of the activity of industrial integration during the years.

-- Changes wrt Y3 deliverable --

No changes with respect to Y3.

2.3 Other Research Teams

The main teams in Europe who are active in industrial flows are all included in ArtistDesign. Of course, the teams do not cover all industrial domains with the same intensity as automotive. The historical Artist group had had their main focus placed on embedded software. In ArtistDesign the periphery has been augmented to include some teams that have architecture, SoC and control expertise that are a necessary complement to the core strength to address the industrial integration issues. Connections to the HYCON NoE (http://www.ist-hycon.org/) were present via PARADES who coordinated the industrial integration of this NoE. However, people involved in industrial integration activities based on control such ETH's Morari and Lygeros are not present in ArtistDesign. HYCON ended its operation last year and in 2010 it has been transformed into HYCON2 with similar group of partners and in particular, with University of Trento, Lund and INRIA who are among the core partners of the ArtistDesign NOE. We do have strong relations with Manfred Morari and John Lygeros of ETH, and with Maria Domenica Di Benedetto, President of EECI, member of HYCON II, and Director of the Center of Excellence, DEWS, University of L'Aquila, who were instrumental in defining the directions of HYCON2 towards the next generation distributed architecture for control applications including wireless sensor networks and we have leveraged this contact.

The communication field is a main focus of parallel groups in the US especially in the area of military applications sponsored by DARPA (e.g., UCLA (Estrin), Berkeley (Culler, Pister, Rabaey), Washington (Borriello)). In Europe, research in wireless sensor networks and their applications is carried out in several academic and industrial research groups. In particular, University of L'Aquila (DEWS), Politecnico di Torino and TU Berlin.

Research groups in the US that work on the issue of industrial integration among others are CHESS (Berkeley), GSRC (multi-university program sponsored by the Semiconductor Industry Association and DARPA), MUSYC (MultiScale System Center, a new MARCO Focus Research Center Program headquartered in Berkeley) and ISIS (Vanderbilt). Teams at CMU have strong industrial program that culminated with the victory of the DARPA Urban Challenge of the GM-CMU team. The double appointment of Alberto Sangiovanni Vincentelli with Berkeley offers an opportunity to link tightly with these groups. In addition, the COMBEST project whose partners are for the large part participating to ArtistDesign has an international collaboration also at the industrial level (for example, UTC, GM, Intel, National Instruments, Mathworks, and Cadence) so that proficuous interactions are guaranteed.

As far as Synthetic Biology is concerned, we note that his field has already made some significant contributions to the need to meet global challenges. The best known is the synthesis of artemisinic acid in E. coli and yeast. Artemisinic acid is needed for artemisinin, the most effective known anti-malarial drug. However, this achievement also represents the high-water mark of metabolic engineering. Relying on the tools of biotechnology and genetic engineering which changed little in three decades, this effort took several years and USD 25 million. We argue that the development of tools such as the ones presented below in collaboration with Boston University and the University of California at Berkeley will help in making the achievement of results that are relevant to industry less expensive and more rapid. The European Union (EU) funds synthetic biology research through its Framework Programmes and specific initiatives. The latter include the New and Emerging Science and Technology programme, which provided early-stage funding for 18 synthetic biology research and policy projects, and Towards a European Strategy for Synthetic Biology (TESSY), which developed a research roadmap for Europe.

-- Changes wrt Y3 deliverable --

The HYCON NOE has ended its operation and has been replaced by HYCON2 NOE that is in close contact with us. Further, Synthetic Biology design using methods and tools developed by the ArtistDesing community has been added to the interests of the NOE.

2.4 Interaction and Building Excellence between Partners

The core groups are internationally renowned in their area of industrial interest. A change with respect to the original proposal occurred in January 2009 when PARADES withdrew from the ArtistDesign Consortium and it has been replaced by Trento. Alberto Sangiovanni Vincentelli transitioned from the PARADES to the Trento team to provide the continuity in the management of the JPRA.

All have multiple industrial segment contacts (transportation, IC, printing, health care, entertainment, consumer, nomadic, security, buildings). They act as agents of change and of spread of excellence in the ArtistDesign community with respect to relation with industry. The interactions with the other clusters and transversal activities are at their inception. Since we selected the final focus area recently, we expect to engage the cluster partners with additional impetus. The active collaboration within this project has also led to the identification of common problems and goals between the partners and national and European companies. This leads to new joint undertakings e.g. within the Artemis framework.

- Changes wrt Y3 deliverable --

No changes with respect to Y3.

2.5 Interaction of the Transversal Activity with Other Communities

The partners for this activity are the majority of the partners in ArtistDesign. Their interactions with the communities are massive. Most of these interactions have been documented in the reports for the other sections. However, we would like to stress here the connection with HYCON that has not been reported elsewhere. The research communities that are connected with this activity include artificial intelligence, high-performance computing, wireless sensor networks, building optimization, IC design, and mechanical engineering. We are connected to UC Berkeley, Boston University, CMU, UCLA, Vanderbilt, University of Pennsylvania, Columbia University, Cadence, General Motors, Xilinx, Qualcomm, UTC and Stevens Institute in the US. In Asia, we are connected with Kyushu University, Hitachi, Toshiba, Panasonic, Samsung and Centre for Embedded Software Technology (CEST).

-- Changes wrt Y3 deliverable --

No changes with respect to Y3.

3. Summary of Activity Progress

3.1 Technical Achievements

The technical achievements are collected under a number of subheadings reflecting the nature of the contribution and the industrial sector being impacted: General Frameworks for system-level design; Applications to the Automotive Sector; Applications to Chip Design; Applications to Buildings; Applications to Wireless communication technology; Timing Analysis and Predictability; Other Applications.

3.1.1 General Frameworks for System Level Design

Platform-Based Design and Frameworks

Participants: Cadence, Trento, UC Berkeley, Sun Microsystems, UTC, National Instruments and Intel.

System-Level Design (SLD) means many different things to many different people. In our view, system-level design is about the design of a whole that consists of several components where specifications are given in terms of functionality with additional:

- constraints on the properties the design has to satisfy and on the components that are available for implementation and
- objective functions that express the desirable features of the design when completed.

This definition is general since it relates to many different application domains, from semiconductors to systems such as cars and airplanes, buildings, telecommunication and biological systems. To deal with system-level problems, our view is that the issue to address is not developing new tools, albeit they are essential to advance the state of the art in design, rather it is the understanding of the principles of system design, the necessary change to design methodologies and the dynamics of the supply chain. Developing this understanding is necessary to define a sound approach to the needs of the system and component industry as they try to serve their customers better, to develop their products faster and with higher quality. This contribution was about principles and how a unified methodology together with a supporting software framework, as challenging as it may seem, can be developed to bring the embedded electronics industry to a new level of efficiency. To demonstrate this view, we presented a number of papers on the challenges in design for the system of the future and a manifesto for the need of a unified methodology. We then addressed a methodology, Platform-Based Design (PBD), that has been developed over the past decade and that we believe can fulfil the needs. We are addressing three test cases in diverse domains: semiconductor chips (a UMTS single-chip design), energy efficient buildings (an indoor air quality control system) and synthetic biology.

Cyber-Physical System Challenges and Opportunities

Participants: Trento, UC Berkeley, Bosch, General Motors, National Instruments,Thales, and Toyota, UTC

Cyber–physical systems (CPSs) are integrations of computation and physical processes. Embedded computers and networks monitor and control the physical processes, usually with feedback loops where physical processes affect computations and vice versa. The design of such systems, therefore, requires understanding the joint dynamics of computers, software, networks, and physical processes. It is this study of joint dynamics that sets this discipline

apart. When studying CPS, certain key problems emerge that are rare in so-called general-purpose computing. For example, in general-purpose software, the time it takes to perform a task is an issue of performance, not correctness. It is not incorrect to take longer to perform a task. It is merely less convenient and therefore less valuable. In CPS, the time it takes to perform a task may be critical to correct functioning of the system. In CPS, moreover, many things happen at once. Physical processes are compositions of many things occurring at the same time, unlike software processes, which are deeply rooted in sequential steps. Abelson and Sussman describe computer science as *procedural epistemology*, knowledge through procedure. In the physical world, by contrast, processes are rarely procedural. Physical processes are compositions of many parallel processes. Measuring and controlling the dynamics of these processes by orchestrating actions that influence the processes are the main tasks of embedded systems. Consequently, concurrency is intrinsic in CPS. Many of the technical challenges in designing and analyzing embedded software stem from the need to bridge an inherently sequential semantics with an intrinsically concurrent physical world.

The goal of [DLSV11] is to highlight progress that has been made, but mostly still not yet adopted by the community, on an enormously difficult and complex problem, the design of CPSs. The major theme of [DLSV11] is on models and their relationship to realizations of CPSs. The models we study are primarily about dynamics, the evolution of a system state in time. We do not address structural models, which represent static information about the construction of a system, although these too are important to system design. Working with models has a major advantage. Models can have formal properties. We can say definitive things about models. For example, we can assert that a model is deterministic, meaning that given the same inputs it will always produce the same outputs. No such absolute assertion is possible with any physical realization of a system. If our model is a good abstraction of the physical system (here, *good abstraction* means that it omits only inessential details), then the definitive assertion about the model gives us confidence in the physical realization. Such confidence is hugely valuable, particularly for embedded systems where malfunctions can threaten human lives. Studying models of systems gives us insight into how those systems will behave in the physical world.

Embedded systems challenges and focus areas

Participants: KTH, ABB, Scania, Ericsson, ÅF, Enea, Stoneridge

During its first year of operation, the KTH Innovative Centre for Embedded Systems (ICES) has directed an effort to define the key focus of its activities. The Embedded systems area is wide, and there are also many possible activities which could be pursued by an embedded systems centre (ranging from continued education to research). In this first ICES Vision and Goals document, key challenges as perceived by the participating industries (telecom, automotive and automation) and related scientific challenges are discussed. The guiding vision for ICES is established in the document: To achieve a flourishing eco-system for industry and academia excelling in embedded systems education, research and innovation. To reach this vision, ICES adopts the role of networker and catalyst with industry, KTH students and KTH faculty as the main stakeholders. The focal technical areas to be addressed by ICES are embedded systems architecture, software, verification and methodology. The Vision and goals document also defines concrete goals and activities for ICES the forthcoming years.

Heterogeneous Composition

Participants: Trento, IST-Austria, UC Berkeley, UTRC

We have addressed the problem of heterogeneous composition from a theoretical point of view, starting from a collaboration with UC Berkeley and later extending it to UTRC to get a better grasp of the actual issues faced by designers when connecting different models of

computation. One of the main results of this research is our belief that heterogeneous composition is relative, and depends on the final outcome that the designer wants to achieve. We have proceeded by focusing on the main principles of platform-based design: the models to be connected should strictly maintain their identity in order to 1) preserve their properties that typically lead to efficient analysis methods, and 2) be reusable in different contexts and with other models of interaction. At the same time, to enact any kind of interaction, the models must come together in a domain, which we have called the *common semantic domain*. The common semantic domain, however, as a common refinement, is unable to preserve identity, and serves the sole purpose of describing the kind of desired interaction. The actual interaction, instead, takes place in a mixed domain, where each model can be embedded separately, and provides a way of describing model adapters. These principles have been applied to an example provided by UTRC (by Alessandro Pinto), and realized both in the SystemC language, and in Metro II, showcasing different kinds of interfaces between data flow and finite state models.

Systems-of-Systems

Participants: Trento, Loughborough University, IBM, IAI, ALES, INRIA, OFFIS, Carmeq, EADS, Sodius, Honourcode

The term System of Systems (SoS) in its more basic form describes a collection of components that are themselves systems designed to achieve a common goal. Based on this 'fractal' description, we can imagine that a component system is itself a SoS until we reach a level of abstraction that one considers the basis of the construction. While this is a conceptually interesting view, it is too generic to convey the importance of the problems addressed and the potential offered by a SoS. In particular, the differentiating factor is the designer's intent for the components versus the whole. The concept of SoS dates back to the early 1970's within the US defense industry community where the idea of an unmanned battlefield was, and still is, of paramount importance. In this domain, the battlefield is typically populated by a number of intelligent devices (autonomous aerial and terrestrial vehicles communicating wirelessly among themselves and with humans geographically distant from the battlefield itself). These devices are managed and coordinated to achieve a common goal and can appear on the scene and (willingly or unwillingly), leave it at any time and in any order.

The most well-known modeling work in SoS is currently undertaken by the US Department of Defense (DoD and UK Ministry of Defence (MOD) through their architectural frameworks - Department of Defense Architecture Framework (DoDAF) and the Ministry of Defence Architecture Framework (MODAF) respectively. These have since been unified in the OMG 2005 Unified Profile for DoDAF/MODAF [1], and are UML profiles specifically intended for capturing most of the important aspects of SoS mainly for military applications. Since then, the SoS domain of interest has gained attention from the research and industrial community, and has today reached a dominant level where the potential of SoS to address civil applications can be comprehended. In this respect, the IBM Smarter Planet initiative[4] is a perfect example of the potential reach of the technology: "*At IBM, we want that intelligence to be infused into the systems and processes that make the world work—into things no one would recognize as computers: cars, appliances, roadways, power grids, clothes, even natural systems such as agriculture and waterways*." To be able to fulfill this vision, many fundamental problems have to be solved to prevent potentially catastrophic outcomes of systems that are so complex to be hardly manageable.

The topic is of clear strategic importance as documented in the EU report of the SoS workshop [2] held in 2009. However, the state-of-the-art in SoS is less than satisfactory including the lack of precise definitions, of specific theories and tools. Indeed, the approaches quoted above are

[4] http://www.ibm.com/smarterplanet/us/en/?ca=v_smarterplanet

intended to provide standards for structural modeling of SoS. As such, they do not offer support for simulation or formal analysis of the systems being modeled. Because of the obvious complexity of SoS, the design of these systems is extremely difficult and must be supported by a semantically sound modeling approach, and a number of tools including analysis and synthesis. In contrast, however, it is often discovered that precise modeling of a SoS cannot keep abreast of the actual changes occurring in the SoS. This conflict requires new paradigms for modeling and for systems engineering.

In [KSV11] we intend to raise the consciousness of the research and industrial communities about SoS that, given the vagueness that surrounds them, is often low. The paper addresses the characteristics that make SoS design challenging and offers a research roadmap as outlined in the research programme ('Designing for Adaptability and evolutioN in System of systems Engineering (DANSE)') funded by the European Commission.

Support for capturing design rationales

Participant: ESI

The design framework integrates storage of design reasoning with the design artefacts and models. In the reporting period the Design Framework was extended, first evaluation results were received and dissemination of the framework was started. The design framework is intended to support system architects in industry in their development process. It will support the capturing design rationales, enable conflict detection, and helps to get an overview on models developed during a design trajectory. The design framework is developed as part of WP 5 of the FP7 Multiform project, for which ESI is WP-leader.

In order to validate whether the tool and its concepts do support them, an observational study was conducted in an architectural team at Vanderlande. For 2 months ESI has participated in their meetings and mapped the discussions, reasoning, design decisions, modeling activities, etcetera on the design framework concepts. This resulted in a better structuring of the development process, along with a number of high level performance models for candidate system designs that were used by Vanderlande as input to take decisions in the development process.

Another action was to disseminate the Design Framework amongst ESI partners in the Dutch Embedded Systems Industry. A workshop was organized, in which (domain) architects of ASML, FEI Company, Océ Technologies, Philips Healthcare and Vanderlande Industries as well as researchers from Twente University participated.

3.1.2 Automotive Applications

Autonomous automotive applications – The grand cooperative driving challenge

Participants: KTH, Scania and Volvo car

The Scoop project was a joint effort between Scania CV AB and KTH Royal Institute of Technology. The intention of the project was to participate in the Grand Cooperative Driving Challenge (GCDC) in May 2011. The GCDC is an international challenge in the field of cooperative driving, organized by TNO of the Netherlands[5]. Each team participated with a vehicle, which was part of a moving platoon of vehicles. The platoon moved through urban city and highway driving scenarios. Within the platoon, motion of the vehicles was autonomous.

[5] GCDC 2011 Rules and Technology Document:
http://www.gcdc.net/mainmenu/Home/technology/Rules_and_Technology

The autonomous motion took advantage of communication between the vehicles comprising the platoon and special roadside infrastructure.

The Scoop team participated with a Scania R730 series tractor unit. KTH and Scania collaborated closely in the system development – in which an external platooning control system was added and integrated with the Scania automotive embedded systems. Only one minor change was required within the truck. KTH researchers in particular contributed to requirements, control and architecture design, and system verification. The competition was very successful. The KTH/Scania team ended up in 4th place (first of the trucks in the competition). The other Swedish teams with Volvo car also did well. Conference and Journal publications have recently been submitted with reference to this achievement.

Model based engineering of automotive embedded systems, beyond Autosar

Participants: KTH, CEA, Volvo, CFR, TUB, Continental, Mentor, Univ. Hull, Mecel

As part of the FP7 Maenad project (a follow up of the ATESST2 project), specific emphasis is placed on maturing the EAST-ADL architecture description language and further enhancing its support for verification and safety. A special investigation has also been conducted to extend the EAST-ADL methodology for the engineering of Fully Electrical Vehicles, FEVs. An initial activity was therefore the definition of user needs in the engineering processes starting from the concept phase. The technical issues related to FEVs during their development have been identified, in order to address especially those that are EV specific. Examples are high voltage, insulation, battery charging, integration with conventional vehicle systems, communication with the infrastructure, new propulsion and energy storage technologies.

The EAST-ADL language is developed by different projects and stakeholders over time. To synchronize further refinement of the language and provide an entry point for EAST-ADL information, an organization has been discussed for some time. September 1st, the **EAST-ADL association** was formed.

The EAST-ADL Association is a non-profit, non-governmental organization with the aim of assisting and promoting the development and application of the EAST-ADL.

The EAST-ADL Association will stipulate the content of new versions of the EAST-ADL language. This will be done through collaboration between the members of the association and within projects and organizations working with EAST-ADL.

Membership in the EAST-ADL Association is open to individuals and organizations who agree to support the purpose of the association. The EAST-ADL Association has no fees or funds, and each member carry any costs for contributing. The initial set of members includes companies and individuals from OEMs, suppliers, tool vendors and research organizations developing EAST-ADL. If you are interested to join the association, please contact info@east-adl.info

System-level architecture exploration for embedded systems

Participants: KTH, Airbus, EADS, CNRS and other partners in the CESAR project

Architecture design concerns the definition of the fundamental organization of a system. The word “fundamental” derives from the fact that this system organization determines key system properties, such as performance and cost. As part of the CESAR project, KTH with other academic and industrial are working a system level design methodology encompassing principles, methods and tooling recommendations. The work has been challenging in trying to reconcile different expectations and industrial scenarios. Key issues of the investigation have included trade-off analysis; encompassing various types of constraints and new as well as product-line based designs. An industrial case study from Airbus is being used to exemplify

and validate the work. The work is currently converging and is being documented as part of a CESAR deliverable and as one dedicated chapter in the “CESAR book” which is due in the spring 2012.

Methods and tools for the timing analysis of automotive systems

Participants: TU Brauschweig, GM

The follow up R&D projects which started in 2010 between iTUBS and GM for further exploitation of the COMBEST results have been finished in 2011 to the complete satisfaction of both partners. The focus of these projects was on the development of methods and tools for the analysis (i) of Ethernet based architectures and (ii) of multi-core platforms. Some of the results were submitted to DATE 2012 [RGE12] and have been accepted for publication.

Participants TU Braunschweig, Daimler AG

New R&D projects between iTUBS and Daimler AG have been initialized to investigate the applicability and the performance (i.e. how useful are the obtainable results) of compositional system level timing analysis when applied to current and future automotive E/E architectures. In this context, two problems of the existing formal approach have been identified. First, for the dynamic segment of FlexRay as it is used in some of the investigated automotive use cases, no suitable analysis exists, making systems containing such components not analyzable. Second, when the compositional analysis was applicable, the obtained system level results, i.e. end-to-end latencies, often overestimated the timing behavior of the real system by such a large amount that the results were deemed unusable by Daimler. Therefore, we developed a new response time analysis for the dynamic segment of FlexRay covering the most recent FlexRay specification and an improved end-to-end latency analysis technique. The results of this cooperation are currently under submission.

Network analysis techniques and multi-core analysis techniques

Participants: TU Brauschweig, Toyota Information Technology Center (T-ITC), Symtavision

The process of industrial integration has been advanced successfully. Feasibility of reliability analysis for real-world systems could be demonstrated based on different CAN bus examples provided by Toyota-ITC. In this context analysis performance could be improved by orders of magnitude compared to former implementations used for internal research purposes only.

Especially the adjustable analysis granularity has been pointed out as an effective measure to accelerate reliability analysis. In this context nearly no loss of accuracy could be detected. Granularity is adapted automatically during analysis, such that reliability analysis is basically executed with an optimal accuracy-performance tradeoff. Most of the algorithmic improvements have been implemented within a prototype plugin for SymTA/S, which is going to be evaluated by our industrial partners by now.

A joint publication together with Symtavision summarizing the results on reliability and safety analysis for CAN buses and multi-core over the last years has been presented at the SAE World Congress 2011 [SAEFJ11]. Results of former research activities on error models and the effect of error correlations on reliability have been published on [PRDC 2011].

Participants: TU Braunschweig, TU Dresden

In collaboration with TU Dresden we designed novel fault-tolerance hardware and software features targeting at the Fiasco L4 Microkernel. This comprises application level redundancy and task restart/rollback on software level as well as a fingerprint based hardware voting mechanism which was also implemented on a FPGA demonstrator.

The timing effects of redundancy and re-execution of embedded real-time software were modeled and analyzed using techniques known from compositional performance analysis. Results have been published at ESWEEK 2011 [ASE11].

Supporting Standardized Software Architectures in Automotive and Aeronautics

Participants: USAAR, AbsInt, SSSA, Airbus, Bosch
The automotive and the aeronautics domains see similar trends from federated to integrated architectures, namely the AUTOSAR and the IMA architectures. Both software architectures select fixed-priority preemptive scheduling for task multithreading. This requires new methods for timing analysis, based on sound and precise estimation of context-switch costs. The delicate part ist he estimation oft he costs caused by additional cache reloads. USAAR together with AbsInt have developed methods to estimate the cache-related preemption delay. This have been taken up in the course oft he PREDATOR project by SSSA in a newly developed schedulability analysis.

3.1.3 Applications to Chip Design

Methods, Tools, and Platforms for cost-efficient certification of safety-critical multicore systems

Participants: TU Braunschweig, Intel, Infineon, Sysgo, Elektrobit, EADS IW, Delphi, TÜV Nord, Thales and others

RECOMP is an ongoing project proposal submitted in response to the second call for proposals of the European JU Artemis. The goal of RECOMP is to develop methods, tools and platforms for enabling cost-efficient certification and re-certification of safety-critical multi-core systems, with special emphasis on the design of mixed-criticality systems. Additionally the integration of the developed techniques should be integrated into certification processes for different domains such as avionics, automotive or industrial automation.

RECOMP is now in its second year. First-year deliverables have laid the foundations with respect to available HW/SW mechanisms for mixed-critical systems [ADNSSE11] in the areas of isolation/virtualization, core-to-core communication and monitoring as well as verification and validation methodologies. Based on these, concepts for architectures have been developed which are currently being implemented. TU Braunschweig focuses on the development of an Integrated Dependable Architecture for Manycores (IDAMC), which represents a research manycore platform with mechanisms for isolation/virtualization and monitoring. This platform is centered around a network-on-chip, which implements most of the mechanisms. RECOMP also includes the analysis of the timing and reliability properties of the platform [DRNSE11, SAEFJ11, ASE11]. We have active cooperations with Thales and EADS which plan to use the IDAMC network-on-chip in their own architectures. TU Braunschweig organizes a Tutorial on the RECOMP results at DATE 2012.

Timing Analysis for Complex Execution Platforms

Participants: USAAR, AbsInt,

Some architectural features make timing analysis particularly difficult. USAAR together with AbsInt has developed analyses and considered the timing predictability issues for such features, e.g. the branch-target buffer.

Cache Analysis for non-LRU Cache Architectures

Participants: USAAR, AbsInt,

More or less all publications about static cache analysis concern caches with LRU replacement. These are expensive in logic and energy consumption. Architects therefore prefer replacement policies such as FIFO or PLRU. No genuine static cache analyses existed until recently.

USAAR has developed such genuine static cache analyses, which are now implemented in the timing analysis tool aiT of AbsInt.

Performance analysis of synchronous models implementations on loosely time-triggered architectures

Participants: UC Berkeley, Trento, General Motors

Synchronous (reactive) models of computation (SR) are the foundation of several modeling and analysis tools to describe and validate systems functionality, including Simulink and SCADE. SR models are popular because of a strong theoretical backing that allows predictability and formal verification of properties. However, the preservation of the formal properties of SR models and therefore of the verification results require a formally correct implementation, which is typically obtained using clock synchronization in a time-triggered architecture. A time-triggered framework may be difficult to achieve, especially on distributed wireless networked systems or when functionality needs to be deployed on an existing platform. Therefore, it is important to investigate what are the conditions and the performance for the implementation of a synchronous model into a less constrained architecture, such as the Loosely Time-Triggered Architecture (LTTA). An LTTA architecture is a distributed architecture in which node clocks are assumed to be loosely synchronized (to be compliant with some types of global contract), the communication bus is reliable and delivers messages with a bounded worstcase delay. The architecture nodes provide basic task activation mechanisms and a communication mechanism called Communication by Sampling (CbS). In 2010, we implemented a generic network of SR machines by a network of processes communicating through bounded FIFO queues regardless of the activation times of the Finite FIFO Platform (FFP) processes to preserve the communication flows. A synchronous model consists of a graph of communicating (possibly infinite-state) Mealy machines. All machines receive streams of data (signals) as input(s) and produce output signals. For simplicity, we assume all the machines at the nodes of the graph perform their computations synchronously and at the same rate, triggered by events coming from a global (logical) clock. The edges in the graph represent the signals communicated from one machine to the other. To allow for a well-formed composition, we assume there is at least one delay element in every loop.

Figure 1. From a synchronous network to an FFP model.

The implementation is correct with respect to the preservation of the communication flows (the signals values), independent of the exact time when they are produced. Each FFP process has the same structure. The computation of the new state and output values is the same as in the original SR machine. Communication is via queues. A process is triggered by its own clock, but it is executed only if its input buffers are non-empty, and its output buffers are non-full, otherwise it is stalled. Activation clocks can be arbitrary or characterized by a lower bound between any two ticks. Performance analysis is preformed using a graphbased approach which involves a reachability graph and the triggering order of processes. It uses a slow triggering policy which assumes that, in each cycle, the process that is triggered next is the one that does not enable other firings (the worstcase triggering order). This approach may be too pessimistic and it may suffer from the exponential numbers of vertices in the analysis graph.

In the domain of real-time schedulability analysis, Real-Time Calculus (RTC) was proposed as a general framework for the modeling and analysis of the time properties of embedded SW task systems. RTC was recently used for the analysis of task systems with feedback (tasks

communicating by finite queues). Although the original aim of the analysis is pipelined multimedia systems, we found that after some appropriate modifications, the general approach is applicable to the analysis of the LTTA implementation of synchronous models. In [LNZSV11] we use RTC, after appropriate modifications needed to overcome the limitations of the present approach presented to model and analyze the mapping performance we developed previously thus significantly improving our previous results. The modifications satisfy the following requirements:

Optimizing Extensibility in Hard Real-Time Distributed Systems

Participants: Intel, UC Berkeley, Trento, UTC

Some applications such as the design of a car typically require upgrading an implementation platform to accommodate new functionality or to fix errors over a product life-time that may extend over a five year horizon. In this case, being able to adjust the design without undergoing a major re-design cycle is imperative for competitive advantage. We addressed the problem of defining the initial solution to the design problem so that it is as robust as possible with respect to addition of new tasks or modifications to existing ones. To do so, we introduce a robustness measure, the extensibility metric, and then develop an efficient algorithm that optimizes this metric. In this work, we focused on hard real-time distributed systems that collect data from a set of sensors, perform computations in a distributed fashion and based on the results, send commands to a set of actuators. The tasks must satisfy tight end-to-end deadline constraints. Extensibility is defined as the amount by which the execution time of tasks can be increased without changing the system configuration while meeting the deadline constraints. With this definition, a design that is optimized for extensibility not only allows adding future functionality with minimum changes, but is more robust with respect to the variance of task execution times. We considered systems based on run-time priority-based scheduling of tasks and messages. In particular, we assumed that input data (generated by a sensor, for instance) are available at one of the system's computational nodes. A periodically activated task on this node reads the input data, computes intermediate results, and writes them to the output buffer from where they can be read by another task or used for assembling the data content of a message. Messages - also periodically activated - transfer the data from the output buffer on the current node over the bus to an input buffer on a remote node. Local clocks on different nodes are not synchronized. Tasks may have multiple fan-ins and messages can be multi-cast. Eventually, task outputs are sent to the system's output devices or actuators. The extensibility optimization problem can be considered as part of the mapping stage in the Platform-Based Design (PBD) design flow, where the functionality of the design (what the system is supposed to do) and its architecture (how the system does it) are captured separately, and then "joined" together, i.e., the functionality is "mapped" onto the architecture. In the application, function blocks communicate through signals, which represent the data dependencies. The architectural description is a topology of computational nodes connected by buses. In this approach, buses and nodes can have different transmission and computation speeds. Mapping allocates functional blocks to tasks and tasks to nodes. Correspondingly, signals can be mapped into local communication or packed into messages that are exchanged over the buses. Task and message priorities are assigned and the mapping is performed in such a way that the end-to-end latency constraints are satisfied in the worst-case. Task allocation, signal to message packing, message allocation and priority assignment are the design variables considered here that are chosen with the objective of optimizing task extensibility.

The first stage of the proposed algorithm is based on MILP programming, where task placement (the most important variable with respect to extensibility) is optimized within deadline and utilization constraints. The second phase features two heuristic algorithms, which iteratively optimize signal-to- message packing and priority assignment. This algorithm runs much faster than randomized optimization approaches (a 20x reduction with respect to

simulated annealing in our case studies). Hence, it is applicable to industrial systems as the case studies, which are of size comparable with the typical case of deployment of a set of additional functionalities in a commercial car, demonstrate in the experimental section. The first case study is a set of active safety functions deployed on a vehicle bus-architecture, with 9 ECUs, 41 tasks, and 83 CAN signals. In this case, optimization takes less than 1800 seconds, compared to more than 12 hours needed by the randomized optimization method, with results of comparable quality. The second test case is a safety-critical distributed control system deployed within a small truck. The key features of this system are the integration of slow and very fast (power electronics) control loops using the same communication network. In this example, we are interested in redesigning an existing system to understand the effects of adding communication and computational resources to the system. The shorter running time of the proposed algorithm allows using the method not only for the optimization of a given system configuration, but also for architecture exploration, where the number of system configurations to be evaluated and subject to optimization can be large. A further advantage of an MILP formulation (even if used only for the first stage) with respect to randomized optimization, is the possibility of leveraging mature technology in solvers, the capability of detecting the actual optimum (when found in reasonable time), or, when the running time is excessive, to compute at any time a lower bound on the cost of the optimum solution, which allows evaluating the quality of the best solution obtained up to that point.

This work was invited for publication on the IEEE Transactions on Industrial Informatics [ZYNSSV10].

Predictable architectures in Automotive and Aeronautics

Participants: USAAR, AbsInt, Airbus, Bosch
Embedded systems with hard real-time constraints need sound timing-analysis methods for proving that these constraints are satisfied. Computer architects have made this task harder by improving average-case performance through the introduction of components such as caches, pipelines, out-of-order execution, and different kinds of speculation. This problem becomes even more pronounced with the introduction of multi-core architectures for cost- and energy preservation. We investigate which architectural features make analysis hard, if not infeasible, but do not or only slightly improve performance. Our article [CFGGMRTW10] explores design principles for predictable (multi-core) architectures. We furthermore investigate how unpredictable architectures can be configured in such a way that the composition of the system becomes more predictable.

3.1.4 Applications to Chip Design

Analog extensions of SystemVerilog Assertions (SVA)

Participants: IST Austria, Cadence, Synopsys, Mentor Graphics, Freescale Semiconductor

The property-based validation for mixed-signal systems received industrial interest in the past few years. The effort on exporting this methodology from digital to analogue and mixed-signal domain resulted in the creation of a standardization committee for an analogue extension of SystemVerilog Assertions (SVA), an IEEE standard specification language used in digital design validation and verification. The ideas explored within the committee are partly inspired by the work done on property-based validation for mixed-signal systems reported in this Deliverable. Among the active participants in the committee are all the major EDA vendors (Cadence, Synopsys and Mentor Graphics) and Freescale Semiconductor. Dejan Nickovic from IST Austria has been actively participating in the committee since its creation. The preliminary results of the committee were presented in an invited tutorial in the FORMATS

conference [HLMN10]. The analogue extensions of SVA represent an on-going work. http://www.eda.org/twiki/bin/view.cgi/VerilogAMS/AmsAssertions.

A Platform-Based Methodology for System-Level Mixed-Signal Design

Participants: Marvel, Scuola di Sant'Anna, Trento, University of California at Berkeley

The complexity of today's embedded electronic systems as well as their demanding performance and reliability requirements are such that their design can no longer be tackled with ad hoc techniques while still meeting tight time to-market constraints.

In [NSWDBSV10], we presented a system level design approach for electronic circuits, utilizing the platform-based design (PBD) paradigm as the natural framework for mixed-domain design formalization. In PBD, a meet-in-the-middle approach allows systematic exploration of the design space through a series of top-down mapping of system constraints onto component feasibility models in a platform library, which is based on bottom-up characterizations. In this framework, new designs can be assembled from the pre-characterized library components, giving the highest priority to design reuse, correct assembly, and efficient design flow from specifications to implementation. We applied concepts from design centering to enforce robustness to modeling errors as well as process, voltage, and temperature variations, which are currently plaguing embedded system design in deep-submicron technologies. The effectiveness of our methodology is finally shown on the design of a pipeline A/D converter and two receiver front-ends for UMTS and UWB communications.

A Methodology for Constraint-Driven Synthesis of On-Chip Communications

Participants: Trento, UC Berkeley, University of Columbia, UTC

With the advances of IC technology, global interconnects have become the dominant factor in determining chip performance: they are not only becoming responsible for a larger fraction of the overall delay and power dissipation but exacerbate also design problems such as noise coupling, routing congestion, and timing closure, thereby imposing severe limitations on design productivity. Because of these characteristics, most VLSI circuits can be considered **distributed systems**, a fact that challenges traditional design methodologies and the electronic design automation tools that are based on them. Systems-on-Chip (SoCs) are typically designed by assembling intellectual property (IP) components from different vendors and/or different divisions of the same company in the attempt of reducing time-to-market by reusing pre-designed and pre-verified elements. However, since these components are designed independently, the assembly step is often a challenging problem that requires *the design of communication interfaces to match different protocols and data parallelism, and the routing of global interconnect wires to meet the constraints imposed by the target clock period*. Borrowing from the communication networks literature, an NoC can be built through the combination of heterogeneous elements such as interfaces, routers, and links. The NoC design is a challenging problem because there are many degrees of freedom (e.g. network topologies, routing protocols, flow-control mechanisms, positions of the communication components and core interfaces) as well as multiple optimization goals (e.g. performance, power, area occupation and reliability). Hence, the problem had been simplified by limiting the number and types of components considered, by focusing on a subset of the relevant objectives, by constraining NoC topology and components positions, and by dividing the optimization process in successive stages. Limiting the degrees of freedom has also the important side effect of reducing implementation and layout complexity. While a rich set of interesting results exists in the literature, few are the examples of practical applications of NoCs. In fact, the debate between those who favor standard bus architectures or variations thereof and those who advocate the adoption of NoC approaches ranging from constrained architectures to custom ones is vibrant. We do not take sides even though the NoC approach has undisputable

fundamental merits that may make it successful in the long run. Instead, we propose a general methodology for the design of on-chip communication that can explore a large number of alternatives including as special cases NoCs, bus architectures and hybrid ones. Thanks to its generality our approach can be used to build a framework where different constrained solutions are compared using a number of evaluation factors. We addressed the synthesis of optimal heterogeneous networks by assembling components from a fine-grained library without enforcing any constraint on their topology other than the ones formally captured in the library. In particular, the network that we obtained need not be direct and not even connected if these constraints are not captured in the composition rules of the communication components.

Methods, Tools, and Platforms for cost-efficient certification of safety-critical multicore systems

Participants: TU Braunschweig, Intel, Infineon, Sysgo, Elektrobit, EADS IW, Delphi, TÜV Nord, and others

RECOMP is an ongoing project proposal submitted in response to the second call for proposals of the European JU Artemis. The goal of RECOMP is to develop methods, tools and platforms for enabling cost-efficient certification and re-certification of safety-critical multi-core systems, with special emphasis on the design of mixed-criticality systems. Additionally the integration of the developed techniques should be integrated into certification processes for different domains such as avionics, automotive or industrial automation. Commonly used safety standards for single-core systems like IEC 61508, ISO 26262 or DO 178B will provide the base for the certification of mixed-criticality multi-core systems. To enable the coverage of the complete safety-related development process a large consortium has been established to address most of the upcoming challenges. For example the consortium contains hardware (e.g. Intel, Infineon) and software (e.g. Sysgo, Elektrobit) vendors, system integrators (e.g. EADS IW, Delphi), certification authorities (TÜV Süd) and several research institutions.

3D integrated DRAM-on-logic for low-power mobile applications

Participants*: IMEC,* INTEL, Micron, Panasonic, Samsung, TSMC, Fujitsu, Sony, Amkor and Qualcomm.

Imec and its 3D integration partners have proven the potential of 3D integration of a commercial DRAM chip on top of a logic IC for next-generation low-power mobile applications. Imec's applied 3D EDA (electronic design automation) tools including thermal models have proven to be valuable means to design next-generation 3D stacked ICs.

The 3D stack resembles as close as possible to future commercial chips. It consists of imec's proprietary logic CMOS IC on top of which a commercial DRAM is stacked using through-silicon vias (TSVs) and micro-bumps. Heaters were integrated to test the impact of hotspot on DRAM refresh times. And, the chip contains test structures for monitoring thermo-mechanical stress in a 3D stack, ESD (electro-static discharge) hazards, electrical characteristics of TSVs and micro-bumps, fault models for TSVs, etc.

Imec's 3D integrated DRAM-on-logic demonstrator showed that a minimum die thickness of 50µm is required to deal with local hot spots on the logic die, which are generated by local power dissipation. Due to the strongly reduced lateral heat spreading capability of thin die, these hot spots are higher in temperature and more confined if the die thickness is reduced.

The hot spots on the logic die cause local temperature increases in the memory die. This may cause a reduction in retention time of the DRAM devices. However, imec's 3D stacked demonstrator has proven that the DRAM may not be thermally isolated from the logic die since the DRAM die also acts as an effective heat spreader for the logic die. As such the intensity of

the hot spot is reduced and thereby the temperature rise in the DRAM device is strongly limited.

http://www2.imec.be/be_en/press/imec-news/archive-2011/imecdramonlogicsemiconwest.html

Breakthroughs in enabling future DRAM and RRAM

Participants: ,Imec, Intel, Micron, Panasonic, Samsung, TSMC, Elpida, Hynix, Fujitsu and Sony.

In the frame of its research on future memory architectures, imec has made breakthroughs for both DRAM and RRAM memories. For DRAM, MIMcap (metal-insulator-metal capacitor) was established as a clear candidate for 1X DRAM scaling. Imec demonstrated a record low leakage current and was able to explain the mechanism for leakage reduction, showing the path for further potential improvement. For Resistive RAM (RRAM), imec built a model to understand the properties of the filaments that result in a stable RRAM operation. Such fundamental understanding of the filament properties is key to bridge the gap in the development of RRAM as a successor memory technology.

These results were obtained in cooperation with imec's key partners in its core CMOS programs Globalfoundries, INTEL, Micron, Panasonic, Samsung, TSMC, Elpida, Hynix, Fujitsu and Sony.

http://www2.imec.be/be_en/press/imec-news/archive-2011/imecmemorysemiconwest.html

Automated Solution for Testing 3D Stacked Ics

Participants: Imec, Cadence

This imec-Cadence collaboration provides the design-for-test (DFT) and automatic test pattern generation (ATPG) technology that will make it easier to test 3D-ICs with "through-silicon via" (TSV) functionality and help ensure that the stacked system will work as intended.

Insights gained during its comprehensive research program on TSV-based 3D-IC design and technology enabled imec to extend the DFT architecture for conventional (2D) ICs with several novel (patent-pending since Q1 2010) features. The 3D DFT architecture is based on the concept of die-level test wrappers, which enable testing of chips with TSVs and micro-bumps both before ("pre-bond test"), during ("mid-bond test"), and after ("post-bond test") stacking, as well as after packaging.

"This new DFT solution is the latest example of our commitment at Cadence® to the emerging area of 3D-IC," said Brion Keller, senior architect at Cadence. "Over the past two years, we've introduced 3D-IC TSV and silicon interposer capabilities, and, just three months ago, the industry's first wide I/O memory controller IP solution, with a robust 3D-IC integration environment. Collaboration is an essential element of effective Silicon Realization and the EDA360 vision we adhere to, and this initiative with imec demonstrates why."

http://www2.imec.be/be_en/press/imec-news/archive-2011/imeccadence.html

Exploration Flows for 3D Ics

Participants: Imec, Atrenta

A flow allowing robust, accurate partitioning and prototyping early in the design process is critical to make cost-effective 3D systems and to get them to market fast. The flow under development allows minimizing the number of design iterations, facilitating a cost- and time-effective search of the solution space. Imec and Atrenta demonstrated their first EDA tool flow dedicated to 3D design exploration at last year's DAC.

3D stacked ICs are a promising technology for many designers. The main advantages are a reduced footprint with shorter and faster interconnects, increased system integration at a lower cost, and higher modularity and reuse. Examples of target applications include: products for mobile and high-performance applications, imagers, stacked DRAM, and solid-state drives.

To design innovative applications with 3D stacked dies, the ability to do early planning and partitioning is critical. The number of potential solutions for any given system design problem (e.g., front to front, front to back, silicon interposer, technology choice for slices, via configurations, partitioning, etc.) is very large. Exploring this solution space through multiple full designs is simply too expensive and time-consuming. This makes it critically important to perform robust, accurate partitioning and prototyping early in the design process, well before detailed implementation begins.
There are other significant challenges for 3D design, such as the thermal profiles (heat dissipation) and the mechanical stress caused by assembly configurations. Imec has developed compact thermal and mechanical models for rapid generation of heat dissipation and mechanical stress maps and has validated them using real 3D DRAM-on-logic packaged devices. When combining the design floor plans produced by Atrenta's SpyGlass® Physical 3D prototyping tool with the stress models developed by imec, different scenarios can be assessed quickly and the best option can be chosen in advance of a full design implementation.

http://www2.imec.be/be_en/press/imec-news/archive-2011/atrenta.html

Development of an Innovative SAW-Less Reconfigurable Transceiver

Participants: Imec, Renesas Electronics
The trend in wireless communication where terminals give their users ubiquitous access to a multitude of services drives the development of reconfigurable radios in deep-submicron CMOS. For emerging standards such as 3GPP-LTE, which use a broad range of operating frequencies and bandwidths, multi-mode capabilities of the radio are a must. Scaldio provides a solution to the handset manufacturers, which face the challenge of developing fully reconfigurable radios for a wide range of networks.

One of the major obstacles today in designing fully reconfigurable radios is making the antenna filters reconfigurable due to their stringent requirements. By making the Scaldio receiver highly linear, more out-of-band blocker interference can be allowed in the RF receiver, avoiding the need of SAW filters and consequently enabling a simplified antenna interface. With 3dB noise figure and capable of handling a 0dBm blocker at 20MHz offset, the receiver has the highest blocker resilience for low noise figures. The fully reconfigurable receiver also achieves the highest linearity (+10dBm IIP3, +70dBm IIP2), and frequency range reported up to now and handles blockers well in any mode.

The transmitter combines adaptive out-of-band noise filtering with voltage-sampling up-conversion to achieve RX band noise down to -162dBc/Hz allowing also here SAW-less operation. SAW-less transmitters become more and more important with the evolution towards future standards such as 3GPP-LTE where transmitters will need to operate in multiple FDD (frequency division duplex) bands.The reconfigurable receiver and transmitter technology is

suitable for mobile handsets and all kind of battery-powered wireless connectivity devices, as well as for base-stations for small cells, and can be programmed to meet the requirements for many standards and dedicated needs.

http://www2.imec.be/be_en/press/imec-news/archive-2011/imecrenesassdr.html

Component-based service model

Participants: DTU, B&O ICEpower

DTU and B&O ICEpower have continued the development of a modelling framework for system level performance estimation of embedded systems including Multi-Processor System on Chip (MPSoC) based configurations. The overall goal is to provide a framework which supports models described at multiple levels of abstraction which will allow designers to perform design space exploration at the various design stages ranging from initial high level specifications to detailed, bit true cycle accurate models.

During year 3, several refinements of the framework has been carried out resulting in minor changes of the modelling methodology. Substantial time and effort has been spent on this refinement implementing the changes in the current implementation of the framework. Also, a lot of time and effort has been put into the definition of a language used to specify models and automatically synthesize fast simulation models based on the specification. This shows promising results but is still work in progress. During year 3 DTU and B&O ICEpower has worked on an elaborate case-study, which has resulted in two publications [THM09a,THM09b].

3.1.5 Application to Smart Energy Efficient Buildings

Energy-neutral distributed sensing for proactive energy management in buildings and plants

Participant: University of Bologna, Telecom Italia
University of Bologna has designed the Energy Harvesting circuit which is the core of the power supply unit of the wireless sensor nodes of the Kaleidos framework developed by Telecom Italia (the main telephone company in Italy). The collaboration deeply exploits wireless sensor networks and wireless actuators to improve and simplify industrial and service operations. To this goal Kaleidos is a middleware platform to collect data and provide anf efficient management of electricity consumption in telecommunication switching plants. University of Bologna provided technology for powering the sensors and recharging the batteries exploiting the electromagnetic fields in the cable grid and using the same AC current sensors used for measurements and data logging.

Warehouse of the future

Participant: ESI, Vanderlande Industries

This activity is a continuation of the work that was already introduced in the previous (year 3) report). The activity aims at overcoming the weaknesses of the existing centralized warehouse control systems. This so-called “warehouse of the future” can be achieved by defining appropriate (software) architecture for warehouse and (quantitatively) showing that such architecture eliminates the weaknesses of the centralized warehouse control system. A main result of the project is an agent-based prototype for a control system for Automatic Case Picking (ACP). Closely connected to this activity is the work ESI does in the FP7 Multiform project where it works on defining a Design Framework that should support integration of model-based methods and techniques. One of the main functionalities of the framework is to navigate through design views based on several types of relationships that exist between the entities that are present in the views.

A Design Flow for Building Design Automation

Participants: University of California at Berkeley, Trento, United Technologies Corporation and Intel

The building stock in the US accounts for 40% of total energy consumption and 70% of electricity consumption. Limits on carbon emissions are driving new regulations that will require buildings to be energy efficient according to standards that are likely to be more stringent than the ASHRAE 90.1. The design of low energy buildings – zero energy in the ideal case – is challenging but not impossible. There are today examples of zero energy buildings, but they are the results of *ad-hoc* designs that are not easy to generalize.

The design methodology used today for large buildings is top-down. Different sub-systems (e.g., mechanical and electrical) are designed in isolation by domain experts following design documents flown down after the bid process. This methodology is not suitable for low energy buildings that require interaction among architects, mechanical engineers and control engineers. Consider for instance adopting low energy solutions such as natural ventilation and active facade. In this case, architectural design (e.g. building orientation), the design of the mechanical equipment of the HVAC system and the design of the control algorithms cannot be done in isolation. In this new context, the design of the building automation system (i.e. the embedded processors and networks supporting the building operations, and the software running on them) is non-trivial. Control algorithms become multi-input, multi-output, hybrid and predictive, as opposed to single-input single-output controllers coordinated by simple switching conditions as today (and mainly dictated by standards). Moreover, several sub-systems such as HVAC, lighting, vertical transportation and fire and security will interact through the network to allow information sharing.

In 2011, we focused on a design flow for building automation systems that bridges the gap between a desirable design entry point – at a high abstraction level using model-based design tools such as Simulink – and the available back-end tools able to generate low-level code.

It enables the integration of models from different high-level languages, allowing the interaction between domain experts. Further, it automatically optimizes the implementation of the control algorithms on a distributed platform by selecting computation and communication resources, and by performing code generation while meeting the specification.

3.1.6 Application to Wireless Communication

Model-based conformance testing of a wireless sensor network node

Participants: Radboud University Nijmegen (NL), University of Twente (NL), Aalborg University (DK), Chess B.V (NL).

Within the European STREP Quasimodo ESI has worked on extensions for quantitative aspects of model-based testing theories, including real-time and data-intensive testing of embedded software. Corresponding tool support has been developed and applied to conformance testing of the gMAC synchronization protocol of a wireless sensor network node developed by Chess B.V. Different model-based testing tools were used and compared - Uppaal-Tron, JTorX, TorXakis - and various discrepancies between the behaviour of the node and the protocol specification were detected.

http://www.quasimodo.aau.dk/Final/Quasimodo-D5.7.pdf

State-of-the-art integrated IR-UWB enabling global high-quality low-power mobile applications

Participants*:* Imec and Holst Centre

With its first ultralow-power integrated solution for the 6-10GHz band, imec and Holst Centre now make UWB communication available for battery-operated applications in the area of personal area networks and positioning sensors worldwide. Examples are short-range video streaming or around-the-body audio streaming (e.g. between a headset and a smartphone). When using the UWB radio for the wireless streaming of audio between for example a smartphone and an earpiece, the battery lifetime of the smartphone will increase by over 3x compared to a conventional Bluetooth-based solution, and the earpiece will have a battery lifetime increase of over 5x. In contrast to the Bluetooth communication, the UWB radio will not suffer from interference from other wireless technologies that operate in the same location and in the same frequency band.

Imec and Holst Centre's solution consists of a transmitter, receiver front-end, and receiver digital baseband. The transmitter delivers 13dBm peak power, with an average power consumption of 3.3mW. The receiver front-end shows -88dBm sensitivity at 1Mbps. A digital synchronization algorithm enables real-time duty cycling, resulting in a mean power consumption of 3mW. A DCO with 100ppm frequency accuracy and a baseband frequency tracking algorithm ensure the coherent reception. A 75dB link budget with a data rate of 1Mbps is achieved.

http://www2.imec.be/be_en/press/imec-news/archive-2011/uwb2011.html

Multi-mode digital TV receiver on reconfigurable processor with record area efficienc

Participants: Imec, Panasonic

Digital broadcasting has recently gained a lot of interest, yet its deployment in products can be hampered by the many different regional standards that have been adopted world-wide. Due to the ultimate programmability, software-defined radio (SDR) solutions are becoming more and more attractive. Reconfigurable processor-based implementations allow saving on design-cost and time-to-market. However, SDR baseband solutions are traditionally reported to come with an area penalty when compared to ASIC counterparts. As area efficiency is one of the most important factors that determine the final cost of commercial chipsets, competitive area efficiency is crucial for SDR baseband solutions.
The instantiation of imec's ADRES (architecture for dynamically reconfigurable embedded systems) processor was optimized by combining innovative algorithms (highly parallel implementation, software optimizations) with architecture improvements (optimized intrinsics, exploration towards leaner instance), resulting in a drastically smaller silicon area than the ASIC counterparts of the considered broadcasting standards. On top of its area efficiency, imec's baseband processor proves to be highly flexible, supporting not only Digital TV standards (ATSC, ISDB-T, DVB-T,...) but also many other wireless communication standards: both an IEEE 802.11n inner receiver and a cat-4 LTE receiver can run real time on the same architecture.

http://www2.imec.be/be_en/press/imec-news/archive-2011/imecadres.html

innovative flexible forward error-correction solution for software-defined radios

Participants: Imec, Target

Imec and Target Compiler Technologies developed a C-programmable flexible FEC (forward error correction) solution fit for future cellular, connectivity and broadcasting standards. This so-called “flex FEC” solution competes in area and throughput with dedicated fixed-function hardwired implementations, yet offers the flexibility to support multiple standards thanks to software programmability. The C-programmable flex FEC ASIP (application-specific instruction-set processor) template supports LDPC (low-density parity check), Turbo and Viterbi decoding. Imec designed and optimized the ASIP architecture and generated a matching software development kit, using IP Designer, Target’s tool-suite for ASIP design.

http://www2.imec.be/be_en/press/imec-news/archive-2011/dac2011.html

3.1.7 Timing Analysis/Predictability

Static Analysis of Synthesized Code

Participants: Universität des Saarlandes, AbsInt, Daimler

The analysis of code synthesised from high-level models often can be improved by utilising model information. For example, code synthesized from the automata component of models often has complex control flow, not easily amenable to existing static analysis tools. The control logic implemented in automata also governs the control flow through the surrounding parts of the model. Information about the reachable states can be used to exclude infeasible paths in the model, potentially reducing the computed worst-case execution time.

Identification of Operating Modes

Participants: Universität des Saarlandes, AbsInt, Bosch

Embedded control often works in different operating modes with different timing constraints. Determining the overall worst-case execution time would be pessimistic for some of the modes. One goal of the cooperation between Universität des Saarlandes, AbsInt and Bosch is the development of a mode-specific timing analysis. This would determine a worst-case execution time for each mode. However, operating modes currently are not explicitly specified and therefore neither visible on the model level nor on the code level. Designers of components typically know them, but have no way to declare them. Upon composition of the components, this information is completely lost for the integrated system. A first step therefore consists of an analysis of the system on the model and/or the code level to identify operating modes.

Integration of Compilers and Timing Analysis

Participants: TU Dortmund, AbsInt, Bosch

TU Dortmund has integrated compilation and timing analysis. The resulting tool WCC initially targeted the Infineon TriCore processor, which is very popular in the automotive industry. This is the first time that a compiler for a real, industrial processor has been integrated with timing analysis. In 2010, WCC has been extended to support other processors more flexibly. WCC has been used to evaluate the potential of a reduction of the worst case execution times (WCETs) of automotive applications in a study by Bosch. Through an exploitation of fast memories, WCC could reduce the WCET by more than 50% if compared to standard gcc.

3.1.8 Multimedia Systems

Multicore Resource Reservation for Real-Time Systems

Participants: Scuola Superiore Sant'Anna of Pisa, University of Lund, University of Kaiserslautern, Ericsson, Evidence srl., EPFL of Lausanne.

Within the European STREP ACTORS, a new programming framework has been developed to support parallel real-time applications on multicore platforms. Three techniques have been combined for this purpose: data-flow programming models, virtualization, and feedback control. Data-flow models provide the proper foundation for specifying parallel computations and efficiently implement component-based algorithms. Virtualization techniques, such as reservation-based scheduling, provide spatial and temporal separation of concerns and enforce dependability and predictability, whereas feedback control is used to handle incorrect reservations, reclaim and redistribute unused resources, and adjust to dynamic changes in resource requirements.

URL: http://www.actors-project.eu/

3.1.9 Other System Applications

Code-generation Infrastructure

Participants: TU Dortmund, ICD, Siemens, Airbus, Bosch, Thales, Intracom, ELMOS, TUV, Raith, Vorwerk.

At Dortmund, most industrial activities are chanelled via the University's IT spin-off, ICD e.V. ICD has been providing a commercial code generation infrastructure to Infineon. This infrastructure is supporting a protocol processor optimized for processing internet packets. The infrastructure is based on the ICD-C compiler design tools. In 2011, the tool set was applied. For example, it was used for a compiler written for ICD's customer Lantiq.. A cut-down version of ICD-C is available for free downloads (see http://www.icd.de/es). ICD-C is offering support and maintenance for some terminated European research projects such as MORE, in cooperation with the original software developers. ICD is led by P. Marwedel, who also leads a group at TU Dortmund. Dortmund is also cooperating with Airbus, Bosch, Thales (France), Intracom (Greece) via projects MNEMEE and PREDATOR. Also, the aiT tool for worst case timing analysis has been integrated into the experimental worst-case execution time aware C compiler WCC. Local contacts exist to ELMOS (a semiconductor manufacturer mostly for the automotive domain) and WILO (see www.wilo.com).

http://www.icd.de

-- The above is new material, not present in the Y3 deliverable --

3.2 Individual Publications Resulting from these Achievements

ESI

[MHP] H. Moneva, R. Hamberg, T. Punter A Design Framework for Model-based Development of Complex Systems, 32nd IEEE Real-Time Systems Symposium, 2nd on Analytical Virtual Integration of Cyber-Physical Systems Workshop. Vienna, Austria – November 29, 2011.

IMEC

[AFR11] Agrawal, P.; Fasthuber, R.; Raghavan, P.; Vander Aa, T.; Catthoor, F. and Van der Perre, L.: Early exploration of partitioning trade-offs for heterogeneous MPSoCs. Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems - ACACES.July 2011

[AFRV11] Agrawal, P.; Fasthuber, R.; Raghavan, P.; Vander Aa, T.; Ahmad, U.; Van der Perre, L. and Catthoor, F.: High level analysis of trade-offs across different partitioning schemes for wireless applications. IEEE Workshop on Signal Processing Systems - SIPS.October 2011

[APAV11] Ahmad, U.; Li, M.; Pollin, S.; Amin, A.; Van der Perre, L. and Lauwereins, R.: Hybrid lattice reduction algorithm and its implementation on an SDR baseband processor for LTE. 19th European Signal Processing Conference - EUSIPCO. Augustus 2011

[AGOGD11] Auer, G.; Giannini, V.; Olsson, M.; Gonzalez, M. and Desset, C.: Framework for energy efficiency analysis of wireless networks. 2nd Int. Conf. on Wireless Communications, Vehicular Technology, Information Theory and Aerospace & Electronic Systems Techn..February 2011

[B11] Badaroglu, M.: 3D system integration. Nano-Tera Microcool 3D-IC Course at EPFL.June 2011

[B11b] Badaroglu, M.: 3D IC architectures. Nano-Tera Microcool 3D-IC Course at EPFL. June 2011

[BZ11] Beyne, E. and Zhang, W.: 3D technology enabling innovative smart system integration. China International Semiconductor Technology Conference - CISTC.March 2011

[BMV11] Beyne, E.; Marchal, P. and Van der Plas, G.: 3D heterogeneous system integration: Application driver for 3D technology development. 48th ACM/EDAC/IEEE Design Automation Conference - DAC.June 2011

[Be11] Beyne, E.: 3D technology-enabling innovative smart systems. Imec Technology Forum, ITF Taiwan.March 2011

[VBSC11] Vengattaramane, K.; Borremans, J.; Steyaert, M. and Craninckx, J.: A standard cell based all-digital time-to-digital converter with reconfigurable resolution and on-line background calibration. 37th European Solid-State Circuits Conference - ESSCIRC.September 2011

[NCGMV11] Noia, B.; Chakrabarty, K.; Goel, S.; Marinissen, E. and Verbree, J.: Test-architecture optimization and test scheduling for TSV-based 3D stacked ICs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. Vol. 30: (11)

[C11] Craninckx, J.: SAW-less radio transceivers in 40nm CMOS. International Microwave Symposium.June 2011

TRENTO

[RPMP11] Tizar Rizano, Roberto Passerone, David Macii and Luigi Palopoli, Model-Based Design of Embedded Control Software for Hybrid Vehicles. In Proceedings of the 6th IEEE International Symposium on Industrial Embedded Systems (SIES11)}, Västerås, Sweden, June 15-17, 2011.

TU Braunschweig

[ADNSSE11] Philip Axer, Jonas Diemer, Mircea Negrean, Maurice Sebastian, Simon Schliecker, und Rolf Ernst, "Mastering MPSoCs for Mixed-Critical Applications" *IPSJ Transactions on System LSI Design Methodology*, vol. 4, August 2011

[ASE11] Philip Axer, Maurice Sebastian, und Rolf Ernst, "Reliability Analysis for MPSoCs with Mixed-Critical, Hard Real-Time Constraints" in *Proc. Intl. Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, (Taiwan), Oktober 2011

[DRNSE11] Jonas Diemer, Jonas Rox, Mircea Negrean, Steffen Stein, und Rolf Ernst, "Real-Time Communication Analysis for Networks with Two-Stage Arbitration" in *Proceedings of the ninth ACM International Conference on Embedded Software (EMSOFT)*, (Taipei, Taiwan), pp. 243-252, ACM, Oktober 2011.

[PRDC11] Maurice Sebastian, Philip Axer and Rolf Ernst, "Utilizing Hidden Markov Models for Formal Reliability Analysis of Real-Time Communication Systems with Errors", in *Proceedings of the 17th IEEE Pacific Rim International Symposium on Dependable Computing (PRDC 2011)*, December 2011.

TU Dortmund

[Ma11] Peter Marwedel. Embedded Systems Design - Embedded Systems Foundations of Cyber-Physical Systems. Springer, 2011. ISBN 978-94-007-0256-1

[MM11] Peter Marwedel and Michael Engel. Embedded System Design 2.0: Rationale Behind a Textbook Revision. *In Proceedings of Workshop on Embedded Systems Education (WESE)*, Taipei, Taiwan, October 2011.

[MJ11] Peter Marwedel, Jeff Jackson, and Kenneth Ricks (eds.). Proceedings of the Workshop on Embedded Systems Education (WESE), Taipei, Taiwan, Oct. 2011

[TW11] Constantin Timm, Frank Weichert, David Fiedler, Christian Prasse, Heinrich Müller, Michael Hompel and Peter Marwedel. Decentralized Control of a Material Flow System enabled by an Embedded Computer Vision System. *In Proceedings of the IEEE ICC 2011 Workshop on Embedding the Real World into the Future Internet*, June 2011.

-- The above are new references, not present in the Y3 deliverable --

3.3 Joint Publications Resulting from these Achievements

Trento, INRIA

[RBBC11] Jean-Baptiste Raclet, Eric Badouel, Albert Benveniste, Benoît Caillaud, Axel Legay and Roberto Passerone. A Modal Interface Theory for Component-based Design. Fundamenta Informaticae, 108(1-2):119-149, 2011.

Trento, ETH

[SRPL11] Alena Simalatsar, Yusi Ramadian, Roberto Passerone, Kai Lampka, Simon Perathoner and Lothar Thiele. Enabling Parametric Feasibility Analysis in Real-time Calculus Driven Performance Evaluation. In Proceedings of the International Conference on Compilers, Architectures and Synthesis of Embedded Systems (CASES11), Taipei, Taiwan, October 9-14, 2011.

Trento, UC Berkeley, Bosch, General Motors, National Instruments,Thales,Toyota, UTC

[DLSV11] Patricia Derler, Edward Lee and Alberto Sangiovanni Vincentelli, Modeling Cyber–Physical Systems, Proceedings of the IEEE, Vol. 100, n.1, January 2012, invited paper.

Trento, UC Berkeley, Scuola di Sant'Anna, GM, National Instruments

[ZDGS11] Haibo Zeng, Marco Di Natale, Arkadeb Ghosal, and Alberto Sangiovanni-Vincentelli. Schedule Optimization of Time-Triggered Systems Communicating over the FlexRay Static Segment. IEEE Transactions on Industrial Informatics, Vol. 7, No. 1, February 2011, 1-17.

Trento, UC Berkeley, Scuola di Sant'Anna, GM

[LDZS11] C.-W. Lin, M. Di Natale, H. Zeng, A. Sangiovanni-Vincentelli, "Performance analysis of synchronous models implementations on loosely time-triggered architectures," in Work-in-Progress Session of IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS-2011), Chicago, IL, Apr. 2011.

Trento, UC Berkeley, United Technologies Corporation

[MPS11] M. Maasoumy, A. Pinto, and A. Sangiovanni-Vincentelli. "Model-based hierarchical optimal control design for HVAC systems." In Dynamic System Control Conference (DSCC), 2011. ASME, 2011

Trento, UC Berkeley, Politecnico di Torino, United Technologies Corporation

[MPPLS11] Mohammad Mozumdar, Alberto Puggelli, Alessandro Pinto, Luciano Lavagno, Alberto L. Sangiovanni-Vincentelli "A hierarchical wireless network architecture for building automation and control systems", The Seventh International Conference on Networking and Services , pages 178 -183, 2011, ISBN: 978-1-61208-133-5, Venice, Italy

[PMPLSV11] Alberto Puggelli, Mohammad Mozumdar, Alessandro Pinto, Luciano Lavagno, Alberto Sangiovanni-Vincentelli. "A Routing-Algorithm-Aware Design Tool for Indoor Wireless Sensor Networks". Proceedings of the IEEE International Conference on Computing, Networking and Communications (ICNC), Maui, HI, USA, 2012.

Trento, UC Berkeley, Scuola di Sant'Anna, IMEC

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TU Braunschweig, GM

[RGE12]Jonas Rox, Rolf Ernst, Paolo Giusto, „Using Timing Analysis for the Design of Future Switched Based Ethernet Automotive Networks”, in Proceedings Design, Automation and Test in Europe (DATE 12) (to appear)

TU Braunschweig, Symtavision

[SAEFJ11] Maurice Sebastian, Philip Axer, Rolf Ernst, Nico Feiertag, und Marek Jersak, **"Efficient Reliability and Safety Analysis for Mixed-Criticality Embedded Systems"** in SAE 2011 World Congress & Exhibition Technical Paper, Detroit, USA, April 2011.

KTH, Carmeq, Continental, CRF, Scania, Volvo, Mentor, Univ. Of Hull

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[AA11] A. A. Alam, F. Asplund, S. M. Behere, M. Björk, L. G. Alonso, F. Khaksari, A. Khan, J. Kjellberg, K.-Y. Liang, R. Lyberger, J. Mårtensson, J.-O. Nilsson, H. Pettersson, S. Pettersson, E. Stålklinga, D. Sundman, M. Törngren, and D. Zachariah., “Cooperative driving according to Scoop,” KTH Royal Institute of Technology, Tech. Rep. TRITAE 2011:051, 2011, Documentation for GCDC 2011. Also presented at RTiS 2011, Västerås.

USAAR, Absint

[GR11]Daniel Grund, Jan Reineke, Gernot Gebhard: Branch target buffers: WCET analysis framework and timing predictability. Journal of Systems Architecture - Embedded Systems Design 57(6): 625-637 (2011)

USAAR, AbsInt, SSSA, Airbus, Bosch

[AM11]Sebastian Altmeyer, Claire Maiza: Cache-related preemption delay via useful cache blocks: Survey and redefinition. Journal of Systems Architecture - Embedded Systems Design 57(7): 707-719 (2011)

[AMR11]Sebastian Altmeyer, Claire Maiza, Jan Reineke: Resilience analysis: tightening the CRPD bound for set-associative caches. LCTES 2011: 153-162

[YB11]Gang Yao, Giorgio C. Buttazzo, Marko Bertogna: Feasibility analysis under fixed priority scheduling with limited preemptions. Real-Time Systems 47(3): 198-223 (2011)

IMEC, Ericsson, Telecom Italy, Alcatel-Lucent

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IMEC, Micron

[SCS11]Spessot, A.; Caillat, C.; Srividya, V.; Fazan, P.; Schram, T. and Mitard, J.: Impact of DRAM process flow on the performance of periphery devices for next generation mobile applications. 2nd International Workshop on Simulation and Modeling of Memory - IWSM2.October 2011

IMEC, Cadence

[DCK11]Deutsch, S.; Chickermane, V.; Keller, B.; Konijnenburg, M. and Marinissen, E.: Automation of DfT insertion and interconnect test generation for 3D stacked ICs. IEEE North-Atlantic Test Workshop - NATW.May 2011

IMEC, Toshiba

[SYY11]Suzuki, T.; Yamada, H.; Yamagishi, T.; Takeda, D.; Horisaki, K.; Vander Aa, T.; Fujisawa, T.; Van der Perre, L. and Unekawa, Y.: High throughput and low power software defined radio using dynamically reconfigurable baseband processor. IEEE Micro. Vol. 31: (6)

Univ. Leiden, Lantiq, Intel, Univ. Lugano, Univ. Cagliari, Dortmund (ICD)

[CG11] Emanuele Cannella, Lorenzo Di Gregorio, Leandro Fiorin, Menno Lindwer, Paolo Meloni, Olaf Neugebauer and Andy D. Pimentel. Towards an ESL Design Framework for Adaptive and Fault-tolerant MPSoCs: MADNESS or not?. *In Proceedings of the 9th IEEE/ACM Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia'11)*, Taipei, Taiwan, October 2011.

TU Munich, SSSA Pisa, TU Dortmund, Univ. Ulm

[CN11] Samarjit Chakraborty, Marco Di Natale, Heiko Falk, Martin Lukasiewyzc and Frank Slomka. Timing and Schedulability Analysis for Distributed Automotive Control Applications. *In Tutorial at the International Conference on Embedded Software (EMSOFT)*, pages 349-350, Taipei, Taiwan, October 2011.

-- The above are new references, not present in the Y3 deliverable --

3.4 Keynotes, Workshops, Tutorials

IMEC:
Wireless Innovation Forum.
Title: Cognitive radio experimentation world (CREW).
Speakers: Pollin, S. and Van der Perre, L.
23-25 June 2011; Brussels, Belgium

IMEC Technology Forum, ITF2011 Smartphone.
Title: Exploiting the 3rd dimension.
Speaker: Beyne, E
11 July 2011; San Francisco, CA, US

International Microwave Symposium.
Title: SAW-less radio transceivers in 40nm CMOS.

Speaker: Craninckx, J.
5-10 June 2011; Baltimore, USA

ESSCIRC Tutorial.
Title: Transceiver design for interference-robust software-defined radios.
Speaker: Craninckx, J
14-15 November 2011; Lund, Sweden

IEEE Semiconductor Wafer Test Workshop - SWTW.
Title: Wafer probing on fine-pitch micro-bumps for 2.5D- and 3D-SICs.
Speaker: Marinissen, E.
18-22 September 2011; Anaheim, CA, USA

TRENTO:

Trento:

Artist Summer School on ICT for Future Energy Systems, July 25-29, 2011

Roberto Passerone and Davide Brunelli have organized a summer school on Energy Systems in Trento, Italy, sponsored by ArtistDesign. The motivations for the school can be summarized as follows: Public administrations, enterprises and citizens are increasingly going green and are looking to the information technology as the way to reduce energy consumption and to become more environmentally responsible in all human activities. In particular reducing buildings overall energy consumption, providing smarter power grids and optimizing industrial processes are certainly some of the major efforts. Distributed and pervasive sensing, monitoring and control will play a key role in achieving this goal and will pose novel research challenges in the development of distributed applications that must integrate aspects related to generation, storage, distribution and efficient use of energy sources.

The goal of this summer school was to:

- Survey the most relevant research domains;
- Present various perspectives and underlying technologies;
- Identify the most important challenges and research themes;
- Interact with distinguished scholars and establish contacts that may lead to research collaborations in the future.

The audience was made of post-graduate students, PhD students, and young researchers from universities and industrial laboratories around the world. There were a total of 21 participants

Each day featured lectures and discussions around a research theme like programming of Cyber Physical Systems and sensor networks for energy control, Smart Grids, Energy efficiency Systems for Green Computing, Energy Buildings managements, monitoring, etc.. The detailed program was as follows:

- Alberto Sangiovanni-Vincentelli (University of Trento, UC Berkeley).
    - Embedded systems for energy efficiency
- Nuno Pereira (Politécnico do Porto)

- Densely Instrumented Energy-Efficient Physical Infrastructures

- Andrea Benigni (E.ON Energy Research Center, RWTH Aachen University)
  - Distributed Control and Estimation in Future Power Grids
- Fabrizio Pilo(University of Cagliari)
  - 1) Planning the future of Power Distribution
  - 2) Reliability of Power Distribution in the era of Smartgrids
- David Atienza Alonso (École polytechnique fédérale de Lausanne EPFL)
  - Multi-Level and Distributed Thermal- and Energy-Aware Design of IT systems and datacenters
- Maher Kayal (École polytechnique fédérale de Lausanne EPFL)
  - 1) Does smart phone approach can inspire smart grid?
  - 2) Toward real time power system using electronics emulation for microgrid /smart grid.
- Dario Petri (University of Trento), Gian Mario Maggio (CREATE-NET):
  - An overview of the Smart Energy Systems research/innovation activities in the Italian node of the EIT-ICT Labs

The material from the school was posted on the ArtistDesign website for future reference and for the community at large. The comments from the students were particularly positive: "Good People either in the organization and among the participants", "Very well organized, good source of information and participation from all over Europe", "Very interesting and well presented topics. Good communication with audience", "Good attendance and mix of participants", "Good topics and very experienced lecturers", "Good presentations on several energy topics. Good selection of the lecturers. Superb University facilities. Lodging is fine."

Trento, IST-Austria, Mälardalen:

A Special Session on the issue of Robustness was organized at the 6th IEEE International Symposium on Industrial Embedded Systems 2011, in Västerås, Sweden.

The orgagnizers of the special session, Roberto Passerone and Dejan Nickovic, have teamed up with the key people from the Modeling and Validation workpackage to provide an overview on the current status of the research on robustness, in collaboration with Thomas Nolte from Mälardalen University. The special session has included a keynote speach:

- Keynote - Jean-François Raskin
  - Synthesis of Robust Controller and Games With Imperfect Information

and a full session with a total of three invited paper contributions, to span the full spectrum of the design issues:

- Specification-Centered Robustness
  - Roderick Bloem, Krishnendu Chatterjee, Karin Greimel, Thomas A. Henzinger and Barbara Jobstmann
- Robustness in Dynamical and Control Systems

- Rafael Wisniewski

- Robustness in Analog Systems: Design Techniques, Methodologies and Tools
  - Pierluigi Nuzzo and Alberto Sangiovanni-Vincentelli

Key Note: The Major Challenges of the EDA Industry in the Next 5 Years

Tel Aviv, May 3, 2011

Alberto Sangiovanni Vincentelli gave the key note address at the Israel Executive Forum addressing the future directions of the EDA industry.

http://www.israelexecutiveforum.com/agenda.aspx

Key Note: 1,000 Electronic Devices Per Living Person: Dream Or Nightmare?, 4th IEEE International Workshop on Advances in Sensors and Interfaces

Borgo Egnazia, June 9th, 2011

Alberto Sangiovanni Vincentelli gave the opening key note talking about the potential offered by the myriad of sensors, controller and actuators that will be soon available.

http://iwasi2011.poliba.it/programme.html

Key Note: 1000 electronic devices per person, dream or nightmare, International Electronic Forum, Future Horizon

Seville, October 7th, 2011

Alberto Sangiovanni Vincentelli delivered this talk to an audience consisting of CEO, COO and CTO of the semiconductor industry.

Key Note: Application Driven Design – New Directions Require New Tools!

Tel Aviv, May 4, 2011

Alberto Sangiovanni Vincentelli gave the key note at this conference stressing the need for new tools for system level design. He was awarded at the Conference with the ChipEx Award for exceptional contribution to the semiconductor industry delivered by the Science and Technology Minister of Israel Professor Daniel Hershkovitz (see picture below).

Key Note: DAC Workshop

San Diego, June 5th, 2011

Alberto Sangiovanni Vincentelli chaired and gave the opening key note talk at the DAC Workshop on Intra and Inter-Vehicle Networking.

Sunday, June 5 8:00am - 5:00pm **Embedded Systems and Software** **Room: 29CD**

DAC WORKSHOP ON INTRA AND INTER-VEHICLE NETWORKING: PAST, PRESENT, AND FUTURE

Chair(s):
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

Organizer(s):
Paolo Giusto - *General Motors Company, Palo Alto, CA*
Haibo Zeng - *General Motors Company, Palo Alto, CA*
Arkadeb Ghosal - *National Instruments Corp., Berkeley, CA*

Speaker(s):
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
Raj Rajkumar - *Carnegie Mellon Univ., Pittsburgh, PA*
Flavio Bonomi - *Cisco Systems, Inc., San Jose, CA*
Wilfried Steiner - *TTTech, Vienna, Austria*
Markus Kuehl - *aquintos GmbH, Karlsruhe, Germany*
Harald Gall - *austriamicrosystems AG, Unterpremstaetten, Austria*
Frank Schirrmeister - *Synopsys, Inc., Mountain View, CA*
Rodney Cummings - *National Instruments Corp., Austin, TX*
Markus Jochim - *General Motors Company, Warren, MI*
Bill Chown - *Mentor Graphics Corp., Wilsonville, OR*
Arthur Marris - *Cadence Design Systems, Inc., Livingston, United Kingdom*
Robert Juliano - *Mirabilis Design Inc., Sunnyvale, CA*
Marek Jersak - *Symtavision GmbH, Braunschweig, Germany*

Market demands and regulations are leading the automotive industry to face increasing design and business challenges due to the fast adoption rates of sophisticated infotainment, advanced safety features, semi-autonomous driving/control, and remote diagnostics. Specifically, requirements for efficient, fast, and reliable communications among modules within a vehicle and between vehicles in a fleet are testing the limits of current network protocols. Existing networking technologies (e.g., CAN, FlexRay) for intra-vehicle communication, and RADAR/LIDAR, camera-based, inter-vehicle sensing may not be able to tackle all the challenges on bandwidth, cost, and reliability. Hence, new protocols for intra-vehicle, vehicle-to-vehicle, and vehicle-to-infrastructure communications must be defined and developed to facilitate the adoption of new features for enhanced safety, driver comfort, and commercial use cases. This workshop focuses on the past, present, and potential future landscape of intra and inter-vehicle communication technologies, including CAN, FlexRay, Ethernet, and DSRC, with emphasis on the potential opportunities for the EDA industry in providing tool support for the analysis and design of Ethernet and DSRC based automotive architectures. Starting from the automotive OEM's requirements for the new technologies and the related tools to facilitate the adoption of new features, the workshop will also focus on the academic research efforts in this area as well as on the technologies and tool providers therein.

Key Note and Workshop: DAC Workshop on Design Analysis and Implementation of Real-Time Systems with Time-Triggered and Event-Triggered Applications

San Diego, June 5th , 2011

Alberto Sangiovanni Vincentelli chaired and presented the Key Note opening address.


Sunday, June 5 9:00am - 5:00pm Embedded Systems and Software Room: 30C

DAC WORKSHOP ON DESIGN, ANALYSIS, AND IMPLEMENTATION OF REAL-TIME SYSTEMS WITH TIME-TRIGGERED AND EVENT-TRIGGERED APPLICATIONS

Chair(s):
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*

Organizer(s):
Arkadeb Ghosal - *National Instruments Corp., Berkeley, CA*
Kaushik Ravindran - *National Instruments Corp., Berkeley, CA*

Speaker(s):
Alberto Sangiovanni-Vincentelli - *Univ. of California, Berkeley, CA*
Hermann Kopetz - *Technische Univ. Wien, Vienna, Austria*
Raj Rajkumar - *Carnegie Mellon Univ., Pittsburgh, PA*
Wolfgang Pree - *Univ. Salzburg, Salzburg, Austria*
Claudio Pinello - *United Technologies, Berkeley, CA*
Hugo Andrade - *National Instruments Corp., Berkeley, CA*
Stavros Tripakis - *Univ. of California, Berkeley, CA*
Stephen Neuendorffer - *Xilinx, Inc., Berkeley, CA*
José Luis Pino - *Agilent, Westlake Village, CA*

In recent years, interest in determinacy, portability, and composability of real-time systems have led to a significant research effort in time-triggered models. Although the time-triggered model of computation can capture the above properties, the model may be too constrained to reflect real-world requirements. This often leads to conservative implementation, over utilization of resources, and high cost of development. A more flexible model is time-triggered tasks overlaid with event-triggered tasks. One example of such a model is the FlexRay communication protocol for automotive embedded systems that allows time-triggered and event-triggered message communication. This workshop will focus on industrial case studies, models of computation, analysis methodologies, and integrated development platforms for mixed-triggered systems.

TED Talk:

Trieste, June 10, 2011

Alberto Sangiovanni Vincentelli gave a talk on the science and art of design at the TEDxTrieste series.

http://www.tedxtrieste.com/wp/?portfolio=alberto-sangiovanni-vincentelli

Invited Talk*:*

Haifa, March 8, 2011

Alberto Sangiovanni Vincentelli gave a distinguished seminar talk at Haifa IBM Research attended by all researchers on System and Contract-Based Design.

Invited Talk:

Lausanne, March 11, 2011

Alberto Sangiovanni Vincentelli gave a distinguished seminar series talk on Interconnect Everywhere at EPFL.

Invited Talk:

Rome April 28, 2011

Alberto Sangiovanni Vincentelli gave a *lectio magistralis* (500 people attending) at the University of Rome on Innovation, Funding New Enterprise and the Importance of a Rich Ecosystem.

Lectio Magistralis: What is Important in the Design of Systems

Politecnico di Bari, December 2nd , 2011

Alberto Sangiovanni Vincentelli delivered the Lectio Magistralis at the Commencement of Politecnico di Bari about the importance of research in and teaching of system design.

Semi-Plenary Talk: **Taming Dr. Frankenstein: Contract-Based Design for Cyberphysical Systems, 2011 Control and Decision Conference**

Orlando, Fl, December 12th, 2011

Alberto Sangiovanni Vincentelli delivered the following talk at the 2011 CDC, the most prominent conference in Control. *Cyber-physical systems* combine a cyber side (computing and networking) with a physical side (mechanical, electrical, and chemical processes). Such systems present the biggest challenges as well as the biggest opportunities in several large industries, including electronics, energy, automotive, defense and aerospace, telecommunications, instrumentation, industrial automation. Engineers today do successfully design cyber-physical systems in a variety of industries. Unfortunately, the development of systems is costly, and development schedules are difficult to stick to. The complexity of cyber-physical systems, and particularly the increased performance that is offered from interconnecting what in the past have been separate systems, increases the design and verification challenges. As the complexity of these systems increases, our inability to rigorously model the interactions between the physical and the cyber sides creates serious vulnerabilities. Systems become unsafe, with disastrous inexplicable failures that could not have been predicted. Distributed control of multi-scale complex systems is largely an unsolved problem. A common view that is emerging in research programs in Europe and the US is "enabling *contract-based design (CBD)*," which formulates a broad and aggressive scope to address urgent needs in the systems industry. We present a design methodology and a few examples in controller design whereby contract-based design can be merged with platform-based design to formulate the design process as a meet-in-the-middle approach, where design requirements are implemented in a subsequent refinement process using as much as possible elements from a library of available components. Contracts are formalizations of the conditions for correctness of element integration (horizontal contracts), for lower level of abstraction to be consistent with the higher ones, and for abstractions of available components to be faithful representations of the actual parts (vertical contracts).

Trento, Scuola di Sant'Anna, General Motors, Intel

Workshop:

TiMoBD: Time Analysis and Model-Based Design, from Functional Models to Distributed Deployments

ESWeek, Taiwan, October 9-14, 2011

Model-based and Model-driven design flows are very popular in the industry because of the possibility of analysis and verification by simulation or model checking and because of the availability of automatic code generation tools that provide a path to implementation. However, in most flows, the timing behavior of the system depends on features of the computation and communication architecture that are modeled late or not modeled at all, bringing the possibility for an inappropriate selection of the computing platform (over- or underperforming) and possibly an incorrect software implementation of the functional model. To this end, timing analysis techniques can provide support for the analysis of architecture solutions and system configurations and also define analytical methods for the synthesis of feasible/correct solutions. Hence, the need for a better integration of timing analysis technologies, methods and tools in model-based and model-driven flows. The workshop attempted at bridging the gap between the three communities of model-based design, real-time analysis and model-driven development, for a better understanding of the ways in which new development flows that go from system-level modeling to the correct and predictable generation of a distributed implementation can be constructed leveraging current and future research results.

TU Braunschweig

Invited Talk: Using Compositional Performance Analysis for Obtaining Viable End-to-End Latencies in Distributed Embedded Systems
(Jonas Rox, Rolf Ernst, TU Braunschweig)
Rigorous Embedded Design 2011 - organized and funded by ARTIST
Salzburg, Austria – April 10th, 2011

The objective of the workshop was to discuss new methodologies for the rigorous design of embedded systems. Through a series of invited talks, the workshop surveyed some of the challenges and emerging approaches in the area. A series of design flows were presented. The workshop mainly discussed performance analysis, correctness (high confidence and security), code generation, and modeling aspects (including timed scheduling and software/hardware interactions). Those concepts were illustrated with examples coming from the aeronautic, automotive, and robotic areas. Interactions between industrials and academic researchers were also facilitated through a series of open discussion sessions.

Invited Talk: Trusted MpSoC Platforms for Safety Related Applications
(Rolf Ernst, TU Braunschweig)
Coolchips Symposium
Yokohama, Japan – April 20 - 22, 2011(per video conference)

COOL Chips is an International Symposium initiated in 1998 to present advancement of low-power and high-speed chips. The symposium covers leading-edge technologies in all areas of microprocessors and their applications.

MpSoCs are efficient platforms for systems integration. However, due to physical resource sharing, safety critical systems integration becomes more challenging compared to distributed systems potentially leading to increasing design and certification cost. There are many issues in efficient error detection and handling, function segregation, timing, or in the RTE interface that require system level hardware/software solutions. Integration frequently leads to mixed critical systems, i.e. systems which combine functions of different criticality levels. One of the main requirements is a flexible trade-off between development, certification, and production cost that is highly influenced by production volume, product lifetime, and system criticality. The talk gave an introduction to the design of safety critical systems, and the derived design challenges for MpSoC based systems. Novel solutions and tool technologies were explained. The talk also gave an overview on several large industrial-academic projects that deal with safety critical MpSoC and their application, such as the ARTEMIS RECOMP project (Reduced Certification Costs for Trusted Multi-core Platforms).

http://www.coolchips.org/

MiniKeynote: MpSoC for safety critical applications – from multicore to manycore
(Rolf Ernst, TU Braunschweig)
11th EDAA/IEEE Forum on Embedded MPSoC and Multicore
Beaune, France – July 8, 2011

In 2010 Prof. Ernst gave a short introduction on requirements and design methods for MpSoC in safety critical applications. The focus was on interference of safety critical and non-critical applications via shared resources and the corresponding requirements imposed by safety standards. In many-core systems interference is even stronger due to multi-hop NoCs and memory hierarchies. The talk in 2011 gave an overview on first results of a research platform under development as part of the European ARTEMIS project RECOMP.

http://www.mpsoc-forum.org/previous/2011/agenda.html

Invited Talk: Formal Performance Analysis in Automotive Systems Design – A Rocky Ride to New Grounds

(Rolf Ernst, TU Braunschweig)
23rd IEEE Conference on Computed Aided Verification (CAV) Symposium
Snowbird, Utah, USA – July 20, 2011

CAV 2011 was the 23rd in a series dedicated to the advancement of the theory and practice of computer-aided formal analysis methods for hardware and software systems. The conference covered the spectrum from theoretical results to concrete applications, with an emphasis on practical verification tools and the algorithms and techniques that are needed for their implementation. The talk given by Prof. Ernst focused on performance challenges in automotive design. Formal performance analysis methods for automotive design were presented and major obstacles from theory to industrial application were highlighted.

http://www.cs.utah.edu/events/conferences/cav2011/

Presentation: IDAMC NoC – Efficient Quality-of-Service Support for Mixed-Critical Networks-on-Chip
RECOMP Technical Day
Porto, Portugal - August 29, 2011.

Jonas Diemer (TU Braunschweig) gave a presentation on the Network-on-Chip used in the IDAMC platform.

Panel Session: ARTEMIS, from successful R&D to cutting-edge Innovation
(Rolf Ernst, TU Braunschweig)
ARTEMIS Strategic Research Agenda Symposium
Brussels, Belgium – October 4, 2011

In the panel session held at the European Parliament Rolf Ernst talk about the key role of embedded systems in industrial innovation. Furthermore it highlighted the benefits of ARTEMIS from the previous research projects on embedded systems e.g. FP6 and FP7.

http://www.artemis-ia.eu/jti_programme

Invited Talks:

1. **Timing Analysis of Ethernet AVB for Real-Time Systems (Jonas Diemer)**
2. **Combining Security with Reliability using Multi-core (Philip Axer)**

Symtavision News Conference
Braunschweig, Germany - October 5, 2011

The SymTA/S NewsConference is an annual event organized by the Symtavision GmbH that brings together engineers, managers, technology experts and researchers in the field of embedded real-time systems. This year continued with the successful implementation of a technical day with parallel practice and research tracks. TU Braunschweig was invited to present current research results on real-time analysis methods for multi-core systems.

Jonas Diemer (TU Braunschweig) gave a presentation on the timing analysis of Ethernet AVB. Philip Axer (TU Braunschweig) gave a presentation on the challenges of reliability and security in multicore systems for safety-critical applications

Invited Talk: Multicore Architectures for Mixed Safety Critical Applications – Challenges and Opportunities
(Rolf Ernst, TU Braunschweig)
SafeTRANS Industrial Day
Hamburg, Germany – November 08, 2011

SafeTRANS ("Safety in Transportation Systems") is a Competence Cluster combining research and development expertise in the area of complex embedded systems in transportation systems. SafeTRANS drives research in human centred design, in system and software development methods for embedded systems, as well as in safety analysis and - for avionics and rail - its integration in certification processes, driven by a harmonised strategy addressing the need of the transportation sector. The topic of the 11th SafeTRANS Industrial Day was "Development processes for Multicore".

Sharing embedded system resources among functions of different safety criticality usually leads to mixed safety and time critical embedded systems. Such mixed critical systems must combine conflicting safety and efficiency requirements and related design processes. The talk gave an overview on mixed critical system design challenges and explained how different criticalities can be properly separated in function and timing. In multicore architectures, separation is more difficult than in networks due to low level resource sharing. The talk showed the effects and provided solutions addressing multicore and manycore systems.

http://www.safetrans-de.org/en_11_Industrial_Day.php

Tutorial / Invited Talk: Multi-Core and Many-Core for Mixed-Critical Systems - Denial of Service and other Performance Challenges
(Mircea Negrean, Rolf Ernst, TU Braunschweig)
BoCSE (Bosch Conference on Systems and Software Engineering)
Ludwigsburg, Germany – November 15 – 17, 2011

The talk was part of a tutorial at the 4th BoCSE-Conference. The conference organized by Bosch brings toghether engineers, managers, technology experts from different departments of the company, from other companies and from academia. In 2011 the event had over 600 participants. The focus of the given presentation was on challenges which arise in case of integrating applications with different criticalities/different safety requirements on multi-core and many-core systems.

Invited Talk: The mixed criticality challenge to embedded system platforms
(Rolf Ernst, TU Braunschweig)
ICT.OPEN
Veldhoven, Netherlands – November 14 - 15, 2011

ICT.OPEN is the principal ICT and Computer Science research conference in the Netherlands. It features plenary key notes and invited speakers, as well as selected oral and poster presentations. The state of art in ICT and Computer Science research is presented and discussed and therefore ICT.OPEN aims to be the place to be for everybody involved or interested in ICT and Computer Science research.

The talk discussed challenges in the design of mixed critical systems with a focus on multi-core architecture. First solutions proposed in major projects which address the mixed-criticality challenge in the larger context of automotive electronics and smart buildings have been presented.

http://www.nwo.nl/nwohome.nsf/pages/NWOP_8M3AYV

TU Dortmund:

Workshop: Software & Compilers for Embedded Systems (SCOPES) 2011

St. Goar, Germany – June 27-28, 2011

SCOPES focuses on the software generation process for modern embedded systems. Topics of interest include all aspects of the compilation process, starting with suitable modelling and specification techniques and programming languages for embedded systems. The emphasis of

the workshop lies on code generation techniques for embedded processors. The exploitation of specialized instruction set characteristics is as important as the development of new optimizations for embedded application domains. Cost criteria for the entire code generation and optimization process include run time, timing predictability, energy dissipation, code size and others. Since today's embedded devices frequently consist of a multi-processor system-on-chip, the scope of this workshop is not limited to single-processor systems but particularly covers compilation techniques for MPSoC architectures.

In addition, this workshop puts a spotlight on the interactions between compilers and other components in the embedded system design process. This includes compiler support for e.g. architecture exploration during HW/SW codesign or interactions between operating systems and compilation techniques. Finally, techniques for compiler aided profiling, measurement, debugging and validation of embedded software were also covered by this workshop, because stability of embedded software is mandatory.

SCOPES 2011 was the 14th workshop in a series of workshops initially called "International Workshop on Code Generation for Embedded Processors". The name SCOPES has been used since the 4th workshop. The scope of the workshop remains software for embedded systems with emphasis on code generation (compilers) for embedded processors.

SCOPES 2011 was organized by Sander Stuijk and Henk Corporaal of TU Eindhoven and was held back-to-back with the MAP2MPSoCs workshop.

http://www.scopesconf.org/scopes-11

Workshop: 4th Workshop on Mapping Applications to MPSoCs, 2011

St. Goar, Germany – June 28-29, 2011

This is the flagship workshop of this cluster. The workshop is now a key forum for discussions in this area. Attendees expressed their strong interest to continue this series of informal workshops as a platform for discussions.

Keynote: Energy-Efficient Embedded Computing
Energy-Aware Computing (EACO) Workshop
Bristol, United Kingdom – July 13-14, 2011

P. Marwedel presented an overview of his group's work on energy models for embedded software, on the life cycle analysis of computing devices and on optimizations for scratch pad memory and GPUs.
http://www.cs.bris.ac.uk/Research/Micro/eaco-2.jsp

Tutorial: Embedded System Foundations of Cyber-Physical Systems
ARTIST Summer School in China 2011
Beijing, China – August 8-12, 2011

P. Marwedel started the summer school with a full-day tutorial on foundations of cyber-physical systems. He introduced the fundamentals of modelling, embedded system hardware, evaluations of embedded systems and the mapping of applications to platforms. Also, he gave a brief introduction to compilation for explicit memory architectures. The tutorial was based on the second edition of the presenter's text book on embedded systems. The tutorial made sure that the attendees were aware of the prerequisites of the remaining presentations of the summer school.
http://www.artist-embedded.org/artist/Overview,2239.html

Workshop: 7th Workshop on Embedded Systems Education, 2011

Taipei, Taiwan – October 13th, 2011

Embedded system education is still a very young area and frequently restricted to teaching the details of microcontroller programming. A long-term objective of this workshop is to improve the

visibility of work in the area and to stimulate the introduction of broader curricula. In 2011, P. Marwedel was again the main organizer of the workshop.

http://www.artist-embedded.org/artist/Topics-and-Focus,2305.htm

Tutorial : Energy modelling
Workshop of Cooperative research center SFB 876
Lüdenscheid, Germany – October 20th, 2011
This tutorial by P. Marwedel demonstrated global trends on the energy consumption of computing and compared the advantages of measurement-based and model-based predictions of the energy consumption in computing. The potential of saving energy through an exploitation of the memory hierarchy was shown. The tutorial closed with an introduction to the life-cycle assessment (LCA) of the energy consumption of personal computers.
http://www.sfb876.tu-dortmund.de

Trento and TU Dortmund:

Workshop: 3rd Workshop on Software Synthesis, 2011

Taipei, Taiwan – October 14th, 2011

An increasing amount of software is not written manually any more. Rather, software is synthesized from abstract models of the required functionality. Software synthesis has been implemented in various disperse communities. The workshop aimed at bringing these communities together. Presenters at this workshop presented industrial as well as academic results. The workshop was organized by P. Marwedel and A. Sangiovanni-Vincentelli and run by P. Marwedel.

http://www.artist-embedded.org/artist/Scope,2309.html

USAAR:

Workshop: Industrial Workshop at CPSWEEK2010

An industrial workshop was held at CPSWEEK 2010 in Stockholm. The second half of the workshop was devoted to predictability results. The purpose of the event was raising awareness in the industry to the problems of predictability.

-- The above is new material, not present in the Y3 deliverable --

4. Overall Assessment and Vision for the Transversal Activity

4.1 Assessment for Year 3

The level of energy at the meetings organized to foster industrial integration was excellent. In 2009, we proposed the change from Nomadic to Energy Efficient Building has had a re-sounding success. This theme is of increased interest to the European community in response to energy conservation concerns. In this respect, in 2009 a detailed plan was drafted for meetings to be held in 2010 and a modus operandi that included international interaction. The GREEMBED Conference was a result of these efforts. In 2010, we launched a new direction in the area of Synthetic Biology, with the sponsorship and participation to the 2010 International Workshop on Bio-Desing Automation. This area is bound to have a strategic impact on research world-wide. The meetings were very well attended and strong positive feedback was received also from some of the companies involves. The funding model of a NoE does not allow substantial research work to be carried out under ArtistDesign umbrella. Most of the actual research is sponsored by other means. The meeting organization and support is indeed the only leverage we can utilize to direct researchers towards a common goal. However, the budget restrictions posed by the rules used for ArtistDesign force a continuous quest for additional resources. ***The budgeting process should be made more liberal in terms of support.***

4.2 Overall Assesment since the start of the ArtistDesign NoE

The overall assessment is in line with Section 4.1 except that the workshop organizations run more smoothly as we learned better how to operate to obtain maximum results from a limited amount of resources. If we project in the future, we believe that the transversal activities can indeed play a fundamental role in ArtistDesign overall goals and as such, they should be strengthened.

4.3 Indicators for Integration

The indicators of integration are related to partners meetings with industry as well as joint papers with industrial participants. In the description of work we indicated meeting and workshops within the automotive, avionics, health-care, including synthetic biology, and energy efficiency domains and in special sessions in conferences. Both have been achieved: In chronological order.

1. The CPS Week was attended by a large number of partners in addition to representatives of all companies we are working with.
2. The Design Automation Conference was also attended by a sizable number of partners and a large group of companies including European, US and Japan groups. We organized two workshops on the car of the future that was attended by more than 200 people and that was an important event of the Conference (the overall conference lists more than 5,000 participants).
3. The WSS11 meeting at ESWEEK 2011 was a technical meeting intended to explore the impact and future outlook of software synthesis. Software design is at the core of the agenda of ArtistDesign and we believe it will have a major impact on the future of the

industry. In particular, the presence of National Istruments and its presentation gave an important input to the research community.

In addition, there have been quite a large number of joint papers with industrial partners addressing design flow issues. In particular, an invited paper on Cyber-Physical Systems appeared on January 2012 with challenges that will form the research agenda for this theme that can be considered one of the follow ups of embedded systems. The other is Systems of Systems and for that we are preparing a paper for the IEEE Systems Journal.

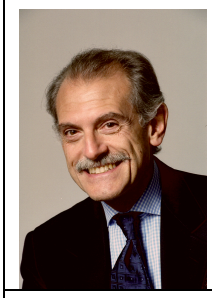
4.4 Long-Term Vision

The industry-motivated transversal activity necessitates additional care as on one hand, we need to understand the concerns of companies that have been investing substantially in embedded system design such as the ones in automotive and aerospace domains; on the other hand, we need to understand the characteristics of emerging domains such as independent living and health, energy efficient buildings and synthetic biology. In the emerging sectors, the links among the different players are not clear as yet when we look at the promises of these markets. We believe that the activity in the more traditional segments will continue along a journey that has begun several years ago and we do not expect major surprises in corralling the industrial participants as well as the ArtistDesign partners. The emerging sectors represent significant new opportunities to impact the formation of new business models and approaches. We expect that the ArtistDesign community will have to dig deep into its accumulated expertise and into its research network to help industry find its path to profitable products and services.

5. Transversal Activity Participants

-- Changes in the Cluster Participants wrt Y3 deliverable Added Martin Thorngren of KTH, Team Leader of IMEC Maya D'Hondt was replaced by Chantal Ykman-Couvreur

5.1 Core Partners

Transversal Activity Leader Activity Leader for "Industrial Integration"	
	Alberto Sangiovanni Vincentelli (Trento) www.eecs.berkeley.edu/~alberto/;
Technical role(s) within ArtistDesign	Bring in Expertise in embedded system modelling, validation, tools and methodologies and IC design. Deep involvement in cooperation with the industry: tools (co-founder Cadence and Synopsys), telecommunications (Telecom Italia), automotive (member of the GM STAB), avionics and energy efficient buildings (UTC). Participation to Venture Capital Activities in US (Walden International (Member of Advisory Board), Xseed (member of Advisory Board) and Europe (Banca Intesa Atlante Venture and Atlante Venture Sud, member of investment committee, Sofinnova, member of Advisory Board, Fondo Next, member of Investment Committee, Innogest, Member of Advisory Board). Involvement in International Boards of Directors (Cadence Design Systems and Sonics Inc (USA), Accent (EU)).
Research interests	Embedded system design methodologies and tools including modelling, validation, synthesis and formal verification, semantic foundations.
Role in leading conferences/journals/etc in the area	Program Committee Member CODES and EMSOFT. Organizer of SEEC 09 Smart and Efficient Energy Council and of the 2009 CPS Forum, Organizer of GREEMBED 2010 and 2011, of Special Sessions on Compositional Approaches (two) at DATE 2011, co-organizer and moderator of Automotive Electronics Panel at DAC 2010, co-organizer and chair of panel

	on Synthetic Biology at DAC 2010. Member of the ARTEMIS High-level Group, Governing Board, Public Authority Board and Steering Committee
Notable projects	SPEEDS - Speculative and Exploratory Design in Systems Engineering Provide a semantics based modelling methods with analysing techniques to support the construction of complex embedded systems by composing heterogeneous subsystems together with a speculative tool-supported design process. Center for Hybrid and Embedded Software Systems (CHESS) co-director Gigascale System Research Center MuSyC, Distributed Sense and Control Systems theme leader COMBEST COMponent-Based Embedded Systems design Techniques
Awards/Decorations	IEEE Fellow, Member National Academy of Engineering, Kaufmann Award for pioneering contributions to EDA, IEEE Graduate Teaching Award, Gulliemin-Cauer Award, Darlington Award, Aristotle Award, University of California Distinguished Teaching Award, IEEE/RSE Wolfson James Clerk Maxwell Medal for groundbreaking contributions that have had an exceptional impact on the development of electronics and electrical engineering or related fields, EDAC R. Newton Impact Award, Honorary Doctorate, Aalborg University

Team Leader	
	Boudewijn Haverkort (Embedded Systems Institute (ESI)) www.esi.nl
Technical role(s) within ArtistDesign	Model-based methods for embedded system engineering; collaborative research with industry
Research interests	Model-driven design and implementation of (embedded) computer-communication systems and the evaluation of their performance, dependability and performability.
Role in leading conferences/journals/etc in the area	Member of IFIP WG6.3 on "performance of communication systems" and of IFIP WG7.3 on "computer performance modelling and analysis" Fellow of the IEEE Member of the editorial board of the journal Performance Evaluation Chair of the steering committee of the IEEE Conference on Quantitative Evaluation of SysTems (QEST); http://www.qest.org/ Chair of the steering committee of the performability evaluation workshop series (PMCCS); http://www.pmccs.net/
Notable past projects	Rocks: Rigorous Dependability Analysis using Model Checking Techniques for Stochastic Systems (DFG/NWO) VOSS I and II: Validation of Stochastic Systems (DFG/NWO)

Team Leader	
	Prof. Dr. Werner Damm (OFFIS) http://www.offis.de
Technical role(s) within ArtistDesign	Bring in Expertise in embedded system modelling and validation. Deep involvement in cooperation with the automotive and avionics industry.
Research interests	His recent research covers foundational research on mathematical models of embedded systems, specification languages, hybrid systems, formal verification methods, and real-time and safety analysis. This is complemented by applied research with industrial partners in avionics, automotive, and train system application. The focus of this research is on enhancing model-based development processes with formal method-based approaches to verification, testing, and safety and real-time analysis, as well as on enabling component-based design for embedded systems.
Role in leading conferences/journals/etc in the area	Program Committee Member CAV2008 Member of the Editorial Board “Formal Methods in System Design” Chairman of the competence cluster SafeTRANS First Chairman of the ARTEMIS Innovation Cluster on Transportation
Notable projects	OMEGA - Correct Development of Real-time Embedded Systems Formal verification of embedded systems based on UML http://www-omega.imag.fr/ AVACS - Automatic Verification and Analysis of Complex Systems This project addresses the rigorous mathematical analysis of models of complex safety critical computerized systems. http://www.avacs.org/ SPEEDS - Speculative and Exploratory Design in Systems Engineering Provide a semantics based modelling method with analysing techniques to support the construction of complex embedded systems by composing heterogeneous subsystems together with a speculative tool-supported design process. http://www.speeds.eu.com/ COMBEST – Component-Based Embedded Systems design Techniques COMBEST will provide a formal framework for component based design of complex embedded systems: 1) formal integration of heterogeneous components; 2) encapsulation of components; 3) prediction of emergent key system characteristics; 4) corresponding certificates. http://www.combest.eu CESAR – Cost efficient methods and processes for safety relevant embedded systems CESAR is an ARTEMIS project which will provide

	innovations within the two engineering disciplines Requirements Engineering and Component-based Design. Furthermore, it will develop a customizable systems engineering "Reference Technology Platform" (RTP) making it possible to integrate or interoperate existing or emerging available technologies. http://www.cesarproject.eu SPES2020 – Software Platform Embedded Systems SPES2020 is a German Innovation Alliance dedicated to model-based design methods for embedded software systems across application domains. http:// www.spes2020.de

	Prof. Dr. Bernhard Josko (OFFIS) http://www.offis.de/
Technical role(s) within ARTIST2	Participating in several activities bringing in the expertise on real-time UML verification
Research interests	Modelling and analysis of embedded systems, formal verification, real-time UML, SysML
Notable projects	OMEGA - Correct Development of Real-time Embedded Systems Formal verification of embedded systems based on UML http://www-omega.imag.fr/ EASIS – Electronic Architecture and System Engineering for Integrated Safety Systems Within WP System Dependability provide formal verification guidelines http://www.easis.org SPEEDS - Speculative and Exploratory Design in Systems Engineering Provide a semantics based modelling methods with analysing techniques to support the construction of complex embedded systems by composing heterogeneous subsystems together with a speculative tool-supported design process. CESAR – Cost efficient methods and processes for safety relevant embedded systems CESAR is an ARTEMIS project which will provide innovations within the two engineering disciplines Requirements Engineering and Component-based Design. Furthermore, it will develop a customizable systems engineering "Reference Technology Platform" (RTP) making it possible to integrate or interoperate existing or emerging available technologies. Leader of sub project “Requirements Engineering” http:// www.cesarproject.eu

Core Teamleader	
	Prof. Dr.-Ing. Rolf Ernst (TU Braunschweig) http://www.ida.ing.tu-bs.de/en/home/faculty_and_staff/ernst/
Technical role(s) within ArtistDesign	Core Teamleader in Platform and MpSoC Design, Platform and MpSoC Analysis, Design for Adaptivity, Integration Driven by Industrial Applications. Affiliated Teamleader in Design for Predictability and Performance
Research interests	Research interests include embedded architectures, hardware-/software co-design, design automation, real-time systems, and embedded systems engineering.
Role in leading conferences/journals/etc in the area	Rolf Ernst chaired major international events, such as the International Conference on Computer Aided Design of VLSI (ICCAD), or the Design Automation and Test in Europe (DATE) Conference and Exhibition, and was Chair of the European Design Automation Association (EDAA). He is a founding member of the ACM Special Interest Group on Embedded System Design (SIGBED), and was a member of the first board of directors. He is an elected member (Fachkollegiat) and Deputy Spokesperson of the "Computer Science" review board of the German DFG (corresponds to NSF). He is an advisor to the German Ministry of Economics and Technology for the high-tech entrepreneurship program EXIST (www.exist.org).
Awards / Decorations	In 1995 he received the Jorck's Foundation Research Award for his research in hardware/software codesign

Team Leader	
	Senior researcher Chantal Ykman-Couvreur IMEC vzw. http://www.imec.be
Technical role(s) within ArtistDesign	Representing IMEC Smart Systems and Energy Technology division in: -Cluster: SW Synthesis, Code Generation and Timing Analysis -Cluster: Operating Systems and Networks -Cluster: Hardware Platforms and MPSoC Design -Intercluster activity: Design for Adaptivity -Intercluster activity: Integration Driven by Industrial Applications
Research interests	Ch. Ykman-Couvreur is currently active in run-time management for embedded multi-core platforms
Role in leading conferences/journals/etc in the area	Ch. Ykman-Couvreur has published in International Journals and Conferences. She is active on several program committees of international conferences and in the organization of international workshops.
Notable projects	Responsible for following FP7 European projects: GENESYS (http://www.genesys-platform.eu 2PARMA (http://www.2parma.eu) COMPLEX (http://complex.offis.de) PHARAON
Team Leader	

	Prof. Dr. Maja D'hondt IMEC vzw. http://www.imec.be
Technical role(s) within ArtistDesign	Representing IMEC Smart Systems and Energy Technology division in: -Cluster: SW Synthesis, Code Generation and Timing Analysis -Cluster: Operating Systems and Networks -Cluster: Hardware Platforms and MPSoC Design -Intercluster activity: Design for Adaptivity -Intercluster activity: Integration Driven by Industrial Applications
Research interests	Maja D'Hondt received her Master and Ph.D degrees in Computer Science from the Vrije Universiteit Brussel in Belgium in 1998 and 2004 respectively. Since 2008 she leads a team of (senior) researchers and PhD students working on run-time resource management middleware for embedded systems.
Role in leading conferences/journals/etc in the area	Maja D'Hondt has published in International Journals and Conferences. She has sat on several program committees of international conferences. She played an active role in the organization of international conferences as workshop and tutorial chair.
Notable past projects	Responsible for Scalopes ARTEMIS project (http://www.scalopes.eu/), OptiMMA IWT project (www.imec.be/OptiMMA), and Stadium IWT project (distrinet.cs.kuleuven.be/projects/stadium/).

Cluster Leader **Activity Leader & Team Leader**	
	Jan Madsen (Technical University of Denmark)
Technical role(s) within ArtistDesign	Member of the Strategic Management Board Leads Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Leader of the JPRA Activity: “Platform and MPSoC Analysis”
Research interests	Research interests include high-level synthesis, hardware/software codesign, System-on-Chip design methods, and system level modeling, integration and synthesis for embedded computer systems.
Role in leading conferences/journals/etc in the area	Program Chair and Vice-Chair of Design Automation and Test in Europe Conference. Tutorial Chair and Special Sessions Chair of Design Automation and Test in Europe Conference. General Chair, Program Chair and Workshop Chair of CODES+ISSS Conference Member of the editorial board of the journal “IEE Proceedings – Computers and Digital Techniques” Member of the technical program committee and organizing committee of several technical conferences, including the Design Automation and Test in Europe Conference, the Real-Time Systems Symposium, the Symposium on Hardware-Software Codesign, and the International Workshop on Applied Reconfigurable Computing. Danish delegate in the Governing Board of ARTEMIS JU
Awards / Decorations	In 1995 he received the Jorck's Foundation Research Award for his research in hardware/software codesign

Team Leader	
	Prof. Dr. Dr. h. c. mult. Reinhard Wilhelm (Saarland University) http://rw4.cs.uni-sb.de/people/wilhelm
Technical role(s) within ArtistDesign	Timing Analysis
Research interests	Compilers, Static Analysis, Timing Analysis
Role in leading conferences/journals/etc in the area	PC member of SCOPES, LCTES, MEMOCODE, RTSS etc. Steering committee member of EMSOFT, member at large of the steering committee of LCTES Member of the ACM SIGBED Executive Committee
Notable past projects	DAEDALUS
Awards / Decorations	Prix Gay-Lussac-Humboldt in 2007 Honorary doctorates of RWTH Aachen and Tartu University in 2008 Konrad-Zuse Medal in 2009 Federal Order of Merit in 2010
Further Information	Co-founder of AbsInt Angewandte Informatik GmbH Scientific Director of the Leibniz Center for Informatics Schloss Dagstuhl

Team Leader **Activity Leader for "Software Synthesis and Code Generation"**	
	Prof. Dr. Peter Marwedel (TU Dortmund) http://ls12-www.cs.tu-dortmund.de/~marwedel/
Technical role(s) within ArtistDesign	Cluster leader, activity leader SW Synthesis and Code Generation Improved code quality for embedded applications is the main goal of the work at Dortmund University. Due to the widening gap between processor and memory speeds, emphasis has been on improving the efficiency of memory accesses, in terms of average and worst case execution time and in terms of the energy consumption.
Research interests	Peter Marwedel's Embedded Systems Group focuses on embedded software. Particular emphasis is on compilers for embedded processors. One of the very first publications in this area, the book "Compilers for Embedded Processors", edited by Peter Marwedel and Gert Goossens, was the result of the CHIPS project, funded by the European Commission. The group's current focus is on advanced optimizations for embedded processors (e.g. by using bit-level data flow analysis) and energy-aware compilation techniques. Current research also includes high-level transformations of algorithms as well as WCET-aware code generation.
Role in leading conferences/journals/etc in the area	Member of the EDAA (European Design and Automation Association) Main Board. Editorial Board Member of the Journal "Design Automation for Embedded Systems" Editorial Board Member of the Journal of Embedded Computing. Editorial Board Member of the Microelectronics Journal. Editor of the Springer series of books on Embedded Systems (http://www.springer.com/series/8563) Co-Founder and Steering Board Chair of the SCOPES Workshop (Software and Compilers for Embedded Systems) Series. >14 years of service for the DATE conference and its predecessors (program chair: 3 times, chairman of the steering committee, European representative to ASPDAC) Various other conferences
Notable past projects	MADNESS: Methods for predictAble Design of heterogeneous Embedded Systems with adaptivity and reliability Support (http://www.madnessproject.org)

	MNEMEE: Memory maNagEMEnt technology for adaptive and efficient design of Embedded systems supported by the European Commission (http://www.mnemee.org) PREDATOR: Design for predictability and efficiency, supported by the European Commission (http://www.predator-projekt.eu) MORE: Network-centric Middleware for group communications and resource sharing across heterogeneous embedded systems, supported by the European Commission http://www.ist-more.org HiPEAC: European NoE on High-Performance Embedded Architecture and Compilation; http://www.hipeac.net MAMS: Multi-Access modular-services framework, national project funded by the German Federal Ministry of Education and Research (BMBF)Others: Various earlier projects supported by the EC, DFG etc.
Awards / Decorations	Teaching award, TU Dortmund, 2003 DATE fellow, 2008 IEEE Fellow (class of 2010)
Further Information	CEO of the Informatik Centrum Dortmund (ICD), a technology transfer centre founded in 1989. Chair of the Education Committee of TU Dortmund

Team Leader	
	Joseph Sifakis (VERIMAG) http://www-verimag.imag.fr/~sifakis/
Technical role(s) within ArtistDesign	Team Leader for Verimag. Contributes with expertise on component-based design, the BIP framework, platform-aware implementation of embedded systems, structural verification. Context-based analysis.

Team Leader	
	Saddek Bensalem (VERIMAG) http://www-verimag.imag.fr/~bensalem/
Technical role(s) within ArtistDesign	Team Leader for Verimag. Contributes with expertise on compositional modelling and verification

Team Leader	
	Prof. Martin Törngren (KTH) http:/www.md.kth.se/~martin
Technical role(s) within ArtistDesign	Team leader together with Prof. Axel Jantsch for KTH. Participation in the Modeling, Validation, Design for Adaptivity, and Industrial integration. Through its Centre for embedded systems ICES (www.ices.kth.se), KTH is establishing a systematic cooperation with industry encompassing networking, education and research. Currently active industrial domains include automotive, automation and telecom. Core technical areas for ICES are systems architecture, verification and methodology. Interactions with industry include seminars, mobility, and working groups on education and research. The main role of ICES is that of a network and catalyst, for example to create spin-off projects.
Research interests	Martin Törngren's Embedded control systems group focuses on model-based development, tool integration, architectures for embedded systems and design methodology. The group was part of the EAST-EAA project and follow up projects ATESST and ATESST2, developing the EAST-ADL modelling language. Further work has focused on architecture design methodology and model integration techniques. As part of the DySCAS project, architectures for self-configuring automotive embedded systems were developed.
Role in leading conferences/journals/etc in the area	Editorial board member of the International Journal of Embedded Systems General chair for the Euromicro real-time systems conference, 2000. Reviewing for numerous embedded systems journals and conferences including the Journal of Real-time systems.
Notable past and present projects	DICOSMOS: Swedish national project, 1993-2001, in cooperation with Volvo, Automotic control at Lund Inst. Of Technology and Computer Engineering at Chalmers, in developing control and computer codesign techniques and design methods. ARTES projects. A number of project within the now ended Swedish national effort on advanced real-time embedded systems (http://www.artes.uu.se/). ARTIST2 – The ArtistDesign predecessor network. ATESST – Advancing Traffic Efficiency and Safety through Software Technology. (www.atesst.org). DYSCAS – Dynamincally and Self-Configuring Automotive Systems

	(www.dyscas.org). ATESST2 – Advancing Traffic Efficiency and Safety through Software Technology. (www.atesst.org), ended in June 2010. CESAR - Cost-efficient methods and processes for safety relevant embedded systems, an Artemis project which started March 2009 (https://cesarproject.eu) MAENAD - Model-based Analysis & Engineering of Novel Architectures for Dependable Electric Vehicles, a new FP7 project acting as a follow-up project of ATESST2 (http://www.maenad.eu/). iFEST – industrial Framework for Embedded Systems Tools, a new Artemis project that started April 2010 (http://www.artemis-ifest.eu/)
Awards / Decorations	The ITEA achievement award 2004 for contributions in the EAST-EEA project SAAB-Scania Award 1994 for qualified contributions in distributed control systems
Further Information	Director for the Innovative Centre for Embedded Systems at KTH (http://www.kth.se/itm/centra/ices?l=en_UK)

6. Internal Reviewers for this Deliverable

- **Jan Madsen**, Technical University of Denmark
- **Martin Törngren**, KTH
- **Roberto Passerone**, Trento