



214373 ArtistDesign
Network of Excellence
on Embedded Systems Design

Project Management Report for Year 4

Executive Summary

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ArtistDesign Consortium

1. Project Objectives

The ArtistDesign NoE is the visible result of the ongoing integration of a community.

The central objective for ArtistDesign is to build on existing structures and links forged since 2001, to become a virtual Centre of Excellence in Embedded Systems Design. This has been achieved through tight integration between the central players of the European research community. These teams have already established a long-term vision for embedded systems in Europe, which advances the emergence of Embedded Systems as a mature discipline.

ArtistDesign is becoming the main focal point for dissemination in Embedded Systems Design, leveraging on well-established infrastructure and links. It will extend its dissemination activities, including Education and Training, Industrial Applications, as well as International Collaboration. ArtistDesign will establish durable relationships with industry and SMEs in the area.

ArtistDesign builds on existing international visibility and recognition, to play a leading role in structuring the area.

The research effort integrates topics, teams, and competencies, grouped into 4 Thematic Clusters: “Modelling and Validation”, “Software Synthesis, Code Generation, and Timing Analysis”, “Operating Systems and Networks”, “Platforms and MPSoC”. “Transversal Integration” covering both industrial applications and design issues aims for integration between clusters.

*-- Changes wrt Y3 deliverable –
No changes with respect to Year 3.*

2. Contact Details and Contractors Involved

2.1 Core Partners

For a complete description including web links, see:

<http://www.artist-embedded.org/artist/-ArtistDesign-Participants-.html>

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3	RWTH AACHEN	AACHEN	Germany
4	AALBORG UNIVERSITET	AALBORG	Denmark
6	ALMA MATER STUDORIUM - UNIVERSITA DI BOLOGNA	BOLOGNA	Italy
7	TECHNISCHE UNIVERSITAET BRAUNSCHWEIG	TUBS	Germany
8	UNIVERSIDAD DE CANTABRIA	CANTABRIA	Spain
9	COMMISSARIAT À L'ENERGIE ATOMIQUE	CEA	France
10	DANMARKS TEKNISKE UNIVERSITET	DTU	Denmark
11	UNIVERSITAET DORTMUND	DORTMUND	Germany
12	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	EPFL	Switzerland
13	EMBEDDED SYSTEMS INSTITUTE	ESI	Netherlands
14	ETH ZUERICH	ETH Zurich	Switzerland
15	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM	IMEC	Belgium
16	INSTITUT NAT. DE RECH. EN INFORMATIQUE & AUTOM.	INRIA	France
17	TECHNISCHE UNIVERSITAET KAISERSLAUTERN	TUKL	Germany
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19	LINKÖPINGS UNIVERSITET	LINKOPING	Sweden
20	LUNDS UNIVERSITET	ULUND	Sweden
21	MAELARDALENS HOEGSKOLA	MDH	Sweden
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29	UPPSALA UNIVERSITET	UPPSALA	Sweden
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33	University of Porto	UnivPorto	Portugal
34	University of Trento	Trento	Italy

-- Changes wrt Y3 deliverable --
No changes with respect to Year 3.

2.2 Affiliated Partners

Affiliated partners play a very strong role in the Spreading Excellence from the core partners to the research and industrial communities at large.

Affiliated partners generally play an active role in the research activities, either participating directly in research, or transferring the results directly to industry.

Each of the JPRA and JPIA activities' deliverables provides the list of the corresponding affiliated partners and roles.

Affiliated Industrial Partners

The complete set of Affiliated Industrial partners, including web links, is available online, here: <http://www.artist-embedded.org/artist/-Affiliated-Industrial-Partners-.html>

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3. Vision and Assessment of the Work Performed

ArtistDesign has financed durable integration between teams and not the concrete elements of the JPA, which most often belong to other projects. These specific technical objectives may or may not be attained (this is the essence of research as opposed to development), but we feel that the main product of ArtistDesign is the emergence of a lasting European research community, that has a significantly enhanced capacity for preparing Europe’s future.

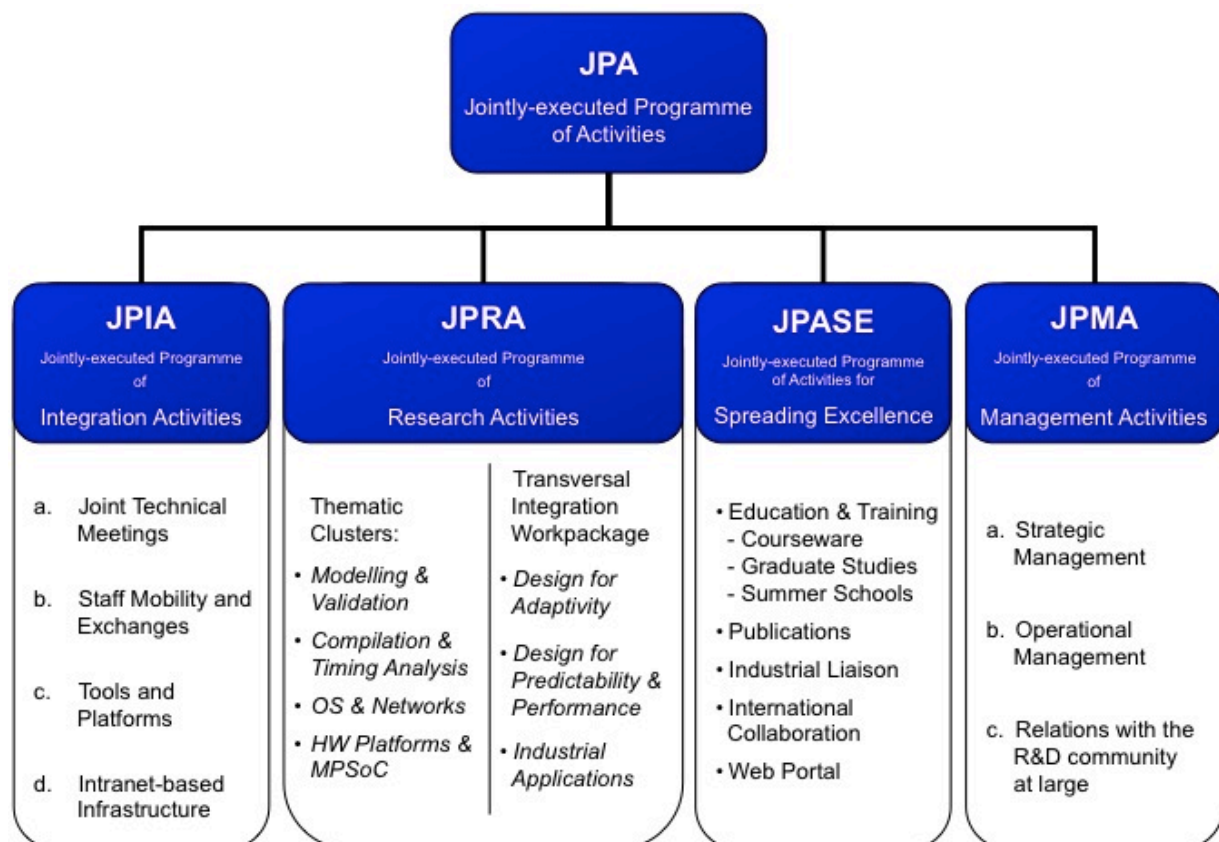
The research has been completed by work in the JPIA (Jointly Executed Programme of Integration Activities) workpackage, which aimed to transform research results into tangible tools and components, and bring teams closer together on a day to day basis.

We believe that the topics chosen provide a good coverage of the area, for embedded software and systems.

The ArtistDesign NoE is a complex construction assembled from world-leading communities, teams, and individuals. This is certainly an asset, but also a source of complexity in management. Each team has two essential characteristics: world-class excellence and strong interaction with top industrial players. ArtistDesign partners play a leading role in the different communities in embedded systems design, and they advance the state of the art in each of these.

It is difficult to abstract out a global synthesis of the overall technical achievements. This is due to the diversity and the low granularity of the actions to be covered (meetings, publications, attendance at workshops, visits, and platforms).

The following is a certainly non-exhaustive assessment of the work in the Joint Programme of Activities’ 4 main branches.



No changes with respect to Year 3.

3.1 Joint Programme of Research Activities (JPRA)

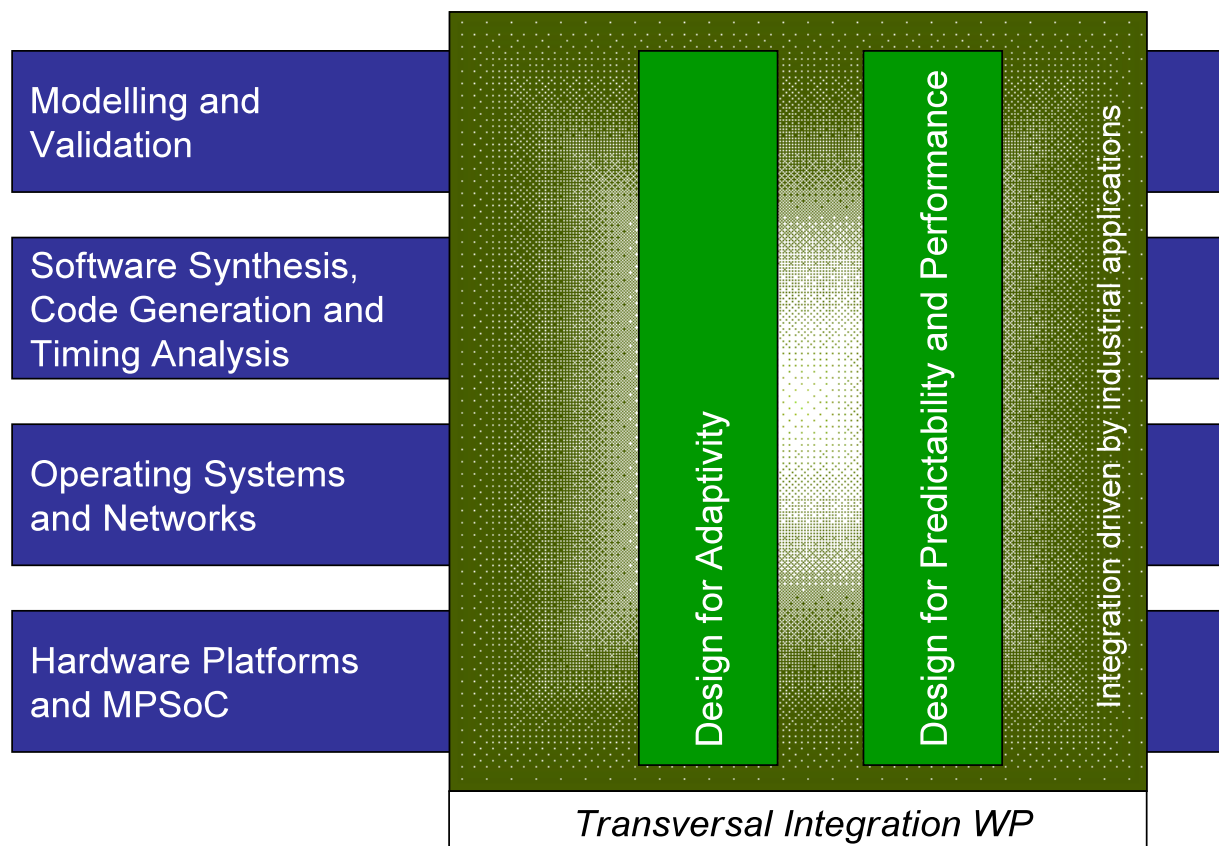
3.1.1 Structure of the Research Effort

The JPRA is composed of intra and inter-cluster research activities on cutting-edge topics in embedded systems design. While the main bulk of financing for these activities is taken up by outside programmes (Integrated Projects, National Programmes, Industrial Contracts, etc), the ArtistDesign NoE finances the extra effort derived from integrating these into a single coherent research programme.

Thus, the essential ingredient within ArtistDesign is the JPRA, which motivates the participating research teams far more than the actual financing, which is tiny in comparison with the overall research aims. It is completed by the Joint Programme of Integrating Activities (JPIA), and the Joint Programme of Activities for Spreading Excellence (JPASE), and overseen by the Joint Programme of Management Activities (JPMA).

The structure of the research activities reflects the following decomposition of the embedded systems design flow.

This design flow is composed of the following cooperating activities, starting with component-based modelling and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality. Accordingly, we have structured the area of embedded systems design into the following topics.



Modelling and Validation. Unlike other computer systems, embedded systems are strongly connected with a physical environment. A scientific foundation for embedded systems must therefore deal simultaneously with software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based. The overall objective of this activity is to develop model and component-based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. The activity brings together the most important teams in the area of model and component based design in Europe.

SW Synthesis, Code Generation and Timing Analysis. There is a continuing demand for higher performance of information processing, which stimulates using a growing amount of parallelism (including using multiple processors). This trend affects the design of embedded systems. We address issues related to multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces. Such processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Timing analysis is also affected by the trend toward the new platforms. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Also, timing analysis beyond the single processor is required. Hence, timing analysis will also consider the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors.

Operating Systems and Networks. We investigate how current real-time operating systems have to be extended or modified to support emerging real-time embedded systems characterized by a high degree of complexity, highly variable resource requirements and parallel processing such as multicores. Most embedded systems are often characterized by scarce resources in terms of processing power, memory, space, weight, energy, and cost. Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, whilst guaranteeing isolation properties. Also, to support dynamic applications with variable resource requirements or to cope with unpredictable resource availability, feedback control techniques for resource management at the operating system and application level are also investigated.

Hardware Platforms and MPSoC Design. While hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application environments is much less clear. The consequence is fragmentation: while many research teams are working on one or more of these domains, there is little communication and integration, this leads to duplication of results and overall slow progress. The teams involved in this activity have a wide-ranging research experience, which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ArtistDesign will help the participants to the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion.

Design for Adaptivity. An embedded hardware-software system is adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is a cross-cutting system characteristic that affects both hardware and software. At the software-level adaptivity is mainly concerned with flexible and adaptive resource scheduling, e.g., CPU time scheduling. At the hardware-level adaptivity includes both adaptation of operation modes, e.g., supply voltage and clock frequency, processor instruction sets, and dynamic management of hardware resources, e.g., processing elements and memory.

Design for Predictability and Performance. Many applications have strict requirements on timing, and limited resources (memory, processing power, power consumption, etc.). All systems also have increasing demands on (average) performance, which has motivated the introduction of features such as caching, pipelining, and (now becoming very prominent) multiprocessor platforms. Almost all such efficiency-increasing features drastically increase variability and decrease analyzability of response-times, etc. and thus have a detrimental effect on predictability. Since the introduction of new architectural features is inevitable, it is important to: a) develop technology and design techniques for achieving predictability of systems built on modern platforms, and b) investigate the trade-offs between performance and predictability.

Integration Driven by Industrial Applications. To have a strong impact on industry and society at large, the results of the Thematic Clusters need to be harmonized in an overall design flow that can sustain the embedded design chain from conception of the product to its implementation. The design chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics). Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company.

-- Changes wrt Y3 deliverable --
No changes with respect to Year 3.

3.1.2 Overview of the Year 4 Research Results

-- Changes wrt Y3 deliverable --
The texts in this section are entirely new.

3.1.2.1 Modelling and Validation (Cluster)

Both research activities with the cluster – the Modelling Activity and the Validation Activity – have progressed substantially within the fourth year, and with significant synergy between proposed modelling formalisms and methods and validation techniques they support:

The work on Component Modeling and Compositional Validation involved several partners that produced significant results on compositional modelling and verification:

Results on modelling can be summarized as follows:

- Composition frameworks for behaviour and properties of heterogeneous systems such as assume/guarantee reasoning, interface automata, modal transition systems as well composition frameworks for tool integration based on meta-models and model-transformations have been consolidated and applied to case studies.
- Resource modelling techniques applied to design space exploration, multi-core scheduling, performance evaluation and derivation of distributed implementations from global specifications.
- Quantitative modelling techniques for weighted automata, priced timed automata and quantitative communication models.

Results on validation can be summarized as follows:

- Quantitative Validation covering a wide range of techniques for WCET analysis, schedulability analysis, frequency analysis of timed automata, analysis of parametric quantitative models, and analysis of resource consumption using energy- and price-extensions of timed automata. These techniques use new notions of metrics and robustness.
- Cross-Layer Validation focusing on model-based testing techniques such conformance testing of real-time systems using time- and data abstractions, asynchronous testing and test-case generation for embedded Simulink, incremental testing of composite systems as well as runtime monitoring.

In addition to these results, the Cluster has endeavoured a considerable integration effort for connecting tools, joint meetings, open workshops and joint publications.

3.1.2.2 Software Synthesis, Code Generation and Timing Analysis (Cluster)

In year 4, we have seen a further proliferation of the basic techniques studied by this cluster. The importance of using multi-processor systems has been continuing to grow. Any session on programming multi-cores and multi-processor systems is filled with people. Fortunately, ArtistDesign is active in this area.

The work on software synthesis and code generation focused on the development of tools and resource-aware compilation. We developed two tools for mapping applications to multi-core or multi-processor platforms (RWTH Aachen, IMEC). Our work on resource-aware compilation

has continued with new results on energy efficiency and thermal behavior control as well as with fundamental machine-learning techniques for optimized code generation.

In program flow analysis, MDH and Tidorum have made advances towards increased soundness by developing an advanced relational value analysis that takes possible overflows and wraparounds into account. This is important for small embedded systems, where wraparounds are common

Additional activities include the organization of an international workshop on Software Synthesis (<http://www.artist-embedded.org/artist/-WSS-11-.html>) and development of new educational material on software synthesis, compilers and timing analysis in the second edition of the textbook on embedded systems by P. Marwedel.

The work on timing analysis and timing predictability has progressed significantly in two directions. The first focuses on enforcing predictability through determinism. It produced new and industrially relevant results on cache analysis and cache-aware memory allocation that have been taken up by commercial tools such as aiT from Absint. The second takes a probabilistic approach and relies on randomization to make timings on micro-level independent. Very promising initial results have been obtained.

Advances in hybrid WCET analysis methods, which include elements of measurements and testing, have been made (MDH, York, TU Vienna). Such timing models can be used to provide worst-case timing estimates early as well as small but appropriate sets of test vectors for tasks with very large input sets, and evaluation of coverage metrics for test-data generation.

Finally, the Cluster has achieved increased integration of timing analysis tools and compilation tools (TU Dortmund, TU Vienna).

3.1.2.3 *Operating Systems and Networks (Cluster)*

The work developed by the cluster involved several partners that produced significant results summarized as follows:

The work on operating systems and middleware focuses on resource reservation and predictability. We developed an implementation of a real-time scheduler in the Linux kernel, with a support for resource reservation. We also developed a programming framework to support resource reservation of concurrent real-time applications on multi-core platforms, considered by Ericsson for software development in next generation cell phones. Finally, we proposed a comprehensive taxonomy for the resources currently used in embedded real-time systems.

Our work on predictability includes cache-aware analysis and scheduling for safety-critical applications, in collaboration with the Cluster on Compilers and Timing analysis.

The Cluster also developed a middleware and communication protocol for teams of mobile robots that are self-reconfigurable and provide efficient support to intensive interactions and which have been adopted by several teams in the RoboCup Middle Size League.

The work on networks includes two toolsets. One for the design, analysis, configuration and deployment of dense WSNs. The other is the MAST (Modelling and Analysis Suite for Real-Time Applications), which was enhanced with more networking components and analysis, namely for switched networks such as AFDX. Also a number of communication protocols and tools, developed for improving predictability and adaptivity in (industrial) networked embedded systems.

The cluster teams have been involved in many European projects, had strong interaction with industry and disseminated their work through active participation in world class conferences, workshops and schools.

3.1.2.4 Hardware Platform and MPSoC Design (Cluster)

The Cluster has continued its efforts to establish an integrated modelling and design methodology that can take into account predictability and resource-awareness with focus on efficiency. This work has benefited from fruitful collaboration with the Cluster on Modelling and Validation and Timing Analysis as well as from the transversal activities on design from adaptivity and predictability.

Main results can be summarized as follows:

- Fault tolerant distributed embedded systems: We have developed results for handling both processor and communication faults in distributed real-time systems for automotive applications, based on CAN or FlexRay communication.
- Performance analysis methods: TU Braunschweig and ETH Zurich have developed very original and relevant results. They have collaborated to establish a method for coupling the tools SymTA/S and MPA. Relying on different analysis techniques each of the two tools can be individually used to evaluate the performance of embedded real-time systems. The interface developed for tool coupling now allows combining the strengths of the two tools. Evaluations have been jointly performed and the work resulted in joint publications.
- MPSoC design: Major activities on MPSoC design have focused on application parallelization, platform mapping, memory hierarchy management, application scenario exploitation, and run-time resource management, including reconfigurable systems. The outcome of these 4 years was the development of related tools, tool integration in tool chains in collaboration with several ArtistDesign partners, and highly referenced publications.
- Energy harvesting: We have developed new node level scheduling techniques (UNIBO and ETHZ) as well as network level routing algorithms (DTU), and have demonstrated that these techniques can lead to considerable extensions of the lifetime of the network. One specific outcome is the founding of the company WISPES srl (Wireless Self-Powered Electronic Systems) that aims at providing technologies and devices able to add wireless communication and local computation to the customer's monitoring and sensing activities.
- Temperature and energy aware optimization: EPFL has developed a novel online thermal management policy based on dynamic voltage and frequency scaling for high-performance 3-D systems with liquid cooling. The approach is able to gain up to 50% as compared to current state-of-the-art thermal control techniques.

Finally, the Cluster has an impressive record of joint publications, invited talks, analysis and design tools and industrial collaborations.

3.1.2.5 Design for Adaptivity (Transversal Integration activity)

The work done includes numerous highlights:

- Scheduling analysis: Efficient and effective scheduling analysis for fixed priority systems has been developed that takes into account tasks arriving and leaving the system. Furthermore, a new method for allocation and scheduling of parallel tasks in soft-real time systems (multimedia decoding) in the presence of post-silicon, process

and ageing induced variability in a nominally homogeneous target multi-core platform has been developed.

- Memory: Dynamically adaptable memory architectures for supporting dynamic real-time process loads have been developed.
- Collaboration frameworks: An adaptable cooperation-based framework for networked embedded systems with heterogeneous nodes has been developed, allowing constrained devices to cooperate with more powerful (or less congested) neighbours, to meet allocation requests and handle stringent constraints, opportunistically taking advantage of global resources and processing power.
- Service adaptation: Techniques have been developed for adapting the service request handling behaviour to the specific requirements of the services in Service Oriented Architectures (SOA). CPU contracts are used to ensure sufficient computation time for dealing with services with special requirements.
- Run-time resource management: An adaptive resource manager for distributed embedded systems aimed at multimedia applications, e.g., broadcast management systems, was developed. Considerable savings in power consumption, hardware cost and system size were reported in an industrial case study. Parallel to this a QoS based adaptive resource management system for homogeneous multicore platforms was developed.
- Run-time analysis: A distributed approach for in-system run-time performance analysis of embedded systems, complemented by a framework enabling access control and runtime-optimization through the use of distributed algorithms.
- Sensor networks: New approaches to adaptive energy management of energy harvesting system using solar cells have been developed. Based on a prediction of the future available energy, the application parameters are adapted in order to maximize the utility in a long-term perspective.
- Control techniques: A new method for optimizing the timing parameters of real-time control tasks in resource-constrained embedded systems has been derived. Also, new feedback scheduling techniques and new event-driven sampling mechanisms have been proposed.
- Adaptivity in networks: Here various ways of adapting a communication channel to varying application requirements or environmental conditions to enhance the efficiency of medium utilization have been proposed. For controlled access networks with isolated virtual channels the guaranteed bandwidth and latency can be adapted online using the Flexible Time-Triggered (FTT) paradigm on switched Ethernet, either with COTS switches (FTT-SE protocol) or enhanced ones (FTT-enabled switch).
- Programmable hardware: A new type of ultra-fault-tolerant FPGA named the eDNA architecture has been conceived all the way from development of the concept, to the implementation of a prototype, to test in a space related case study NASA JPL.
- WCET analysis: Parametric WCET bounds, where the WCET bound depends on the values of certain inputs, can be used in adaptive real-time systems where the scheduling of tasks adapts to external factors such as varying data sizes affecting the running times of tasks. A general method for parametric WCET analysis, which combines a number of advanced symbolic techniques including relational abstract

interpretation, counting of integer points in polyhedra, and parametric integer programming has been developed and implemented in the WCET analysis tool SWEET.

- Reference architectures: A reference architecture for automotive embedded systems that addresses the needs for flexible and automatic run-time reconfiguration has been proposed. The research focus was the development of technical support in terms of middleware services for a closed adaptation of distributed embedded systems. In addition to the reference architecture an information model of the control parameters that represent the target system configuration alternatives, environmental parameters, and internal conditions has been defined and a functional design has been performed.

3.1.2.6 *Design for Predictability and Performance (Transversal Integration activity)*

The Predator project has made strong progress in its attempt to reconcile Predictability with Performance. The integration of the AbsInt timing-analysis tool aiT with the WCET-aware compiler of TUDortmund is described separately. Another recent achievement of the project concerns the determination of context-switch costs, which provides support for schedulability analysis for preemptive scheduling strategies. Insights into the predictability properties of architectural features have found their way into the embedded-systems industry, e.g., as a result of collaboration in European projects. These insights, however, are still at odds with trends at the processor manufacturers side. Suppliers of time-critical embedded systems cannot find platforms with the required predictability properties on the market.

The trends to multi-core platforms presents a significant challenge to the building of predictable and performant systems, and there is still significant hesitation to migrating embedded systems to multi-cores. Significant advances on isolation and analysis techniques have been made (to a large extent by ARTIST-Design partners): progress is made, e.g., in the area of deterministic access protocols and controllers for shared resources such as buses or memory. However, the worst-case delay used in safe approximations is still often too high to be acceptable.

A good collection of insights was gathered at the PPES workshop, organized by ARTIST-Design, jointly with Predator and Merasa, as a satellite event of DATE 2011 in Grenoble. Overviews about architecture and software issues were given, e.g including a survey on predictability and performance requirements in avionics systems, and a template for, partly analytically, partly intuitively, estimating the predictability of hardware features was presented.

During year 4, development of support for the MARTE standard (initiated during ARTIST2), led by U. Cantabria, has provided increased support for scheduling and code generation. The work on integration between timing analysis tools has matured: several of the leading timing analysis tools have been integrated by efforts in the All-Times project (described in the report on Timing analysis).

A notable trend during Year 4 has been the work on reconciling predictability with performance, developing techniques for optimizing performance along several dimensions (e.g., combing WCET with average-case timing). Work in this direction (by Bologna, ETHZ, Linköping, Trento) has considered different forms of multi-objective optimization of embedded software; such possibilities also exist in the WCC compiler. Another increasingly important topic has been to make scheduling and timing analysis robust to inaccuracies in assumptions about, e.g., execution times, interferences, etc.

Work on the integration of timing analysis and compilation, in the context of the WCC compiler, aimed at removing some of the earlier restrictions. The work started at TU Dortmund considering WCET-aware basic block reordering has been finished. Unconditional branches

are avoided and the prediction of conditional branches is supported by the developed techniques. A genetic approach applies evolutionary algorithms considering the WCET of the program to optimize as fitness value with the costs of high optimization times. Thus, an integer-linear programming-based approach has been developed which determines the optimal order of basic blocks and also takes the branch prediction into account [PKFM11]. Furthermore, WCET-aware cache locking and code positioning has been improved. The integration and enhancement of a framework for the static analysis of software and hardware as announced in last year's report has been advanced. The extension of WCC's native analysis capabilities allows for novel approaches especially in the domain of multitask- and multicore-aware compilation. A much higher degree of control over system states directly affected by optimization decisions can thus be achieved. The primary effort was made in the direction of tightening timing estimations and the evaluation and improvement of cache analysis techniques with a focus on improving compiler optimizations [KFM11].

<http://ls12-www.cs.tu-dortmund.de/research/activities/wcc>

3.1.2.7 Industrial Integration (Transversal Integration activity)

This activity groups a set of industrial interactions and collaborations with ArtistDesign teams. The long-term goal is to understand industrial design methodologies and identify the research results that could be applied in these methodologies.

The activities include both technical achievements and dissemination work on the following: General Frameworks for system-level design; Applications to the Automotive Sector; Applications to Chip Design; Applications to Buildings; Applications to Wireless communication technology; Timing Analysis and Predictability; Other Applications.

The level of energy at the meetings organized to foster industrial integration was excellent. This theme is of increased interest to the European community in response to energy conservation concerns.

3.2 Joint Programme of Integration Activities (JPIA)

3.2.1 Structure of the Integration Effort

The JPIA activities promote integration of geographically dispersed teams and have long-lasting effects:

Joint Technical Meetings. Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

Staff Mobility and Exchanges. This is essential for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. Mobility is justified by and refers to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

Tools and Platforms. A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

The detailed information regarding the JPIA activities is available in the JPIA deliverable.

-- Changes wrt Y3 deliverable –
No changes with respect to Year 3.

3.2.2 Assessment

The ArtistDesign Network of Excellence is a significant evolutionary step for integrating the leading embedded systems design research teams in Europe.

The overall assessment for the WP at the end of ArtistDesign of the NoE (Jan 2008–Mar 2012) is very positive - both in terms of impact on the overall structuring and lasting integration within the consortium and more generally within the area in Europe.

- The ArtistDesign clusters have been actively pursuing operational integration through joint meetings, staff mobility, and shared platforms and tools.

- The level of activity shows that the Cluster / Activity structure and research topics defined for ArtistDesign make sense, and are viable vehicles for integrating the area. In operational terms, they generate sufficient interest for the partners and individual researchers to participate actively in the joint meetings, to exchange personnel, and to orient the tools and platforms developed to make sense within this structure.
- There is clearly a growing level of maturity for tools and platforms – and the partner teams are actively pursuing a policy of implementing tools, demonstrators, and in many cases their accompanying methodologies.
- Nonetheless, it is important to remember that these are tools and platforms for research. The aim is not necessarily always for these to lead to commercially viable tools and start-up companies. In general, they are the concrete realisation of the state-of-the-research, allowing to explore possibilities for future research and later tools (some of which may in turn lead to commercially viable products).

In particular, in Y4 we have had 52 joint technical meetings (public and private), covering a broad spectrum of topics and bringing together a wide audience.

The NoE has facilitated the mobility of 58 researchers in Year 4. This is widely considered to be the best way to integrated research teams, through the physical transfer of persons and competencies. They lead to lasting collaboration and synergy.

The level of effort has been maintained. We currently have 50 tools and platforms developed in collaboration with ArtistDesign, covering the technical domains of the NoE.

-- Changes wrt Y3 deliverable –

Updated to take into account the Year 4 results.

3.3 **Jointly-executed Programme of Activities for Spreading Excellence** (JPASE)

ArtistDesign leverages on the worldwide visibility of its activities. It is progressively creating a European embedded systems design community and spreading the “Artist culture” in all major research institutions.

To ensure that the next generation of researchers will continue in this direction we, as a consortium, have devoted a great deal of effort to Spreading Excellence, in both academic and industrial circles. Furthermore, through our links with both core and affiliated partners, we actively set up permanent links between industry and public research, based on existing partner collaborations with major industrial players in the area.

The JPASE activities spread excellence and structure the community at large. They are planned by the Strategic Management Board, and are implemented by ArtistDesign core and affiliated partners.

The NoE leverages on its members and teams, who play a main role in the organisation of world-class scientific events, to disseminate results in the area. We expect that the NoE’s structured and authoritative dissemination will have a strong effect on the community as a whole, for orienting and creating synergy for research.

3.3.1 *Education and Training*

- Courseware – The NoE has the ambition to serve as a resource and point of reference for the area, including by collecting and disseminating course materials for teaching embedded systems design.
- Graduate Studies – The NoE will provide support for selected graduate studies programmes, as the means for training engineers and researchers in embedded systems design.
- Summer Schools – The NoE will actively support and participate in summer schools and seminars in embedded systems design.
- International Workshop on Embedded Systems Education – We will continue this series of international workshops, started in ARTIST2. Dortmund leads this activity.
- Implement a high-visibility International Summer School. The ArtistDesign NoE organise each year a high-visibility international Summer School, drawing top European lecturers in Embedded Systems Design. The audience is researchers, PhD students, and engineers. This year, attendance at the summer school reached selected 100 participants.
- Training Engineers – Many partners are already active in this area, such as IMEC, EPFL, ESI, and Aalborg’s CSI. The ArtistDesign NoE will provide logistical, financial dissemination through the Web Portal.

3.3.2 *Publications in Conferences and Journals*

The ArtistDesign consortium is very active in publishing in scientific journals and conferences, as attested by the list of significant publications by the partners’ teams.

The NoE leverages on its members and teams, who are strongly implicated in collaboration with industry, to organize and structure industrial relations, and develop mutually beneficial

interactions. Furthermore, through Industrial Liaison, ArtistDesign receives useful feedback about the relevance of work directions and priorities.

3.3.3 *Links to Artemisia*

ArtistDesign has strong links to ARTEMIS, through:

- Representation on the **ARTEMIS Industry Association Steering Board**:
 - Joseph Sifakis is the CNRS representative
 - Luca Beninni is the University of Bologna representative
- Partner membership in **ARTEMIS “B”** (Research Organisations & Universities)
http://www.artemisia-association.org/member_status
 - Arne Skou is the Aalborg University representative
 - Denis Platter is the CEA representative
 - Joseph Sifakis is the CNRS-Verimag representative
 - Boudewijn Haverkort is the Embedded Systems Institute representative
 - Rudy Lauwereins is the IMEC representative
 - Jean-Pierre Banâtre is the INRIA representative
 - Eduardo Tovar is the Instituto Superior de Engenharia do Porto representative (Instituto Politécnico do Porto in ArtistDesign)
 - Gunnar Landgren is the KTH representative
 - Bernhard Josko is the OFFIS representative
 - Jan Madsen is the TU Denmark representative
 - José Carlos Gómez Sal is the University of Cantabria representative
 - Luca Benini is the University of Bologna representative
 - Farid Ouabdesselam is the Université Joseph Fourier representative
- Strong *informal* links. For example, the ArtistDesign Strategic Management Board was asked to review and comment on the latest edition of the Strategic Research Agenda, published in 2011.
- Strong representation by ArtistDesign partners in ARTEMIS projects,

3.3.4 *International Collaboration*

The ArtistDesign “*International Collaboration*” activities allow ArtistDesign to be visible internationally, and to monitor the evolution of the state of the art in the area worldwide.

International Collaboration fits into a global win-win strategy for achieving the participants’ long-range aims. Examples of activities include:

- **High-level meetings** gathering top representatives from industry, funding agencies, and research, to discuss avenues for International Collaboration, including on R&D and standards.
- **International Summers Schools** over the course of the NoE, we organized a very large number of world-class schools in Europe, China, South America, and Morocco.
- Organization and sponsoring of international conferences and schools, to disseminate recent research results, and promote the emergence of embedded systems as a discipline.

- Sponsoring for International conferences, such as CPS Week, DATE, FORMATS and ES Week.
- International Collaboration workshops, such as WESE, ISS, MemoCode, WFCD.
- International Collaboration **Publications**.

International Collaborations is implemented through collaborations with both the USA and Asia, building on existing links developing new ones.

3.3.5 *Web Portal*

The ArtistDesign Web Portal continues to be a major tool for Spreading Excellence within the Embedded Systems Community. It aims to be the focal point of reference for events and announcements of interest to the embedded systems community.

This plays a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large. We believe the web portal will be an essential mechanism for achieving integration.

It acts as a repository of knowledge in the area, including courseware, information about standards, methods and tools, research publications and results. This web portal will be made available within the NoE core and affiliated partners, and to other parties.

This repository is to be the reference for the embedded systems design community. It includes several features that help keep it coherent and up to date:

- Authorised users (principally, the ARTIST partners) can access the back end of the site to modify and update information directly. The changes are immediately visible on the site, which greatly streamlines the updating process.
- It's possible to track changes and go back to previous versions of individual web pages.
- Events are automatically sorted by date, and transferred to 'Past Events'. When appropriate.
- Structural information (hierarchy of pages) is maintained automatically.
- Ergonomics are set for the entire site. The "look and feel" of the site is always homogeneous throughout the site. It's possible to change these ergonomics, and these changes are applied homogeneously throughout the site, via automated mechanisms.

The ArtistDesign Web Portal offers information about:

- **Workshops, Conferences, Schools and Seminars**
Provide information about the main scientific events in the area, and in particular those organised by ArtistDesign.
- **International Collaboration**
Advertise the ArtistDesign International Collaboration events, and provide pointers to the most visible International Projects (either about significant projects outside Europe, or joint International Collaboration projects).
- **Publications**
Publications from core partners, with emphasis on Position Papers, White Papers, etc. that may have a particularly deep impact.
- **Course Materials Available Online**
The web portal will centralize course materials from as many sources as possible, to make them available to the general public.

-- Changes wrt Y3 deliverable –
Updated to reflect changes in Y4.

3.4 Managing the Network of Excellence (JPMA)

We believe that the current two-tiered Management structure - dividing the management amongst cluster leaders and the Strategic Management Board composed of both cluster leaders and a limited number of other selected prominent core partners – has been the right one for managing such a large research entity. It has provided the right combination of flexibility and accountability, while leaving room for innovation and evolution.

-- Changes wrt Y3 deliverable –
No changes with respect to Year 3.

4. Reviewers' Recommendations

4.1 Recommendation 1

Continue efforts for increasing tool interoperability, to ease deployment towards industry by allowing the building of integrated development environments.

This recommendation is addressed directly on a case by case basis for each tool developed by the partners, in D3-1.0-Y4 "Jointly-executed Programme of Integrating Activities" (JPJA), section 4 "Tools and Platforms".

4.2 Recommendation 2

Develop use cases and scenarios inspired by various industrial sectors.

Focus this use cases and scenarios to target more deeply various, even though limited, industrial sectors for design flows and related tool chains so as to guide future transitioning, which would secure the mutual understanding of the research outcome by the industrials and the requirements to have this outcome successfully deployed (acceptance through integration in a seamless development environment). Objective should be to build a success story that would then be supportive for raising interest of the industrial players.

This recommendation is also addressed directly on a case by case basis for each tool developed by the partners, in D3-1.0-Y4 "Jointly-executed Programme of Integrating Activities" (JPJA), section 4 "Tools and Platforms".

4.3 Recommendation 3

Increase inter-cluster coordination by exploiting common focus on MC and MPSoC

This recommendation is addressed in the Hardware Platforms and MPSoC cluster's deliverables: D2-(0.2e)-Y4, D12-(6.1)-Y4, and D13-(6.2)-Y4.

4.4 Recommendation 4

Document the insights gained during the last four years in special issues, and other publication forms – including position papers.

4.4.1 Modelling and Validation

Insights gained

Both research activities with the cluster – the *Modeling Activity* and the *Validation Activity* – have progressed substantially within the four years of the project, and with significant synergy between proposed modeling formalisms and methods and validation techniques they support:

Within the sub-activity *Component Modeling*, the main focus was on defining and composing models with heterogeneous semantics. We considered rich models including non-functional issues, architectures and assumptions on the environment (contracts) and corresponding

modeling and/or synthesis environments. Some of the most visible achievements on modeling have been obtained by collaboration in multi-partner projects that mostly have evolved from collaborations within ARTIST. In particular, the European projects ACROSS, ATTEST (1 and 2), CESAR, COMBEST and SPEEDS have been set up due to collaborations in ARTIST and have come up with important results.

Within the sub-activity *Resource Modeling*, we studied the design of resource-constrained systems, where the resource can be quantitative (e.g. energy consumption) or not (e.g. shared memory access). In particular, we considered here problems related to scheduling and resource allocation, to Design Space Exploration and to modeling for performance. The methods and tools developed by the cluster partners have been applied to real-world applications, for example the thermal behavior of an MRI scanner and printers, the Salzburg Helicopter platform, and energy regulation for intelligent buildings.

Within the sub-activity *Quantitative Modeling*, we specifically focused on design frameworks for quantitative modeling. We have mainly focused on timing and probabilities, but also on multi-valued evaluation. We have in particular also considered the extraction of quantitative properties from non quantitative models, as well as models and theories for non-usual “quantities” such as evolvability, extendability, flexibility and robustness. There was an important focus on synthesis.

Within the sub-activity *Compositional Validation* the main focus has been on methods for deriving non-functional properties from properties of their components, with the purpose of developing scalable compositional techniques for performance analysis and verification. Also validation methods based on abstractions and refinements for quantitative models have been developed.

Within sub-activity *Quantitative Validation*, the focus was on design frameworks for quantitative modeling, in particular Markov models, timed automata, priced timed automata, memory models involving stacks and queue and linear hybrid. A main achievement has been the wealth of algorithmic techniques allowing for efficient and scalable validation of formalism whose expressive power was previously out of reach. A particular scalable technique which has emerged is that of statistical model checking which allows several performance properties of very rich models to be established on the basis of simulation *up to a desired level of confidence*.

Within the sub-activity *Cross-Layer Validation* a substantial line of results have been obtained with respect to improved schedulability analysis and WCET analysis supporting multiprocessor and multi-core applications. The methods include WCET analysis and schedulability analysis addressing mixed-criticality systems including tool implementation using model checking, as well as introduction new task models (e.g. Digraph based) allowing for more scalable and efficient schedulability analysis. Main results within *Cross-Layer Validation* concerns automatic controller synthesis from various rich game models (timed and probabilistic) with possible partial observability, and with a number of industrial successful application already having been achieved (e.g. the automatic synthesis of climate control in pig-stable, and synthesis of optimal control of hydraulic pumps). This shows that the distance from fundamental theoretical breakthroughs to industrial impact may be very short. Also, a number of results have been obtained with respect to conformance testing of non-functional properties based on quantitative model. Finally, within the theory of timed automata substantial effort has been made towards the analysis of their robustness: i.e. to what extent does the realization of the model on a non-perfect platform preserve properties already established.

Note that the cluster has organised relatively few closed ARTIST meetings, but we considered more interesting to meet at the margin of conferences and workshops organised by the cluster partners or collaborators from other ARTIST clusters. The organisation activities of the cluster and the intervention of cluster members as invited speakers of conferences and summer

schools have been quite consequent, as can be seen from the list provided in the activity reports of the cluster.

Bibliography

2008

Thomas A. Henzinger. Two challenges in embedded systems design: Predictability and robustness. *Philosophical Transactions of the Royal Society A* 366:3727-3736, 2008

G.M. Bonnema, P.D. Borches, Design with Overview - how to survive in complex organizations, *Proceedings of INCOSE*. 2008

[Mul08c] G. Muller, When and What to Standardize; An Architecture Perspective, *INCOSE Proceedings*. 2008

A.Sangiovanni-Vincentelli. Is a Unified Methodology for System-Level Design Possible? *IEEE Design and Test of Computers, Special Issue on Design in the Late and Post-Silicon Eras*, Vol. 25, N. 4, pp. 346-358, July-August 2008.

Susanne Graf. Special issue on "Omega -- Correct development of Real Time Embedded Systems". In *SoSyM, int. Journal on Software & Systems Modelling* vol. 7 (2) 2008

W Damm, B. Josko, A. Metzner, M. Di Natale, H. Kopetz, A. Sangiovanni Vincentelli. *Software Components for Reliable Automotive Systems*. In *Proceedings Date*, 2008.

Thomas A. Henzinger *Grand Challenges for Real-Time Systems*. 20th Euromicro Conference on Real-Time Systems (ECRTS), Prague, Czech Republic, July 2008

Thomas A. Henzinger. "Challenges in Embedded Systems Design: Predictability and Robustness. Invited lecture, Royal Society Meeting: From Computers to Ubiquitous Computing, London, United Kingdom, March 2008

Joseph Sifakis. *Embedded Systems Challenges and Research Directions*. Onassis Foundation, The 2008 Lectures in Computer Science: Embedded Systems: Theory and Applications, July 2008, Heraklion Greece
<http://www.forth.gr/onassis/lectures/2008-07-21/programme.html>

K. Chatterjee, L. Doyen, T. Henzinger. *Quantitative Languages*, in *Computer Science Logic (CSL'08)*, 2008.

2009

Model-Based Development of Middleware for Self-Configurable Embedded Real-Time Systems: Experiences from the DySCAS Project. Tahir Naseer Qureshi, Magnus Persson, DeJiu Chen, Martin Törngren and Lei Feng. Work-in-Progress session at Model-Driven Development for Distributed Real-Time Embedded Systems Summer School (MDD4DRES), Aussois, France, April 22, 2009

Robert Passerone, Imen Ben Hafaiedh, Albert Benveniste, Daniela Cancila, Arnaud Cuccuru, Wermer Damm, Alberto Ferrari, Sébastien Gérard, Susanne Graf, Bernhard Josko, L. Mangeruca, T. Peikenkamp, Alberto Sangiovanni-Vincentelli and François Terrier, Meta-models in Europe: Languages, Tools and Applications, in IEEE Design & Test of Computers (IEEE Computer Society), Special Issue on Metamodeling for Design and Test, Volume 26, Number 3, pp. 38-53, Mai/June 2009.

Philippe Cuenot, Patrik Frey, Rolf Johansson, Henrik Lönn, Yiannis Papadopoulos, Mark-Oliver Reiser, Anders Sandberg, David Servat, Ramin Tavakoli Kolagari, Martin Törngren, Matthias Weber. The EAST-ADL Architecture Description Language for Automotive Embedded Software. Invited chapter in the LNCS volume on "Model-Based Engineering of Embedded Real-Time Systems", Holger Giese, Bernard Rumpe, Bernard Schätz, Editors. 2009

Reinhard Wilhelm, Daniel Grund, Jan Reineke, Marc Schlickling, Markus Pister, and Christian Ferdinand, Memory Hierarchies, Pipelines, and Buses for Future Architectures in Time-Critical Embedded Systems. Systems IEEE Transactions on CAD, Special Issue on DATE 08 Automotive Day Volume: 28 Issue: 7 July 2009

Christoph Kirsch, Invited Panelist. What are visionary and futuristic domains where advances in CPS will have broad impact? CPSWEEK 2009, San Francisco

2010

A. David, K.G. Larsen, U. Nyman, A. Legay, and A. Wasowski. Methodologies for specification of real-time systems using timed i/o automata. In Proceedings of FMCO 2009, Lecture Notes in Computer Science

2011

Patricia Bouyer, Ulrich Fahrenberg, Kim G. Larsen, and Nicolas Markey. Quantitative modelling and analysis of embedded systems. Communications of the ACM, 2011. Invited paper.

Joseph Sifakis A vision for computer science - the system perspective. - Central Europ. J. Computer Science

Methods and tools for component-based system design. Joseph Sifakis - Design,

Automation and Test in Europe, DATE 2011, Grenoble, France, March 14-18, 2011

Patricia Derler, Edward Lee and Alberto Sangiovanni Vincentelli, Modeling Cyber–Physical Systems, Proceedings of the IEEE, Vol. 100, n.1, January 2012, invited paper.

P. Nuzzo, A. Sangiovanni Vincentelli, X. Sun, A. Puggelli, A Methodology for the Design of Analog Integrated Interfaces Using Contracts, IEEE Sensors Journal, 2012, invited paper.

4.4.2 SW Synthesis, Code Generation and Timing Analysis

Insights gained

The cluster made good progress in all the areas of its scope and also contributed to overlapping and neighboring areas.

- For code generation, upcoming MPSoCs were considered to be the major challenge. When the network started, appropriate tools were hardly visible. Given the novelty of the aims and goals, we could not expect to be able to just integrate existing tools. Instead of starting the development of tools from resources of the network, we focused on interfacing the relevant researchers and to reach out to specialists beyond the network, including non-European partners. During the lifetime of the network, several new tools for this problem were designed, each one with a slightly different goal. At the end of 2011, several tools are available: including DOL (ETH Zürich), Daedalus (Univ. Leiden and Amsterdam), MAPS (RWTH Aachen), Mnemee (IMEC, Dortmund, TU Eindhoven and others), SystemCodesigner (Univ. Erlangen Nuremberg), Hopes (Seoul National University) and a tool from the City University of Hong Kong. In addition, many initiatives support the development of software for multi-core processors. In total, the scene has changed significantly since the proposal of this network was written. Time will tell, which of these approaches will be commercially successful and which not.
- Resource-aware compilation has also seen a good amount of attention. In particular, energy-aware compilation has become one particular aspect of saving energy and has been linked to green computing. In this sense, it has become included in a mega-trend.
- While the problem of mapping applications to MPSoCs is not yet completely solved, the next problem in code generation has popped up. General purpose computing on graphical processing units (GPGPU) has been found to offer dramatic potential for an increased performance. Researchers at TU Dortmund have also demonstrated that GPGPU also leads to the corresponding savings in consumed energy (more precisely, in the amount of electrical energy converted into heat). However, GPGPU programming can be rather cumbersome and advanced code generation techniques are required to get around this issue. This does very naturally lead to the necessity for synergies between high performance computing and code generation for embedded systems.
- Software synthesis is based on techniques which synthesize software from models in a model-based design environment. Software synthesis, if compared to manually written software, has the potential of providing safer software at a reduced development time. Techniques for software synthesis have been proposed in different communities, not all of which could be included as partners of our cluster. Therefore, we focused on attracting these communities to our workshop on software synthesis. This approach worked well. In 2011, we attracted top researchers to the workshop. More communication between these

researchers is still required. We expect more research to be performed in this area in the future.

- The cluster has also made good progress advancing the state of the art in timing analysis and timing predictability. In this area, we have achieved significant results for single-core systems with single or multiple tasks. For multi-processor systems, important design principles for ensuring timing predictability have been formulated and are being evaluated. Work on more pragmatic, test-based methods has also progressed significantly.
- One of the key achievements is the integration of timing analysis and compilers. In cooperation with AbsInt and Saarland University, TU Dortmund has implemented the WCET-aware compiler WCC. WCC incorporates a tight integration of timing analysis into compiler optimizations. The potential for making standard optimizations WCET-aware has been explored in depth. It turned out that the largest potential is in exploiting the memory hierarchy. It was demonstrated that scratchpads offer a large potential for WCET-improvements, but even WCET-aware register allocation can contribute toward WCET-efficiency. Recent extensions include code generation beyond the TriCore architecture, the support of multi-processing and multi-processors as well as multiple objectives.
- The level of collaboration between partners was significant. In addition to collaborative research, tools and prototypes have been developed and tools are integrated. This level of integration is indicative of the successful collaborative structure of the cluster.
- In year 1, many teams have analyzed the requirements and started to work. In year 2, initial versions of tools became available. In year 3, these tools have started to see widespread use. This use has continued in year 4. Also, several teams extended their scope well beyond the classical code synthesis, code generation and timing analysis areas. Resource aware design, energy efficiency, timing predictability and multi-cores are now found in several application areas and ArtistDesign stimulated this spreading of techniques.

Bibliography

Andreas Ermedahl and Peter Puschner, eds. Journal of Systems Architecture, Volume 57, Issue 7, Pages 675-734 (August 2011), special issue on Worst-Case Execution-Time Analysis

4.4.3 *Operating Systems and Networks*

Insights gained

During the 4 years of activity within the NoE, significant results have been achieved in a number of areas (the main ones being listed in section 2,1 of the three deliverables from this activity), but in terms of an overview the international resource management/scheduling community has been primarily concerned with the topic of multi-core architectures and multiprocessor allocation and scheduling issues. Considerable and significant work has been published by ArtistDesign partners (and of course by others internationally). Five years ago there were a large number of open issues; some of which still remain, but the research landscape is now much clearer. For example, it is now known that for the Sporadic task model (the more general of the usually employed task models) an optimal allocation of tasks or jobs to processors is intractable. For partitioned systems effective priority assignment schemes now exist that make them almost as effective as dynamic placement schemes. Empirical studies have confirmed this view (as partitioned schemes are much more efficient to implement). For systems with significant number of large tasks (that themselves require over 50% of a processor) semi-partitioned approaches now seem to be the most appropriate

schemes to use in industrial engineering practice. As well as the task/job allocation and scheduling issues, multi-core platforms have also lead to increased attention been given to on-chip networking and shared-bus traffic control. The latter issue is leading to a merging of the previously separate research areas of scheduling analysis and worst-case execution time analysis.

More particularly in Y4:

- The implementation of a real-time scheduler in the Linux kernel, with a support for resource reservation.
- A programming framework to support resource reservation of concurrent real-time applications on multi-core platforms, considered by Ericsson for software development in next generation cell phones.
- The integration of cache-aware analysis and limited-preemptive scheduling (together with the Cluster on Compilers and Timing Analysis) to increase predictability as well as efficiency of safety critical applications. The work has been carried out in collaboration with Airbus (for avionic applications) and Bosch (for automotive systems).
- The toolset to design, analyse, configure and deploy dense WSNs, in part built within the ARTEMIS EMMON project, including the Open-ZB ZigBee protocol stack and the Z monitor.
- A middleware and communication protocol for teams of mobile robots that are self-reconfigurable and provide efficient support to intensive interactions and which have been adopted by several teams in the RoboCup Middle Size League.
- The MAST suite (Modelling and Analysis Suite for Real-Time Applications), which was enhanced with more networking components and analysis, namely for switched networks such as AFDX;
- A number of communication protocols and tools, developed for improving predictability and adaptivity in (industrial) networked embedded systems.
- The development of a comprehensive taxonomy for the resources currently used in embedded real-time systems.

Bibliography

1. R.I. Davis and A. Burns, A Survey of Hard Real-Time Scheduling for Multiprocessor Systems, ACM Computing Surveys, 43 (4), Article 35, October 2011.
2. "Special Issue on Real-Time and Network Systems," Sanjoy Baruah and Yves Sorel, Eds., Real-Time Systems, Vol. 48, No. 1, January 2012.
3. "Special Issue on Real Time Systems Resource Management," James H. Anderson Ed., Real-Time Systems, Vol. 47, No. 5, September 2011.
4. "Special Issue on Embedded and Real-time Computing Systems and Applications," Eduardo Tovar, Ed., Real-Time Systems, Vol. 47, No. 3, May 2011.
5. "Special Issue on Energy Aware Real-Time Systems," Daniel Mossé, Julius Leite and Dara Kusic, Eds., Real-Time Systems, Vol. 47, No. 2, March 2011.
6. "Special Issue on Real-Time and Network Systems," Maryline Chetto and Mikael Sjödin, Eds., Real-Time Systems, Vol. 46, No. 3, December 2010.
7. "Special Issue on Euromicro Conference on Real-Time Systems," Isabelle Puaut, Ed., Real-Time Systems, Vol. 46, No. 1, September 2010.

8. "Special Issue on Real-Time Networking Systems," Pascale Minet, Ed., Real-Time Systems, Vol. 43, No. 2, October 2009.
9. "Special Issue on Euromicro Conference on Real-Time Systems," Alan Burns, Ed., Real-Time Systems, Vol. 43, No. 1, September 2009.
10. "Special Issue on Euromicro Conference on Real-Time Systems (ECRTS 2007)," Michael González Harbour, Ed., Real-Time Systems, Vol. 40, No. 3, December 2008.
11. "Special Issue on Euromicro Conference on Real-Time Systems (ECRTS 2006)," Giuseppe Lipari, Ed., Real-Time Systems, Vol. 39, No. 1-3, August 2008.
12. "Special Section on Real-Time Applications and Tools Design," Giorgio Buttazzo and Tei-Wei Kuo, Eds., in IEEE Transactions on Industrial Informatics, Vol. 6, No. 4, November 2010.
13. "Special Issue on Real-Time Systems - Part II," Giorgio Buttazzo and Tei-Wei Kuo, Eds., in IEEE Transactions on Industrial Informatics, Vol. 5, No. 1, February 2009.
14. "Special Issue on Real-Time Systems - Part I," Giorgio Buttazzo and Tei-Wei Kuo, Eds., in IEEE Transactions on Industrial Informatics, Vol. 4, No. 4, November 2008.

4.4.4 Hardware Platforms and MPSoC Design

Insights gained

A short summary of a few of the insights gained are given below:

- **Fault tolerance:** One of the important results produced by the cluster is the approach developed by Linköping University and DTU to the analysis and design of safety critical, fault tolerant embedded applications with soft and hard real-time constraints. Techniques have been developed to handle both processor and communication faults in distributed real-time systems based on CAN or FlexRay communication. The goal is to guarantee the deadlines for the hard processes even in the case of faults, while maximizing the overall utility.

One of the very important insights gained is that a cross-layer approach to the problem is significantly increasing the efficiency of solutions. Thus, a solution in which hardware and software fault tolerance techniques are combined, has been proposed. The basic trade-off is between processor hardening in hardware and process re-execution in software which, together, have to provide the required levels of fault tolerance against transient faults with the lowest-possible system costs. In this context, design optimization heuristics have been developed, to select the fault-tolerant architecture and decide process mapping such that the system cost is minimized, deadlines are satisfied, and the reliability requirements are fulfilled. Experiments have shown that, by selecting the appropriate level of hardware hardening and software re-executions, we can satisfy the reliability and time constraints of the applications with considerable reduction of the total cost. Another insight the two groups had over the course of collaboration is that the design of safety-critical systems has to take into account the practical realities of the field, i.e., that many of these applications are mixed-criticality and that they have to be implemented on multicores and certified, which is very costly. Out of this insight, a new EU project called RECOMP (Reduced Certification Costs for Trusted Multi-core Platforms) was started, and new research on mixed-criticality applications on multicores has been undertaken.

- **Fault tolerant distributed embedded systems:** Linköping and DTU have collaborated on fault tolerance, in particular related to automotive systems. The work covers approaches to

handle both processor and communication faults in distributed real-time systems based on CAN or FlexRay communication. Several timing analysis and cost optimisation methods have been proposed. The work resulted in highly referenced publications, a DATE best paper award, invited talks at major conferences.

- **Predictable Real-Time Systems on Multiprocessor Architectures:** A clear trend in modern embedded systems is towards implementation on multicore architectures. A fundamental problem in this context is to provide predictability in the presence of a shared communication infrastructure. The traffic on the bus does not solely originate from data transfers due to data dependencies between tasks, but is also affected by memory transfers as result of cache misses. In this context, the groups in Linköping and Bologna have cooperated towards the development of an efficient technique to provide predictable implementations of hard real-time applications on multiprocessor systems with shared communication infrastructure.

One important insight gained is that an efficient predictable implementation is possible on top of a TDMA bus protocol. Bus access policies and bus access scheduling algorithms have been developed which (1) guarantee predictability and (2) provide efficiency in terms of system performance (worst case and average delays). Another important insight gained is that, with adequate optimization techniques, it is possible to achieve both worst and average case performance optimizations. Thus, we have proposed a technique for optimizing the average case and the worst case simultaneously, allowing for a good average-case execution in the context of hard worst case constraints.

- **MPSoC Design:** The major activities of IMEC focused on the following challenges in MP-SoC design: application parallelization, memory hierarchy management, application scenario exploitation, and run-time resource management. The outcome of these 4 years was the development of related tools, tool integration in tool chains in collaboration with several ArtistDesign partners, and highly referenced publications.
- **Emerging technologies – Biochips:** A new and emerging research field related to embedded systems is that of design optimization for digital microfluidic biochips. Microfluidic biochips (also referred to as lab-on-a-chip) represent a promising alternative to conventional biochemical laboratories, and are able to integrate on-chip all the necessary functions for biochemical analysis using microfluidics, such as, transport, splitting, merging, dispensing, mixing, and detection.

One important insight is that digital microfluidic biochips are expected to be integrated with microelectronic components in next generation system-on-chips. Consequently, models and techniques for the analysis and design of such systems are needed, including “biochemical compilers” which are able to efficiently map a biochemical application onto digital microfluidic biochip. DTU has shown that many of the techniques and methods used for MPSoC can be adapted to solve problems like scheduling, allocation and mapping for both droplet-based and continuous flow-based microfluidic biochips.

- **Energy Harvesting:** Powering a wireless sensor network by harvesting energy from the environment, allows for obtaining zero-power systems. However, there are major challenges when having to synchronize and compute with unreliable energy resources. Partner from the MPSoC cluster have developed new node level scheduling techniques (UNIBO and ETHZ) as well as network level routing algorithms (DTU).

One important insight is that these technologies can lead to considerable extensions of the lifetime of the network. One specific outcome is the founding of the company WISPES srl (Wireless Self-Powered Electronic Systems) which aims at providing technologies and devices able to add wireless communication and local computation to the customer's monitoring and sensing activities. Core technology is consists of small non intrusive self-powered sensors able to bring a real time overview of the surrounding environment

- **Performance analysis methods:** Over the last years, the intense activity on developing performance analysis methods for multi- and many-core systems led to valuable solutions that have been published in different international journals and conference proceedings. Collaborations and discussions with members of the Timing Analysis Cluster helped to address challenges in the analysis of multi-core systems with shared resources. Some of the developed analysis methods were prototypically implemented (in the tool SymTA/S) and used in collaboration with industrial partners for the analysis of realistic use cases (e.g. in the automotive domain). This has increased the acceptance of formal analysis methods and triggered the integration of the research solutions in the commercially available version of the tool SymTA/S. The theoretical and practical results of the last four years are further exploited in other research projects, e.g. in the project “ModeWaves” (financed by the German Research Foundation / DFG) which deals with the timing analysis of multi-mode systems or in the ARTEMIS project “RECOMP” (Reduced Certification Costs for Trusted Multi-core Platforms) which aims at establishing methods, tools and platforms for cost-efficient certification and re-certification of safety-critical multi-core systems. Worth to be highlighted is also the joint work of TU Braunschweig and ETH Zurich on system level performance analysis methods for distributed systems. The two groups established a method for coupling the tools SymTA/S and MPA. Relying on different analysis techniques each of the two tools can be individually used to evaluate the performance of embedded real-time systems. The interface developed for tool coupling now allows combining the strengths of the two tools. Evaluations have been jointly performed and the work resulted in joint publications.
- **MPSoC design:** Major activities on MPSoC design have focused on application parallelization, platform mapping, memory hierarchy management, application scenario exploitation, and run-time resource management, including reconfigurable systems. The outcome of these 4 years was the development of related tools, tool integration in tool chains in collaboration with several ArtistDesign partners, and highly referenced publications.
- **Energy harvesting:** Powering a wireless sensor network by harvesting energy from the environment, allows for obtaining zero-power systems. However, there are major challenges when having to synchronize and compute with unreliable energy resources. Partner from the MPSoC cluster have developed new node level scheduling techniques (UNIBO and ETHZ) as well as network level routing algorithms (DTU), and have demonstrated that these techniques can lead to considerable extensions of the lifetime of the network. One specific outcome is the founding of the company WISPES srl (Wireless Self-Powered Electronic Systems) which aims at providing technologies and devices able to add wireless communication and local computation to the customer's monitoring and sensing activities. Core technology consists of small non intrusive self-powered sensors able to bring a real time overview of the surrounding environment
- **Temperature and energy aware optimization:** EPFL has developed a novel online thermal management policy based on dynamic voltage and frequency scaling for high-performance 3-D systems with liquid cooling. The approach is able to gain up to 50% as compared to current state-of-the-art thermal control techniques.

Bibliography

Keynote : Certification of Trusted MPSoC Platforms
(Rolf Ernst, TU Braunschweig)

International Forum on Embedded MPSoC and Multicore, MPSoC'2010
Gifu, Japan - June 29, 2010

Tutorial: Modeling and Analyzing Real-Time Multiprocessor Systems
(Simon Schliecker, TU Braunschweig, Lothar Thiele, ETHZ and other participants)
Embedded Systems Week (ESWeek) 2010
Scottsdale AZ, USA, October 24 -29, 2010

Invited Talk: Trusted MpSoC Platforms for Safety Related Applications
(Rolf Ernst, TU Braunschweig)
Coolchips Symposium
Yokohama, Japan – April 20 - 22, 2011(per video conference)

Invited Talk: Multicore Architectures for Mixed Safety Critical Applications – Challenges and Opportunities
(Rolf Ernst, TU Braunschweig)
SafeTRANS Industrial Day
Hamburg, Germany – November 08, 2011

Simon Schliecker, Jonas Rox, Mircea Negrean, Kai Richter, Marek Jersak and Rolf Ernst,
"System Level Performance Analysis for Real-Time Automotive Multi-Core and Network Architectures,"
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, vol. 28, No. 7, pp. 979-992, July 2009

Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst and Michael González Harbour, "Influence of different abstractions on the performance analysis of distributed hard real-time systems,"
Journal Design Automation for Embedded Systems (available as "online first", April 2008), vol. 13, No. 1, pp. 27-49, June 2009

Simon Schliecker, Mircea Negrean und Rolf Ernst, "Response Time Analysis in Multicore ECUs with Shared Resources" IEEE Transactions on Industrial Informatics, vol. 5, No. 4, November 2009

Philip Axer, Jonas Diemer, Mircea Negrean, Maurice Sebastian, Simon Schliecker, und Rolf Ernst, "Mastering MPSoCs for Mixed-Critical Applications" IPSJ Transactions on System LSI Design Methodology, vol. 4, August 2011

Philip Axer, Maurice Sebastian, und Rolf Ernst, "Reliability Analysis for MPSoCs with Mixed-Critical, Hard Real-Time Constraints" in Proc. Intl. Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), (Taiwan), Oktober 2011

Invited talk: Synthesis of Fault-Tolerant Embedded Systems,
DATE 2008 Conference, Munich, Germany - March 10, 2008

Speaker: Petru Eles

Invited talk: Scheduling and Optimization of Fault-Tolerant Embedded Systems,
ACM SIGPLAN/SIGBED Conference on Languages, Compilers, Tools and Theory for Embedded Systems (LCTES 2011), Chicago, IL, USA, 12-14 April 2011.

Speaker: Petru Eles

Invited talk: Predictable Implementation of Real-Time Applications on Multiprocessor Systems on Chip,
Ninth International Workshop on Worst-Case Execution Time Analysis, Dublin, June 30, 2009.

Speaker: Petru Eles

Invited talk: Audio Driven Video Surveillance System using COMPLEX design flow

DATE workshop on designing for embedded parallel computing platforms: architectures, design tools, and applications, Grenoble, March 2011.

Authors: Fabien Colas-Bigey (Thales), Sara Bocchio (ST-I), Chantal Couvreur (IMEC), Gianluca Palermo (POLIMI), Philipp A. Hartmann (OFFIS) "Audio Driven Video Surveillance System using COMPLEX design flow",

Summer school: Platform-Based Design: From Multi-Core Platforms to Biochips and beyond

Artist Summer School in China, Beijing, China, August 8-12, 2011

Speaker: Jan Madsen

Invited Talk: Recent Research and Emerging Challenges in the System-Level Design of Digital Microfluidic Biochips

SOCC 2011, Taipei, Taiwan

Speaker: Paul Pop

Tutorial: Digital Microfluidic Biochips: Functional Diversity, More than Moore, and Cyberphysical Systems

Embedded Systems Week, Taipei, Taiwan - 9.11.2011

Speaker: Krishnendu Chakrabarty, Duke University, USA; Paul Pop, DTU; Tsung-Yi Ho, National Cheng Kung University Tainan, Taiwan

Simon Schliecker, Jonas Rox, Mircea Negrean, Kai Richter, Marek Jersak and Rolf Ernst, "System Level Performance Analysis for Real-Time Automotive Multi-Core and Network Architectures," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 28, No. 7, pp. 979-992, July 2009

Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst and Michael González Harbour, "Influence of different abstractions on the performance analysis of distributed hard real-time systems," *Journal Design Automation for Embedded Systems (available as "online first", April 2008)*, vol. 13, No. 1, pp. 27-49, June 2009

Simon Schliecker, Mircea Negrean und Rolf Ernst, "Response Time Analysis in Multicore ECUs with Shared Resources" *IEEE Transactions on Industrial Informatics*, vol. 5, No. 4, November 2009

Philip Axer, Jonas Diemer, Mircea Negrean, Maurice Sebastian, Simon Schliecker, und Rolf Ernst, "Mastering MPSoCs for Mixed-Critical Applications" *IPSI Transactions on System LSI Design Methodology*, vol. 4, August 2011

Philip Axer, Maurice Sebastian, und Rolf Ernst, "Reliability Analysis for MPSoCs with Mixed-Critical, Hard Real-Time Constraints" in *Proc. Intl. Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, (Taiwan), Oktober 2011

[PIEP 09] P. Pop, V. Izosimov, P. Eles, and Z. Peng, Design Optimization of Time- and Cost-Constrained Fault-Tolerant Embedded Systems with Checkpointing and Replication, *IEEE Trans. on Very Large Scale Integrated (VLSI) Systems*, V17, N3, 2009, pp. 389-402.

[IPPEP 09] V. Izosimov, I. Polian, P. Pop, P. Eles, and Z. Peng, Analysis and Optimization of Fault-Tolerant Embedded Systems with Hardened Processors, Design Automation and Test in Europe (DATE) Conference, Nice, 2009, pp. 682-687.

[IPEP 09] V. Izosimov, P. Pop, P. Eles, and Z. Peng, Scheduling and Optimization of Fault-Tolerant Embedded Systems with Transparency/Performance Trade-Offs, *ACM Transactions on Embedded Computing Systems (TECS)* - in print.

[TBEP 11] B. Tanasa, U. D. Bordoloi, P. Eles, Z. Peng, Reliability-Aware Frame Packing for the Static Segment of FlexRay, The Intl. Conf. on Embedded Software (EMSOFT11), Taipei, Taiwan, October 9-14, 2011.

[AEP08] A. Andrei, P. Eles, Z. Peng, J. Rosén, Predictable Implementation of Real-Time Applications on Multiprocessor Systems on Chip, Proceedings of 21st IEEE Intl. Conference on VLSI Design, 2008, pp. 103-110.

[RNE+ 11] J. Rosén, C. F. Neikter, P. Eles, Z. Peng, P. Burgio, L. Benini, Bus Access Design for Combined Worst and Average Case Execution Time Optimization of Predictable Real-Time Applications on Multiprocessor Systems-on-Chip, 17th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'11), Chicago, IL, USA, April 11-14, 2011.

'Enabling run-time memory data transfer optimizations at the system level with automated extraction of embedded software metadata information', Bartzas, A.; Peon-Quiros, M.; Mamagkakis, S.; Catthoor, F.; Soudris, D. and Mendias, J., Asia and South Pacific Design Automation Conference - ASP-DAC , 2008

'Optimization Methodology of Dynamic Data Structures based on Genetic Algorithms for Multimedia Embedded Systems', Baloukas, C.; Risco Martin, J.; Atienza, D.; Poucet, C.; Papadopoulos, L.; Mamagkakis, S.; Soudris, D.; Hidalgo, J.; Catthoor, F. and Lancares, J., Elsevier Journal of Systems and Software (JSS), 2008

'MOSART: Mapping Optimisation for Scalable multi-core ARchiTecture', B. Candaele, A. Jantsch, T. Ashby, K. Tiensyrjä, F. Ieromnimon, B. Vanthournout, P. Di Crescenzo, D. Soudris, 16th IFIP/IEEE International Conference on Very Large Scale Integration - VLSI-SOC, 2008.

"Scalable Multi-core Architectures: Design Methodologies and Tools", Eds D. Soudris and A. Jantsch, Springer Science+Business Media, 2012.

A. Bartzas, P. Bellasi, I. Anagnostopoulos, C. Silvano, W. Fornaciari, D. Soudris, D. Melpignano, C. Ykman-Couvreux, "Runtime Resource Management Techniques for Many-core Architectures: The 2PARMA Approach", International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'11), Monte Carlo Resort, Las Vegas, Nevada, USA, July 18-21 2011.

[Hansen, Michael Reichhardt](#); [Jakobsen, Mikkel Koefoed](#); [Madsen, Jan](#) (2011): Modelling of Energy Harvesting Aware Wireless Sensor Networks. In: Tan, Yen Kheng (Ed.) *Sustainable Energy Harvesting Technologies - Past, Present and Future* Intech, pp. 3 - 24, 2011

M. K. Jakobsen, J. Madsen, S. H. A. Niaki, I. Sander, J. Hansen, "System level modeling with open source tools", to appear in proceedings of Embedded World 2012

4.4.5 Design for Adaptivity

Insights gained

During the four years of ArtistDesign a number of results have been achieved related to adaptivity in embedded systems. These are best summarized in Section 3.1 in the corresponding annual reports. The highlights of the achievements for all the four years are also summarized in Section 4.1.1 in this year's annual report. In addition to this the insights listed below have been gained:

- The increasing complexity, the hardware development, the demands for resource efficiency, and the increasing reliance on software and/or programmable approaches in embedded systems will without doubt increase the demands for adaptivity in the future.

- Adaptivity in embedded systems covers a wide range of subjects from mode change protocols for hard real-time scheduling to run-time reconfiguration of programmable hardware. Hence, to develop a common theoretical basis for adaptivity in embedded systems is extremely challenging. The work performed within ArtistDesign can merely be considered as a starting point for this.
- In order to move adaptivity from the research community to industrial practice it is essential that adequate support for adaptivity is included in COTS software and hardware, including OS and middleware. This includes in particular sensing and actuation mechanisms.
- There is a fundamental tradeoff between adaptivity and predictability. Hence, for applications with severe requirements on predictability, adaptive mechanisms are less suitable.
- In embedded systems the adaptation mechanisms themselves must be very resource efficient. Also, the requirements which they pose on the applications and the knowledge they require about the applications must be small. This in combination means that the adaptation mechanisms must be quite simple in order to be practically useful.
- The thermal control, power control, and application performance control needed in multi/many-core embedded systems have very strong relationships with the same problems in server systems and data centers. Hence, a unified approach to resource management of computing systems is a realistic future goal. This was one of the conclusions of the Workshop on Control of Computing Systems organized in Lund, in Dec 2011.

Bibliography

"Special Issue on Adaptive Embedded Systems," Karl-Erik Årzén, Ed., Real-Time Systems, In preparation, 2012. (Several of the submitted manuscript originate from the members of the adaptivity activity.)

Several of the joint and individual papers generated in the activity can be viewed as position papers. Some examples are:

Enrico Bini, Giorgio Buttazzo, Johan Eker, Stefan Schorr, Raphael Guerra, Gerhard Fohler, Karl-Erik Årzén, Vanessa Romero Segovia, Claudio Scordino, "Resource Management on Multicore Systems: The ACTORS Approach", IEEE Micro, 31:3, pp. 72-81, May 2011.
<http://doi.ieeecomputersociety.org/10.1109/MM.2011.1>. (Describes the outcome of the EU STREP ACTORS project, the largest joint project on adaptivity performed during the years of ArtistDesign.)

Steffen Stein, Moritz Neukirchner, Harald Schrom, und Rolf Ernst, "Consistency Challenges in Self-Organizing Distributed Hard Real-Time Systems," in Workshop on Self-Organizing Real-Time Systems - SORT 2010, 2010 (Position paper on self-organization)

Steffen Stein, Moritz Neukirchner, Rolf Ernst. Admission Control and Self-Configuration in the EPOC framework, Proc. of International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS XI), 2011 (Position paper on self-configuration)

DeJiu Chen, Martin Törngren, Magnus Persson, Lei Feng and Tahir Naseer Qureshi. "Towards Model-Based Engineering of Self-Configuring Embedded Systems". Model-Based Engineering of Embedded Real-Time Systems. Holger Giese, Bernard Rumpe, Bernard

Schätz (eds). Series: Lecture Notes in Computer Science. Vol. 6100. Springer Verlag, 2010. ISBN: 978-3-642-16276-3. (Results of the DySCAS project)

Richard Anthony, DeJiu Chen, Mariusz Pelc, Magnus Persson and Martin Törngren. Context-Aware Adaptation in DySCAS. Electronic Communications of the EASST. Volume 19: Context-Aware Adaptation Mechanism for Pervasive and Ubiquitous Services 2009. CAMPUS 2009. ISSN 1863-2122. (Results of the DySCAS)

Paterna, F.; Acquaviva, A.; Caprara, A.; Papariello, F.; Desoli, G.; Benini, L.; , "Variability-Aware Task Allocation for Energy-Efficient Quality of Service Provisioning in Embedded Streaming Multimedia Applications," Computers, IEEE Transactions on , vol.PP, no.99, pp.1, 0 doi: 10.1109/TC.2011.127 (Adaptivity in embedded multimedia)

Additionally, since adaptivity is a cross-cutting concern several of the special sessions and issues organized by the ArtistDesign clusters, e.g, the Operating Systems and Networks cluster, are also of relevance with respect to adaptivity.

4.4.6 Design for Predictability

Insights gained

- In the COMPOSE Project, TU Braunschweig cooperated with Intel Braunschweig on novel network-on-chip (NoC) architectures that enable future multi- and many-core processors to efficiently execute real-time applications with guaranteed timing requirements. The NoC enables data transfers with predictable timing and service guarantees for real-time and streaming applications. The architecture developed in the COMPOSE project forms the basis of the many-core research platform (IDA-MC: Integrated Dependable Architecture for Manycores) which is currently developed by TU Braunschweig in the RECOMP project.

Bibliography

Presentation: Predictability in General-Purpose Many-Cores
Intel® European Research & Innovation Conference, ERIC 2010
Braunschweig, Germany, September 21-22, 2010

Presentation: IDAMC NoC – Efficient Quality-of-Service Support for Mixed-Critical Networks-on-Chip
RECOMP Technical Day
Porto, Portugal - August 29, 2011

Philip Axer, Jonas Diemer, Mircea Negrean, Maurice Sebastian, Simon Schliecker, und Rolf Ernst, "Mastering MPSoCs for Mixed-Critical Applications" IPSJ Transactions on System LSI Design Methodology, vol. 4, August 2011

4.4.7 *Integration Driven by Industrial Applications*

Insights gained

- The industry-motivated transversal activity necessitated additional care as on one hand, we need to understand the concerns of companies that have been investing substantially in embedded system design such as the ones in automotive and aerospace domains; on the other hand, we needed to understand the characteristics of emerging domains such as independent living and health, energy efficient buildings and synthetic biology. In the emerging sectors, the links among the different players are not clear as yet when we look at the promises of these markets. We believe that the activity in the more traditional segments will continue along a journey that has begun several years ago and we do not expect major surprises in corralling the industrial participants as well as the ArtistDesign partners. The emerging sectors represent significant new opportunities to impact the formation of new business models and approaches. We expect that the ArtistDesign community will have to dig deep into its accumulated expertise and into its research network to help industry find its path to profitable products and services. With the end of the NoE, new mechanisms will have to be applied if the EU wants to continue injecting innovation into the EU industrial sector in the system domain and sustain the successful collaboration established among partners in pursuing the goal of industrial integration.
- Over the four years the process of industrial integration has been advanced successfully. In the context of different R&D projects between TU Braunschweig and partners from the industry (GM, Toyota-ITC, Daimler, Syntavision) several analysis methods have been developed and implemented as a prototype plugin for the tool SymTA/S. Evaluation by industrial partners showed that the analysis solutions provide tight analysis results for realistic use cases (e.g. in-vehicle communication networks or multi-core setups). This has increased the acceptance of formal analysis methods and also increased the user value of the tool SymTA/S.

Bibliography

See the many keynotes given by partners listed in deliverable D16-(7.3)-Y4.

Thomas Nolte and Roberto Passerone. Guest editorial special section on real-time and (networked) embedded systems. *IEEE Transactions on Industrial Informatics*, 5(3):198-201, August 2009.

Thomas Nolte and Roberto Passerone. Guest editorial special section on real-time and (networked) embedded systems - II. *IEEE Transactions on Industrial Informatics*, 6(4):475-478, November 2010.

Thomas Nolte and Roberto Passerone. Guest editorial special section on real-time and (networked) embedded systems - III. *IEEE Transactions on Industrial Informatics*, in press, 2012.

Alberto Sangiovanni-Vincentelli, Werner Damm and Roberto Passerone. Taming Dr. Frankenstein: Contract-Based Design for Cyber-Physical Systems. *European Journal of Control*, in press, 2012.

F. Balarin, M. D'Angelo, A. Davare, D. Densmore, T. Meyerowitz, A. Pinto, A. Sangiovanni-Vincentelli, A. Simalatsar, Y. Watanabe, G. Yang, Q. Zhu, "Platform-Based Design and Framework: Metropolis and Metro II", *Model-Based Design of Heterogeneous Embedded Systems* (Editors: G. Nicolescu, P. Mosterman), CRC Press , 2009.

L. Benvenuti, A. Balluchi, A. Bemporad, S. Di Cairano, B. Johansson, R. Johansson, A. Sangiovanni-Vincentelli and P. Tunestal, Automotive Control, in J. Lunze and F. Lamnabhi-Lagarrigue, editors, Handbook of Hybrid Systems Control: Theory, Tools, Applications, Cambridge University Press, pp. 439-470, 2009.

A. Sangiovanni-Vincentelli, Is a Unified Methodology for System-Level Design Possible?, IEEE Design and Test of Computers, Special Issue on Design in the Late and Post-Silicon Eras, Vol. 25, N. 4, pp. 346-358, July-August 2008.

A. Sangiovanni-Vincentelli, and M. Di Natale, Challenges and Solutions in the Development of Automotive Systems, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Volume: 28, Issue: 7, pp. 937-940, July 2009.

A. Sangiovanni-Vincentelli, S. Shukla, J. Sztipanovits, G. Yang, D. Mathaikutty, "Metamodeling: An Emerging Representation Paradigm for System-Level Design", Special Section on Meta-Modeling, IEEE Design & Test, vol. 26, no. 3, pp. 54-69, May/June 2009.

R. Passerone, S. Graf, A. Benveniste, D. Cancila, A. Cuccuru, S. Gerard, F. Terrier, W. Damm, A. Ferrari, L. Mangeruca, B. Josko, T. Peikenkamp, and A. Sangiovanni-Vincentelli. "Metamodels in Europe: Languages, Tools, and Applications," IEEE Design and Test of computers, Vol. 26, No. 3, pp: 38-52, 2009.

M. Di Natale and A. Sangiovanni Vincentelli, Moving from Federated to Integrated Architectures in Automotive: The Role of Standards, Methods and Tools, Proceedings of the IEEE, Volume 98, n. 4, pp. 603-620, April 2010, Invited Paper, Special Issue on Automotive Electronics

A. Sangiovanni-Vincentelli, Corsi e Ricorsi: The EDA Story, IEEE Solid State Circuits Magazine, Vol. 2 n. 3, pp. 6-26, Summer 2010, Invited Paper, Special Issue on the work of Alberto Sangiovanni Vincentelli

Simon Schliecker, Jonas Rox, Mircea Negrean, Kai Richter, Marek Jersak und Rolf Ernst, "System Level Performance Analysis for Real-Time Automotive Multi-Core and Network Architectures" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 28, No. 7, pp. 979-992, Juli 2009

Jonas Rox, Rolf Ernst, Paolo Giusto, "Using Timing Analysis for the Design of Future Switched Based Ethernet Automotive Networks", in Proceedings Design, Automation and Test in Europe (DATE 12) (to appear).

Rodney Cummings, Kai Richter, Rolf Ernst, Jonas Diemer und Arkadeb Ghosal, "Exploring Use of Ethernet for In-Vehicle Control Applications: AFDX, TTEthernet, EtherCAT, and AVB" in SAE 2012 World Congress & Exhibition, SAE Technical Paper 2012-01-0196, April 2012 (to appear).

4.5 Recommendation 5

Continue deployment of actions targeting sustainability of the outcome and initiated actions... In particular, leverage the cooperative activities and sharing events which are the best outcomes such as summer school, workshops, portals and joint publications.

The NoE will continue many of its visible actions well beyond the end of the NoE, in particular:

- Creation of an academic Special Interest Group called "ADSIG" within EDAA, the permanent structure that organizes the DATE conference. The ADSIG will host a web portal offering many of the same services to the academic community that are offered

by the current ArtistDesign web portal, including hosting for workshops and events, links to external events and publications, mailing lists, etc.

- The ARTIST Summer School will continue to be organized. The next edition will be in Aix-Les-Bains in September 2012, co-organized by ADSIG and EPFL.
- We believe that the forward movement initiated within ARTIST for cooperation at the European level on embedded systems design will continue well into the future. This will in turn lead to further joint research and papers by the existing ARTIST partners.

4.6 Recommendation 6

Provide the “reading grid” for the joint activities that have been performed and will go on being initiated, so as to get a roadmap for these in terms of self-defined objectives and achievements (the fruitful results and the dead-ends that definitely have an interest to be known, why these tracks were not fruitful, in order to enrich the overall research community knowledge)

These ArtistDesign main joint activities are covered in some detail in are the “WP7: Transversal Integration” activities, which are documented in some detail in the corresponding deliverables: D14-(7.1)-Y4, D15-(7.2)-Y4, and D16-(7.3)-Y4.

4.7 Recommendation 7

There is a significant research impact perceived. However more measurable evidence of this impact should be provided.

There is a need to show how this group influences science and industry. Quantified evidence in that regard would be good for the consortium and the commission.

Ideas about some metrics could be:

- *How big is the material produced by the consortium*
- *How many universities are using the material*
- *How many students are reached*

Also impact of collaborations should be quantified.

The consortium has produced a huge amount of material over the past 4 years (not including Artist2, or Artist FP5):

- Approximately 975 joint papers have been published by the partners (joint papers have authors from two or more ARTIST partners). The number of papers published individually by partners is far higher.
- Approximately 1000 keynotes and tutorials have been delivered by leading ARTIST researchers.
- It’s our belief that every university or research center in the world, that is involved in Embedded Systems Design uses the material produced by the NoE partners.
- The consortium has held numerous International Summer Schools, representing overall approximately 960 students all over the world:
 - 4 editions of the Summer School in Europe,
 - 4 editions of the Summer School in China

- 3 editions of the Summer School in South America
- 1 edition of the Summer School in Morocco
- Additionally, we have organized a very large number of graduate schools and international workshops. The full list of these is detailed in the Y4 edition of the deliverable: D4-(2.0)-Y4 Spreading Excellence Report (JPASE).

The impact of these collaborations is difficult to measure in any precise terms, but it's clear that the ArtistDesign NoE has had a deep, overall structuring effect on the research activities of all the partners, and on the European research landscape as a whole.

4.8 Recommendation 8

There are some steps going into the direction of a “survival” of the effort. However this is still too vague. A roadmap on embedded systems could be one step in that direction including a new vision for the future checking this vision against other activities like ARTEMIS, ITEA2, etc and including a priority list of themes to be dealt with.

The ARTEMIS SRA Strategic Research Agenda (SRA) defines the vision and the future directions for the large European ARTEMIS projects that shall drive industrial innovation in embedded systems. The new 2011 SRA, which is an update of the 2006 SRA, describes the importance of embedded systems to address upcoming societal challenges and elaborates on concrete areas and usage scenarios as illustrative examples. These scenarios are then used to derive relevant embedded system research topics and innovation goals. This SRA is used as guideline for the ARTEMIS Work Programme which is updated on a regular basis.

TU Braunschweig (R. Ernst) was one of the main contributors to the 2011 SRA. That ArtistDesign partner was also responsible for all initial public presentations of the vision and scientific background of that agenda at industrial and political events. This indicates the importance of the NoE as a source of new ideas for ARTEMIS and, consequently, for industrial innovation in embedded systems and their application.

TU Braunschweig and ETH Zürich have also been consulted in the definition of the FP7 calls and in the preparation of Horizon2020.



214373 ArtistDesign
Network of Excellence
on Embedded Systems Design

Project Management Report for Year 3

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ArtistDesign Consortium

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5. Overview

5.1 Project Objectives and Major Achievements

A detailed description of objectives, and particularly the main aims for integration, is provided for each cluster in the sections labelled « State of Integration in Europe ».

5.2 Deliverables for the Reporting Period

WP0: Joint Programme of Management Activities (JPMA)

D2-(0.2)-Y4 Project Management Report
UJF/Verimag D2-(0.2a)-Y4 **ch. 1 - Executive Summary and Overview**
Aalborg D2-(0.2b)-Y4 **ch. 2 - Modelling and Validation**
Dortmund D2-(0.2c)-Y4 **ch. 3 - SW Synthesis, Code Generation and Timing Analysis**
Pisa D2-(0.2d)-Y4 **ch. 4 - Operating Systems and Networks**
DTU D2-(0.2e)-Y4 **ch. 5 - Hardware Platforms and MPSoC Design**
UJF/Verimag, D1-(0.1)-Y4 **Periodic Report**
Floralis

WP1: Joint Programme of Integration Activities (JPJA)

UJF/Verimag D3-(1.0)-Y4 **Integration Activities Report**

WP2: Joint Programme of Activities for Spreading Excellence (JPASE)

UJF/Verimag D4-(2.0)-Y4 **Spreading Excellence Report**

WP3: Modeling and Validation (JPRA)

UJF/Verimag D5-(3.1)-Y4 **Modelling**
Aalborg D6-(3.2)-Y4 **Validation**

WP4: Software Synthesis, Code Generation and Timing Analysis (JPRA)

Dortmund D7-(4.1)-Y4 **Software Synthesis, Code Generation**
Saarland D8-(4.2)-Y4 **Timing Analysis**

WP5: Operating Systems and Networks (JPRA)

Pisa D9-(5.1)-Y4 **Resource-aware Operating Systems**
York D10-(5.2)-Y4 **Scheduling and Resource Management**
Univ. Porto D11-(5.3)-Y4 **Embedded Real-Time Networking**

WP6: Hardware Platforms and MPSoC (JPRA)

Bologna D12-(6.1)-Y4 **Platform and MPSoC Design**
DTU D13-(6.2)-Y4 **Platform and MPSoC Analysis**

WP7: Transversal Integration (JPRA)

Lund D14-(7.1)-Y4 **Design for Adaptivity**
Uppsala D15-(7.2)-Y4 **Design for Predictability**
Trento D16-(7.3)-Y4 **Integration Driven by Industrial Applications**

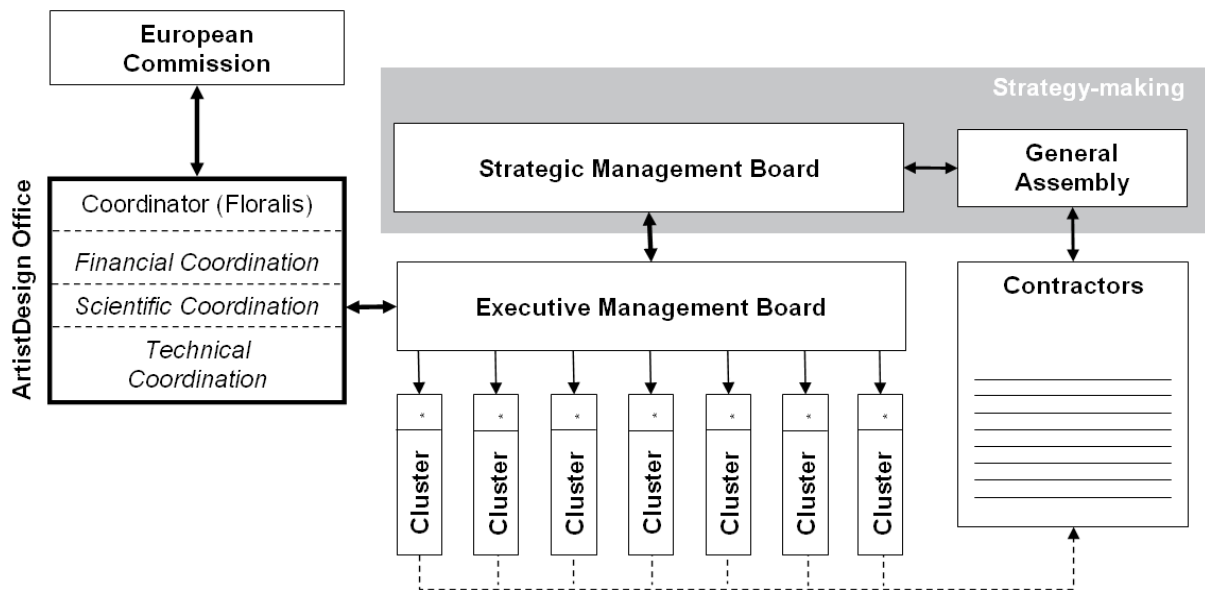
5.3 Consortium Management

-- **Changes wrt Y3 deliverable** –
Updated the deliverables' IDs.

5.3.1 Governance Structure

Scientific Coordinator: Joseph Sifakis Tel: +33 4 56 52 03 51 Joseph.Sifakis@imag.fr	Technical Coordinator: Bruno Bouyssounouse Tel: +33 4 56 52 03 68 Bruno.Bouyssounouse@imag.fr
Mailing address: Verimag Laboratory - Centre Equation - 2, ave de Vignate - 38610 Gières - France	

The methodology adopted for achieving the JPA objectives follows the same lines as for managing a laboratory. The activities, their objectives, their technical description, the partners involved, their roles, and the resources available have been clearly defined in the initial Description of Work, and updated in the deliverables. This will be monitored and guided by a tight and rigorous management, as defined in the diagram below:



The main governance bodies are:

The **General Assembly** is composed of one representative per core partner. It is convened at the beginning of the project and meets once per year. It is chaired by the Scientific Manager.

The **Strategic Management Board** is initially composed of the NoE cluster leaders, and a representative of the Coordinator – who attends, with no voting rights. It is chaired by the Scientific Manager, assisted by the Technical Manager. It meets at least once per year – close to the General Assembly meeting. Its members are elected by the General Assembly every two years, according to modalities to be determined in the Consortium Agreement.

The **Cluster Leaders** (who compose the Executive Management Board) are responsible for the overall coordination of the activities led by their cluster. A cluster functions as a virtual team – with a degree of autonomy for defining its internal meetings and day to day management.

5.3.2 *Partners Involved*

This is provided in the publishable Executive Summary, in the first part of this document.

5.3.3 *Contractors*

There were no changes to the consortium in Year 4.

5.3.4 *Project Timetable*

The JPA is organized into activities. The activities should not be considered as tasks of a workprogramme, with begin/end and synchronisation dependencies. Of course, the detailed description of an activity could be decomposed into sub-tasks and intermediate milestones, but this would imply a granularity that is too fine for research activities.

5.3.5 *Other Issues*

None

5.3.6 *Plan for using and disseminating the knowledge*

The main instruments for using and disseminating knowledge are:

- Workshops and Schools organised.
The list is quite impressive, and is provided in the deliverable on “Spreading Excellence”.
- ArtistDesign Web Portal.
Here also, the quantity of information made available to the greater embedded systems community is quite impressive, and continuously growing. This is possible through the efforts of the entire consortium, who now have direct access for updating the contents.
- Course Materials.
There is a growing body of course materials made available via the ARTIST web portal.
- Publications.
The ArtistDesign consortium is very prolific in publishing research articles, surveys, textbooks, roadmaps, and position papers.