
IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Cluster Progress Report for Year 4

Cluster:
# Software Synthesis, Code Generation and Timing Analysis

Cluster Leader:

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*Policy Objective (abstract)*

*The objective of this activity is to provide software synthesis, code generation and timing analysis tools which are required for modern embedded architectures. A particular focus is on multi-processor systems. The parallelism and communication structures found in such architectures pose a particular challenge.*

# Versions

| number | comment | date |
|---|---|---|
| 1.0 | First version delivered to the reviewers | Jan. 30th, 2012 |

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# 1. Overview of the Cluster (2008-2011)

## *1.1 High-Level Objectives*

There is a continuing demand for higher performance of information processing. This growing demand stimulates using a growing amount of parallelism (including using multiple processors), due to limitations of increasing clock speeds any further. This trend also affects the design of embedded systems. Hardware platforms, containing connected processors, are becoming increasingly parallel. Actually, there are various kinds of connectivity. In multi-processors in a system on a chip (MPSoC), processors are tightly connected and communication is fast. In other cases, networked processors may be less tightly connected and communication may be slower. In this project, we would like to address the issues resulting from the use of multiple processors, in particular in the form of multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces.

These processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Mapping techniques can be either based on task graphs or on sequential applications. The latter require the use of automatic parallelization techniques. In this cluster, we provide at least partial solutions to the problem of mapping specifications of embedded systems to networks of embedded processors. These networks are characterized by different speed parameters reflecting the communication and memory architectures. These parameters are considered during the mapping. We focus on mappings from simple sequential code from C or C-like languages. However, we also look at the generation of code from other specifications, being based, for example, on MATLAB or UML. Such languages could simplify the mapping since such specifications may be inherently parallel (and also more appropriate for embedded systems). In general, mapping techniques are indispensable for using future architectures.

Timing analysis is also affected by the trend toward the new platforms. In addition, timing analysis beyond single processors is required. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Hence, timing analysis also considers the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors. In addition, overcoming the traditional separation between compilers and timing analysis is on the agenda.

The design of efficient embedded systems also requires additional work. In particular, minimizing the energy consumption, addressing the memory wall problem and customizing instruction sets are hot topics, for which integrated approaches from various partners are extended and exploited.

Partners in this cluster also participated in the activities of the thematic activities of the Transversal Integration work package, where they addressed adaptivity and predictability of complex systems comprising MPSoCs. Predictability was also addressed in the cooperation between partners of the two activities of this cluster.

Partners were also contributing to orthogonal work, such as running workshops on embedded system education, writing textbooks, and editing a new series of books on embedded systems through Springer (see http://www.springer.com/series/8563).

It is understood that the project could only help integrating work that provides potential solutions. The actual work on those solutions has to be mostly paid through other projects

**-- Changes wrt Y3 deliverable --**

*Updated from the text of Y3 to reflect the end of funding.*

## *1.2 Industrial Sectors*

**Software Synthesis and Code Generation:** The work performed in the cluster is relevant for all industrial sectors using embedded software. This includes semiconductor houses, system houses, companies working on audio processing, video processing, data streaming applications in the TV, Set Top boxes, DVD players and recorders, mobile phones, base stations, printers and disk drives. Efficiency of embedded software, in particular the efficiency of memories, is relevant for high-speed embedded systems. Most mobile devices provide some kind of multimedia processing. Dortmund's compiler for the PP32 processor of Lantiq is an example of the industrial use of tools designed by the partners.

**Timing Analysis**: WCET estimations are relevant for all industrial sectors using hard real-time systems. Therefore, industrial sectors in this case include avionics, automotive, defense and some areas where control systems are applied. In other words, this includes all sectors for which *cyber-physical systems* are relevant. Especially in the automotive and the aeronautical domains, there is a need to have precise knowledge on the worst-case timing behavior of safety critical software. Therefore, timing-analysis tools entered industrial practice and are in routine use in the aeronautics and automotive industry. This need is underlined by the fact that the worst-case timing of large parts of the software used within the new Airbus A380 has been analyzed using AbsInt's aiT. With the certification of the A380's time-critical subsystems, aiT has acquired the status of a *validated* tool**.**

**Link between timing analysis and compilers**: Since the code of safety critical applications is typically generated by a compiler, the compiler should also be aware of worst-case timings. This work is relevant in all areas for which a physical environment is integrated with software, that is, areas were *cyber-physical systems* are used. The focus is on sectors having safety critical applications. The WCC compiler, integrating timing analysis and compilation, was evaluated at Bosch and is considered to be used in early development phases.

**-- Changes wrt Y3 deliverable --**

*Updated from the text of Y3.*

## *1.3 Main Research Trends*

Mapping of applications to MPSoCs can be considered as an extension of scheduling. Traditionally, scheduling mostly focused on independent tasks. This assumption is not valid for most applications of embedded systems. Additional research is performed in the multi-core context. Multi-core processors are usually considered to be homogeneous. For embedded systems, this assumption is also not valid. Therefore, new mapping techniques are required. Some papers have been published in this area. It is a trend to combine the mapping problem with non-traditional objectives. For example, minimization of the operating temperatures, maximization of the life-time of processors, and dependability in the presence of failing processors etc. are considered. However, these approaches mostly consider tasks as black boxes with little information, for example, on the memory access characteristics. This can lead

to sub-optimal mappings. This trend toward higher performances is important in all industrial areas in which high performance embedded computing is required.

Taking the well-known (frequently negative) results on automatic parallelization in high-performance computing into account, automatic parallelization is being experimented with in a way which is appropriate for embedded systems. Results obtained (for example at the Universities of Edinburgh, Passau, Aachen and Dortmund) indicate that this parallelization is feasible within a restricted scope of applications and architectures.

Energy efficiency, initially a topic considered mostly for embedded systems, is now mainstream. Energy availability is continuing to be the most challenging constraint for embedded system design, but performance constraints also exist. Therefore, the design of efficient embedded systems continues being important. Constraints are most dominating for small, mobile products.

The importance of timing is slowly being recognized by larger groups of people, especially in the context of cyber-physical systems. For example, there is increasing interest in the automotive domain. The new ISO standard, ISO 26262, even requires timing analysis for safety-critical hard real-time systems. At the same time, researchers are also giving timing issues more attention. In-line with this, the first compiler including a fully integrated WCET estimator was designed during the lifetime of this network. This research direction is finding increasing attention.

WCET analysis has so far almost exclusively dealt with sequential code running on uni-processors. The main trend has been towards managing more complex sequential hardware architectures. Increasing the level of automation, e.g., by more advanced analyses constraining the possible program flows, is also a topic of active research. As multi-core and MPSoC architectures arise, the research focus is shifting towards analysis of parallel systems. The requirements of sound timing-analysis methods have so far not been recognized by the designers of multi-core architectures. Current designs employ shared resources such that the timing-behavior of multi-threaded systems is not predictable. The PREDATOR project has elaborated principles for multi-core platforms that support sound and precise timing analysis. Finally, a new trend is to use timing analysis for fast estimates of execution times rather than for stringent timing verification. Such estimates can be used to aid time budgeting, and hardware dimensioning.

**-- Changes wrt Y3 deliverable --**

*The IT-community pays more and more attention to the problem of compiling and timing analysis for multi-processor systems.*

# 2. State of the Integration in Europe

## *2.1 Brief State of the Art*

**Software Synthesis and Code Generation:** Mapping applications to MPSoCs is an important topic in various places in the world, due to its extreme relevance for industry. In Europe, Ed Deprettere et al. (U. Leiden) performed significant work, working together with adjacent universities on the Daedalus tool. Also, the group of Jürgen Teich from the University of Erlangen-Nürnberg is proposing the SystemCoDesigner tool. ETH Zürich has worked on the DOL system design tool. Hopes is a system design tool from Seoul National University. In the automotive context, additional work has been performed at TU Braunschweig. Metropolis by Sangiovanni-Vincentelli et al. is a tool working on a global level. Charmed by Bhattacharyya places emphasis on signal processing applications. Recent tools try to combine task allocation with non-standard cost functions such as energy (e.g. Chang at DAC 2008), temperature (e.g. Ciskun at DATE 2007), lifetime or dependability.

The design of efficient embedded systems is the target of numerous optimization tools. There are clearly too many tools to make any attempt to present a survey in limited space useful. Even within the more restricted area of optimization of the memory structure, many approaches have been proposed by computer architects. Due to the increasing speed gap between processors and memories, efforts for improving the performance of systems have been predicted to hit the “memory wall”. Work was done in the context of caches (loop caches, filter caches etc.). However, these approaches have mostly focused on hardware approaches for reaching the goals. For these approaches, compilers were considered to be black boxes and untouchable. Only few authors have taken a holistic approach, looking at hardware and software issues (see various papers by Barua, Catthoor, Dutt, Kandemir, and Egger).

Software synthesis is being applied in various domains. For example, software synthesis is being used for the generation of control software, for tailored operating systems, for digital signal processing and multimedia applications, and for lab instrumentation (e.g. by National Instruments). This work is fragmented and the ArtistDesign network has contributed to interfacing the different communities with each other.

**Timing Analysis:** Several commercial WCET tools are available. They have experienced positive feedback from extensive industrial use in the automotive and aeronautics industry. The existing tools serve some particular and highly relevant points in this space. AbsInt’s tool for example has been used in the development and the certification of safety-critical systems in the Airbus A380. However, they currently do not serve distributed architectures well.

Important steps have been taken towards the interfacing and integration of timing analysis tools. The ALL-TIMES FP7 project created integrated tool chains that are now being made available to industry.

Basic design principles for timing-predictable multicore/MPSoC architectures have been established. These principles build on de-sharing, i.e., reducing the use of shared resources to a minimum.

TU Dortmund demonstrated the **integration of compilers and timing analysis** and can be considered leading this research area.

**-- Changes wrt Y3 deliverable --**

*The general impression is that compiling for multi-cores and timing predictability are receiving more attention, and so is the integration of compilers and timing analysis.*

## 2.2 Main Aims for Integration and Building Excellence through ArtistDesign

The Compiler and Timing Analysis Cluster and the Execution Platforms Cluster aim at advancing the methodology for resource aware design and compilation and at increasing predictability while retaining a high performance. The main aim of using the ArtistDesign network is to get access to competences, knowledge and tools that are not available locally at each of the institutions. The cooperation provides the required size of research teams, necessary to handle the complexity of today's technology. Furthermore, a major goal is the combination of areas of excellence of the different partners by defining and implementing interfaces between their design flows and tools in order to achieve compilation platforms applicable to a wider problem scope.

For software synthesis, the aim is to facilitate the cooperation between fragmented groups of researchers working on software synthesis in different domains.

WCET analysis of parallel systems, including MPSoC, is a more or less novel research area. However, it is becoming rapidly important as MPSoCs become increasingly used. Therefore, it is urgently needed to initiate more research in this area, and the ArtistDesign network will be used for this. The network will also be used for research initiation activities within the WCET analysis area. Contacts with other clusters, such as the HW Platform and MPSoC design cluster, will also be of importance since the success of the cluster's activities depends critically on the properties of the underlying hardware design.

**-- Changes wrt Y3 deliverable --**

*Updated from the text of Y3.*

## 2.3 Other Research Teams

For mapping applications to MPSoCs, section 2.1 contains a brief description of the work of other research teams in this area. Ed Deprettere (U. Leiden), Jürgen Teich and some of their students participated in the working meeting at Düsseldorf in November 2008 as well as in the second workshop on "Mapping of applications to MPSoCs". Ed Deprettere helped to set up an activity on benchmarking. Jürgen Teich presented his advanced SystemCoDesigner concept. Both are clearly candidates for being added as affiliates. Fortunately, we were able to reach out beyond Europe as well. Soonhoi Ha of Seoul National University gave a keynote talk at the second Rheinfels workshop. His HOPES system is one of the leading systems worldwide. He became an ArtistDesign affiliate during the lifetime of the network. Qiang Xu of the City University of Hong Kong considers the impact of mapping decisions on the reliability. His talk at the Rheinfels workshop was also well-received. Finally Tajana Simunic Rosing of UC San Diego presented her work on the consequences of mapping tasks on energy consumption and thermal management.

Essentially three more research teams have competed with Europe in the area of Timing Analysis, one at Seoul National University (SNU), one at Florida State University, now with some branches in North Carolina etc., and National University of Singapore. Seoul has turned to power-aware computing, and flash memory based components research. Singapore and

Florida have cooperated with the ArtistDesign partners in writing a survey paper. Singapore has participated in the WCET Tool Challenge, arranged within ArtistDesign, with their academic prototype. They are also international affiliate partner in ArtistDesign. There is a continuous exchange of PhD students and PostDocs with the team of Prof. Sang Lyul Min at SNU.

Only few groups have been working on the integration of worst-case execution times and compilers. Smaller, apparently volatile efforts have been reported from Sweden and South Korea. Some work was performed in the group of David Whalley at the Computer Science Department of the Florida State University. However, only very simplified timing models and highly predictable processor architectures are considered at Florida. A larger effort takes place at the group of Abhik Roychoudhury from the National University of Singapore (NUS). Cooperation between TU Dortmund and NUS has been intensified through mutual visits from both teams.

WCET analysis for multi-core systems has been considered by Petru Eles et. al. at Linköping University (Artist-Design Core partner in the Hardware Platforms and MPSoC Design cluster), Their approach builds on a TDMA scheduling policy for the bus, which makes memory access times predictable and thus enables a more precise WCET analysis.

Additional work has been performed at INRIA/Rennes by Isabelle Puaut et al., and Christine Rochange et al. at IRIT/Toulouse. More information about the work of other teams is available in section 1.5 of the two related activity reports.

**-- Changes wrt Y3 deliverable --**

*No major changes with respect to Year 3.*

## *2.4 Interaction of the Cluster with Other Communities*

For mapping application to MPSoCs, links have been established with the execution platform cluster of ArtistDesign, where some related work is being performed, for example, at Zürich, Bologna, and TU Denmark. For timing analysis, the same applies for the modeling and validation cluster: There is now an increased interest in how to apply model checking to timing analysis, and how to combine it with traditional timing analysis techniques. Cluster members Peter Marwedel and Rainer Leupers performed further teaching activities at ALARI, Lugano, together with ArtistDesign members like Luca Benini (Bologna), Rudy Lauwereins (IMEC) and Lothar Thiele (Zürich). Further links of ArtistDesign members exist to the EURETILES/SHAPES project and to the HiPEAC Network of Excellence.

**RWTH Aachen:**

RWTH Aachen participated in the HiPEAC network of excellence and worked on cooperations related to code optimization, e.g. with Edinburgh University, on simulation techniques and computer architecture, e.g. with FORTH in Greece and also on (MP)Design technologies, e.g. with Tampere University of Technology in Finland. In the context of HiPEAC project, on June 16, 2011, RWTH Aachen visited Department of Computer Systems in Tampere University of Technology for a one-day joint seminar, which covered the topics such as fast simulation, MPSoC programming and processor design. Furthermore, Aachen maintained tight industry cooperations, e.g. with Synopsys, Huawei, ACE and Compaan. One joint Master thesis between Aachen and ACE is currently underway in 2011 in the context of source-to-source optimizations for embedded DSP processors. RWTH Aachen also invites ACE regularly to give a guest lecture every year in the course of “Compiler Construction” for Master-level students. Since Oct 2006, RWTH Aachen is running the UMIC research cluster (http://www.umic.rwth-

aachen.de) of the German excellence initiative. In particular, the flagship project "Nucleus" in the "RF Subsystems and SoC Design" addresses the design challenges of heterogeneous MPSoC platforms for software-defined radio applications, which is in co-operation with TU Kaiserslautern.

**TU Dortmund:**

The group promotes education in embedded systems through a published textbook ("Embedded System Design"). The second edition became available at the end of 2010 / beginning of 2011. Consistent with the request of the reviewers for quantified information about the size of the material provided, we include the following details about the material which comes with this book: The book is complemented by 1150 slides, which can be freely downloaded from the internet at http://ls12-www.cs.tu-dortmund.de/daes/daes/mitarbeiter/prof-dr-peter-marwedel/embedded-system-text-book/slides/slides-2011.html. Also, currently 9 hrs 50 mins of recorded lectures are available through the same link, with more videos to come. As per Jan. 26th, 2012, we have recorded 2060 accesses to these videos since May 2011. About 1300 downloads and 500 physical copies of the textbook were aquired in 2011. A list of courses using the book is available at the book's home page: http://ls12-www.cs.tu-dortmund.de/~marwedel/es-book. The following table lists citations for some of the textbooks in the embedded market, as per Jan. 26th, 2012. Obviously, more recent books will increase their numbers.

| Author | Title | Published | Citations (Harzing/ Google) |
|---|---|---|---|
| Wayne Wolf | Computers as components: Principles of Embedded Computing Design | 2001 & 2008 | 387 |
| Frank Vahid | Embedded System Design: A Unified hardware/software introduction | 2002 | 306 |
| Peter Marwedel | Embedded System Design (1st & 2nd ed.) | 2003 & 2011 | 276 |
| Daniel Gajski | Embedded System Design: Modeling, Synthesis and Verification | 2009 | 34 |
| Edward Lee | Introduction to Embedded Systems: A Cyber-Physical Systems Approach | 2011 | 14 |

The group at TU Dortmund also organizes the WESE workshop on embedded system education. The group leader teaches at ALARI (Lugano) and is the European editor for the Springer series on embedded systems (see http://www.springer.com/series/8563). Currently, about 20 different volumes are available in the series.

Much interaction took place at workshops organized by TU Dortmund, including the SCOPES series of workshops on compilation for embedded systems, the workshop on the mapping of applications to MPSoCs and the workshop on software synthesis, held during the embedded systems week 2011. The activity report on software synthesis and code generation contains overall conclusions concerning the publication of a special issue of the IEEE Journal on Industrial Informatics on software synthesis and code mapping to MPSoCs.

TU Dortmund has and is working on the integration of timing analysis and compilation. The corresponding work on the WCC-Compiler led to a general interest in this type of work. This

work has been performed in close cooperation with Airbus, Bosch, Saarland University, AbsInt, University of Bologna, and ETH Zürich.

The interaction with the local technology transfer centre ICD (see http://www.icd.de/index_eng.html) is key for interacting with industry. ICD is headed by Peter Marwedel and is used for transferring research results to industry. It provides its development tool ICD-C to several partners, including TU Eindhoven and Saarland University.

Resource-aware compilation is an area in which TU Dortmund has worked for several years. The main focus is on memory-architecture aware compilation, implemented through pre-pass compilation tools. This work also includes the mapping to multi-processors. In this context, TU Dortmund cooperated with several partners, for example with TU Eindhoven and IMEC.

TU Dortmund secured the funding for a Collaborative Research Center on "Providing Information by Resource-Constrained Data Analysis" (SFB 876, http://www.sfb876.tu-dortmund.de), supported over an initial period of 4 years with possible extensions for an additional 8 years by Deutsche Forschungsgemeinschaft (DFG). Under this scheme, a total of 12 projects involving 19 research teams are jointly executed. The projects started in January 2011. A key target of this Center is to provide a bridge between machine learning and embedded systems. P. Marwedel is the vice-chair of this center.

Recently, TU Dortmund started to work on the dependability of future embedded systems through its participation in the focused program of DFG on "Dependable Embedded Systems" (SPP 1500, http://spp1500.itec.kit.edu/63.php). TU Dortmund works on software-based fault tolerance (http://ls12-www.cs.tu-dortmund.de/research/activities/fehler).

In 2011, P. Marwedel visited the group of B. Franke at the University of Edinburgh and participated in a PhD defense there.

**IMEC:**

IMEC is integrated in European research networks, including HiPEAC. IMEC also has many industry co-operations including most large European multi-media and communication systems oriented companies.

**U. Passau:**

The group at the University of Passau is internationally well connected in parallelism and programming methodology. This is most visibly documented by Christian Lengauer's chairmanship of the steering committee of the yearly international conference series Euro-Par (Parallel Computing in Europe) and the IFIP Working Group 2.11 on Program Generation. On issue in this group is program optimization via parallelization.

Passau has also been a member of the CoreGRID network of excellence which terminated in August 2008 but continues as an informal interest group. Some of the software engineering and parallelization issues of CoreGRID are also relevant to ArtistDesign.

In the past years, Lengauer had spear-headed the submission of a proposal for a national priority programme ("Schwerpunktprogramm") to the German Research Foundation ("Deutsche Forschungsgemeinschaft") with the title "Manycores for everyone". One of several application areas targeted was the use of multi-cores and many-cores in embedded systems. After these attempts were not met with success, a follow-on, special action was launched in the summer of 2011, to propose a priority programme called "Software for Exascale Computing". Lengauer participated in this proposal, which was granted with the number SPP 1648 in October 2011 and is going to run for six years, starting in January 2013, with a funding of 4 million Euros per year. Lengauer is on the programme's steering committee, responsible for the research area of programming methods.

Passau's main research activity in parallelism has been the further development and extension of the polyhedron model for automatic loop parallelization. Recent extensions pursued in

Passau targeted the Grid (activities in the CoreGRID network) and generally programmable graphical processing units, short GPGPUs (activity in ArtistDesign). Armin Größlinger's dissertation on the latter issue (among others) received the prize of the CommuniGate GmbH in Passau in 2010.

Passau also has close connections to the GRAPHITE project (http://gcc.gnu.org/wiki/Graphite), whose aim is to incorporate polyhedral methods into the GCC compiler. From April 2009 to March 2010, Größlinger was a visiting scientist in the GRAPHITE group of Prof. Albert Cohen at INRIA, Paris. In 2011, Tobias Grosser (the main developer of Polly originating from Passau) has joined Prof. Cohen's group as doctoral student, fostering the connections between the two groups.

A further two-year, renewable DFG-funded project with the name of MapReduceFoundation started in the summer of 2011 and concerns the type-safe design of imperative MapReduce implementations.

**Mälardalen:**

The WCET analysis group maintains close contacts with several industrial partners, such as Ericsson and Volvo. The group also interacts heavily with the Component-based Software Engineering community, through the national centre PROGRESS for research on component-based software design for embedded systems. Björn Lisper is one of the founders of the Swedish Multicore Initiative (http://www.multicore.se/), whose purpose is to promote research and dissemination of knowledge in the area of multicore computing.

The group participates in the ITEA2 project TIMMO-2-USE, with partners primarily from automotive industry in Germany, Sweden, and France and academic partners Chalmers, Univ. Braunschweig, Univ. Paderborn, C-LAB, and INRIA Sophia-Antipolis. The topic of the project is languages, methodologies and methods for specification and verification of timing properties of automotive systems at different levels of abstraction.

Researchers at Mälardalen maintain the very popular "Mälardalen benchmark suite" (http://www.mrtc.mdh.se/projects/wcet/benchmarks.html). This benchmark is intended for evaluating timing analysis tools, but has also found use outside the timing analysis community.

A link has been established with ArtistDesign member Wang Yi at Uppsala regarding how to combine model checking over timed automata with traditional timing analysis techniques. The target is time-critical software on multicore architectures.

**Saarland University**:

Timing-Analysis activities in the cluster interacted closely with the Execution-Platform cluster in the area of increasing the timing-predictability of real-time systems. Saarland University has coordinated the FP7 project PREDATOR, which has aimed at reconciling performance with predictability. The project, in which several ArtistDesign partners participated as well as Airbus and Bosch, started in February 2008 and has lasted until January 2011. Saarland University has worked together with several partners, such as AbsInt on timing analysis and SSSA on cache-aware scheduling. Airbus has provided insight into the particular problems posed by the IMA movement, going from federated to integrated architectures. Bosch and Daimler provide collaborations for the related AUTOSAR movement in the automotive industry. Bosch has applied the results of PREDATOR to improve the timing-predictability of their next-generation automotive platform.

Saarland University has developed new techniques for the determination of context-switch costs as required for preemptive scheduling. SSSA has taken these up to do schedulability analysis of preemptive scheduling strategies in the light of realistic context-switch costs.

Saarland University has improved the coverage of cache architectures developing efficient and precise cache-analysis methods for caches with FIFO and PLRU replacement strategies. In

another line of research Saarland University has developed the first cache-analysis techniques for programs using dynamic allocation on the heap.

Reinhard Wilhelm has taught timing-analysis methods at Saarland University, at Dresden University, at Technical University Munich, and at Beihang University (Beijing). His slide sets have been used at Oldenburg University, at University of Pennsylvenia, at University of California Berkely, at Erlangen University, and many other universities.

**ACE:**

ACE worked closely with ST and with Philips having both a commercial relationship with them as well as being co-members of EU project consortia – in one case along with Verimag. ACE has been working closely with Aachen in this domain for some time. One of the results of this cooperation has been the integration of compiler technology in a start-up company that span out of the university. Cooperation with Imperial College and Edinburgh continued.

**AbsInt:**

Within the EmBounded project (IST-510255), AbsInt was involved in the development of the Hume compiler. Hume is a domain-specific high-level programming language for real-time embedded systems. In the ALL-TIMES project (IST-215068), AbsInt combined its timing analyzer with tools of other partners, in particular the SWEET tool of Mälardalen. After the successful end of the PREDATOR project, AbsInt became partner of the new projects T-CREST (FP7 ICT-288008) and CERTAINTY (FP7 ICT-288175). AbsInt is importing the results of PREDATOR on the predictability of hardware configurations and its experience from the participation in the set-up of a WCET-aware compiler into these new projects.

AbsInt has integrated an efficient, approximative method for the determination of context-switch costs. Symbolic methods from model checking have been experimentally tried to reduce the problematic space consumption of pipeline analysis.

**TU Berlin:**

TU Berlin is generally involved in methods and tools for software engineering for embedded systems. TU Berlin has cooperated with Edinburgh University (Björn Franke) concerning the optimization of compilers based on machine learning techniques. Furthermore, TU Berlin has done research on the verification of embedded operating systems, also by cooperating with the Fraunhofer institute FIRST. Finally, TU Berlin visited and was visited by other cluster members.

**Tidorum, York:**

Tidorum (and partially York through Rapita Systems) were engaged in a project for the European Space Agency to study the timing and verification aspects of cache memories in space systems. The PEAL project ended in February 2007. An extension was started in late 2007 and ended with a final presentation in April 2009. The main partner from the aerospace domain was Thales Alenia Space, France.

**TU Vienna:**

TU Vienna has continued work on an open timing-analysis platform as a framework for testing new hardware platforms and software tools wrt. worst-case execution time analysis. As part of this activity TU Vienna cooperated with MDH, where the Swedish tool SWEET was integrated into a first prototype of the analysis platform.

In the T-CREST project TU Vienna and the project partners have started to work on the requirements and the definition of a time-predictable multi-core processor. This will be followed by work on code generation strategies for time-predictable code with support for hardware-specific WCET-oriented optimizations.

**-- Changes wrt Y3 deliverable --**

*Interactions with affiliates and external groups continued at the high level established in Y3.*

# 3. Overall Assessment and Vision for the Cluster

## *3.1 Final Overall Assessment*

The cluster made good progress in all the areas of its scope and also contributed to overlapping and neighboring areas.

For code generation, upcoming MPSoCs were considered to be the major challenge. When the network started, appropriate tools were hardly visible. Given the novelty of the aims and goals, we could not expect to be able to just integrate existing tools. Instead of starting the development of tools from resources of the network, we focused on interfacing the relevant researchers and to reach out to specialists beyond the network, including non-European partners. During the lifetime of the network, several new tools for this problem were designed, each one with a slightly different goal. At the end of 2011, several tools are available: including DOL (ETH Zürich), Daedalus (Univ. Leiden and Amsterdam), MAPS (RWTH Aachen), Mnemee (IMEC, Dortmund, TU Eindhoven and others), SystemCodesigner (Univ. Erlangen Nuremberg), Hopes (Seoul National University) and a tool from the City University of Hong Kong. In addition, many initiatives support the development of software for multi-core processors. In total, the scene has changed significantly since the proposal of this network was written. Time will tell, which of these approaches will be commercially successful and which not.

Resource-aware compilation has also seen a good amount of attention. In particular, energy-aware compilation has become one particular aspect of saving energy and has been linked to green computing. In this sense, it has become included in a mega-trend.

While the problem of mapping applications to MPSoCs is not yet completely solved, the next problem in code generation has popped up. General purpose computing on graphical processing units (GPGPU) has been found to offer dramatic potential for an increased performance. Researchers at TU Dortmund have also demonstrated that GPGPU also leads to the corresponding savings in consumed energy (more precisely, in the amount of electrical energy converted into heat). However, GPGPU programming can be rather cumbersome and advanced code generation techniques are required to get around this issue. This does very naturally lead to the necessity for synergies between high performance computing and code generation for embedded systems.

Software synthesis is based on techniques which synthesize software from models in a model-based design environment. Software synthesis, if compared to manually written software, has the potential of providing safer software at a reduced development time. Techniques for software synthesis have been proposed in different communities, not all of which could be included as partners of our cluster. Therefore, we focused on attracting these communities to our workshop on software synthesis. This approach worked well. In 2011, we attracted top researchers to the workshop. More communication between these researchers is still required. We expect more research to be performed in this area in the future.

The cluster has also made good progress advancing the state of the art in timing analysis and timing predictability. In this area, we have achieved significant results for single-core systems with single or multiple tasks. For multi-processor systems, important design principles for ensuring timing predictability have been formulated and are being evaluated. Work on more pragmatic, test-based methods has also progressed significantly.

One of the key achievements is the integration of timing analysis and compilers. In cooperation with AbsInt and Saarland University, TU Dortmund has implemented the WCET-aware compiler WCC. WCC incorporates a tight integration of timing analysis into compiler optimizations. The potential for making standard optimizations WCET-aware has been

explored in depth. It turned out that the largest potential is in exploiting the memory hierarchy. It was demonstrated that scratchpads offer a large potential for WCET-improvements, but even WCET-aware register allocation can contribute toward WCET-efficiency. Recent extensions include code generation beyond the TriCore architecture, the support of multi-processing and multi-processors as well as multiple objectives.

The level of collaboration between partners was significant. In addition to collaborative research, tools and prototypes have been developed and tools are integrated. This level of integration is indicative of the successful collaborative structure of the cluster.

In year 1, many teams have analyzed the requirements and started to work. In year 2, initial versions of tools became available. In year 3, these tools have started to see wide-spread use. This use has continued in year 4. Also, several teams extended their scope well beyond the classical code synthesis, code generation and timing analysis areas. Resource aware design, energy efficiency, timing predictability and multi-cores are now found in several application areas and ArtistDesign stimulated this spreading of techniques.

**-- The above text has been updated from the text present in the Y3 deliverable --**

## *3.2 Assessment for Year 4*

In year 4, we have seen a further proliferation of the basic techniques studied by this cluster. The importance of using multi-processor systems has been continuing to grow. Any session on programming multi-cores and multi-processor systems is filled with people. Fortunately, ArtistDesign is active in this area.

Several tools for mapping of applications to MPSoCs are available (e.g. from RWTH Aachen, IMEC, Erlangen-Nuremberg and Seoul National University). The number and breadth of the attendance of this community at the Rheinfels workshop has stayed at a high level. The importance of this topic has been recognized on a world-wide basis. In year 4, a special session (consisting of presenters at the Rheinfels meetings) was held during ESWEEK at Taipei. One joint paper is resulting from that session.

Work on resource-aware compilation has continued. Energy efficiency has become one of the mega-trends and researchers working on this topic find a lot of interest among audiences these days. Consideration of thermal behavior and reliability is becoming more important.

The workshop on Software Synthesis continued to be the main forum for the exchange of ideas in this area. This year's workshop was held at Taipei during ESWEEK (see http://www.artist-embedded.org/artist/Scope,2309.html). We were able to really attract top level experts to the workshop, even though it was held at the last day of ESWEEK. Presenters included S. Bhattacharyya (Univ. of Maryland), Kaushik Ravindran (National Instruments), Marco di Natale (SSSA, Pisa), Rajeev Alur (Univ. of Pennsylvania) and Nicolas Halbwachs (IMAG). They all agreed very strongly that they should have been in contact with each other much earlier and that a follow-up workshop is urgently needed, despite the end of funding for ArtistDesign.

The work on timing analysis and timing predictability has progressed significantly. The work on predictable architectures has proliferated in two different directions, both highly relevant for the timing predictability of multicore/MPSoC systems. In the first direction - keep systems deterministic and analyzable by keeping the parts, and their interaction, deterministic - we have seen further progress in cache analyses. These analyses are now being taken up in commercial analysis tools such as aiT from AbsInt. The work has also proliferated into novel analyses for cache-related preemption delay, now being applied in system-level response-time analysis, and cache-aware memory allocation. The other direction is to obtain predictability as

an emergent behavior. Contrary to the first approach, this approach is probabilistic and relies on randomization to make timings on micro-level independent. Here, promising initial work has been made.

An interesting development in cache analysis in year 4 is to combine model checking and abstract interpretation to obtain both the precision of model checking, and the scalability of abstract interpretation. Work at NUS shows that both scalable and precise analyses can be obtained in this way.

In program flow analysis, MDH and Tidorum have made advances towards increased soundness by developing an advanced relational value analysis that takes possible overflows and wraparounds into account. This is important for small embedded systems, where wraparounds are common.

Advances in hybrid WCET analysis methods, which include elements of measurements and testing, have been made (MDH, York, TU Vienna). The work to automatically identify timing models from observations has continued, and a method to identify approximate timing models for source code has been developed. Such timing models can be used to provide worst-case timing estimates early, to aid time budgeting and hardware dimensioning. Work has also been done towards identifying small but appropriate sets of test vectors for tasks with very large input sets, and evaluation of coverage metrics for test-data generation.

We see increased integration around timing tools and tool platforms. TU Vienna is developing an open and extensible platform for the evaluation of architectures, compilers, and timing analysis strategies with respect to timing properties and -predictability. The aim is to make the platform freely available to the timing analysis community. As a first integration example, a bridge has been built between the platform and SWEET from MDH. Concerning the goal of reconciling timing analysis with compilation as stated in item 2 of Section 1.2, the WCET-aware compiler WCC developed at TU Dortmund has been extended beyond the initial TriCore hardware platform and toward multi-objective optimization.

Proliferation of the fundamental techniques of this cluster includes a bridge between machine learning and resource-aware design. The Collaborative Research Center SFB 876 at TU Dortmund targets the use of machine learning techniques in embedded system design as well as the development of machine learning algorithms taking tight resource constraints into account. For example, project A3 extends compiler optimization techniques developed for embedded systems to the compilation for R, a language used for statistical approaches to machine learning. A second example is project B2. In this project, image analysis algorithms for a virus sensor are implemented through techniques mapping applications to MPSoCs. The center started to work in 2011.

Proliferation also includes a new link between reliability, compilers, operating systems and real-time systems. TU Dortmund works on the analysis of tradeoffs between reliability and meeting real-time constraints. This work is supported by the Deutsche Forschungsgemeinschaft (DFG) through its focused program SPP 1500. This work builds on top of the expertise gained from research on compilers and timing predictability. Work started in late 2010 and continued throughout 2011.

Finally, proliferation comprises the inclusion of educational material on software synthesis, compilers and timing analysis in the second edition of the textbook on embedded systems by P. Marwedel. This second edition provides a major update of the initial edition published in 2003. A wide-spread distribution of the book can be expected. The German translation of the book is “almost complete”. The publication of the Greek and Portuguese translations is delayed.

**-- The above is new text, not present in the Y3 deliverable --**

### *3.3 Indicators for Integration*

Partners promised the following interactions:

- The partners promised to organize at least one open, internationally visible workshop on software generation, compilers and timing analysis per year. This promise was kept: the SCOPES workshop was held in June 2011. In addition, the WCET Workshop was held in July 2011. Cluster members also organized the fourth workshop on mapping applications to MPSoCs, the WESE workshop on embedded system education, and the WSS workshop on software synthesis. So, in total, five workshops instead of one workshop were organized.
- The partners promised to integrate at least one timing analysis tool with an experimental compiler, to design optimizations within this compiler considering multiple objectives (including worst-case execution times) and to generate a detailed set of results demonstrating the advantages and limitations of such an integration. This promise was kept: the integration of aiT and WCC has been completed. The results are being demonstrated in an increasing list of papers (see references). We have started to study tradeoffs between multiple objectives.
  http://ls12-www.cs.tu-dortmund.de/research/activities/wcc/
- Partners announced an integration of techniques developed by the high-performance computing community and the compiler for embedded systems community. They predicted having at least one tool flow demonstrating the advantages of combining these approaches and having examples demonstrating the power of the integrated techniques for MPSoCs. Work on automatic parallelization and on general purpose computing on graphical processing units (GPGPU) demonstrates the synergy between high-performance and embedded system communities.
- The partners promised to publish at least four joint papers per year. This promise was kept. There are a total of twelve joint papers for the software synthesis and code generation activity (including papers with coauthors from outside the cluster) and additional joint papers for the timing analysis activity (see section 2.4. of the activity report on timing analysis).
- The activity reports contain information about further cooperation between the partners. We prefer not to repeat it in this report.

The partners also contributed to the transversal activities and dissemination.

**-- Changes wrt Y3 deliverable --**

*No major changes with respect to Year 3.*

### *3.4 Future Directions*

The long-term vision related to the project includes visions on software synthesis, code generation and timing analysis, as well as an integration of these areas.

The importance of software synthesis will be increasing. More and more applications will work with software generated through some time of model-based design. This way, some of the pitfalls of manually generated code can be avoided. However, this requires that specialists

from fragmented communities will find ways of improving their communication. Also, we expect to see more formal methods in this area.

Code generation constantly has to cope with new architectural features of processors. The usual trend is that architectural feature $n$+1 is introduced before code generation for architectural feature $n$ is mature. Resource-aware platform mapping still needs further research. Currently, we are starting to see -at least in academia- support for MPSoCs, which is a big step forward happening during the lifetime of this network. In the future, we expect to see such tools to further mature and being introduced into industry. Code generation for graphical processing units (GPUs) is another new challenge. More work for compiling for efficient execution on GPUs will be required.

We predict that an increasing amount of industrial areas will require a guaranteed timing, especially for cyber-physical systems. However, the trend toward higher performances and the use of multi-processor systems with shared resources is working in the opposite direction. It will be required to raise the awareness of timing issues.

We predict that the need for predictable timing in industry will increase as embedded real-time systems and cyber-physical systems are becoming even more commonplace. This implies a need for timing analysis tools and techniques that can cope with future hardware/software architectures. Therefore, we see the following main future directions for timing analysis:

- Timing analysis of multicore/manycore/MPSoCs: This includes both timing-predictable architectures, as well as improved methods to analyze software sunning on such systems with respect to timing.
- Improved usability of timing analysis tools (higher level of automation), and integration into tool chains and development environments. This is crucial for increasing the industrial uptake.
- Methods for fast, approximate timing estimation that can be done with limited information, typically early in the development process.

Partners from this cluster will continue to leverage cooperative activities and sharing events. The WESE, WSS, WCET and MAP2MPSoC/SCOPES workshops and other workshops will be continued. For the latter of these, reservations have been made and the call is out. For WESE and WSS, the call will be distributed later this year. In the context of timing analysis and predictability, a COST action is being defined.

**-- The above text has been updated from the text of Y3 --**

# 4. Cluster Participants

**-- Changes in the Cluster Participants wrt Y3 deliverable --**

*No changes with respect to Y3.*

## *4.1 Core Partners*

| **Cluster Leader**<br>**Activity Leader for "Software Synthesis and Code Generation"** | |
|---|---|
|  | Prof. Dr. Peter Marwedel (TU Dortmund)<br>http://ls12-www.cs.tu-dortmund.de/~marwedel/ |
| Technical role(s) within ArtistDesign | Cluster leader, activity leader SW Synthesis and Code Generation<br>Improved code quality for embedded applications is the main goal of the work at Dortmund University. Due to the widening gap between processor and memory speeds, emphasis has been on improving the efficiency of memory accesses, in terms of average and worst case execution time and in terms of the energy consumption. |
| Research interests | Peter Marwedel's Embedded Systems Group focuses on embedded software. Particular emphasis is on compilers for embedded processors. One of the very first publications in this area, the book "Compilers for Embedded Processors", edited by Peter Marwedel and Gert Goossens, was the result of the CHIPS project, funded by the European Commission. The group's current focus is on advanced optimizations for embedded processors (e.g. by using bit-level data flow analysis) and energy-aware compilation techniques. Current research also includes high-level transformations of algorithms as well as WCET-aware code generation. |
| Role in leading conferences/journals/etc in the area | Member of the EDAA (European Design and Automation Association) Main Board.<br>Editorial Board Member of the Journal "Design Automation for Embedded Systems"<br>Editorial Board Member of the Journal of Embedded Computing.<br>Editorial Board Member of the Microelectronics Journal.<br>Editor of the Springer series of books on Embedded Systems (http://www.springer.com/series/8563) |

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| | Co-Founder and Steering Board Chair of the SCOPES Workshop (Software and Compilers for Embedded Systems) Series.<br>>14 years of service for the DATE conference and its predecessors (program chair: 3 times, chairman of the steering committee, European representative to ASPDAC)<br>Various other conferences |
| Notable past projects | MNEMEE: Memory maNagEMEnt technology for adaptive and efficient design of Embedded systems supported by the European Commission (http://www.mnemee.org)<br>PREDATOR: Design for predictability and efficiency, supported by the European Commission (http://www.predator-projekt.eu)<br>MORE: Network-centric Middleware for group communications and resource sharing across heterogeneous embedded systems, supported by the European Commission http://www.ist-more.org<br>HiPEAC: European NoE on High-Performance Embedded Architecture and Compilation; http://www.hipeac.net<br>MAMS: Multi-Access modular-services framework, national project funded by the German Federal Ministry of Education and Research (BMBF)Others: Various earlier projects supported by the EC, DFG etc. |
| Awards / Decorations | IEEE Fellow (class of 2010)<br>DATE Fellow, 2008<br>Teaching award, TU Dortmund, 2003 |
| Further Information | CEO of the Informatik Centrum Dortmund (ICD), a technology transfer centre founded in 1989.<br>Chair of the Education Committee of TU Dortmund |

| **Activity Leader for "Timing Analysis"** | |
|---|---|
|  | Prof. Björn Lisper (Mälardalen University)<br>http://www.idt.mdh.se/personal/blr/ |
| Technical role(s) within ArtistDesign | Activity for "Timing Analysis"<br>Timing analysis, program analysis. |

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| Research interests | Timing analysis, static program analysis, language design for embedded and real-time systems, program transformations, parallelism |
| Notable past projects | FP7 STREP ALL-TIMES, Integrating European Timing Analysis Technology (coordinator). http://www.all-times.org<br>Several national projects, funded by Swedish Research Council, VINNOVA, KKS, SSF, Ericsson |

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|  | Senior researcher Chantal Ykman-Couvreur<br>IMEC vzw.<br>http://www.imec.be |
| Technical role(s) within ArtistDesign | Representing IMEC Smart Systems and Energy Technology division in:<br>-Cluster: SW Synthesis, Code Generation and Timing Analysis<br>-Cluster: Operating Systems and Networks<br>-Cluster: Hardware Platforms and MPSoC Design<br>-Intercluster activity: Design for Adaptivity<br>-Intercluster activity: Integration Driven by Industrial Applications |
| Research interests | Ch. Ykman-Couvreur is currently active in run-time management for embedded multi-core platforms |
| Role in leading conferences/journals/etc in the area | Ch. Ykman-Couvreur has published in International Journals and Conferences. She is active on several program committees of international conferences and in the organization of international workshops. |
| Notable past projects | Responsible for following FP7 European projects:<br>GENESYS (http://www.genesys-platform.eu<br>2PARMA (http://www.2parma.eu)<br>COMPLEX (http://complex.offis.de)<br>PHARAON |

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|  | Prof. Dr. Christian Lengauer<br>http://www.infosun.fim.uni-passau.de/cl/staff/lengauer |
| Technical role(s) within ArtistDesign | Strengthen link between high-performance computing and parallel programming and embedded systems |
| Research interests | Parallel systems, program analysis, programming methods |
| Role in leading conferences/journals/etc in the area | Journal editor for: *Parallel Processing Letters*, World Scientific Publ. Co. ; *Science of Computer Programming*, Elsevier Science B.V. ; *Scientific Programming*, IOS Press; *Int. J. of Parallel, Emergent and Distributed Systems*, Taylor & Francis; Chair of the Euro-Par steering committee, Chair of the IFIP WG 2.11 on Program Generation, programme committee member of various conferences |
| Notable present and past projects | LooPo: a loop parallelizer based on the polytope model (past and present DFG funding); MapReduceFoundation: Typing of MapReduce (DFG: 2011-2013, renewable); FeatureFoundation: Feature-Oriented Program Synthesis (DFG: 2008-2012, renewable); Meta-Programming (DAAD: 2004-2005, EC FP6: from 2004) PolyAPM: abstract parallel machines for the polytope model (DFG: 2000-2002); HDC: a language for parallel higher-order divide & conquer (DFG: 1996-2000) ; SAT: performance-directed parallel programming (1994-98) ; PLR: parallel linear recursion (1994-98) ; OSIDRIS: object-oriented specification of distributed systems (DFG: 1993-97) |

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|  | Prof. Dr. Rainer Leupers<br>http://www.ice.rwth-aachen.de |
| Technical role(s) within ArtistDesign | SW Synthesis and Code Generation, code optimization |
| Research interests | Compilers, ASIP design tools, MPSoC design tools |
| Role in leading conferences/journals/etc in the area | TPC member of DAC, DATE, ICCAD etc.<br>Co-founder of SCOPES workshop<br>General Co-Chair of MPSoC Forum 2008 (www.mpsoc-forum.org) |
| Notable past projects | HiPEAC NoE, SHAPES IP, several DFG-funded projects |

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| | Industry-funded projects with Infineon, Philips, Microsoft, Synopsys, ACE, Tokyo Electron etc. |
| Awards / Decorations | Several IEEE/ACM best paper awards |
| Further Information | Co-founder of LISATek Inc. (acquired by CoWare Inc. and Synopsys Inc,)<br>European Commission expert in FP7<br>Editor of "Customizable Embedded Processors", Morgan Kaufmann, 2006<br>Steering committee member of UMIC (Ultra High-Speed Mobile Information and Communication) research cluster (www.umic.rwth-aachen.de) |

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|  | Prof. Dr. Dr. h.c. mult. Reinhard Wilhelm (Saarland University)<br>http://rw4.cs.uni-sb.de/people/wilhelm |
| Technical role(s) within ArtistDesign | Timing Analysis |
| Research interests | Compilers, Static Analysis, Timing Analysis |
| Role in leading conferences/journals/etc in the area | PC member of SCOPES, LCTES, MEMOCODE, RTSS etc.<br>Steering committee member of EMSOFT, member at large of the steering committee of LCTES<br>Member of the ACM SIGBED Executive Committee |
| Notable past projects | DAEDALUS |
| Awards / Decorations | Prix Gay-Lussac-Humboldt in 2007<br>Honorary doctorates of RWTH Aachen and Tartu University in 2008<br>Konrad-Zuse Medal in 2009 |
| Further Information | Co-founder of AbsInt Angewandte Informatik GmbH<br>Scientific Director of the Leibniz Center for Informatics Schloss Dagstuhl |

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|  | Prof. Dr. Peter Puschner (TU Vienna)<br><br>Real-Time Systems Group<br>Institute of Computer Engineering<br>Vienna University of Technology<br><br>http://www.vmars.tuwien.ac.at/people/puschner.html |
| Technical role(s) within ArtistDesign | Peter Puschner and his group are participating in the Timing-Analysis activities of the Compilation and Timing Analysis cluster. Within ArtistDesign the contributions are in the area of path-description languages for static WCET analysis, compilation support for WCET analysis, methods and problems of measurement-based execution-time analysis, and on software and hardware architectures that support time predictability. |
| Research interests | Peter Puschner's main research interest is on real-time systems. Within this area he focuses on Worst-Case Execution-Time Analysis and Time-Predictable Architectures. |
| Role in leading conferences/journals/ etc in the area | Member of the Euromicro Technical Committee on Real-Time Systems, the steering committee of the Euromicro Conference on Real-Time Systems (ECRTS)<br><br>Member of the advisory board and organizers committee of the IEEE International Symposium on Object- and Component-Oriented Distributed Computing (ISORC) conference series<br><br>Chair of the Steering Committee of the Euromicro Workshop on Worst-Case Execution-Time Analysis (WCET) series |
| Notable past projects | DECOS - Dependable Embedded Components and Systems<br>Develop the basic enabling technology to move from a federated distributed architecture to an integrated distributed architecture.<br>http://www.decos.at<br><br>MoDECS - Model-Based Development of Distributed Embedded Control Systems<br>Model-based construction of distributed embedded control systems: shift from a platform-oriented towards a domain-oriented, *platform-independent* development of composable, distributed embedded control systems.<br>http://www.modecs.cc<br><br>NEXT TTA<br>Enhance the structure, functionality and dependability of the |

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| | time-triggered architecture (TTA) to meet the cost structure of the automotive industry, while satisfying the rigorous safety requirements of the aerospace industry.<br>http://www.vmars.tuwien.ac.at/projects/nexttta/ |

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|  | Dr. Iain Bate (University of York)<br>http://www-users.cs.york.ac.uk/~ijb/ |
| Technical role(s) within ArtistDesign | Responsible for the WCET cluster at University of York. Also involved in the Design for Adaptivity cluster. |
| Research interests | Worst-case execution time analysis. Design and certification of critical real-time systems. Design for flexibility. Search-based systems engineering. Use of novel computation techniques, e.g. Artificial Immune Systems. |
| Further Information | Also director of Origin Consulting (York) Ltd. a spin-off company providing consultancy on the design and certification of critical systems. |

### *4.2 Affiliated Industrial Partners*

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| | Joseph van Vlijmen (ACE, Netherlands) |
| Technical role(s) within ArtistDesign | The design and construction of extensions to CoSy required for ArtistDesign projects. |
| Research interests | The development and exploitation of compilation techniques and development systems in the wider contexts of SoC and EDA supported by descriptions of the system including application and target architectures. Particular interests include MPSoC and highly parallel system. |
| Role in leading conferences/journals/etc in the area | Programme Committees of SCOPES and DATE. |
| Notable past projects | COMPARE/PREPARE ESPRIT projects:<br>These projects particularly COMPARE, were precursors for CoSy. PREPARE focused on retargetable compilation for Fortran 90 and High Performance Fortran using massively parallel MIMD machines.<br><br>MESA/NEVA (ongoing):<br>Framework IPs addressing the challenges of designing and |

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| | constructing multi-processor systems. |
| Further Information | Principal architect of the CoSy. Previously, architect of ACE's shared memory heterogeneous multiprocessor UNIX OS. |

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| | Dr. Marco Bekooij (NXP) |
| Technical role(s) within ArtistDesign | Strengthen link to work on code synthesis and industry |
| Research interests | Design of predictable systems |

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|  | Dr.ir. Bart Kienhuis (Compaan Design B.V., Leiden)<br>http://www.liacs.nl/~kienhuis/ |
| Technical role(s) within ArtistDesign | Strengthen link to work on code synthesis and industry |
| Research interests | Design of predictable systems |

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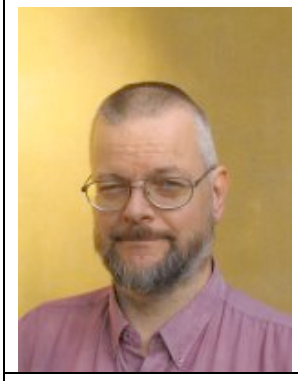
|  | Dr. Niklas Holsti (Tidorum Ltd)<br>http://www.tidorum.fi |
| Technical role(s) within ArtistDesign | Participate in the definition of the common WCET tool-set architecture, the analysis modules and the interchange representations (languages, file formats).<br>Adapt Tidorum's WCET tool, Bound-T, to integrate with the architecture and interchange formats defined in ArtistDesign |
| Research interests | Static analysis of the worst-case execution time of embedded programs. |

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|  | Dr. Christian Ferdinand (AbsInt Angewandte Informatik GmbH)<br>http://www.absint.com/ |
| Technical role(s) within ArtistDesign | Christian Ferdinand coordinates the activities of AbsInt within Artist Design. |
| Research interests | Timing analysis, program optimization, and compiler construction. |
| Notable past projects | Transferbereich 14 "Run-time Guarantees for modern Processor Architectures" of the German DFG.<br>DAEDALUS: RTD project IST-1999-20527 of the European FP5 program on the validation of software components embedded in future generation critical concurrent systems by exhaustive semantic-based static analysis and abstract testing methods based on abstract interpretation.<br>http://www.di.ens.fr/~cousot/projects/DAEDALUS/index.shtml<br>INTEREST: EU Framework VI Specific Targeted Research Project IST-033661 aiming at overcoming the lack of integration and interoperability of tools for developing Embedded Systems software.<br>INTERESTED: EU Framework 7 Collaborative Project IST-214889 aiming at realising a European-wide tool reference development environment validated by major tool users through real-life Industrial Validators, ensuring an integrated, lower cost, highly dependable, safe and efficient development process. http://interested-ip.eu/<br>ALL-TIMES: EU Framework 7 Collaborative Project IST-215068 aiming at combining currently available timing tools, enabling interoperability of tools and developing integrated tool chains using open tool frameworks and interfaces. http://www.all-times.org/<br>PREDATOR: EU Framework 7 Collaborative Project IST-216008 PREDATOR on design for predictability and efficiency, studying the interplay between efficiency requirements and critical constraints in embedded system design. http://www.predator-project.eu/ |
| Awards / Decorations | Dr. Ferdinand received the Dr. Eduard Martin Preis in 1999 (award for best PhD Thesis in computer science at Saarland University).<br>AbsInt has been awarded a 2004 European Information Society Technology (IST) Prize for its timing analyzer aiT. |

### 4.3 Affiliated Academic Partners

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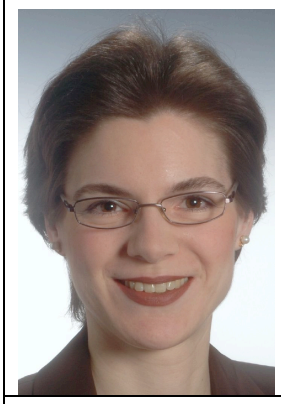
|  | Prof. Dr. Sabine Glesner (Technical University of Berlin)<br>http://www.pes.tu-berlin.de |
| Technical role(s) within ArtistDesign | Affiliated PartnerCompiler Verification, Optimizing Compilers |
| Research interests | Compilers, Verification, Embedded Systems and Software, Formal Semantics |
| Role in leading conferences/journals/etc in the area | PC Member of Compiler Construction 2007, 2011<br>PC Member of European Symposium on Programming (ESOP) 2008<br>Date'06, Design, Automation and Test in Europe, TPC Member of Topic B9 on Formal Verification<br>Workshop Compiler Optimization meets Compiler Verification COCV, ETAPS Conferences, PC Member in 2005 and 2006, Program Co-Chair in 2007<br>Workshop Formal Foundations of Embedded Software and Component-Based Software Architectures (FESCA), ETAPS Conferences, PC Member 2005 and 2006<br>Editorial Board Member of “Informatik – Forschung und Entwicklung” by Springer, starting with Vol. 21, No. 1 |
| Notable past projects | KorMoran (Correct Model Transformations), funded by DFG<br>MeMo (Methods for Model Quality), funded by the Investitionsbank Berlin, in cooperation with Berner & Mattner Systemtechnik GmbH and Model Engineering Solutions GmbH<br>VATES (Verification and Transformation of Embedded Systems), funded by DFG<br>Aktionsplan Informatik (Emmy Noether-Program), funded by DFG, support for young researchers to build a research group, with a focus on optimization and verification in the compilation of higher programming languages, from 2004 to 2009<br>Correct and Optimizing Compilers for Modern Processor Architectures, funded by a PostDocs excellence program of Baden-Württemberg, Germany, 2003-2005<br>Grant in the Wrangell-Habilitation Program of Baden-Württemberg, Germany, 2001-2005 |

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| Awards / Decorations | Award of the “Forschungszentrum Informatik” for one of the two best PhD theses of the Faculty for Computer Science, University of Karlsruhe, 1998/99<br>Member of the “Studienstiftung des deutschen Volkes”, the German national scholarship organization, 1991-1996<br>Fulbright grant to study at the University of California, Berkeley, 1993-1994<br>Member of the Siemens Internationaler Studenten / Doktorandenkreis, 1993-1999 |

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|  | Dr. Björn Franke (Lecturer, University of Edinburgh)<br>http://homepages.inf.ed.ac.uk/bfranke/Welcome.html |
| Technical role(s) within ArtistDesign | Provide a link to work on program analysis and parallelization |
| Research interests | Compilers, embedded systems |

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|  | Prof. Paul Kelly (Imperial College, London)<br>http://www.doc.ic.ac.uk/~phjk/ |
| Technical role(s) within ArtistDesign | Provide a link to work on program analysis and parallelization |
| Research interests | Software performance optimization |

Dr. Alain Darte

Scientific leader of Inria Project Compsys
(Compilation and Embedded Computing Systems)

Laboratoire de l'Informatique du Parallélisme

CNRS, Inria, UCBL, ENS-Lyon

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| http://perso.ens-lyon.fr/alain.darte | |
| Technical role(s) within ArtistDesign | Activity in automatic parallelization, source to source transformations for high-level synthesis of hardware accelerators, possibly WCET. |
| Research interests | Code optimizations for embedded computing systems: back-end code optimizations (SSA form, register allocation, static/JIT compilation), source-to-source code transformations for HLS tools (code rewriting, memory and communication optimizations). |
| Role in leading conferences/journals/etc in the area | Editorial board of ACM Transactions on Embedded Computing Systems (ACM TECS). Program committees in 2008-09: SCOPES 2009, PLDI 2008, CC 2008. Before 2008: many DATE, CASES, ASAP, ICS, CGO, etc. |
| Notable past projects | Minalogic project SCEPTRE<br>Collaboration with STMicroelectronics, funded by French Ministry of Research and Région Rhône-Alpes |
| Awards / Decorations | Best paper awards: IPDPS 2002, CGO 2007 |

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|  | Prof. Dr.-Ing. Jürgen Teich (U. Erlangen-Nürnberg, Germany)<br>http://www12.informatik.uni-erlangen.de/people/teich/ |
| Technical role(s) within ArtistDesign | Mapping of applications to MPSoCs |
| Research interests | Hardware/software codesign |
| Notable past projects | SystemCoDesigner and others |

| | |
|---|---|
|  | Prof. Ed Deprettere (Leiden University, Netherlands)<br>http://www.liacs.nl/~edd/ |
| Technical role(s) within ArtistDesign | Mapping of applications to MPSoCs |
| Research interests | Multimedia and Signal Processing Algorithms, Architectures and Applications |
| Notable past projects | Daedalus and others |

### *4.4 Affiliated International Partners*

Prof. Abhik Roychoudhury

(Associate Professor, National University of Singapore)

http://www.comp.nus.edu.sg/~abhik/

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| Technical role(s) within ArtistDesign | Timing Analysis |
| Research interests | Software Analysis/Validation, Design Tools for Embedded Systems, Formal Methods in System Design. |
| Role in leading | Recent Program Committee work includes: |

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| conferences/journals/etc in the area | RTSS 2010/2011, DATE 2012, WCET 2010/2011, LCTES 2012 |
| Notable past projects | "Timing Analysis of Behavioural System Models" (2007 -10) http://www.comp.nus.edu.sg/~abhik/projects/model-timing/<br>"EASEL: Engineering Architectures and Software for the Embedded Landscape" (2006-09), Funded by A*STAR Singapore under Embedded and Hybrid Systems Programme.<br>"Chronos: Architectural Modelling for Timing Analysis of Embedded Software" (2003 – 07) http://www.comp.nus.edu.sg/~rpembed/chronos/ |
| Awards / Decorations | Tan Kah Kee Young Inventor's Award 2008. |

Prof. Soonhoi Ha

(Professor, Seoul National University)

http://iris.snu.ac.kr/sha/

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|---|---|
| Technical role(s) within ArtistDesign | Mapping of applications to MPSoCs |
| Research interests | Hardware-software codesign, design methodology for embedded systems and embedded software |
| Role in leading conferences/journals/etc in the area | Recent Program Committee work includes:<br>Program chair, CODES/ISSS 2006 |
| Notable past projects | PeaCE: Codesign Environment (http://peace.snu.ac.kr/research/peace/)<br>HOPES |

# 5. Internal Reviewers for this Deliverable

- **Prof. C. Lengauer** (U. Passau)
- **Prof. Dr. Olaf Spinczyk** (TU Dortmund)