IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Cluster Progress Report for Year 4

Cluster:
Hardware Platform and MPSoC Design

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Policy Objective (abstract)

The purpose of this cluster is to integrate different view points and approaches to MPSoC design and programming. The cluster will consider the hardware architecture and software components in their interaction, investigate tools for accurate estimation of certain design parameters (power, performance), and provide the designer with adequate support for design space exploration and optimization.

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1. Overview

In relation to the ArtistDesign network, it is the overall goal of the topic on hardware platforms and MPSoC design to extend the current state in composability towards issues like modeling of non-functional constraints, power and energy, end-to-end real-time behavior, timing and performance analysis and heterogeneous models of computation.

Many application domains require adaptive real-time embedded systems that can change their functionality over time. In such systems it is not only necessary to guarantee timing constraints in every operating mode, but also during the transition between different modes. Therefore, it is one of the goals to develop new methods for the design and analysis of adaptive multi-mode systems.

One of the most critical issues to be faced in the research on execution platform is their rapidly growing complexity. Complexity increase is pushed by Moore's law, and by the ever-increasing demand for high performance computing. In addition, the boundaries between hardware and software domains are getting more blurred (dynamically re-configurable hardware, adaptable embedded systems, breakthrough in power consumption and performance) and challenging questions are at the border (trade-offs in mapping applications to hardware and software components, re-configurable hardware, WCET, performance of distributed computer and communication systems).

The cluster attempts to combine the diverse knowledge and to integrate different approaches in the area of execution platforms for embedded systems available in Europe and beyond.

1.1 High-Level Objectives

The purpose of this cluster is to integrate different view points and approaches to MPSoC design and programming. Therefore, the work is based on existing and future hardware platforms and their expected properties as well as anticipated application domains. The cluster will consider the hardware architecture and software components in their interaction, investigate tools for accurate estimation of certain design parameters (power, performance) based on appropriate models for hardware and software components, and provide the designer with adequate support for design space exploration and optimisation.
The importance of resource awareness in embedded systems is growing very rapidly. One major aspect is predictability, in particular concerning the timing behaviour. With the growing software content in embedded systems, and the diffusion of highly programmable and re configurable platform, software is given an unprecedented degree of control on resource utilization. Therefore, the major focus of the combined activities is to establish a design methodology that;

- scales to massively parallel and heterogeneous multiprocessor architectures,
- allows for predictable system properties
- uses the available hardware resources in an efficient manner.

Promising approaches are based on increasing the adaptivity on various levels and on composable frameworks.

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

1.2 Industrial Sectors

As hardware platforms are the backbone of embedded systems, the activities of this cluster spans all industrial sectors. A recent and accelerating trend is the move towards multicore platforms.

In the automotive domain, the increasing number of functions has led to automotive networks with a large number of distributed ECUs and increasing complexity with several busses and gateways that is difficult to handle. In next generation systems, large automotive OEMs are therefore proposing new structured hardware topologies, that focus on the application of powerful domain controllers connected over a high speed bus and several dedicated busses for the different functional domains. Multicore control units (MCUs) are perceived as a co-enabler for this technology, by allowing the integration of a large number of functions, at relatively low power and with various reliability and fail-safe options.

A similar trend can be observed in the aerospace domain, where multicore components need to be integrated into complex networks with commonly very high reliability requirements.

In the multimedia domain, the emerging trend for multimedia applications on mobile terminals, combined with a decreasing time-to-market and a multitude of standards have created the need for flexible and scalable computing platforms that are capable of providing considerable (application specific) computational performance at a low cost and a low energy budget. Platforms like TI OMAP, ST Nomadik, Philips Nexperia and IBM/Toshiba/Sonys CELL, contain multiple heterogeneous, flexible processing elements, a memory hierarchy and I/O components. All these components are linked to each other by a flexible on-chip interconnect structure. These architectures meet the performance needs of multimedia applications, while limiting the power consumption.

Also in the mechatronics domain, which traditionally was a rather sequential process, there is a trend towards multi-core platforms and the need to support the designer to make well-founded choices for an execution platform. Techniques from the multimedia domain are now being extended and adapted to deal with control-dominated high-tech applications as well.

Another clear trend is towards reconfigurable architectures, in general, and configurable processors, in particular. The generic goal is to achieve a high degree of flexibility (traditionally available only with software implementation) at an power consumption, which is much lower than achievable with a traditional software implementation using general purpose processors.

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

1.3 Main Research Trends

Many embedded system applications are implemented today using distributed architectures, consisting of several hardware nodes interconnected in a network. Each hardware node can consist of a processor, memory, interfaces to I/O and to the network. The networks are using specialized communication protocols, depending on the application area. For example, in the automotive electronics area communication protocols such as CAN, FlexRay and TTP are used. One important trend today is toward the integration of multiple cores on the same chip, hence embedded systems are not only distributed across multiple boards or chips, but also within the same chip.

As the complexity of the functionality increases, the way it is distributed has changed. If we take as an example the automotive applications, initially, each function was running on a

dedicated hardware node, allowing the system integrators to purchase nodes implementing required functions from different vendors, and to integrate them into their system. Currently, number of such nodes has reached more than 100 in a high-end car, which can lead to large cost and performance penalties. Moreover, with the advent of poly-core (i.e. high cardinality multi-core) single-chip platforms, the effective number of processing nodes tends to grow in a "fractal" way, and future distributed systems with thousands of processing nodes are not a far away dream.

Not only the number of nodes has increased, but the resulting solutions based on dedicated hardware nodes do not use the available resources efficiently in order to reduce costs. For example, it should be possible to move functionality from one node to another node where there are enough resources (e.g., memory) available. Moreover, emerging functionality, such as brake-by-wire, is inherently distributed, and achieving an efficient fault-tolerant implementation is very difficult in the current setting.

Moreover, as the communications become a critical component, new protocols are needed that can cope with the high bandwidth and predictability required. The trend is towards hybrid communication protocols, such as the FlexRay protocol, which allows the sharing of the bus by event-driven and time-driven messages. Time-triggered protocols have the advantage of simplicity and predictability, while event-triggered protocols are flexible and have low cost. A hybrid communication protocol like FlexRay offers some of the advantages of both worlds. The need for scalable and predictable communication is not only a characteristic of automotive designs, but even multimedia and signal processing systems are increasingly communication dominated.

While computation and communication are clear targets, common consensus has been growing on the criticality of memory architecture and related memory management software challenges. Even predictable and efficient processors and communication fabrics are not sufficient to provide a predictable and efficient application level view of the platform if not adequately supported by a memory system.

The trend towards distributed architectures introduces a new challenge. A lot, if not most of the traditional software is sequential in nature. Major reason for this is that most modern programming languages are sequential and do not have adequate language-level concurrency support. Traditionally the timing performance of software increased as a result of the increase in clock speed of the individual processing cores. However, this free lunch is over because clock speeds have hardly increased since 2003. Multi-core and hyperthreading techniques are now used to boost platform performance. Modern compilers based on sequential programming languages are not able to sufficiently utilize these additional computational resources. New languages, techniques and tools are required that seamlessly match modern execution platforms, for instance by adequate application-level concurrency support. Although a number potential techniques already exist, getting more momentum in these directions is crucial to deal with future complexity and performance requirements.

With growing embedded system complexity more and more parts of a system are reused or supplied, often from external sources. These parts range from single hardware components or software processes to hardware-software (HW-SW) subsystems. They must cooperate and share resources with newly developed parts such that the design constraints are met. There are many software interface standards such as CORBA, COM or DCOM, to name just a few examples that are specifically designed for that task. Nevertheless in practice, software integration is not a solved but a growing problem. This is especially true when performance and energy efficiency can be achieved only if a sufficient degree of parallelism in application execution is achieved.

New design optimization tools are needed to handle the increasing complexity of such systems, and their competing requirements in terms of performance, reliability, low power

consumption, cost, time-to-market, etc. As the complexity of the systems continues to increase, the development time lengthens dramatically, and the manufacturing costs become prohibitively high. To cope with this complexity, it is necessary to reuse as much as possible at all levels of the design process, and to work at higher and higher abstraction levels, not only for specification of overall system functionality, but also for supporting communication among a number of parallel executing nodes.

One of the most significant achievements in the cultural landscape of low-power embedded systems design is the consensus on the strategic role of power management technology. It is now widely acknowledged that resource usage in embedded system platforms depends on application workload characteristics, desired quality of service and environmental conditions. System workload is highly non-stationary due to the heterogeneous nature of information content. Quality of service depends on user requirements, which may change over time. In addition, both can be affected by environmental conditions such as network congestion and wireless link quality.

Power management is viewed as a strategic technology both for integrated and distributed embedded systems. In the first area, the trend is toward supporting power management in multi-core architectures, with a large number of power-manageable resources. Silicon technology is rapidly evolving to provide an increased level of control of-on chip power resources. Technologies such as multiple power distribution regions, multiple power-gating circuits for partial shutdown, multiple variable-voltage supply circuits are now commonplace. The challenge now is how to allocate and distribute workload in an energy efficient fashion over multiple cores executing in parallel. Also, one open issue is how to cope with the increasing amount of leakage in nanometer technologies, which tends to over-emphasize the cost of inactive logic, unless it can be set in a low-power idle state (which in many cases implies storage losses and high wakeup cost).

In the area of distributed low-power systems, wireless sensor networks are the key technology drivers, given their tightly power constrained nature. One important trend in this area is toward “battery free” operation. This can be achieved through energy storage devices (e.g. super-capacitors) coupled with additional devices capable of harversting energy from environmental sources (e.g. solar energy, vibrational energy). Battery-free operation requires carefully balancing harvested energy and stored energy agains the energy consumed by the system, in a compromise between quality of service and sustainable lifetime.

The concept of Multiprocessors-on-a-chip (MPSoC) has been discussed since some years but it appears that recently, the area has gained much more interest. In terms of industrial support, an increasing number of companies are active in the design of corresponding architectures as well as introducing the first products in the market. Whereas there are major breakthroughs in terms of new hardware architectures, corresponding programming environment are still at their infancy. In particular, ease of application specification, scalability, predictability of the overall system, parallelization, low power operation, efficiency and support of legacy code are just some of the main problems the community is facing.

A major industrial concern that comes with the integration of previously independent functions onto a single multicore or multiprocessor-system-on-chip is the resulting reliability of the individual functions. Depending on the criticality of a function, OEMs and indirectly their suppliers deliver guarantees to lawmakers on the overall failure rate of the system or component, with higher cost associated with the certification of higher level of reliability. Integration of functions with different reliability levels is then not cost efficient, if the resulting system needs to be verified for the highest level of reliability. A major research direction is therefore the investigation of methods that allow the co-integration of such functions. The researchers in ArtistDesign investigate countermeasures to this problem, for example by orthogonalization of the shared memory (e.g. Linköping University), or conservative bounds on the use of shared resources (e.g. TU Braunschweig).

A new and emerging research field related to embedded systems is that of design optimization for digital microfluidic biochips. Microfluidic biochips (also referred to as lab-on-a-chip) represent a promising alternative to conventional biochemical laboratories, and are able to integrate on-chip all the necessary functions for biochemical analysis using microfluidics, such as, transport, splitting, merging, dispensing, mixing, and detection. Biochips offer a number of advantages over conventional biochemical procedures. By handling small amount of fluids, they provide higher sensitivity while decreasing the reagent consumption and waste, hence reducing cost. Moreover, due to their miniaturization and automation, they can be used as point-of-care devices, in areas that lack the infrastructure needed by conventional laboratories. Due to these advantages, biochips are expected to revolutionize clinical diagnosis, especially immediate point of care diagnosis of diseases. Other emerging application areas include drug discovery, DNA sequencing, tissue engineering and chemical detection. Biochips can also be used in monitoring the quality of air and water, through real-time detection of toxins.

The digital microfluidic biochip is based on the manipulation of discrete, individually controllable droplets, on a two-dimensional array of identical cells. Due to the analogy between the droplets and the bits in a digital system, where are many similarities between the design of digital systems and digital microfluidic systems. Biochips, consisting of hundreds and thousands of cells have already been successfuly designed and commercialized. The actuation of droplets is performed by software-driven electronic control, without the need of micro-structures. Since each cell in the array is controlled individually, cells can be reconfigured during the execution of an assay to perform differents operations. Digital microfluidic biochips are expected to be integrated with microelectronic components in next generation system-on-chips. Consequently, models and techniques for the analysis and design of such systems are needed, including “biochemical compilers” which are able to efficiently map a biochemical application onto a digital microfluidic biochip.

In resent years, the Embedded Systems, i.e. information processing systems embedded into enclosing products, through which they interact with the physical world, has played an increasing role for our society and the importance and challenges related to the linking to physics has been stressed even more, leading to the new term Cyber-Physical Systems (CPS). CPSs are engineered systems focusing on the integration of computation and physical processes. Computation and communication are deeply embedded in and interacting with the physical processes, thereby adding new capabilities to physical systems.

CPSs will be a key technology for industrial innovation across a wide variety of industrial sectors, such as energy, healthcare, manufacturing, transportation and civil infrastructure. The added complexity arising from CPSs formed by open networks of embedded systems that are combining multiple application domains, will increase the challenges in designing, implementing, operating and maintaining such systems. In order to address these challenges new and extended design and analysis methods, supported by tools, are needed. The competences of and research directions by partners of ArtistDesign, cover many of these challenges. The hardware platforms and MPSoC design cluster has intensified its research within CPS by extending the work on distributed emebedded systems and wireless sensor networks, as well as in the area of control applications. This as among others lead to an increased focus on medical and biomedical applications and devices.

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

2. State of the Integration in Europe

2.1 Brief State of the Art

Modern embedded systems for multimedia, imaging, and signal processing are characterized by high performance requirements on the one hand and stringent power requirements on the other hand. Often, these requirements can no longer be satisfied by embedded system architectures based on a single processor. Thus, emerging embedded system-on-chip platforms are increasingly becoming multiprocessor architectures. To compensate the high nonrecurring costs for designing and manufacturing multiprocessor chips, however, they need to be flexible such that they can be reused in different systems. This flexibility calls for programmability and sometimes reconfigurability. As a result, embedded systems platforms often have a heterogeneous architecture consisting of fully dedicated hardware components and different programmable processor cores.

A considerable number of multi-processor design frameworks have been proposed in the past, such as Artemis, Distributed Operation Layer (DOL), Embedded System-Level Platform Synthesis and Application Mapping (ESPAM), Koski, or StreamIt. While all frameworks provide an automated path from application specification to system implementation, they focus on different aspects of the design flow. In ArtistDesign, we attempt to unify the approaches developed by the various partners and extend them towards new methods for performance analysis, design space exploration and adaptivity.

The past several years have seen an increasing interest in wireless sensor nodes that are scavenging energy from their environment. In [5], several technologies have been discussed how, e.g., solar, thermal, kinetic or vibrational energy may be extracted from a node‘s physical environment. In particular, techniques to harvest energy via photovoltaic cells have attracted the interest of the sensor network community [6]. Solar energy is certainly one of the most promising energy sources and typical environmental monitoring applications have access to solar energy. If sensor nodes are equipped with photovoltaic cells as energy transducers, the autonomy of sensor nodes is increased substantially since frequent recharging and replacement of the batteries becomes unnecessary. Ideally, sensor nodes once deployed in a harsh environment benefit from a drastically increased operating time and become virtually immortal.

Clearly, the power generated by small solar cells is limited. Sensor nodes executing a given application may frequently run out of energy in times with insufficient illumination. If one strives for predictable, continuous operation of a sensor node, common power management techniques have to be reconceived. In addition to perform classical power saving techniques, the sensor node has to adapt to the stochastic nature of solar energy. Goal of this adaptation is to maximize the utility of the application in a long-term perspective. The resulting mode of operation is sometimes also called energy neutral operation: The performance of the application is not predetermined a priori, but adjusted in a best effort manner during runtime and ultimately dictated by the power source. Therefore, storage devices like batteries are solely used as energy buffers to compensate the variations of the underlying energy source. It is the goal of the interaction in ArtistDesign to improve the state-of-the-art in energy scavenging and the corresponding algorithms to adapt the running applications so as to optimize a long-term reward function.

Design and analysis of biochip platforms from a computer science point of view is still largely inexplored in Europe. Only a few groups are working on CAD techniques for digital microfluidic based biochips. More groups are working on these biochips from the physical and materials science perspective.

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

2.2 Main Aims for Integration and Building Excellence through ArtistDesign

Following the activities presented in the previous section, the cluster on execution platforms follows the following strategy and uses the following mechanisms to spread the knowledge and integration achieved so far:

- Summer Schools and Training Activities to distribute the knowledge acquired in ArtistDesign to (a) other countries, (b) other communities and (c) young researchers.
- Tutorials at major conferences to reach new and larger research communities.
- Joint publications between partners, which not only show the integration within the cluster but are an excellent instrument to disseminate the integration results.
- New research projects with industrial partners, which allow us to apply the obtained results at an industrial scale. This way, we also receive feedback and ideas for new research directions.

Cooperation with other research groups, especially outside the EU (mostly USA and Asia). In this case, spreading excellence is not the only objective. The cluster participants can be exposed to new research problems and new approaches that can be then explored and improved within the cluster.

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

2.3 Other Research Teams

It appears that main research groups in Europe dealing with execution platforms for embedded systems are in the ArtistDesign network, either as full or as affiliated partners. There are some exceptions though, caused by the fact that not all are accepting a European network of Excellence as a viable funding instrument. In the following, some of these groups are listed together with their relation to ArtistDesign.

The University of North Carolina at Chapel Hill, Sanjoy Baruah and Jim Anderson. Sanjoy Baruah and Jim Anderson are known in particular for their research in the domain of multiprocessor real-time scheduling.

University of Dresden, Hermann Härtig. Hermann Härtig is a leading researcher in the domain of micro-kernel based real-time operating systems.

Low power embedded systems design: In the area of low power embedded systems design, several new and relevant research thems are explored by other teams, not included in the ARTIST2 network. In particular research groups in the USA have a long tradition of excellence in low power research. We can mention the group lead by prof. Jan Rabaey in UC Berlely, which is carrying out ground-breaking work on hardware platforms for wireless sensor networks. In the same area, several other groups are performing top-level research, e.g. Anantha Chandrakasan's group at MIT and David Blaauw's group at University of Michigan.

Low power execution platforms are not relevant only for wireless sensor network, but also for mobile computing and even for servers and traditional computing infrastructure (e.g. servers). In these areas, the groups lead by Profs. Vijaykrishnan Narayanan, Mahmut Kandemir and Mary Jane Irwin at Penn State University, has produced a large number of interesting results in the last few years. We mention in particular their work on power issues for 3D integration and their analysis of power vs. reliability tradeoffs in high-performance computing. In this area, very interesting work is also performed by the group of prof. Kevin Skadron. The focus of this group is on thermal issues, which are very significant for high-performance system.

Universita degli Studi di Verona/Electronic Design Automation (EDA) group, Prof. Franco Fummi. Main research activities of the EDA group concern system verification, system synthesis and optimization, hardware description languages, power consumption, language abstraction, and system testing. Interactions with members of the execution platforms cluster are, for example, by participation in European projects (e.g. the STRP “Vertigo”) together with the Linköping group.

University of Southampton,/Electronic Systems Design Group, Prof. Bashir Al Hashimi. The Electronic Systems Design (ESD) Research Group is internationally recognized in two main areas - the development of novel algorithms and methodologies for Electronic Design Automation to support the design and test of large systems, and for intelligent sensor micro-systems. The group is working in the areas of system modeling, simulation, and synthesis, SoC design and testing, as well as smart sensors. Several cooperation projects have been undertaken, in particular with the Linköping group.

Carnegie Mellon University/System Level Design Group/Prof. Radu Marculescu. The System Level Design group performs research on formal methods for system-level design of embedded applications. They, in particular, focus on fast methods for power and performance analysis that can guide the design process of portable information systems. Important results have been obtained with regard to the communication-centric SOC design, providing formal support for analysis and optimization of novel on-chip communication architectures. In particular, this work addresses fundamental research problems for defining scalable and flexible communication schemes via the Network-on-Chip (NoC) approach. Interaction has been by, for example, PhD student exchanges with the Linköping group.

Marco Caccamo (Univ. of Illinois at Urbana-Champaign): Real-time embedded systems are increasingly using Commercial-Off-The-Shelf (COTS) components in an effort to raise performance and lower production costs. In particular, fast multicore CPUs and high-performance DMA peripherals are required to service demanding applications such as video processing that are becoming more and more popular in markets such as automotive and avionic systems. Unfortunately, COTS components are not designed with timing predictability in mind, which makes it challenging to integrate them in real-time systems. In particular, most COTS architectures feature a single-port main memory that is shared among all CPU cores and peripherals. When a task suffers a cache miss, contention for access to main memory can significantly delay cache line fetch and greatly increase the worst case execution time (WCET) of the task. ETH Zuerich in cooperation with Marco Caccamo (Univ. of Illinois at Urbana-Champaign) developed a WCET analysis method for multi-core systems where tasks share a single memory. In particular, the joint work as published in DATE2010 provides the following contributions: (1) the computation of a curve bounding the memory traffic for each core, given a set of executed tasks. (2) an innovative algorithm that computes a delay bound for a task given traffic curves for all other cores and peripheral buses in the system. The algorithm is able to distinguish the behaviour of DMA peripherals, whose traffic is buffered, from the behaviour of CPU cores, which stall on cache misses. Overall this allows one to compute memory delay bounds for systems comprising any number of cores and any number of peripheral buses sharing a single main memory.

Lech Jozwiak (Department of Information and Communication Systems, Eindhoven University of Technology) is well known for his research on quality-driven design methodology, including intelligent design space exploration methods. His research focuses on the theory, methods and tools for modelling, analysis, synthesis and optimisation of digital circuits and (embedded) hardware/software systems.

Martin Radetzki, University Stuttgart, leads a group with a strong activity on fault tolerant techniques for Networks-on-Chip, in particular on network layer fault models and routing techniques. KTH has a collaboration in this area, one activity being to write a comprehensive survey on fault tolerant techniques in Networks-on-Chip

ETH and Zurich has established new research relations to *Kalray* and *Thales* in the area of certification, levels of criticality and fault tolerance. The goal is to extend the currently available methods to (a) different criticality targest (run-time, functional faults, temperature, memory) and (b) to end up with a component-based design approach that allows certification of individual functions with re-certification of the whole application.

DTU has developed a close collaboration with *Intel in Eindhoven (former Silicon Hive)*. This collaboration aims a extending the multi-ASIP platform toolflow with early design space exploration. Furthermore, DTU has extended its collaboration with *ARM in UK*, giving access to the complete set of tools from ARM.

EPFL has developed a close collaboration with the *Intel research lab in Braunschweigh, Germany*. This collaboration emphasizes the physical design 3-D systems, where the primary research efforts are on synchronization and power distribution and analysis. The overall objective is to explore the capabilities of these envisaged multi-layer circuits and to provide design methods and tools to overcome the related challenges. Several publications have stemmed from this collaboration at conferences within Europe, such as DATE, while EPFL has an active participation in an annual event organized by Intel related to the research in Europe. Furthermore, postgraduate students visit Intel premises to exchange ideas, report findings, and brainstorm on open research problems. The primary outcome of this collaboration, which is expected to continue over the following years, is a PhD degree and several master projects.

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Prof. Radetzki and the collaborations with Kalray, Thales, ARM and Intel has been added to the list.

2.4 Interaction of the Cluster with Other Communities

In terms of the design of highly reliable distributed embedded systems there is a close relationship to the Wireless Sensor Network Community. Especially ETH Zurich maintains close relations in terms of joint research activities and organization of conferences. One of the major conferences in this community, i.e. SENSYS, will be hosted by ETH Zurich in 2010. In terms of research, it is still an open issue how to design highly reliable and dependable sensor networks for applications in safty and security. The area of wireless sensor networks had a huge impact on the research in various fields related to electrical engineering and computer science. Spatially distributed sensor nodes are used as a new kind of measurement instruments to collect physical or environmental data. Examples of related research topics are low-power hardware design including wireless transceivers and microcontrollers, energy scavenging technologies, protocols for ad-hoc networks including multi-hop routing and

topology control, operating systems and middleware, security, mobility, simulators and deployment support. Much of this work was driven by the early vision of SmartDust [JM Kahn, RH Katz and KSJ Pister: Next century challenges: mobile networking for “Smart Dust”, 1999] where the individual devices will eventually be the size of a grain of sand, or even a dust particle. As a result of this challenging and inspiring vision of self-contained sensing, computation, communication and power, research in several of the above themes has been concentrating on concepts that reach the overall functionally of sensing network by means of redundancy and basic concepts of self-organization. One of the corner stones to achieve the required quality of service in terms of sensing density in time and space is over-provisioning.

The field of wireless sensor networks is now in a stage where serious applications of societal and economical importance are in reach such as industrial process monitoring and control, environment monitoring, logistics, healthcare applications, home automation, and traffic control.

The above mentioned concept of ‘reliability via over-provisioning’ that underlies much of the wireless sensor networks research so far is not suited to application domains that require dependability. Instead, all measurements are precious and must not be lost, reliable data must arrive in real-time, sensors are relatively expensive, and deployment of a sensor network and repair/update are very labor-intensive and expensive. One can argue that in order to significantly advance application domains by using a wireless sensor network as a novel means of observation and interaction, it is inevitable that such a tool be created as a quality scientific instrument with known and predictable properties and not a research toy delivering average observations at best. As a result, a new path in wireless sensor network research must be entered that is clearly distinguished from classical approaches and opens up new perspectives and challenges.

Research and development of several advanced sensing technologies and their systemlevel integration via systems and software engineering will be necessary: (a) Model-based design to ensure dependable operation in a highly resource-constraint setting. (b) Optimized use of harvested solar energy through long-term reward maximization. (c) Multi-objective optimization of the multi-processor hardware platforms (signal processor for preprocessing and sensor fusion, communication infrastructure) of a hierarchical system set-up. (d) Development of energy-efficient algorithms for real-time event detection. All of these research challenges are closely related to efforts in Cluster 2 of ARTISTDesign and a close relation to the WSN community is necessary for information exchange and joined research activities.

Participants of the MPSoC cluster (DTU, TU Braunschweig, Symtavision) and other ArtistDesign members (e.g. Aalborg University) are also contributing to the RECOMP project proposal, that was submitted in response to the second call for proposals of the European JU Artemis. Here, partners from automotive, avionics, and industrial automation (e.g. Intel, Infineon, Sysgo, Elektrobit, EADS IW, Delphi, TÜV Nord, and others) come together. The goal is to develop methods, tools and platforms for enabling cost-efficient certification and re-certification of safety-critical multi-core systems, with special emphasis on the design of mixed-criticality systems.

The research topics of this cluster with respect to multicore systems are mirrored by an increasing interest from industrial partner. For example, TU Braunschweig and GM Labs collaborate in the COMBEST project on the definition of methods and tools for the timing analysis of automotive systems based on a mix of complex communication protocols/software scheduling techniques. Already in 2008, a research cooperation between TU Braunschweig, Toyota Information Technology Center (T-ITC), and Symtavision GmbH has been initiated, investigating the effects of errors on reliability and safety of real-time networks.

KTH has a strategic and increasing collaboration with Fudan University in Shanghai and National University of Defense Technology in Changsha, China. It has been facilitated and

fostered by visits of faculty, joint courses, exchange of students and joint research projects. At KTH the Electronic Systems department hosts and educates almost ten PhD students from these two Universities and we expect this number to grow further as part of exchange programs. KTH faculty has given many short and long courses at Fudan during the last five years and several joint research projects in the areas of NoC, low power techniques and RFIDs have been initated. We believe in the mutual benefit of these partnerships due to complementare competence profiles (NoC and MPSoC at KTH; computer architecture at NUDT; security and RFID at Fudan) and complementary application profiles (telecom and multimedia at KTH; high end computing at NUDT; distributed low power embedded systems at Fudan).

CEA, DTU, TUBS, UNIBO from the MPSoC cluster has together with other partners of ArtistDesign (e.g. Verimag) submitted a research proposal on Smart Multicore Embedded Systems (SMECY) to ARTEMIS JU. The project has been accepted for funding and is currently under contract negotiations. The mission of the SMECY project is to develop new programming technologies enabling the exploitation of many (100s) core architectures. Multi-core technologies are strategic to keep and win market shares in all areas of embedded systems.

DTU and TUBS from the MPSoC cluster has, together with TU Eindhoven, UNICA, Silicon Hives, ACE, ST and Compann, submitted a research proposal on Automatic Architecture Synthesis and Application Mapping (ASAM) to ARTEMIS JU. The project has been accepted for funding and is currently under contract negotiations. This project addresses a uniform process of automatic architecture synthesis and application mapping for heterogeneous adaptive multi-processor embedded systems, defining a new unified
multi-processor system design methodology, as well as, supporting synthesis and prototyping tools and tool-chains.

ETHZ had an intense collaboration with Marco Caccamo, University of Illinois, concerning the formal analysis of shared buses and memories in multi-core systems. This cooperation lead to various new results and several publications on high-level conferences.

In addition, ETHZ had various collaborations with University of Munich (Samarjit Chakraborty) and University Karlsruhe (Jian-Jia Chen) on issues related to modular performance analysis, real-time calculus and its applications to power-aware scheduling disciplines.

TU Braunschweig has together with other partners from industry (e.g. Infineon, Siemens, ST Microelectronics, Elektrobit and others) and academia submitted a research proposal on Internet of Energy for Electric Mobility (IoE) to ARTEMIS JU. The project has been accepted and will start 2011. The objective of the IoE project is to develop hardware, software and middleware for seamless, secure connectivity and interoperability achieved by connecting the Internet with the energy grids. Reference designs and embedded systems architectures for high efficiency smart network systems will be addressed with regard to requirements of compatibility, networking, security, robustness, diagnosis, maintenance, integrated resource management, and self-organization.

KTH has started a collaboration with Martin Radetzki from University of Stuttgart on the topic of fault tolerant on-chip communication networks. In the last few years the group at Univeristy of Stuttgart has developed a strong activity on fault tolerant networks and developed techniques for fault tolerant routing and link level data integrity. Martin Radetzki has been visiting KTH in the three months period October – December 2010 to facilitate this research cooperation and to provide a graduate course on high level deign and modelling.

KTH is participating in the iFest Artemis project starting in summer 2010. It is coordinated by ABB and focuses on integrating and improving embedded systems tool chains and methodologies.

The Linköping group has strong cooperation with several leading groups from the control community. The work is in the area of control/computer co-design aiming at efficient implementation of control applications on distributed embedded systems. Common projects and PhD student exchanges have been running with the groups at Lund (Prof. Karl-Erik Årzén), UCLA (Prof. Paulo Tabuada), and University of Notre Dame (Prof. Michael Lemmon).

ETHZ has established new collaborations with environmental science communities in the are areas of pollution monitoring and geophysics. We are jointly setting up distributed measurement infrastructures based on research results obtained in ArtistDesign. Of particular relevance are methods that lead to dependable and fault-tolerant architectures that work under extreme environmental conditions. In addition, high requirements in terms of resource efficiency (energy, storage) need to be followed.

ETHZ has established new research relations to Korea, in particular the group of Soonhoi Ha, leading to student exchange and joint publications.

New R&D projects between TU Braunschweig and Daimler AG have been initialized to investigate the applicability and the performance (i.e. how useful are the obtainable results) of compositional system level timing analysis when applied to current and future automotive E/E architectures.

DTU and AAU has established new research collaborations with ISCAS (Institute of Software Chines Academy of Science) in Beijing and ENCU (East Normal University of China) in Shanghai. The collaboration is aimed at developing a theoretical foundation for Cyber Physical Systems.

-- Changes wrt Y3 deliverable --

Last five sections are new.

3. Overall Assessment and Vision for the Cluster

3.1 Final Overall Assesment

Over the 4 years periode, the MPSoC cluster has continued its efforts to establish an integrated modelling and design methodology that can take into account predictability and efficiency constraints. A major topic has been to involve all current layers with a particular emphasis on a resource-aware design trajectory. In this effort, we have focused on multi- and many-core platforms and platforms for distributed networked systems. A particular challenge has been to include and handle the concequences of new technological developments, such as 3D chip integration, variability, microfluidic components, and wireless sensors (e.g. for Cyber Physical Systems).

Within multicore SoC architectures the major themes are predictability, Network-on-Chip, programming models and resource awareness. The activities related to predictability have resulted in a better understanding of the subject of shared resource interference in multiprocessor systems, where the competition for e.g. a shared memory leads to a “feedback” on the task timing that breaks the predominant analysis approaches (in which the task timing is investigated in isolation). Open issues and possible improvements on the modelling and analysis approaches of multi-core systems with shared resources have been indentified and discussed with members of the Timing Analysis Cluster. Solutions have been presented that allow circumnavigating this problem in a formal performance analysis. Furthermore, efforts on the applicability of formal scheduling theory to realistic foreseeable industrial architectures (e.g. in the automotive domain) have been investigated. Applying formal methods to realistic use cases generally increases the user acceptance of formal analysis methods. Collaboration among partners has resulted in a number of analysis tools to analyse resource usage and timeliness. A new direction within on-chip network structures is the use of 3D structures that allows the stacking of cores. These new structures need to be captured by the design and analysis tools. A particular challenge is to capture thermal effects, allowing for temperature-aware design methods and tools. Another new research direction for NoC, has been the addressing of fault-tolerance for both transient and wear-out faults. Effort in understanding how to program multicore SoC has been investigated. This covers both programming models and how to use the parallel architectures to support adaptivity, including task distribution and migration. It also includes activities related to memory architechtures and on-chip memory management, resulting in new domain specific memory allocation techniques. There has been an increased focuse on the definition of runtime services for dynamic resource allocation and power management in the context of non-stationary system workloads, which has lead to the definition and design of a software runtime layer for the management of many-core systems. There has been an increasing interest in heterogeneous modelling at the system level which allows for both simulation and formal analysis and a new framework, the ForSyDe multi-MoC (Model of Computation) framework, has been included as one of the new platforms provided by the cluster. Finally, initial exploration of new emerging biochip platforms has been explored. It is expected that one of the next integration steps for SoC is to include capabilities for biochemical analysis and “computation”.

Within distributed architectures the major themes are reliability and fault-tolerance, and resource awareness, in particular energy. The activities related to fault-tolerance have resulted in new techniques where hardware and software tolerance techniques are combined and where hard real-time and soft real-time tasks can coexist gauranteing that hard real-time task will meet their deadlines in case of faults, while soft real-time tasks will experience a graceful degradation. The focus of the resource awareness has focused on the design of wireless sensor networks powered by energy harvesters. Emphasis has been on both node level

energy awareness and network level (system level) energy awareness. Results have shown that dynamic adaptation can result in significantly extended lifetime of wireless sensor networks. Modelling and QoS optimization of control applications is a new area of focus which had lead to very interesting work, with good publications.

3.1.1 Selected Highlights

A short summary of a few of the highlights are given below:

- **Fault tolerant distributed embedded systems:** Linkoping and DTU have collaborated on fault tolerance, in particular related to automotive systems. The work covers approaches to handle both processor and communication faults in distributed real-time systems based on CAN or FlexRay communication. Several timing analysis and cost optimisation methods have been proposed. The work resulted in highly referenced publications, a DATE best paper award, invited talks at major conferences.
- **Performance analysis methods:** Over the last years, the intense activity on developing performance analysis methods for multi- and many-core systems led to valuable solutions that have been published in different international journals and conference proceedings. Collaborations and discussions with members of the Timing Analysis Cluster helped to address challenges in the analysis of multi-core systems with shared resources. Some of the developed analysis methods were prototypically implemented (in the tool SymTA/S) and used in collaboration with industrial partners for the analysis of realistic use cases (e.g. in the automotive domain). This has increased the acceptance of formal analysis methods and triggered the integration of the research solutions in the commercially available version of the tool SymTA/S. The theoretical and practical results of the last four years are further exploited in other research projects, e.g. in the project “ModeWaves” (financed by the German Research Foundation / DFG) which deals with the timing analysis of multi-mode systems or in the ARTEMIS project “RECOMP” (Reduced Certification Costs for Trusted Multi-core Platforms) which aims at establishing methods, tools and platforms for cost-efficient certification and re-certification of safety-critical multi-core systems. Worth to be highlighted is also the joint work of TU Braunschweig and ETH Zurich on system level performance analysis methods for distributed systems. The two groups established a method for coupling the tools SymTA/S and MPA. Relying on different analysis techniques each of the two tools can be individually used to evaluate the performance of embedded real-time systems. The interface developed for tool coupling now allows combining the strengths of the two tools. Evaluations have been jointly performed and the work resulted in joint publications.
- **MPSoC design:** Major activities on MPSoC design have focused on application parallelization, platform mapping, memory hierarchy management, application scenario exploitation, and run-time resource management, including reconfigurable systems. The outcome of these 4 years was the development of realted tools, tool integration in tool chains in collaboration with several ArtistDesign partners, and highly referenced publications.
- **Energy harvesting:** Powering a wireless sensor network by harvesting energy from the environment, allows for obtaining zero-power systems. However, there are major challenges when having to synchronize and compute with unreliable energy resources. Partner from the MPSoC cluster have developed new node level scheduling techniques (UNIBO and ETHZ) as well as network level routing algorithms (DTU), and have demonstrated that these technoques can lead to considerable extensions of the lifetime of the network. One specific outcome is the founding of the company WISPES srl (Wireless Self-Powered Electronic Systems) which aims at providing technologies and devices able to add wireless communication and local computation to the customer's monitoring and sensing activities. Core technology is consists of small non intrusive self-powered sensors

able to bring a real time overview of the surrounding environment

- **Temperature and energy aware optimization:** EPFL has developed a novel online thermal management policy based on dynamic voltage and frequency scaling for high-performance 3-D systems with liquid cooling. The approach is able to gain up to 50% as compared to current state-of-the-art thermal control techniques.

3.1.2 Metrics

The vision for the MPSoC cluster for the 4-year period was to increase the interaction and collaboration between partners in order to advance theory, methods and tools for the design and analysis of MPSoCs and to disseminate this to industry and the scientific community. We set a goal of producing 40 joint publications, 4 workshops, 4 educational activities and 12 tutorials/special sessions. We have more than met these goals, e.g.,

- 82 joint publications related to hardware platform and MPSoC design has been generated.
- 249 individual publications related to hardware platform and MPSoC design has been generated.
- 8 tools for analysis and design of MPSoCs have been developed.
- 2 spin-off companies have been founded based on research results related to the cluster, and 1 spin-off company is in the pipeline for being founded.
- 9 workshops have been organized.
- 19 tutorials and 10 special sessions have been given at international conferences.
- The partners have given 64 invited talks.
- The partners have created a large amount of industrial contacts, where many are based on the activities created during ArtistDesign.
- The collaborations among the partners started in ArtistDesign are now being continued in several EU (many funded by Artemis JU) and national projects.

-- The above is new text, not present in the Y3 deliverable --

3.1.3 List of Joint Publications

The following list contains publications, where authors are in different research sites that are participating in the ArtistDesign network and where at least one author is in the cluster on Execution Platforms. It clearly shows the degree of integration that has been achieved. The following list collects all joint publications since the start of ArtistDesign:

Publications 2008

1. Viacheslav Izosimov, Paul Pop, Petru Eles, Zebo Peng, “Synthesis of Flexible Fault-Tolerant Schedules with Preemption for Mixed Soft and Hard Real-Time Systems”, 11th EUROMICRO CONFERENCE on DIGITAL SYSTEM DESIGN (DSD 2008), Parma, Italy, September 3-5, 2008, pp. 71-80.

2. Petru Eles, Viacheslav Izosimov, Paul Pop, Zebo Peng, “Synthesis of Fault-Tolerant Embedded Systems”, Design, Automation, and Test in Europe (DATE 2008), Munich, Germany, March 10-14, 2008, pp. 1117-1122.
3. Wu, K., Madsen, J., Kanstein, A., Mladen, B., *MT-ADRES: Multithreading on Coarse-Grained Reconfigurable Architecture*, Intel. Journal of Electronics (IJE), Volume 95, Issue 7, July 2008. Page(s): 761-776.
4. Anders Tranberg-Hansen, Jan Madsen, Bjørn Sand Jensen, A Service Based Estimation Method for MPSoC Performance Modelling, to appear in the proceedings of the 3rd International Symposium on Industrial Embedded Systems, June 2008.
5. A Reactive and Cycle-True IP Emulator for MPSoC Exploration Mahadevan, S.; Angiolini, F.; SparsSparso, J.; Benini, L.; Madsen, J. Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Volume 27, Issue 1, Jan. 2008 Page(s):109 – 122
6. ‘Enabling run-time memory data transfer optimizations at the system level with automated extraction of embedded software metadata information’, Bartzas, A.; Peon-Quiros, M.; Mamagkakis, S.; Catthoor, F.; Soudris, D. and Mendias, J., Asia and South Pacific Design Automation Conference - ASP-DAC, 2008
7. ‘Optimization Methodology of Dynamic Data Structures based on Genetic Algorithms for Multimedia Embedded Systems’, Baloukas, C.; Risco Martin, J.; Atienza, D.; Poucet, C.; Papadopoulos, L.; Mamagkakis, S.; Soudris, D.; Hidalgo, J.; Catthoor, F. and Lancares, J., Elsevier Journal of Systems and Software (JSS), 2008
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11. Traian Pop, Paul Pop, Petru Eles, Zebo Peng, Alexandru Andrei, “Timing Analysis of the FlexRay Communication Protocol”, Real-Time Systems Journal, Volume 39, Numbers 1-3, August, 2008, pp 205-235.
12. Traian Pop, Paul Pop, Petru Eles, Zebo Peng, Alexandru Andrei, “Analysis and Optimisation of Hierarchically Scheduled Multiprocessor Embedded Systems”, Intl. Journal of Parallel Programming, Volume 36, Number 1, February, 2008, pp. 37-67.
13. Bengt Jonsson, Simon Perathoner, Lothar Thiele, Wang Yi: Cyclic Dependencies in Modular Performance Analysis. ACM & IEEE International Conference on Embedded Software (EMSOFT), ACM Press, Atlanta, Georgia, USA, pages 179-188, October, 2008.
14. Simon Perathoner, Ernesto Wandeler, Lothar Thiele, Arne Hamann, Simon Schliecker, Rafik Henia, Razvan Racu, Rolf Ernst, Michael González Harbour: Influence of Different Abstractions on the Performance Analysis of Distributed Hard Real-Time Systems Design Automation for Embedded Systems, Springer Science+Business Media, LLC, 2008.

15. Davide Brunelli, Clemens Moser, Luca Benini, Lothar Thiele: An Efficient Solar Energy Harvester for Wireless Sensor Nodes. Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.
16. Clemens Moser, Lothar Thiele, Davide Brunelli, Luca Benini: Robust and Low Complexity Rate Control for Solar Powered Sensors Design, Automation and Test in Europe (DATE 08), Munich, Germany, March, 2008.
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24. Davide Brunelli, Clemens Moser, Lothar Thiele and Luca Benini Design of a Solar Harvesting Circuit for Battery-less Embedded Systems Accepted for publication in *IEEE Transactions on Circuits and Systems I*, 2009, regular papers.
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27. 3. S. Samii, P. Eles, Z. Peng, A. Cervin, "Quality-Driven Synthesis of Embedded Multi-Mode Control Systems," Design Automation Conference (DAC), San Francisco, California, USA, July 2009, pp. 864 - 869.

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73. [SMBM11] C. Seiculescu, S. Murali, L. Benini, and G. De Micheli. ”Design and Analysis of NoCs for Low-Power 2D and 3D SoCs”. In C. Silvano, M. Lajolo, and G. Palermo, editors, Low Power Networks-on-Chip, number 3, pages 199-222, Springer New York, 2011.
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76. Jakob Ròsen, Carl-Fredrik Neikter, Petru Eles, Zebo Peng, Paolo Burgio and Luca Benini , “Bus Access Design for Combined Worst and Average Case Execution Time Optimization of Predictable Real-Time Applications on Multiprocessor Systems-on-Chip”, in: Real-Time and Embedded Technology and Applications Symposium (RTAS), 2011 17th IEEE, Chicago, IL, pages 291 - 301, 2011
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Raghavan, C. Ykman-Couvreur, A. Bartzas, S. Xydis, D. Soudris, T. Kempf, G. Ascheid, R. Leupers, H. Meyr, J. Ansari, P. Mahonen and B. Vanthournout, "2PARMA: Parallel Paradigms and 3 Run-time Management Techniques for Many-Core Architectures", pp. 65-79, in "VLSI 2010 Annual Symposium", Selected Papers, Editors: N. Voros, A. Mukherjee, N. Sklavos, K. Masselos, M. Huebner, Lecture Notes in Electrical Engineering, Volume 57, 1st Edition., 2011, VIII, 331 p., Springer Netherlands, August 31, 2011, ISBN 978-94-007-1487-8

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80. C. Silvano, W. Fornaciari, S. Crespi Reghizzi, G. Agosta, G. Palermo, V. Zaccaria, P. Bellasi, F. Castro, S. Corbetta, E. Speziale, D. Melpignano, J.M. Zins, H. Hubert, B. Stabernack, J. Brandenburg, M. Palkovic, P. Raghavan, C. Ykman-Couvreur, I. Anagnostopoulos, A. Bartzas, D. Soudris, T. Kempf, G. Ascheid, H. Meyr, J. Ansari, P. Mahonen, B. Vanthournout, "Parallel programming and Run-time Resource Management Framework for Many-core Platforms: The 2PARMA Approach", accepted for presentation in the 6th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC'2011), Montpellier, France, June 20-22 2011 (invited paper).
81. Fabien Colas-Bigey (Thales), Sara Bocchio (ST-I), Chantal Couvreur (IMEC), Gianluca Palermo (POLIMI),Philipp A. Hartmann (OFFIS) “Audio Driven Video Surveillance System using COMPLEX design flow”, DATE workshop on designing for embedded parallel computing platforms: architectures, design tools, and applications, Grenoble, March 2011.
82. M. K. Jakobsen, J. Madsen, S. H. A. Niaki, I. Sander, J. Hansen, “System level modeling with open source tools”, to appear in proceedings of Embedded World 2012.

3.2 Assessment for Year 4

The following gives a list of some of the major achievements for year 4. Details and more information can be found in the two activity reports by the cluster, one on design and one on analysis.

LINKÖPING-DTU: Linköping and DTU have continued their work on fault tolerant embedded systems. This has resulted in joint development and publications. Prof. Paul Pop and Prof. Petru Eles have visited Linköping and DTU, respectively.

LINKÖPING-LUND: Linköping has a close cooperation with Lund (Artist design partner Cluster: Operating Systems and Networks) in the area of modelling and QoS optimisation of control applications. This has resulted in joint development and publications. Soheil Samii and Anton cervin have visited Lund and Linköping, respectively.

IMEC-KTH: IMEC and KTH continued their collaboration in the context of the European project MOSART (http://www.mosart-project.org). The Co-Ware virtual multi-core platform developed by IMEC was transferred to KTH for integration of the NoC architecture in the platform model.

IMEC-NTNU: there has been cooperation on data value driven scenario identification and reuse of epilepsy detection kernel as additional biomedical demonstrator for scenario related research.

IMEC has been concentrating on the following issues: i) Run-time monitoring of application parameters, within the European project 2PARMA, about parallel paradigms and run-time management for many-core architectures; ii) Distributed and hierachical run-time resource management, within the European project COMPLEX, aboutr codesign and power mangement in platform-based design space exploration; iii) Monitoring and control techniques in the middleware of the system to automatically adapt platform services to application requirements, within the European project Pharaon, about parallel and heterogeneous architecture for real-time applications

ETHZ – UDORT: By combining the expertise in evolutionary multiobjective optimization and compiler technologies, new approachs to improve the predictability of code while maintaining efficiency have been developed.

ETHZ- EPFL: A rigorously formal and compositional style for obtaining key performance and/or interface metrics of systems with real-time constraints has been developed by coupling the independent and different by nature frameworks of Modular Performance Analysis with Real-time Calculus (MPA-RTC) and Parametric Feasibility Analysis (PFA).

ETHZ-UDORT: New methods to map algorithms to MPSOCs have been developed and described in an overview article at CODES-ISSS.

ETHZ-UPISA: In a joint work with Giorgio Buttazzo, a new framework for analysing real-time servers has been developed and published.

ETHZ – TU Braunschweig: The collaboration between ETHZ and TU Braunschweig on coupling the tools SymTA/S and MPA continued with a study on the trade-off between results accuracy and analysis runtime. Despite the fact that a lossless conversion interface between the event models used by the two tools could not be achieved, the study showed that a precision threshold can be identified such that accurate results can be obtained in an acceptable amount of time.

EPFL-UNIBO: Interaction between EPFL and UNIBO was very active in Year 4. Major problems tackled include: 1) Network on Chips models and tools for 2-D and 3-D low power SoCs 2) Topology exploration to guarantee worst-case Quality of Service in critical flows; 3) Study of DRAM integration in NoC-based MPSoCs.

Exchanges with University of Bologna (UNIBO) continued from the previous years. Prof. Benini spent 1 month at EPFL as Visiting Professor.

UNIBO and EPFL have also interacted in developing a novel parallel simulation technology that leverages the computational power of widely-available and low-cost GPUs. UNIBO and EPFL developed a new simulation technology to deploy a parallel simulator for 1000-core systems on top of GPGPUs. The simulated architecture is composed by several cores (i.e. ARM ISA based), with instruction and data caches, connected through a Network-on-Chip (NoC).

UNIBO and ETHZ have collaborated in the porting of the DOL tool, modified in order to deal with 3D architectures, on a custom MPARM version which can model 3D platforms.

UNIBO-VERIMAG: the BIP system of VERIMAG has been connected to MPARM simulator for Bologna, with the final goal of validating on a cycle-accurate platform the BIP environment.

UNIBO-STM: MPARM simulator has been extended in order to model the P2012 architecture from STM. MPARM tool is indeed a cycle accurate simulator, and therefore it allowed several accurate design space explorations concerning different architectural choices in the final P2012 design.

DTU-KTH: The collaboration between DTU and KTH has been very active in year 4, with several joint technical meeting. A particular emphasis of year 4 has been to develop a SystemC version of the ForSyDe model that allows companies (and in particular SMEs) to use the formal framework. The framework and SystemC templates are available as Open Source, and a book with emphasis on practical usage of the framework is currently in draft.

-- The above is new text, not present in the Y3 deliverable --

3.3 Indicators for Integration

During year 4 we have done the following interactions between partners:

- *15 joint publications* have been produced. The plan was 10 Joint publications / year describing the results in terms of new methods and tools.
- Joint organization of workshops, tutorials, special sessions in international highly recognized conferences. In year 4 the following was accomplished:
  - Organized CODES+ISSS at Embedded Systems Week in Taipei, Taiwan, 2011
  - Organized workshop on Cyber Physical Systems at DAC, San Diego, USA, 2011
  - Organized Artist Summer School in China, Beijing, 2011
  - Organized a Summer School on Future Energy System in Trento (Italy), 2011
  - Organized a Summer School on Body arewa Network in Lausanne, 2011
  - Organized workshop on designing for embedded parallel computing platforms at DATE, Grenoble, France, 2011
  - Organized and gave tutorial at Symposium of System-on-Chip, Tampere, Finland, 2011
  - Gave a tutorial on multi-ASIP platforms at DATE, Grenoble, France, 2011
  - Gave a tutorial on memory architectures at DATE, Grenoble, France, 2011
  - Gave a tutorial on Microfluidic Biochips at Embedded Systems Week, Taipei, Taiwan, 2011
  - Organizing a Hot Topic session on Synthetic Biology at DATE, Dresden 2012
  - Organizing the ASYNC conference in Denmark, 2012
  - Organizing the NOCS conference in Denmark, 2012
  - Gave 8 tutorials at leading conferences
  - Gave 35 keynotes and invited talks at conferences and workshops, including ARTIST Summer School, RSP, and MPSoC.
- Yearly target is 1 workshop, 1 PhD course/school, 2-3 conference tutorials and special sessions.
- Integration of tools existing at the partner sites, and definition of tool flows integrating tools from the different partners.
  - The tool integration work is being continued. This covers both integration of tools within the cluster, between clusters of ArtistDesign and with external partners.
  - 8 tools have been produced by the cluster.
- Mobility, i.e. the number of PhD student and faculty exchanges. This integration activity will also introduce the concept of “student clusters”, where more than two PhD students from different partners will work together in a single location.
  - 6 PhD student visits
  - 6 faculty/researcher visits
  - 2 focused meetings

- Impact on industrial practice in the area of MPSoC design and analysis. This objective will leverage student internships at associated industrial partner's sites.
- A SME has been founded by PhD students formed under ArtistDesign NoE collaborations. The company is WISPES srl (Wireless Self-Powered Electronic Systems) and aims at providing technologies and devices able to add wireless communication and local computation to the customer's monitoring and sensing activities. Core technology is consists of small non intrusive self-powered sensors able to bring a real time overview of the surrounding environment.
- A SME is currently in the process of being founded by a PhD student formed under ArtistDesign collaborations. The company, eDNA Technologies, aims at providing a self-organizing and self-healing hardware platform for safety-critical systems.

Several PhD students have worked together with industry (and spent time in the companies) to apply tools and methods developed in the cluster in an industrial context.

-- Changes wrt Y3 deliverable --

Numbers and concrete events have been updated to reflect Y4.

3.4 Future Directions

The long-term vision for this activity is to advance the theory, methods and tools for the modeling, analysis and design of embedded systems and to disseminate this to advance academic excellence, education and industrial innovation.

Embedded systems are growing more software and communication centric. As a consequence, new models and new analysis and design space exploration tools are needed in order to support optimal implementation of applications on distributed embedded architectures such as MPSoC. Embedded systems are characterized by continuously increasing complexity and strong constraints on safety, performance, power consumption, and costs. To be able to design such systems, it is needed to (1) consider the hardware platform and software components of MPSoC systems in their interaction, in order to produce a system which satisfies the requirements at low cost, (2) support the designer with tools for accurate estimation of certain design parameters (power, performance) based on appropriate models for hardware and software components and (3) provide the designer with adequate support for design space exploration and optimisation.

Embedded architectures and heterogeneous distributed embedded systems have grown to extremely complex computation and communication patterns, and to an increasing level of reconfigurability (including adaptivity and run-time resource management). There will continue to be a need for new and better performance models and a corresponding theory.

The partners of the MPSoC cluster are already collaborating in several EU projects, many of which are in an industrial context (Artemis JU projects). The partners will hence, continue the joint effort of advancing theory, methods and tools for the modeling, analysis and design of embedded systems. Several partners are partners in the Guardian Angels project, aiming at becoming an EU FET Flagship project.

-- The above is text has been updated from the text in the Y3 deliverable --

4. Cluster Participants

-- Changes in the Cluster Participants wrt Y3 deliverable --

Senior researcher Chantal Ykman-Couvreurl has replaced Prof. Dr. Maja D'hondt as team leader for IMEC.

4.1 Core Partners

Cluster Leader Activity Leader & Team Leader	
	Jan Madsen (Technical University of Denmark)
Technical role(s) within ArtistDesign	Member of the Strategic Management Board Leads Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Integration Driven by Industrial Applications Leader of the JPRA Activity: "Platform and MPSoC Analysis"
Research interests	Research interests include high-level synthesis, hardware/software codesign, System-on-Chip design methods, and system level modeling, integration and synthesis for embedded computer systems.
Role in leading conferences/journals/etc in the area	Program Chair and Vice-Chair of Design Automation and Test in Europe Conference. Tutorial Chair and Special Sessions Chair of Design Automation and Test in Europe Conference. General Chair, Program Chair and Workshop Chair of CODES+ISSS Conference Member of the editorial board of the journal "IEE Proceedings – Computers and Digital Techniques" Member of the technical program committee and organizing committee of several technical conferences, including the Design Automation and Test in Europe Conference, the Real-Time Systems Symposium, the Symposium on Hardware-Software Codesign, and the International Workshop on Applied Reconfigurable Computing.

	Danish delegate in the Governing Board of ARTEMIS JU
Awards / Decorations	In 1995 he received the Jorck's Foundation Research Award for his research in hardware/software codesign

Team Leader	
	Lothar Thiele (ETH Zurich)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems and Software Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance
Research interests	Research interests include models, methods and software tools for the design of embedded systems, embedded software and bioinspired optimization techniques.
Awards / Decorations	In 1986 he received the "Dissertation Award" of the Technical University of Munich, in 1987, the "Outstanding Young Author Award" of the IEEE Circuits and Systems Society, in 1988, the Browder J. Thompson Memorial Award of the IEEE, and in 2000-2001, the "IBM Faculty Partnership Award". In 2004, he joined the German Academy of Natural Scientists Leopoldina. In 2005-2006, he was the recipient of the Honorary Blaise Pascal Chair of University Leiden, The Netherlands.

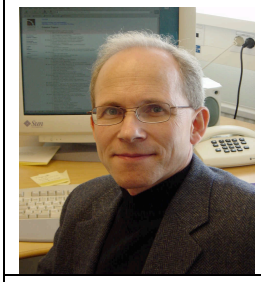
Team Leader	
	Prof. Luca Benini, University of Bologna http://www-micrel.deis.unibo.it/%7Ebenini/
Technical role(s) within ArtistDesign	Member of the Strategic Management Board Co-leads Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Leader of the JPRA Activity: “Platform and MPSoC Design”

Research interests	(i) Development of power modeling and estimation framework for systems-on-chip. (ii) Development of optimal allocation and scheduling techniques for energy-efficient mapping of multi-task applications onto multi-processor systems-on-chips. (iii) Development of energy-scavenging techniques for ultra-low power sensor network platforms.
Role in leading conferences/journals/etc in the area	▪ Program chair and vice-chair of Design Automation and Test in Europe Conference. ▪ Member of the 2003 MEDEA+ EDA roadmap committee 2003. ▪ Member of the IST Embedded System Technology Platform Initiative (ARTEMIS): working group on Design Methodologies ▪ Member of the Strategic Management Board of the ARTIST2 Network of excellence on Embedded Systems ▪ Member of the Advisory group on Computing Systems of the IST Embedded Systems Unit. ▪ Member of the technical program committee and organizing committee of several technical conferences, including the Design Automation Conference, International Symposium on Low Power Design, the Symposium on Hardware-Software Codesign. He is Associate Editor of the IEEE Transactions on Computer-Aided Design of Circuits and Systems and of the ACM Journal on Emerging Technologies in Computing Systems. ▪ Fellow of the IEEE.
Notable past projects	ICT-Project **REALITY - *Reliable and variability tolerant system-on-a-chip design in more-moore technologies.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.1 Next-Generation Nanoelectronics Components and Electronics Integration. Start date: 01/01/2008; Duration: 30 months; Contract Type: Collaborative project; Project Reference: 216537; Project Cost: 4.45 million euro; Project Funding: 2.9 million euro. ICT-Project **PREDATOR - *Design for predictability and efficiency.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.3 Embedded Systems Design. Start date: 01/02/2008; Duration: 36 months; Contract Type: Collaborative project; Project Reference: 216008; Project Cost: 3.93 million euro; Project Funding: 2.8 million euro. ICT-Project **GALAXY - *interface for complex digital system integration.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.3 Embedded Systems Design. Start date: 01/12/2007; Duration: 36 months; Contract Type: Collaborative project; Project Reference: 214364; Project Cost: 4.08 million euro; Project Funding: 2.9 million euro. ICT-Project **DINAMICS - *Diagnostic Nanotech and Microtech Sensors.*** Funded under 6th FWP (Sixth Framework Programme). FP6-NMP 'Nanotechnologies and nanosciences, knowledge-based multifunctional materials and new production processes and devices'. Contract Type: Integrated project; Project Reference:IP 026804-2. Start date: 01/04/2007. Duration: 18 + 30 months. Project

	Cost:7276856 Euro. Project Funding: 4499542 Euro. http://www.dinamics-project.eu/ ICT-Project **SHARE - *Sharing open source software middleware to improve industry competitiveness in the embedded systems domain.*** Funded under 7th FWP (Seventh Framework Programme). ICT-2007.3.7 Network embedded and control systems. Start date: 01/05/2008; Duration: 24 months; Contract Type: Coordination and support actions; Project Reference: 224170; Project Cost: 1.1 million euro; Project Funding: 590000.00 euro.

Team Leader	
	Rolf Ernst (TU Braunschweig)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Participates in Intercluster activity: Integration Driven by Industrial Applications
Research interests	Research interests include embedded architectures, hardware-/software co-design, real-time systems, and embedded systems engineering.
Role in leading conferences/journals/etc in the area	He chaired major international events, such as the International Conference on Computer Aided Design of VLSI (ICCAD), or the Design Automation and Test in Europe (DATE) Conference and Exhibition, and was Chair of the European Design Automation Association (EDAA), which is the main sponsor of DATE. He is a founding member of the ACM Special Interest Group on Embedded System Design (SIGBED), and was a member of the first board of directors. He is an elected member (Fachkollegiat) and Deputy Spokesperson of the "Computer Science" review board of the German DFG (corresponds to NSF). He is an advisor to the German Ministry of Economics and Technology for the high-tech entrepreneurship program EXIST (www.exist.org).

Team Leader

	Petru Eles (Linköping University)
Technical role(s) within Artist2	Main areas of research: Embedded Systems Participates in Hardware Platforms and MPSoC Design Participates in Intercluster activity: Design for Adaptivity Participates in Intercluster activity: Design for Predictability and Performance Participates in Intercluster activity: Integration Driven by Industrial Applications
Research interests	Research interests include electronic design automation, hardware/software co-design, real-time systems, design of embedded systems and design for testability.
Role in leading conferences/journals/etc in the area	- Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems; - Associate Editor, IEE Proceedings - Computers and Digital Techniques; - TPC Chair and General Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS). - Topic chair, Design Automation and Test in Europe (DATE). - Topic Chair, Int. Conference on Computer Aided Design (ICCAD). - Program chair of the Hw/Sw Codesign track, IEEE Real-Time Systems Symposium (RTSS). - TPC Chair IEEE Workshop on Embedded Systems for Real-Time Multimedia (ESTIMedia). - Steering Committee Chair, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS).
Awards / Decorations	- Best paper award, European Design Automation Conference (EURO-DAC), 1992. - Best paper award, European Design Automation Conference (EURO-DAC), 1994. - Best paper award, Design Automation and Test in Europe (DATE), 2005. - Best presentation award, IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS), 2003. - IEEE Circuits and Systems Society Distinguished Lecturer, for 2004 - 2005.

Team Leader

	Senior researcher Chantal Ykman-Couvreurl MEC vzw. http://www.imec.be
Technical role(s) within ArtistDesign	Representing IMEC Smart Systems and Energy Technology division in: -Cluster: SW Synthesis, Code Generation and Timing Analysis -Cluster: Operating Systems and Networks -Cluster: Hardware Platforms and MPSoC Design -Intercluster activity: Design for Adaptivity -Intercluster activity: Integration Driven by Industrial Applications
Research interests	Ch. Ykman-Couvreur is currently active in run-time management for embedded multi-core platforms
Role in leading conferences/journals/etc in the area	Ch. Ykman-Couvreur has published in International Journals and Conferences. She is active on several program committees of international conferences and in the organization of international workshops.
Notable past projects	Responsible for following FP7 European projects: GENESYS (http://www.genesys-platform.eu 2PARMA (http://www.2parma.eu) COMPLEX (http://complex.offis.de) PHARAON

Team Leader	
	Professor Axel Jantsch KTH http://web.it.kth.se/~axel/
Technical role(s) within ArtistDesign	A. Jantsch contributes to KTH participation and to the work on formal models of computation and communication and the ForSyDe framework. Furthermore, he also contributes to Hardware Platforms and MPSOC Design with focus on run-time environments and analysis techniques.
Research interests	A. Jantsch's main research topics are models of computation,

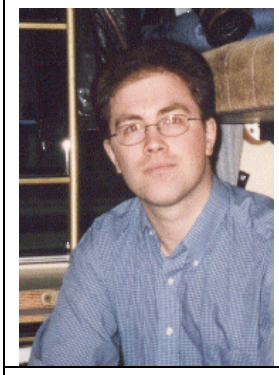
	modelling and analysis of embedded systems and SoCs, networks on chip.
Role in leading conferences/journals/etc in the area	TPC cochair of NoC Symposium 2009 Guest editor for IEEE Transactions on CAD TPC member of NOCS, DATE, CODES
Notable past projects	**ANDRES** (Analysis and Design of run-time Reconfigurable, heterogeneous Systems) Project) – EU FP6 (http://andres.offis.de/) **SPRINT** (Open SoC Design Platform for Reuse and Integration of IPs): EU FP6 (http://www.ecsi-association.org/sprint) **MOSART** (Mapping Optimization for Scalable multi-core ARchiTecture) – EU FP7 (http://www.mosart-project.org/) SYSMODEL: System Level Modeling Environment for SMEs – Artemis project (http://www.sysmodel.eu/)

Team Leader	
	Raphaël David, Ph.D (CEA LIST)
Technical role(s) within ArtistDesign	Participates in Hardware Platforms and MPSoC Design
Research interests	Main research interests are related to the exploration of new execution models for multiprocessing System-on-Chip and on development of exploration framework for multi- and many-core architectures. He is also studying advance strategies for the deployment and the management of multi-task applications onto multi- and many-core devices. He is also involved in the implementation of dynamically reconfigurable processors for image processing and low power design.

Team Leader	
	Professor Giovanni De Micheli EPFL http://si2.epfl.ch/~demichel/
Technical role(s) within	Giovanni De Micheli contributes to EPFL participation and to the work on models of computation for 3D integrated circuits, as well as

ArtistDesign	on models as policies for thermal evaluation and control
Research interests	De Micheli's research interests include several aspects of design technologies for integrated circuits and systems, such as synthesis, hw/sw codesign and low-power design, as well as systems on heterogeneous platforms including electrical, micromechanical and biological components.
Role in leading conferences/journals/etc in the area	General Chair of DATE 2010
Notable past projects	**Nano-tera.ch** (Engineering Complex Systems for Health, Security and the Environment) Swiss Federal grant (http://www.nano-tera.ch/) **PROD3D (**Programming for Future 3D Architecture with Many Cores): *EU FP7 starting project*

4.2 Affiliated Industrial Partners

	Daniel Karlsson (Volvo Technology Corporation)
Technical role(s) within ArtistDesign	Architecture and Design of Automotive Embedded Systems

	Kai Richter (SymTAVision GmbH)
Technical role(s) within ArtistDesign	Formal Performance Analysis and Optimization of Embedded Systems, Reliable System Integration, Early Architecture Exploration

	Dr. Arne Hamann (Robert Bosch GmbH)
Technical role(s) within ArtistDesign	Automotive Software Architectures

	Matthias Gries (Intel Germany)
Technical role(s) within ArtistDesign	Microprocessor Technology Lab, new computer architecture for embedded systems

	Rune Domsteen (Prevas A/S)
Technical role(s) within ArtistDesign	Embedded systems platform development

	Morten Kragh (Bang & Olufsen ICEpower)
Technical role(s) within ArtistDesign	Execution platforms for audio signal processing

	Dr. Valter Bella (Telecom Italia Lab)
Technical role(s) within ArtistDesign	Architecture and Design of Wireless Sensor Networks and Embedded Systems for Ambient Intelligence

4.3 Affiliated Academic Partners

	Ass. Professor Dimitrios Soudris (NTUA/ formerly DUTH) www.microlab.ntua.gr www.ee.duth.gr
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	Dimitrios Soudris received his Diploma in Electrical Engineering from the University of Patras, Greece, in 1987. He received the Ph.D. Degree in Electrical Engineering, from the University of Patras in 1992. He is currently working as Assistant Professor in Electrical and Computer Engineering, National Technical University of Athens (NTUA), Greece. His research interests include low power design, parallel architectures, embedded systems design, and VLSI signal processing. He was leader and principal investigator in numerous research projects funded from the Greek Government and Industry as well as the European Commission (ESPRIT II-III-IV and 5th, 6th and 7th IST). He is a member of the IEEE, the VLSI Systems and Applications Technical Committee of IEEE CAS and the ACM.
Role in leading conferences/journals/etc in the area	Dimitrios Soudris has (co-)authored over 180 papers in international journals and conferences, and has coauthored and edited 4 text books. He has served as General Chair and Program Chair for PATMOS' 99 and 2000 and General Chair IEEE/CEDA VLSI-SOC

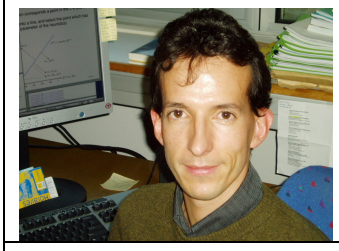
	2008. He received an award from INTEL and IBM for the project results of LPGD #25256 (ESPRIT IV) and 4th position in ASP-DAC 2005 Design Contest for AMDREL IST-34793.
Notable past projects	LPGD project Design of a low power GFSK/GMSK modulator/demodulator for DECT receivers. AMDREL project Development of dynamic memory management design methodologies for emebedded syetems. Design of a low energy FPGA and a software supported design flow.
Awards / Decorations	Dimitrios Soudris received an award from INTEL and IBM for the project results of LPGD #25256 (ESPRIT IV) and 4th position in ASP-DAC 2005 for AMDREL IST-34793.
Further Information	Dimitrios Soudris is also member at the Institute of Communications and Computer Systems

	Prof. David Atienza (EPFL, Switzerland, and Complutense University of Madrid, Spain) http://esl.epfl.ch/
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	David Atienza received his MSc and PhD degrees in Computer Science from Complutense University of Madrid (UCM), Spain, and Inter-University Micro-Electronics Center (IMEC), Belgium, in 2001 and 2005, respectively. Currently he is Professor and Director of the Embedded Systems Laboratory (ESL) at Ecole Polytechnique Fédérale de Lausanne, Switzerland, and Adjunct Professor at the Computer Architecture and Automation Department of UCM. His research interests focus on design methodologies for high-performance embedded systems and Systems-on-Chip (SoC), including new thermal management techniques for Multi-Processor SoCs, dynamic memory management and memory hierarchy optimizations for embedded systems, novel architectures for logic and memories in forthcoming nano-scale electronics, Networks-on-Chip interconnection design, and low-power design of embedded systems.
Role in leading conferences/journals/etc in the area	In these fields, David Atienza is co-author of more than 90 publications in prestigious journals and international conferences, such as, IEEE TCAD, IEEE Micro, IEEE T-VLSI Systems, ACM TODAES, Elsevier-Integration: The VLSI Journal, DAC, ICCAD, DATE, ASP-DAC, etc. Also, he is part of the Technical Program Committee of the DATE, ICCAD, GLSVLSI, VLSI-SoC, RTAS, SBCCI and PATMOS

	conferences, and Associate Editor of IEEE Transactions on CAD (in the area of System-Level Design) and Elsevier Integration: The VLSI Journal. He is the general chair of VLSI-SoC 2010 and organizer of several conferences including GLSVLSI '09, ISVLSI '09 and SBCCI '09.
Notable past projects	MDDTNSB-B22: "Materials, Devices and Design Technologies for Nanoelectronic Systems Beyond 22 nm CMOS" project *Development of reliability-aware design methodologies for emerging nano-scale electronics.* CMOSAIC project *Design of design 3D stacked processing architectures with interlayer cooling.* TIN2005-ARCHITECT project *HW/SW technologies for the design of high-performance processing systems*
Awards / Decorations	David Atienza received the nomination as co-author for the "2004 DAC Best Paper Award" and the "2006 ICCAD Best Paper Award". In September 2008 he was named IEEE Young Gold Member Coordinator in the area of EDA.
Further Information	Since 2008, he an elected member of the Executive Committee of the IEEE Council of Electronic Design Automation (CEDA).

	Associate Professor Per Gunnar Kjeldsberg (NTNU) www.iet.ntnu.no/en
Technical role(s) within ArtistDesign	Collaboration with IMEC vzw.and contribution to the Hardware Platforms and MPSoC cluster and the Software Synthesis, Code Generation and Timing Analysis cluster.
Research interests	Per Gunnar Kjeldsberg received his Sivilingeniør degree (MSc) in electrical engineering in 1992 from the Norwegian Institute of Technology. In 2001 he received the degree of Doktor ingeniør (PhD) from the same institution (now Norwegian University of Science and Technology, NTNU). During his doctoral studies, he focused on storage requirement estimation and optimization for data intensive applications. The research was performed in close cooperation with IMEC, in Leuven, Belgium, where he was a visiting researcher for nine months in all. His research interests are embedded hw/sw systems, with a focus on multi-media and digital signal processing applications. Between October 2005 and June 2006, Kjeldsberg was a visiting researcher at University of California, Irvine, Center for Embedded Computer Systems.
Role in leading conferences/journals/etc in the area	Kjeldsberg has (co-)authored a large number of conference and journal papers, and has been coauthor of a book in his field of interest. He is frequently used as reviewer for several international journals and conferences.

Notable past projects	CUBAN project Co-optimized Ubiqutious Broadband Access Networks with focus on cross-layer optimized implementation of DSP algorithms. CoDeVer/Embla Codesign, verification, and languages for embedded systems in close cooperation with industry partners
Further Information	Between 1992 and 1996 Kjeldsberg worked as a design engineer at Eidsvoll Electronics, designing communication control equipment based on embedded hw/sw solutions. Currently he is an Associate Professor at the Department of Electronics and Telecommunications, NTNU. Here he teaches several extensive undergraduate and graduate courses, and supervises a number of students at master and PhD level. Kjeldsberg is and has been a member of the board of directors both at the Faculty and in private companies.

	Alain Girault (INRIA Grenoble Rhône-Alpes)
Technical role(s) within ArtistDesign	Main areas of research: Embedded Systems ArtistDesign activities and role: formal methods for the design of embedded systems, predictable real-time systems, dependability analysis and design, fault tolerance.
Research interests	Research interests include embedded and real-time systems, formal methods, dependability, fault tolerance.
Role in leading conferences/journals/etc in the area	- Associate Editor, Eurasip Journal on Embedded Systems; - TCP co-chair of the Workshop on Model-driven High-level Programming of Embedded Systems (SLA++P'08).

4.4 Affiliated International Partners

	Prof. Krishnendu (Krish) Chakrabarty, Department of Electrical and Computer Engineering, Duke University, USA

Technical role(s) within ArtistDesign	Collaboration with DTU on microfluidics-based biochips. Contributions to the Hardware Platforms and MPSoC cluster.
Research interests	Design and test of system-on-chip integrated circuits, microfluidics-based biochips (digital microfluidics, microelectrofluidics), and wireless/sensor networks.
Role in leading conferences/journals/etc in the area	He is an Editor of the Journal of Electronic Testing: Theory and Applications (JETTA), an Associate Editor of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on VLSI Systems, IEEE Transactions on Biomedical Circuits and Systems, and ACM Journal on Emerging Technologies in Computing Systems. He serves on the editorial board of IEEE Design & Test of Computers. During 2006-2007, he served as an Associate Editor of IEEE Transactions on Circuits and Systems I, and before that as an Associate Editor of IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing.
Awards / Decorations	Prof. Chakrabarty is currently serving as an ACM Distinguished Speaker. He served as a Distinguished Visitor of the IEEE Computer Society for 2005-2007, and a Distinguished Lecturer of the IEEE Circuits and Systems Society for 2006-2007. He is also a recipient of the Humboldt Research Fellowship, awarded by the Alexander von Humboldt Foundation, Germany, in 2003.
Further Information	http://people.ee.duke.edu/~krish/

	Assist. Prof. Patrick Schaumont, Department of Electrical and Computer Engineering, Virginia Tech, USA
Technical role(s) within ArtistDesign	Collaboration with DTU on hardware description languages for MPSoC platforms. Contributions to the Hardware Platforms and MPSoC cluster.
Research interests	Design methods and architectures for secure embedded systems.
Further Information	http://www.ece.vt.edu/schaum/

5. Internal Reviewers for this Deliverable

- **Prof. Bengt Jonsson** (Upsala University)
- **Assoc. Prof. Paul Pop** (DTU)