



IST-214373 ArtistDesign
Network of Excellence
on Design for Embedded Systems

Activity Progress Report for Year 4

Software Synthesis and Code Generation

Cluster:

SW Synthesis, Code Generation and Timing Analysis

Activity Leader:

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Policy Objective (abstract)

The objective of this activity is to provide software synthesis and code generation tools which are required for modern embedded architectures. Due to the constraints of such architectures, the tools have to generate very efficient code. A particular focus is on the mapping of applications to multi-processor systems on a chip (MPSoCs). The parallelism found in such architectures poses a particular challenge. In addition, other selected tools (linking, for example, timing analysis and compilation) are also considered.

Versions

number	comment	date
1.0	First version delivered to the reviewers	Jan. 12, 2012

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1. Overview of the Activity (2008-2011)

1.1 ArtistDesign participants and their role within the Activity

Prof. Dr. Peter Marwedel – TU Dortmund, Dortmund (Germany)

Prof. Marwedel's role is to lead this activity. His team works on resource aware compilation, worst-case execution time (WCET) aware compilation and provides results on compilation for MPSoCs.

Senior researcher Chaantal Ykman-Couvreur– IMEC, Leuven (Belgium)

Novel source code parallelization and source-to-source optimizations for MPSoC platforms aiming at an exploitation of the memory hierarchy.

Prof. Dr. Christian Lengauer – U. Passau, Passau (Germany)

Prof. Lengauer's team has advanced knowledge in program analysis techniques. This knowledge was initially generated in the context of high-performance computing and shall now be used for compilation to MPSoCs.

Prof. Dr. Rainer Leupers – RWTH Aachen, Aachen (Germany)

The team led by Prof. Leupers works on compiler platforms, adaptive compilation, and MPSoC compilation. The group's MAPS project provides a reference for tools mapping algorithms to MPSoCs.

-- Changes wrt Y3 deliverable --

At IMEC, the responsible person changed.

1.2 Affiliated participants and their role within the Activity

Joseph van Vlijmen – ACE, Amsterdam (Netherlands)

ACE (including van team member van Vlijmen) is a key player in the compiler domain in Europe and the world. This partner provides a view on industrial requirements and practices.

Dr. Björn Franke – University of Edinburgh, Edinburgh (UK)

Dr. Franke's team has advanced knowledge in program analysis techniques. This knowledge was initially generated in the context of high-performance computing and shall now be used, for example, for compilation to MPSoCs.

Prof. Dr. Sabine Glesner – TU Berlin, Berlin (Germany)

The team led by Prof. Glesner provides its expertise on program verification and compiler optimization to the network. This expertise will help verifying transformations as well as developing optimizing compiler transformations of single programs and applications.

Prof. Dr. Paul Kelly – Imperial College, London (UK)

Prof. Kelly's team has advanced knowledge in program analysis techniques. This knowledge was initially generated in the context of high-performance computing and shall now be used, for example, for compilation to MPSoCs.

Prof. Dr. Alain Darté – ENS, Lyon (France)

Prof. Darté's team has advanced knowledge in program analysis techniques. This knowledge was initially generated in the context of high-performance computing and shall now be used, for example, for compilation to MPSoCs.

Dr. Marco Bekooji, Ruben van Royen – NXP, Eindhoven (Netherlands)

The team led by Dr. Bekooji has advanced knowledge in software synthesis from non-imperative models of computation. Within its area of expertise, the team has already designed tools mapping applications to multi-processors.

Dr. Bart Kienhuis – Compaan Design B.V., Leiden (Netherlands)

This partner's team has advanced knowledge in software synthesis from non-imperative models of computation. Within its area of expertise, the team has already designed tools mapping applications to multi-processors.

Prof. Dr. Ed Deprettere – Leiden Embedded Research Center, Leiden Institute of Advanced Computer Science, Leiden University (Netherlands)

This team is making its expertise on the Daedalus framework available in the network. Team members have been actively participating in the Rheinfels workshops on mapping of applications to MPSoCs and will continue to do so.

Prof. Dr. Soonhoi Ha – Seoul National University (South Korea)

The group of Soonhoi Ha has a strong history of working on the HOPES framework for mapping applications to MPSoCs. Due to being an affiliated member of the network, the expertise resulting from the design of HOPES is available in the network.

Prof. Dr.-Ing. Jürgen Teich – University of Erlangen-Nuremberg (Germany)

This partner's team has been working on the SystemCoDesigner framework for mapping applications to MPSoCs. Due to being an affiliated member of the network, the expertise resulting from the design of SystemCoDesigner is available in the network.

-- Changes wrt Y3 deliverable --

No changes with respect to Year 3.

1.3 Starting Date, and Expected Ending Date

This activity started with day 1 of the network. This activity includes the difficult problem of mapping applications to MPSoCs. We cannot expect that this problem will be completely solved at the end of the funding period. Therefore, work on this problem will be required for a number of years, even though the activity will formally be finished at the end of the funding period.

-- Changes wrt Y3 deliverable --

None.

1.4 Policy Objective

Software synthesis, code generation, and timing analysis tools provide the necessary link between embedded execution platforms and applications. The recent trend toward multi-processor systems has amplified the need for research in this area.

In order to achieve the required critical mass without increasing the number of partners beyond a manageable number, affiliated partners are added. These affiliated partners complement the work done by the core partners.

-- Changes wrt Y3 deliverable --

Adding more affiliated and external partners has been stopped.

1.5 Background

Software synthesis and code generation tools are indispensable for developing embedded systems. They are frequently assumed to be available. New architectural features are introduced all the time, assuming that “somebody” will provide the expected tools. However, the design of such tools poses many very difficult challenges. There is always the risk of major losses of investments if the expected tools cannot be designed in the available time.

Existing compilers represent very valuable software components which cannot be easily replaced by new methods. Many companies hesitate to replace their existing proven compilers by less well-debugged research results. Therefore, this cluster is extensively considering software synthesis and pre-pass source-to-source optimization tools, which can be used with several standard compilers. Pre-pass optimizers decouple the process of code generation and that of particular optimizations for certain architectural features.

The following is an enumeration of the background in the various areas of this activity:

1. Parallelism as available in MPSoCs is a particularly challenging new architectural feature. Significant effort on automatic parallelization has been spent in the context of high performance computing. Due to this effort, automatic parallelization has become feasible provided certain assumptions about the applications are met. The same results are not yet available for embedded systems. For embedded systems, the situation is different in various respects. MPSoCs, for example, are characterized by communication speeds which are comparable to the speeds of larger on-chip memories. As a result, communication based on the message-passing interface (MPI) is completely ill-designed, since it uses memory buffers extensively. Due to its limitations, special variants of MPI exist. Also, embedded system applications are different from general purpose or high performance computing. They are typically more “well-behaved” in that features like recursion, dynamic loop bounds, dynamic memory allocation, pointers, dynamic class loading etc. are much less frequent, simplifying the analysis. However, heterogeneity of processing elements, real-time constraints, streaming data, limited communication resources and multiple objectives (like energy consumption, thermal behavior, reliability) impose additional restrictions.
2. Most embedded systems are integrated into a physical environment. In such an environment, time is frequently the most critical resource. It has been found that the lack of timing in the core abstraction of computer science is a serious flaw (see, for example, Edward A. Lee, <http://ptolemy.eecs.berkeley.edu/publications/papers/05/APOT/APOT.pdf>). Reconciling code generation and timing models should therefore receive more attention.
3. Efficiency of embedded systems is a main concern. Therefore, optimized architectures are required and resource allocation has to be handled with care. There are many proposals for optimizing architectures. For example, customized instruction sets, exploitation of attached FPGAs and multimedia instructions have been suggested. Most of these features require special consideration in compilers and code generation. Resource allocation includes the allocation of execution time, energy, memory space, bandwidth etc. Traditionally, these resources have been allocated independently.

Integrated resource allocation is still not generally available. Memory allocation can be considered as a special case of resource allocation. Access times and energy consumption increase with the size of the memory. There is a growing gap between the speed of processors and the speeds of memories, even for larger on-chip memories of MPSoCs. Memory hierarchies are introduced to ease the problems resulting from this gap. Memory hierarchies are extremely important. Currently available memory hierarchies are typically designed to provide a good average-case performance. However, methods for increasing the average-case performance often deteriorate the worst-case performance and the timing predictability. Hence, timing predictability is becoming a key bottleneck for high-performance embedded systems and the memory system is a key source of unpredictability. Furthermore, memory hierarchies have not been designed for an efficient use of the available energy. In general, the link between memory architectures and compilation techniques is rather weak.

4. Software generation has evolved to a level where compilers are key components, but not the only components that are useful for generating executable code. New models of computations such as data-flow based models aim at avoiding the well-known disadvantages of imperative programming styles. Software synthesizers generate imperative code from abstract specifications such as Matlab, or Kahn process networks. It can also be expected that the link between software engineering and embedded systems will become stronger. Hence, trends like the use of UML-based system models do have to be respected as well. For the above models, code is synthesized from specifications in non-imperative languages.
5. Many applications in the embedded systems domain are not only resource-restricted but also safety-critical. This in turn requires compilers for embedded processors to be both efficient and correct. One crucial phase in the compiler is the code generation. Due to its complexity, further increased by reason of parallel processing which needs substantial support, it is highly error prone. Hence, verification of code generation is necessary to ensure that transformations preserve the semantics during compilation.
6. Work on this activity is also linked to the ArtistDesign transversal clusters.

-- Changes wrt Y3 deliverable --

None, except stressing the importance of considering multiple objectives.

1.6 Technical Description: Joint Research

In order to make the results available to as many designers as possible, tools will be based on pre-pass source-to-source optimization tools whenever feasible. This way, the mapping of applications to MPSoCs can be added to many existing, proven tool flows. Investments into compilers can be protected, the development effort can be reduced and the focus on new optimization techniques can be increased. The key advantage of pre-pass optimizers is their applicability in a large number of tool chains. Such tool chains do not require new compilers to be written. They may be using a compiler from a family of compilers (such as gcc) or specially designed compilers. Pre-pass optimizers can easily support a family of compilers without any modification and different compilers with only few modifications. Pre-pass optimizers do already exist for memory-architecture aware compilation and program parallelization. IMEC and partners at the Universities of Dortmund, Passau, and Edinburgh have significant experience with the design of pre-pass optimizers. They reflect the fact that the resources of a network of excellence are limited.

The following joint work with a focus on integration has been performed in this activity:

1. *Compilation techniques for MPSoCs* could not be developed from scratch since the problems to be solved are very challenging. The current project could certainly not provide enough resources to develop completely new techniques. Fortunately, we could build upon compilation techniques for high-performance computing. Using the limited resources, we established a link between the high-performance computing and the embedded system domain. Integration activities comprised an analysis of the applicability of techniques designed in one domain to the other domain. For this purpose, it was very essential that the proposed project included enough expertise in different areas of applications. Knowledge about hardware architectures would not be sufficient to really check the applicability of the techniques. The University of Passau is a link to the high-performance community. Cooperation with core partners and selected affiliates was used to check which of the existing techniques could be employed in embedded systems and which extensions were needed. 48 months after the start of the project, many techniques for mapping applications to MPSoCs have become available. The whole area has become a standard area, finding the interest of a large community. Most of the approaches proposed until today have been presented at our Rheinfels workshop. The ArtistDesign network has been considered essential when this area was established. P. Marwedel was asked to chair a session on this area at the Design Automation Conference (DAC) in 2011. Also, a special session on the topic was held at ESWEEK 2011. This process is expected to continue: Invitations for the next joint SCOPES/MAP2MPSoC event at Rheinfels in May 2012 have already been mailed.
2. Reconciliation of compilers and timing analysis bridges the two activities of this cluster. The work in this area builds on top of the integration work performed in the Artist2 network of excellence. The existing integration of timing analysis and compilers has been used to explore the potential of this approach further. The impact of optimizing for WCET has been studied further. The influence of context switches has been analyzed. Techniques for reducing the number of calls of timing analyzers have been explored. A detailed list of papers is included in sections 2.2. and 2.4.
3. The efficiency of designs has been dealt with in ArtistDesign. It can be achieved with many different means. Research on new optimizations has been performed. Memory architectures have been considered in-depth, due to their potential for contributing toward an overall efficiency. Memory architectures are very important for the mapping to networked processors. Indeed, the mapping of applications to processing elements may be significantly affected by the connectivity of the memories. Hence, optimized mappings to memories have been considered as well. Such techniques provide optimization techniques taking several objectives into account.
4. Work on software synthesis was added to the scope of our cluster. The activity includes affiliate partners specializing on software synthesis and cooperating experts from other clusters. The third workshop in this area (WSS), held during ESWEEK 2011, had top-level presenters.
5. In addition to topics 1 to 4, members of this activity also extended the areas for which the correctness of compilers has been shown via formal verification, focusing on the crucial code generation phase during compilation. The work in this area built on top of the work performed in the Artist2 network of excellence.
6. The members of this activity contributed to the thematic activities of the Transversal Integration work package, focusing on predictability and adaptivity issues. This area has not been tackled in the Artist2 network.

-- Changes wrt Y3 deliverable --

The text has been updated from the Y3 deliverables. Software synthesis has been given even more attention, as requested by the reviewers. The presenters at the WSS workshop in Taipei were really top-level presenters. No other changes.

2. Work Achieved in the NoE

2.1 *Synthesis View of the Main Overall Achievements*

During the planning of the network, members of this cluster realized the large and growing importance of exploiting future multi-processor platforms efficiently. They also noticed that future platforms for embedded systems will most likely be heterogeneous and the fact that this is likely to be a key distinction between general purpose and embedded computing. The partners were also aware of the complexity of future tools for exploiting these parallel platforms. A new workshop series was started in order to provide a forum for discussions on the topic.

This workshop series was well accepted. It was possible to attract almost all the relevant groups working on this area to attend the workshop and to give a presentation there. In particular, we would like to mention presentations by members of RWTH Aachen (on the MAPS tools), by members of the Universities of Leiden and Amsterdam (on the Daedalus tools), by members of ETH Zürich (on DOL tools), by Soonhoi Ha (on HOPES), by Qiang Xu from the City University of Hong Kong, by Jürgen Teich and Christian Haubelt from the University of Erlangen-Nuremberg, by ArtistDesign members from the Universities of Bologna and the Technical University of Denmark, by T. Simunic from UC San Diego, and by members of the Mnemee European project, involving teams from Dortmund, Eindhoven, Leuven, Paris, and Athens. The workshop involved members from other clusters as well as affiliates and researchers not formally related to the network. During the lifetime of the network, an increasing number of objectives became relevant. In addition to the usual performance metrics, temperature and reliability became important. Several models of computation were considered as starting points, including the sequential von-Neumann model as well as Kahn process networks (KPNs). No single approach is currently providing the union of all the features.

RWTH Aachen has worked on the front of mapping applications onto MPSoCs continuously during the ArtistDesign period and the main result, MAPS tool-suite, has grown from individual point tools to a comprehensive tool-framework that enables programming of real-life complex MPSoC platforms. Individual milestones have been presented at the annual MAP2MPSoC workshop as well as other academic conferences. This work has also resulted in collaboration with other ArtistDesign partners such as ACE and Compaan. Dissemination of the research work into the industry has been made via a number of special sessions and exhibition booths at leading conferences like DAC and DATE. In September 2011, the first MAPS User Group Workshop has been held in Aachen to present this new technology to a wider industrial audience, receive feedback for future enhancements, and make MAPS accessible to early adopters in industry.

Dortmund and IMEC cooperated in the Mnemee project (<http://www.mnemee.org>), supported through the 7th framework program. As a result, the comprehensive Mnemee tool chain has been designed. The Mnemee tool chain starts with the detection of possible parallelism involves the implementation of parallelism using IMEC's MH tools and also includes the mapping to processors (using either tools designed at TU Dortmund or TU Eindhoven). A mapping to scratchpad memories complements these tools. Also, the Mnemee tool suite includes the optimization of dynamic data structures by tools designed at the University of Athens. For these tools, the two industrial partners, observed a reduction of the design time by 76% respectively 38%.

While the mapping to MPSoCs posed a major challenge to the project partners, even more compilation issues popped up. Using graphics processing units (GPUs) for non-graphics processing has allowed to drastically reduce computation times and also the energy consumption for many applications. However, the exploitation of GPUs is very time-consuming

unless it is supported by appropriate tools. Fortunately, research results available at the University of Passau could be adopted for the new compilation challenge. Techniques for loop parallelization based on polyhedra provided exactly the background needed for these new, unforeseen platforms. It is therefore not surprising that the University of Passau to be one of the initiators of the new priority programme SPP 1648 supported by Deutsche Forschungsgemeinschaft (DFG) (www.dfg.de). Tools from Passau could also be used for the programming of GPUs at TU Dortmund in the context of the collaborative research center SFB 876 (see <http://www.sfb876.tu-dortmund.de>).

In addition to the work on the mapping to MPSoCs, members of the network also worked on the efficiency of embedded systems. During the years of the network, the importance of energy efficiency has increased. Green computing is now a term used very much in public discussions. Concerning the power consumed in processors and memories, scratch pads are now seen as one of the key options for energy reduction. A paper published at the CODES/ISSS workshop by TU Dortmund and IIT Delhi in 2002 has become one of the key references in that area.

Software synthesis from model-based specifications has also been addressed by the partners in the cluster. During the lifetime of the project, increasingly prominent researchers could be attracted to the workshop on software synthesis, held on the last day of ESWEEK. It turned out that such a workshop is needed in order to bring specialists from a scattered community into contact. So far, there has been little cooperation between specialists from control theory, signal processing, instrumentation, and language and compilation specialists (e.g. for synchronous languages). Also, in this area, it is extremely important to improve contacts between industry and academia. As a result, attendees of the workshop in Taipei expressed their strong interest in follow-up workshops. The first follow-up workshop is scheduled for Tampere for October 2012.

-- The above is new material, not present in the Y3 deliverable --

2.2 Work achieved in Year 1 (Jan-Dec 2008)

The following work was performed for the different areas of the activity:

1. It was important to set up the required interaction of the partners regarding compilation for MPSoCs. The partners started with an intensive workshop in June, 2008. The workshop was held from June 16 to June 17, 2008 at Rheinfels Castle, St. Goar, Germany. Due to the complexity of the problem and the limited manpower of the network, we invited a number of European groups known to be working in relevant areas to the workshop, including members of the HIPEAC network of excellence and the ACOSTES project. This way, we tried to reach out far beyond the limited set of ArtistDesign partners, using these partners as the seed for a larger network of cooperating partners. A more detailed report is available in the Y1 deliverables as well as on the workshop web pages (see <http://www.artist-embedded.org/artist/Mapping-of-Applications-to-MPSoCs.html>). A summary from the workshop was presented at the CASA workshop held as part of the Embedded Systems Week in Atlanta on Oct. 19th, 2008.

In addition, several smaller meetings took place. This work was performed in cooperation with the execution platforms cluster and involved teams outside the ArtistDesign network.

2. Regarding the reconciliation of compilers and timing analysis, significant work was performed as well. The key questions to be solved were: how much would a compiler benefit from a tight integration with timing analysis? How much different are the code

generation results for an optimization of the average case and of the worst case? Will the average run time increase if we optimize for the worst case?

3. Regarding the work on design efficiency, the problem tackled concerned the integration of various tools from various partners (not just limited to this activity).
4. For software synthesis, the question was how to find a link to the work on mapping of applications to MPSoCs.
5. Concerning the support for verification of code generation, TU Berlin has continued its work on formalizing important parts of the semantics of the intermediate representation, of assembler and machine code and examples of transformation rules that describe the compilation between intermediate forms. In particular, we investigated the different kinds of number representations and the rules describing their compilation. Using the Isabelle/HOL theorem prover, we formalized various kinds of integer data types in assemblers. In one of the code generation rules of a compiler developed at TU Berlin (using the CoSy tool from ACE, Amsterdam), we found a mistake arising from a copy&paste bug when deriving one rule from a very similar, already existing rule.
Besides the research on compiler verification, TU Berlin was also involved in research on compiler optimization. The work on compiler optimizations for parallel architectures has been continued. A demonstrator has been completed together with research on VLIW optimizations based on machine learning. Furthermore, current work deals with optimizations for MPSoCs.
6. For transversal integration, getting requirements from industry was a key goal

Resources of the network were used to support the cooperation. Research work was paid through other resources.

-- No changes wrt Y3 deliverable --

This section was already presented in the Y3 deliverable, in section 1.7.

2.3 Work achieved in Year 2 (Jan-Dec 2009)

1. Work on the mapping of applications to MPSoCs has been continued. First of all, the second workshop on mapping of applications to MPSoCs was held at Rheinfels Castle in June 2009. We managed to reach out far beyond the ArtistDesign partners by inviting prominent European, Asian and American researchers in the field. The road toward new integrated tools has been followed. The work on MAPS at Aachen continued in cooperation with other partners. TU Dortmund and ETH Zürich worked on an extension of the mapping and optimization framework DOL which was developed at Zürich. As a result DOL was extended by the integration of memory hierarchies in the mapping decision and design space exploration of the tool. Work on the integration of energy optimization is still ongoing.
2. Regarding the reconciliation of compilers and timing analysis: The impact of WCET minimization has been analyzed for additional optimizations, including optimizations for registers and scratch pad memories.

Machine learning has shown its capabilities for an automatic generation of heuristics used by compiler optimizations. In Y2, supervised learning approaches are studied for the first time in the context of an automatic minimization of the WCET. Using a reconciling of a WCET-aware compiler and a machine learning tool, heuristics for a WCET-aware function inlining and loop invariant code motion have been developed. The model selection problem,

i.e., selecting learning algorithms and their respective parameters, has been tackled by an evolutionary algorithm that automatically finds good solutions within the large search space.

3. Regarding the work on design efficiency; The MPARM simulator has been used by a number of partners. In addition, TU Dortmund has ported IMEC's RTLlib, thus allowing us to use MPARM together with IMEC's MPA tools.

MPA parallelization assistant tool and MH static memory assignment tool by IMEC have been integrated more tightly. The main problems tackled were in respect with cleaning sequential source code in order to parallelize it more efficiently, parallelization exploration, FIFOs sizing and FIFOs access management.

The MH static memory assignment tools by IMEC have been integrated tighter with the DMM dynamic memory assignment tools by NTUA. The main problem tackled was in respect with data interdependencies and sharing physical memory resources.

4. Going beyond the plan, software synthesis was not integrated into the second Rheinfels workshop. Rather, we organized a separate workshop on this issue during the Embedded Systems Week at Grenoble. This approach required a bit more work, but turned out to be more useful, since we could maintain a clear focus for both workshops.
5. Concerning the support for verification of code generation, TU Berlin continued its cooperation and its work on formalizing important parts of the semantics of the intermediate representation.
6. Members of the cluster also contributed to work on predictability and industrial applications.

Also, the educational workshop WESE was organized by the leader of this activity. The workshop attracted top researchers. For example, the keynote was given by Edward A. Lee (UC Berkeley). In order to improve the visibility of the results, WESE papers are now included in the ACM digital library.

Another problem perpendicular to the cluster structure was tackled by the leader of the cluster: in order to extend the accessibility of results, the activity leader became editor for a special series of books on embedded systems published by Springer (see <http://www.springer.com/series/8563>).

Several months of work was spent on improving available educational material: the bulk of the work on the next (extended) edition of the textbook "Embedded System Design" by P. Marwedel was completed. It is being tested in a course held during the winter of 2009/2010. The second edition is scheduled to be published during the first quarter of 2010.

Technical achievements include the following

1. A high-level virtual platform for early MPSoC software development (RWTH Aachen, ACE)
<http://www.iss.rwth-aachen.de>
2. Integration RTLlib and MPARM (TU Dortmund, IMEC)
<http://ls12-www.cs.tu-dortmund.de/staff/heinig/research/projects/r2g/>
3. CleanC, MPA parallelization assistant and MH static memory allocation for MPSoC (IMEC vzw)
<http://www.imec.be/cleanc>
4. Scheduling and data management using system scenarios (IMEC vzw, NTUA, TU/e)
5. Mapping of applications to HW/SW-platforms comprising FPGAs (University of Passau)
6. Making the LooPo loop optimizer available in the embedded world (University of Passau, TU Dortmund)
<https://www.infosun.fim.uni-passau.de/trac/LooPo/>

7. Extending the polyhedron model for automatic loop parallelization to include non-linearities (University of Passau)

Details on the achievements can be found in the Y2 deliverable.-- No changes wrt Y3 deliverable --

This section was already presented in the Y3 deliverable, in section 1.8.

2.4 Work achieved in Year 3 (Jan-Dec 2010)

1. In order to improve the cooperation on solving the problem of mapping applications to MPSoCs, we continued to run the Rheinfels series of workshops. The third workshop was held on June 28-29, 2010 (see <http://www.artist-embedded.org/artist-map2mpsoc-2011-.html>). The SCOPES workshop was held back-to-back at Rheinfels Castle. It was held on June 27-28, 2010 (see <http://www.artist-embedded.org/artist-SCOPES-2010-.html>). Also, work on actual mapping tools was continued. The MAPS tool was extended in cooperation with other partners. Cooperation between ETH Zürich and TU Dortmund was continued.
2. Work on code optimizations taking the WCET into account was extended toward multi-objective optimization, multi-cores and links with operating systems. More information on this work linking the two activities of this cluster can be found in the deliverable on timing analysis.
3. We continued to contribute to the state of the art in Embedded Systems Education. The 2nd edition of the text book "Embedded System Design" by P. Marwedel was published. The book is one of the components of a comprehensive solution for an initial embedded systems course, since slides, simulation software and (new by the end of 2010) recorded lectures are also provided on the web (see <http://ls12-www.cs.tu-dortmund.de/en/staff/marwedel/es-book/slides10/> for the most recent information). Translations into various languages are either available or being scheduled. Furthermore, P. Marwedel continued to work on the publication of a series of books on Embedded Systems to be published by Springer (see <http://www.springer.com/series/8563>). Also, the network was involved in the organization of the WESE workshop in 2010.
4. We organized the second workshop on software synthesis during the Embedded Systems Week (<http://www.artist-embedded.org/artist/Scope,2121.html>). Top-level experts (e.g. from UC Berkeley) presented at the workshop. Also, we organized a call for a special edition of the journal *IEEE Transactions on Industrial Informatics*. This topic does now receive increased attention.

This section is a subset of what was already presented in the Y3 deliverable, in sections 1.9.

2.5 Work achieved in Year 4 (Jan-Dec 2011)

1. In order to keep the cooperation on solving the problem of mapping applications to MPSoCs on a high level, we continued running the Rheinfels series of workshops. The fourth workshop took place on June 28-29, 2011 (see <http://www.artist-embedded.org/artist/-map2mpsoc-2011-.html>). The SCOPES workshop was held at Rheinfels Castle on June 27-28, 2011 (see <http://www.artist-embedded.org/artist/-SCOPES-2011-.html>). Also, work on actual mapping tools continued. The MAPS tool

was extended in cooperation with other partners. Cooperation between ETH Zürich and TU Dortmund continued.

2. Work on code optimizations taking the WCET into account was extended toward multi-objective optimization, multi-cores and links with operating systems.
3. Work on memory-architecture-aware compilation tools was continued. The focus was on pre-pass compilation tools and on the support of multi-processor systems. Reliability was added as an additional objective.
4. We continued to contribute to the state of the art in Embedded Systems Education. The translation of the second edition of the text book "Embedded System Design" into German was completed. The translation into Greek and Portuguese, initially scheduled for 2011, will be delayed. P. Marwedel also continued to work on the publication of a series of books on Embedded Systems to be published by Springer (see <http://www.springer.com/series/8563>). Also, the network organized the WESE workshop in Taipei.
5. As suggested by the reviewers, software synthesis was given more attention.

We organized the third workshop on software synthesis during the Embedded Systems Week in Taipei. Top-level experts presented at the workshop. These experts were from different areas. S. Bhattacharyya presented results of his work on synthesis from dataflow graphs. K. Ravindran (National Instruments) talked about the path from streaming models to software and hardware implementations. M. di Natale (SSSA, Pisa) described the deployment of real-time functions in automotive systems. R. Alur (University of Pennsylvania) demonstrated results in the area of software synthesis for control applications. These included relations between sampling rates and control precision. N. Halbwachs (IMAG) gave an overview over code generation for synchronous languages. There was a universal consensus among the experts that this workshop was extremely useful for them. Many actually met for the first time. Experts expressed their strong interest in continuing this workshop in 2012. Also, Ted Baker (National Science Foundation, NSF) expressed the interest of his organization. We are planning to run the workshop also as part of ESWEEK 2012 in Tampere on Oct. 12th.

Regarding the planned special issue of the IEEE Journal on Industrial Informatics, the situation is as follows: An open call for contributions in the area of software synthesis and the mapping of applications to MPSoCs had been published. A total of nine papers were submitted to the editor-in-chief by October 2010. One of these was rejected for formal reasons. The remaining papers represented both areas of the call. Only three papers were finally accepted as a result of the comprehensive review process. All three papers involve ArtistDesign members or affiliates. With just three papers remaining, it became impossible to publish a special issue of the journal. Only the paper by Soonhoi Ha et al. (Seoul National University) is a paper on software synthesis. It deals with the use of libraries in actor-based programming. One paper by Leupers et al. (RWTH Aachen) is about the mapping to multi-processors using the MAPS tool presented at the MAP2MPSoC workshops. The third paper by J. Madsen et al. (TU Denmark) proposes annotations for reducing the amount of false dependencies between tasks in task graphs. Obviously, the other papers did not yet meet the standards for a journal publication.

As a result of the above activities, we may come to the conclusion that software synthesis still requires support from the community in order to become an area whose maturity level is comparable to that of well-established areas.

6. Work on compiler verification was continued.
7. The partners also contributed to other activities, such as the transversal activities

-- The above text has been updated from the original text of Y3. The text on software synthesis is new. --

3. Detailed view of the progress in Year 4 *(Jan-Dec 2011)*

3.1 Technical Achievements

MPSoC Mapping Exploration by using Calibrated Models (RWTH Aachen)

RWTH Aachen has worked on using calibrated MPSoC models for the SW mapping exploration in the context of MAPS project. Efficient software mapping exploration of streaming applications, representing typical embedded applications targeted at MPSoC hardware, is becoming more and more important to cope with the increasing demand of multiple applications running simultaneously. As state of the art simulators usually have the accuracy versus speed trade off, a tool flow to automatically generate and calibrate abstract MPSoC models of streaming applications has been proposed. The methodology and tool flow have been applied to a real life dual ARM/DSP SoC, TI's heterogeneous OMAP3530 and the results are promising. This work has been presented initially in the MAP2MPSOC workshop (June 2011) as an extended abstract and the full paper appeared in the SoC conference (Nov. 2011).

<http://www.ice.rwth-aachen.de/research/tools-projects/entry/detail/maps-mpsoc-application-programming-studio-sss/>

Dependable Embedded Real-Time Systems (TU Dortmund)

TU Dortmund is working on dependability issues which will occur in future embedded systems. Due to smaller structure sizes as well as reduced operating voltages, future embedded systems will be exposed to non-negligible rates of transient errors in memory as well as in logic components. The FEHLER research project intends to find flexible, software-based methods to handle errors in real-time critical systems. Two initial publications analyze the vulnerability of a real-time critical multimedia application to transient memory errors. Using a novel classification approach, error handling can take place while adhering to real-time constraints. The FEHLER project is funded for two years in the context of the German Research Foundation (DFG) priority programme SPP1500 (see <http://spp1500.itec.kit.edu>).

Optimizing Execution Runtimes of R Programs (TU Dortmund)

The GNU R language is very popular in the domain of statistics. Its functional character supports the rapid development of biostatistical analyses and algorithms. Due to a time consuming evaluation and processing by a runtime interpreter, such R programs require immense computing power and waste a lot of performance compared to imperative languages.

In this activity, TU Dortmund planned the design of a sophisticated compiler tool chain for GNU R which automatically should translate R programs automatically to efficient code. In case studies, Java- and C-based approaches were compared. An evaluation showed that the resulting machine code could outperform the GNU R interpreter by a factor of up to 90. A decision was taken to cooperate with the Oracle research centre at Potsdam on the design of fast compilation of R using Graal. This activity is supported by the Collaborative Research Centre SFB 876 (see <http://www.sfb876.tu-dortmund.de>).

MH – an integration of MPA parallelization assistant and MH static memory allocation for MPSoC (IMEC vzw, Nat. Techn. Univ. of Athens, TU Dortmund)

MH is in regular use now. It is used as a parallelization backend, for example at TU Dortmund.

Accelerator Programming (Passau, TU Dortmund, Erlangen)

Dortmund and Passau are cooperating on the optimizations of loop codes for embedded many core systems, especially for GPUs. In Dortmund, low-cost and low-power GPUs are used for real-time processing of images obtained from optical biosensors. So far, GPU codes have been written by hand and require manual fine-tuning for high performance. The loop parallelizer LooPo (developed in Passau) is being extended to generate optimized image

processing code for GPUs from given sequential code. At TU Dortmund, accelerator programming continued in 2011.

Christian Lengauer was external examiner of the dissertation by Hritam Dutta, advised by Jürgen Teich in Erlangen and entitled “Synthesis and Exploration of Loop Accelerators for Systems-on-a-Chip”. Hritam Dutta applies polyhedral methods in the hardware-software codesign of domain-specific accelerators. The thesis was defended on March 3, 2011.

In two mutual visits between members of the groups in Erlangen and Passau, collaboration based on the LooPo extension Polly was initiated. In Polly, polyhedral methods can be applied at the level of intermediate code (precisely: LLVM-IR), liberating the polyhedron model from a dependence on a specific source programming language: see the master thesis of Tobias Grosser (Passau). A master thesis connecting Polly with the DSL compiler written by Richard Membarth (Erlangen) is under way. The thesis will use Polly to extract image processing (and codes with similar structure) from program code in general-purpose languages, detect parallelism using LooPo, and use the DSL compiler to generate optimized parallel code for GPUs (OpenCL or CUDA). Extensions necessary to connect the hardware synthesis tools developed in Erlangen to Polly have been discussed and are in the process of being implemented.

German DFG Priority Programme on Software for Exascale Computing (SPP 1648)

Christian Lengauer is co-initiator of a new DFG-funded German research initiative on software for exascale computing and is on its steering committee responsible for programming methods. The programme is to begin in January 2013 and run for six years with a yearly funding level of 4 million Euros. A call for projects has been issued in November 2011. Part of the call is the topic of hardware-software codesign.

<http://www.sppexa.de>

Type-safe MapReduce (Passau)

In the summer of 2011, Passau started a two-year DFG project (renewable) on making imperative MapReduce implementations type-safe and easier to use. A first publication appeared around that time (see citation list).

<http://www.infosun.fim.uni-passau.de/cl/MapReduceFoundation/>

Encyclopedia of Parallel Computing (Passau)

David Padua and Springer-Verlag have been putting together an encyclopedia of parallel computing. Christian Lengauer has been co-editor and contributor of four entries on modeling and verification (see the citation list).

<http://www.springer.com/computer/swe/book/978-0-387-09765-7>

Static Analysis of Run-time Modes in Process Networks (TU Berlin)

For modeling modern streaming-oriented applications, Process Networks (PNs) are used to describe systems with changing behavior, which must be mapped on a concurrent architecture to meet the performance and energy constraints of embedded devices. Finding an optimal mapping of Process Networks to the constrained architecture presumes that the behavior of the Process Network is statically known. In this activity, TU Berlin has worked on a static analysis for synchronous PNs that extracts different run-time modes by using polyhedral abstraction. The result is a Mealy machine whose states describe different run-time modes and the edges among them represent transitions. This machine can be used to guide optimizing backend mappings from PNs to concurrent architectures.

-- The above is new material, not present in the Y3 deliverable --

3.2 Individual Publications Resulting from these Achievements

RWTH Aachen

Castrillon, J., Shah, A., Murillo, L., Leupers, R., and Ascheid, G. Backend for Virtual Platforms with Hardware Scheduler in the MAPS Framework. *In Proceedings of the 2nd IEEE Latin American Symposium on Circuits and Systems LASCAS'11*. Feb. 2011

Castrillon, J., Sheng, W., and Leupers, R. Trends in Embedded Software Synthesis. *In International Conference On Embedded Computer Systems: Architecture, Modeling, and Simulation (SAMOS'11) (Carro, L. and Pimentel, A. D., eds.) pp. 347–354*. July 2011

Weiss, M., Castrillon, J., and Leupers, R. Novel Architecture and Programming Support for High-speed, Low Power, and Flexible Next Generation Communication ICs. *In Proceedings of the Semiconductor Conference Dresden 2011 (SCD'11) pp. 1–4*. Sept. 2011

Castrillon, J., Schürmans, S., Stulova, A., Sheng, W., Kempf, T., Leupers, R., Ascheid, G., and Meyr, H. Component-Based Waveform Development: The Nucleus Tool Flow for Efficient and Portable Software Defined Radio. *In Analog Integrated Circuits and Signal Processing, vol. 69, no. 2, pp. 173–190*. Oct. 2011.

Sheng, W., Schürmans, S., Odendahl, M., Leupers, R., and Ascheid, G. Automatic Calibration of Streaming Applications for Software Mapping Exploration. *In Proceedings of the International Symposium on System-on-Chip (SoC)*. November 2011.

Castrillon, J., Leupers, R., and Ascheid, G. MAPS: Mapping Concurrent Dataflow Applications to Heterogeneous MPSoCs. *In IEEE Transactions on Industrial Informatics*. Nov. 2011.

Sheng, W., Castrillon, J., Stulova, A., Odendahl, M., Leupers, R., and Ascheid, G. Programming Heterogeneous MPSoCs using MAPS. *First International Software Technology Exchange Workshop 2011*. Nov. 2011.

TU Dortmund

Constantin Timm, Frank Weichert, Peter Marwedel and Heinrich Müller. Multi-Objective Local Instruction Scheduling for GPGPU Applications. *In Proceedings of the International Conference on Parallel and Distributed Computing Systems (PDCS) 2011, Dallas, USA, December 2011*.

Constantin Timm, Frank Weichert, Peter Marwedel and Heinrich Müller. Design Space Exploration Towards a Realtime and Energy-Aware GPGPU-based Analysis of Biosensor Data. *Computer Science - Research and Development, Special Issue International Conference on Energy-Aware High Performance Computing (ENA-HPC), September 2011*

Constantin Timm, Pascal Libuschewski, Dominic Siedhoff, Frank Weichert, Heinrich Müller and Peter Marwedel. Improving Nanoobject Detection in Optical Biosensor Data. *In Proceedings of the 5th International Symposium on Bio- and Medical Informatics and Cybernetics, BMIC 2011, July 2011*.

Frank Weichert, Constantin Timm, Marcel Gaspar, Alexander Zybin, Evgeny L. Gurevich, Heinrich Müller and Peter Marwedel. GPGPU-basierte Echtzeitdetektion von Nanoobjekten mittels Plasmonen-unterstützter Mikroskopie. *Bildverarbeitung für die Medizin*, pages 39-43, March 2011.

Heiko Falk, Norman Schmitz and Florian Schmoll. WCET-aware Register Allocation based on Integer-Linear Programming. *In Proceedings of the 23rd Euromicro Conference on Real-Time Systems (ECRTS)*, pages 13-22, Porto / Portugal, July 2011

Heiko Falk and Helena Kotthaus. WCET-driven Cache-aware Code Positioning. *In Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, pages 145-154, Taipei, Taiwan, October 2011

Heiko Falk and Helena Kotthaus. WCET-driven Cache-aware Code Positioning. *In Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, pages 145-154, Taipei, Taiwan, October 2011

Jan C. Kleinsorge, Heiko Falk and Peter Marwedel. A Synergetic Approach To Accurate Analysis Of Cache-Related Preemption Delay. *In Proceedings of the International Conference on Embedded Software (EMSOFT)*, pages 329-338, Taipei, Taiwan, October 2011.

Jan C. Kleinsorge, Heiko Falk and Peter Marwedel. A Synergetic Approach To Accurate Analysis Of Cache-Related Preemption Delay. *In Proceedings of the International Conference on Embedded Software (EMSOFT)*, pages 329-338, Taipei, Taiwan, October 2011.

Michael Engel, Florian Schmoll, Andreas Heinig and Peter Marwedel. Unreliable yet Useful -- Reliability Annotations for Data in Cyber-Physical Systems. *In Proceedings of the 2011 Workshop on Software Language Engineering for Cyber-physical Systems (WS4C)*, Berlin / Germany, October 2011.

Michael Engel, Florian Schmoll, Andreas Heinig and Peter Marwedel. Temporal Properties of Error Handling for Multimedia Applications. *In Proceedings of the 14th ITG Conference on Electronic Media Technology*, Dortmund / Germany, February 2011.

Peter Marwedel and Michael Engel. Embedded System Design 2.0: Rationale Behind a Textbook Revision. *In Proceedings of the Workshop on Embedded Systems Education*, Taipei, Taiwan, October 2011.

Sascha Plazar, Jan C. Kleinsorge, Heiko Falk and Peter Marwedel. WCET-driven Branch Prediction aware Code Positioning. *In Proceedings of the International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, pages 165-174, Taipei, Taiwan, October 2011.

IMEC

A. G. Vanmeerberbeek, T.J. Ashby: MPA: parallelization made easy. Book chapter in: *Scalable Multi-core Architectures*, D. Soudris and A. Jantsch (Eds), Springer Science, 2012

University of Passau

Paul Feautrier and Christian Lengauer: The Polyhedron Model, *Encyclopedia for Parallel Computing*, David Padua et al. (eds.), Springer-Verlag, 2011

Christian Lengauer: Owicki-Gries Method of Axiomatic Verification of Parallel, Shared-Memory Programs, *Encyclopedia for Parallel Computing*, David Padua et al. (eds.), Springer-Verlag, 2011

Christian Lengauer. Axiomatic Verification of Monitors, *Encyclopedia for Parallel Computing*, David Padua et al. (eds.), Springer-Verlag, 2011

Martin Fränzle and Christian Lengauer. Semantic Independence, *Encyclopedia for Parallel Computing*, David Padua et al. (eds.), Springer-Verlag, 2011

Jens Dörre, Sven Apel, and Christian Lengauer. Static Type Checking of Hadoop MapReduce Programs. In *Proceedings of the International Workshop on MapReduce and its Applications (MapReduce)*, pages 17–24. ACM Press, June 2011.

Tobias Grosser, Hongbin Zheng, Ragesh Aloor, Andreas Simbürger, Armin Größlinger, and Louis-Noël Pouchet. Polly – Polyhedral Optimization in LLVM. In Christophe Alias and Cédric Bastoul, editors, *Proceedings of the First International Workshop on Polyhedral Compilation Techniques (IMPACT)*, 6pp. INRIA Grenoble Rhône-Alpes, April 2011.

Tobias Grosser. Enabling Polyhedral Optimizations in LLVM, Master Thesis, Department of Informatics and Mathematics, University of Passau, April 2011.

TU Berlin

Michael Beyer and Sabine Glesner. Static Analysis of Run-time Modes in Synchronous Process Networks. *Perspectives of Systems Informatics, 8th International Andrei Ershov Memorial Conference*. Springer Verlag, 2011.

Michael Beyer and Sabine Glesner. Static Run-time Mode Extraction by State Partitioning in Synchronous Process Networks. *SCOPES '11: Proceedings of the 14th International Workshop on Software and Compilers for Embedded Systems*. ACM, 28–37, 2011.

Dirk Tetzlaff and Sabine Glesner. Towards Predicting Recursion Depth using Machine Learning. *4th Workshop on Mapping Applications to MPSoCs 2011*.

University of Erlangen-Nuremberg

Joachim Falk, Christian Zebelein, Christian Haubelt and Jürgen Teich. A Rule-Based Static Dataflow Clustering Algorithm for Efficient Embedded Software Synthesis. *Proceedings of Design, Automation and Test in Europe (DATE'11)*, 2011.

Frank Hannig, Sascha Roloff, Gregor Snelting, Jürgen Teich and Andreas Zwinkau. Resource-Aware Programming and Simulation of MPSoC Architectures through Extension of X10. In *Proceedings of the 14th International Workshop on Software and Compilers for Embedded Systems (SCOPES)*, pp. 48-55, St. Goar, Germany, June 27-28, 2011.

Joachim Keinert and Jürgen Teich. Design of Image Processing Embedded Systems Using Multidimensional Data Flow. *Series Embedded Systems*, Springer, New York, 1st edition, 2011.

P. Marwedel, J. Teich, G. Kouveli, I. Bacivarov, L. Thiele, S. Ha, C. Lee, Q. Xu and L. Huang. Mapping of Applications to MPSoCs. *Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Taipei, Taiwan. October 9-14, 2011.

Stefan Wildermann, Felix Reimann, Daniel Ziener and Jürgen Teich. Symbolic Design Space Exploration for Multi-Mode Reconfigurable Systems. *Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Taipei, Taiwan. October 9-14, 2011. (Best Paper Candidate)

Joachim Falk, Christian Zebelein, Christian Haubelt and Jürgen Teich. A Rule-Based Quasi-Static Scheduling Approach for Static Islands in Dynamic Dataflow Graphs. *ACM Transactions on Embedded Computing Systems*. (written in 2011), to appear.

-- The above are new references, not present in the Y3 deliverable --

3.3 Interaction and Building Excellence between Partners

Main interaction between the partners was through the 4th workshop on the mapping of applications to MPSoCs on June 28-29, 2011.

TU Dortmund is cooperating with ETH Zürich on exploring the idea of extending the design space exploration from ETZ Zürich with memory-aware techniques.

The partners from Dortmund (at ICD), Leuven (at IMEC) and Eindhoven (at TU Eindhoven, member in another ArtistDesign cluster) have been jointly working on the MNEMEE project funded through the 7th framework (see <http://www.mneme.org>). TU Eindhoven is actively using the compiler development framework ICD-C (see <http://www.icd.de/es/index.html>) into some of its tools.

Dortmund and Passau have cooperated on the programming of graphics processors (GPUs).

The partners from IMEC, DUTH and KTH have been jointly working on the MOSART project funded through the 7th framework (see <http://www.mosart-project.org>).

The partners from RWTH Aachen and TU Dortmund are jointly teaching a course in retargetable compilation (including memory-architecture aware compilation) at the Advanced Learning and Research Institute (ALARI) in Lugano, Switzerland (see <http://www.alari.ch>).

The partners from Dortmund and members of other ArtistDesign activities (Bologna, Pisa, Saarbrücken, Zürich) have been jointly working on the PREDATOR project funded through the 7th framework (see <http://www.predator-project.eu>).

RWTH Aachen is also a member of the HIPEAC Network of Excellence where they lead the research cluster on Design Methodology and Tools. Within this NoE and carrying the ARTIST banner they have interacted with the top level academic and industrial partners. Now the HiPEAC is entering the HiPEAC3 phase gradually and RWTH Aachen continues to play a big role in the network.

RWTH Aachen is participating in a large scale project funded by the German government, the excellence cluster "Ultra high-speed Mobile Information and Communication" (UMIC) where they lead the sub-area "RF Subsystems and SoC Design". In the "Nucleus" project of UMIC, Aachen has been looking into the research topics on designing and mapping SDR (software-defined radio) applications onto heterogeneous MPSoC platforms. MAPS project has also been funded by the UMIC to further mature as a complete solution for embedded MPSoC programming.

RWTH Aachen and ACE are co-operating on a technique to perform source-to-source (C-to-C) transformations for code optimizations on various embedded processors. This is currently ongoing during a master thesis work.

TU Dortmund and TU Eindhoven have continued to cooperate closely, for example on the organization of the SCOPES workshop, on the PhD defense of Akash Kumar and on the preparation of a book on the results of the Mnemee project.

TU Berlin also cooperated with the University of Edinburgh by jointly advising the Master's Thesis of Volker Seeker. Volker Seeker was a master student at TU Berlin and worked for his thesis together with Björn Franke at the University of Edinburgh. Volker Seeker's master's thesis won the price in the category "Best Information Technology Student" at this year's SET (Science, Engineering and Technology) Awards in London. Since November 2011, Volker

Seeker continues his research at the University of Edinburgh with the goal to work towards a PhD.

-- Changes wrt Y3 deliverable --

The above text has been updated from the text for Y3.

3.4 Joint Publications Resulting from these Achievements

F. Engel, R. Leupers, G. Ascheid, M. Ferger, and M. Beemster. Enhanced structural analysis for C code reconstruction from IR code. *In 14th International Workshop on Software and Compilers for Embedded Systems*, pp. 21–27, ACM. June 2011

Paul Lokuciejewski, Sascha Plazar, Heiko Falk, Peter Marwedel and Lothar Thiele. Approximating Pareto optimal compiler optimization sequences - a trade-off between WCET, ACET and code size. *Software: Practice and Experience*, May 2011. DOI 10.1002/spe.1079

Jörg Henkel, Lars Bauer, Joachim Becker, Oliver Bringmann, Uwe Brinkschulte, Samarjit Chakraborty, Michael Engel, Rolf Ernst, Hermann Härtig, Lars Hedrich, Andreas Herkersdorf, Rüdiger Kapitza, Daniel Lohmann, Peter Marwedel, Marco Platzner, Wolfgang Rosenstiel, Ulf Schlichtmann, Olaf Spinczyk, Mehdi Tahoori, Jürgen Teich, Norbert Wehn and Hans-Joachim Wunderlich. Design and Architectures for Dependable Embedded Systems. *In Proceedings of Embedded Systems Week (ESWeek 2011)*, Taipei, Taiwan, October 2011

Emanuele Cannella, Lorenzo Di Gregorio, Leandro Fiorin, Menno Lindwer, Paolo Meloni, Olaf Neugebauer and Andy D. Pimentel. Towards an ESL Design Framework for Adaptive and Fault-tolerant MPSoCs: MADNESS or not? *In Proceedings of the 9th IEEE/ACM Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia'11)*, Taipei, Taiwan, October 2011.

Samarjit Chakraborty, Marco Di Natale, Heiko Falk, Martin Lukasiewicz and Frank Slomka. Timing and Schedulability Analysis for Distributed Automotive Control Applications. *In Tutorial at the International Conference on Embedded Software (EMSOFT)*, pages 349-350, Taipei, Taiwan, October 2011

Timon Kelter, Heiko Falk, Peter Marwedel, Sudipta Chattopadhyay and Abhik Roychoudhury. Bus-Aware Multicore WCET Analysis through TDMA Offset Bounds. *In Proceedings of the 23rd Euromicro Conference on Real-Time Systems (ECRTS)*, pages 3-12, Porto / Portugal, July 2011.

Timon Kelter, Heiko Falk, Peter Marwedel, Sudipta Chattopadhyay and Abhik Roychoudhury. Bus-Aware Multicore WCET Analysis through TDMA Offset Bounds. Technical Report #837, TU Dortmund, Faculty of Computer Science 12, January 2011

Daniel Cordes, Andreas Heinig, Peter Marwedel and Arindam Mallik. Automatic Extraction of Pipeline Parallelism for Embedded Software Using Linear Programming. *In Proceedings of the Seventeenth IEEE International Conference on Parallel and Distributed Systems (ICPADS 2011)*, Tainan, Taiwan, December 2011.

Peter Marwedel, Jeff Jackson, Kenneth Ricks (eds.). Proceedings of the Workshop on Embedded Systems Education (WESE), Taipei, Oct. 2011, <http://dl.acm.org/citation.cfm?id=2077370>.

Peter Marwedel, Jürgen Teich, Georgia Kouveli, Iuliana Bacivarov, Lothar Thiele, Soonhoi Ha, Chanhee Lee, Qiang Xu and Lin Huang. Mapping of Applications to MPSoCs. *In Proceedings*

of the *International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, Taipei, Taiwan, October 2011.

Oscar Almer and Igor Böhm and Tobias Edler von Koch and Björn Franke and Stephen Kyle and Volker Seeker and Christopher Thompson and Nigel Topham. Scalable Multi-Core Simulation Using Parallel Dynamic Binary Translation. *Proceedings of the International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS'11)*

A. Mallik, S. Mamagkakis, C. Baloukas, L. Papadopoulos, D. Soudris, S. Stuijk, O. Jovanovic, F. Schmoll, D. Cordes, R. Pyka, P. Marwedel, F. Capman, S. Collet, N. Mitas and D. Kritharidis: MNEMEE – An automated toolflow for parallelization and memory management in MPSoC platforms, *DAC, 2011, (presentation at the user's forum)*

-- The above are new references, not present in the Y3 deliverable --

3.5 Keynotes, Workshops, Tutorials

PEPPHER Workshop

Heraklion, Crete, January 22, 2011

C. Lengauer is member of the PEPPHER Advisory Board.

<http://www.par.univie.ac.at/project/peppher/hipeac11/>

Tutorial: Mnemee design flow: a framework for memory management and optimization of static and dynamic data in MPSoC system

ARCS 2011, Lake Como, Italy, February 22, 2011

Speakers: P. Marwedel, D. Soudris, S. Stuijk, A. Mallik, D. Cordes, S. Collet, D. Kritharidis

This tutorial addressed the Mnemee tool flow that performs source-to-source transformations to automatically optimize the original source code and map it on the target platform. The optimizations aim at reducing the number of memory accesses and the required memory storage of both dynamically and statically allocated data. Moreover the Mnemee tool flow performs optimal assignment of all data on the memory hierarchy of the target platform.

Tutorial: MPSoC hardware/software architectural and design challenges/solutions

DATE 2011, Grenoble, France, March 15th, 2011

Speakers: G. Vanmeerbeeck, K. Tiensyrja, A. Jantsch, D. Soudris, B. Candaele

Mapping software onto multi-processor platforms requires efficient parallel programming techniques while achieving non-functional requirements. The fundamentals, design steps and alternative programming models to implement such embedded applications onto multi-cores were discussed in the tutorial. The need to accommodate a large number of applications on these massively parallel computing platforms requires the system engineer to quickly evaluate the performances of application mappings. The tutorial reviewed mainstream evaluation techniques based on simulation, abstract workload and processing capacity models. On-chip and in-package memory organization and efficient data management are key to high performance. The tutorial reviewed various memory architectures and techniques to address space management, cache coherency, memory consistency, and dynamic application specific memory allocation techniques.

Software for Exascale Computing

Bonn, Germany, May 23-24, 2011

This workshop at the DFG prepared the proposal for the SPPEXA programme, which was accepted in October (see Section 2.1). C. Lengauer provided a vision of programming methods for exascale computing.

<http://www.sppexa.de>

**Keynote: Energy-Efficient Embedded Computing
Energy-Aware Computing (EACO) Workshop**

Bristol, United Kingdom – July 13-14, 2011

P. Marwedel presented an overview of his group's work on energy models for embedded software, on the life cycle analysis of computing devices and on optimizations for scratch pad memory and GPUs.

<http://www.cs.bris.ac.uk/Research/Micro/eaco-2.jsp>

Workshop: Software & Compilers for Embedded Systems (SCOPES) 2011

St. Goar, Germany – June 27-28, 2011

SCOPES focuses on the software generation process for modern embedded systems. Topics of interest include all aspects of the compilation process, starting with suitable modeling and specification techniques and programming languages for embedded systems. The emphasis of the workshop lies on code generation techniques for embedded processors. The exploitation of specialized instruction set characteristics is as important as the development of new optimizations for embedded application domains. Cost criteria for the entire code generation and optimization process include run time, timing predictability, energy dissipation, code size and others. Since today's embedded devices frequently consist of a multi-processor system-on-chip, the scope of this workshop is not limited to single-processor systems but particularly covers compilation techniques for MPSoC architectures.

In addition, this workshop puts a spotlight on the interactions between compilers and other components in the embedded system design process. This includes compiler support for e.g. architecture exploration during HW/SW codesign or interactions between operating systems and compilation techniques. Finally, techniques for compiler aided profiling, measurement, debugging and validation of embedded software were also covered by this workshop, because stability of embedded software is mandatory.

SCOPES 2011 was the 14th workshop in a series of workshops initially called "International Workshop on Code Generation for Embedded Processors". The name SCOPES has been used since the 4th workshop. The scope of the workshop remains software for embedded systems with emphasis on code generation (compilers) for embedded processors.

SCOPES 2011 was organized by Sander Stuijk and Henk Corporaal of TU Eindhoven and was held back-to-back with the MAP2MPSoCs workshop.

<http://www.scopesconf.org/scopes-11>

Workshop: 4th Workshop on Mapping Applications to MPSoCs, 2011

St. Goar, Germany – June 28-29, 2011

This is the flagship workshop of this cluster. The workshop is now a key forum for discussions in this area. Attendees expressed their strong interest to continue this series of informal workshops as a platform for discussions.

<http://www.artist-embedded.org/artist/Program,2298.html>

IFIP WG 2.11 (Program Generation)

Bordeaux France, August 3-5, 2011, Scotland, March 1-3rd, 2010

C. Lengauer presided the meeting

<http://resource-aware.org/do/view/WG211/M10Schedule>

Tutorial: Embedded System Foundations of Cyber-Physical Systems**ARTIST Summer School in China 2011***Beijing, China – August 8-12, 2011*

P. Marwedel started the summer school with a full-day tutorial on foundations of cyber-physical systems. He introduced the fundamentals of modeling, embedded system hardware, evaluations of embedded systems and the mapping of applications to platforms. Also, he gave a brief introduction to compilation for explicit memory architectures. The tutorial was based on the second edition of the presenter's text book on embedded systems. The tutorial made sure that the attendees were aware of the prerequisites of the remaining presentations of the summer school.

<http://www.artist-embedded.org/artist/Overview,2239.html>

Workshop: 1st MAPS User Group Workshop (MUG 2011)*Aachen, Germany – September 28-29, 2011*

On Sep 28/29, ICE of RWTH Aachen organized the 1st MAPS User Group Workshop (MUG 2011) in the UMIC research center. MAPS is a programming tool suite for heterogeneous multicore architectures that has been developed in the context of the UMIC cluster. It uses both sequential C and a C language extension (CPN) for describing applications in the form of process networks, and it performs optimized temporal and spatial task-to-processor mapping for embedded MPSoC platforms. MUG 2011 attracted more than 20 participants from 15 international companies. The workshop covered an introduction to the MAPS programming model, task mapping and scheduling techniques, C code partitioning and various demonstrations. Moreover, the participants had lots of opportunities for hands-on work with the MAPS tools. MUG 2011 was very well received and provided many new contacts and valuable practical feedback to the MAPS team for its future roadmap.

<http://www.ice.rwth-aachen.de/news/news-detail/browse/seite-2/angebote/1st-maps-user-group-workshop-mug-2011//185/>

Workshop: 7th Workshop on Embedded Systems Education, 2011*Taipei, Taiwan – October 13th, 2011*

Embedded system education is still a very young area and frequently restricted to teaching the details of microcontroller programming. A long-term objective of this workshop is to improve the visibility of work in the area and to stimulate the introduction of broader curricula. In 2011, P. Marwedel was again the main organizer of the workshop.

<http://www.artist-embedded.org/artist/Topics-and-Focus,2305.htm>

Workshop: 3rd Workshop on Software Synthesis, 2011*Taipei, Taiwan – October 14th, 2011*

An increasing amount of software is not written manually any more. Rather, software is synthesized from abstract models of the required functionality. Software synthesis has been implemented in various disperse communities. The workshop aimed at bringing these communities together. Presenters at this workshop presented industrial as well as academic results. The workshop was organized by P. Marwedel and A. Sangiovanni-Vincentelli and run by P. Marwedel. Please see section 2.5 (item 5) of this deliverable for a description of results.

<http://www.artist-embedded.org/artist/Scope,2309.html>

Tutorial: Energy modeling**Workshop of Collaborative Research Center SFB 876***Lüdenscheid, Germany - 20.10.2011*

This tutorial by P. Marwedel demonstrated global trends on the energy consumption of computing and compared the advantages of measurement-based and model-based predictions

of the energy consumption in computing. The potential of saving energy through an exploitation of the memory hierarchy was shown. The tutorial closed with an introduction to the life-cycle assessment (LCA) of the energy consumption of personal computers.

<http://www.sfb876.tu-dortmund.de>

-- The above is new material, not present in the Y3 deliverable --

4. Internal Reviewers for this Deliverable

- Prof. C. Lengauer (U. Passau)
- Prof. Dr. Olaf Spinczyk (TU Dortmund)