PROJECT PERIODIC REPORT

Draft version until the 31st of March 2012

Grant Agreement number: 214373

Project acronym: ARTISTDESIGN

Project title: ArtistDesign – Design for Embedded Systems

Funding Scheme: Full cost

Date of latest version of Annex I against which the assessment will be made: 14/12/2011

Periodic report: **1st** ☐ **2nd** ☐ **3rd** ☐ **4th** ☒

Period covered: **from 1st January 201 to 31st March 2012**

Name, title and organisation of the scientific representative of the project's coordinator[1]**:**

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CONTENT

1. Declaration by the scientific representative of the project coordinator

I, as scientific representative of the coordinator of this project and in line with the obligations as stated in Article II.2.3 of the Grant Agreement declare that:

- The attached periodic report represents an accurate description of the work carried out in this project for this reporting period;
- The project (tick as appropriate) [1]

  X has fully achieved its objectives and technical goals for the period;

  ☐ has achieved most of its objectives and technical goals for the period with relatively minor deviations.

  ☐ has failed to achieve critical objectives and/or is not at all on schedule.

- The public website, if applicable

  X is up to date

  ☐ is not up to date

- To my best knowledge, the financial statements which are being submitted as part of this report are in line with the actual work carried out and are consistent with the report on the resources used for the project (section 3.4) and if applicable with the certificate on financial statement.
- All beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs, have declared to have verified their legal status. Any changes have been reported under section 3.2.3 (Project Management) in accordance with Article II.3.f of the Grant Agreement.

Name of scientific representative of the Coordinator: Joseph Sifakis

Date: 05./ 03/2012

For most of the projects, the signature of this declaration could be done directly via the IT reporting tool through an adapted IT mechanism.

[1] If either of these boxes below is ticked, the report should reflect these and any remedial actions taken.

2. Publishable summary

a. Overview

ArtistDesign is a driving force for federating the European research community in Embedded Systems Design. It brings together 31 of the best research teams as core partners, 15 Industrial and SME affiliated Industrial partners, 25 affiliated Academic partners, and 5 affiliated International Collaboration partners who participate actively in the technical meetings and events.

The central objective for the ArtistDesign European Network of Excellence on Embedded Systems Design is to build on existing structures and links forged in the FP6 Artist2 NoE, to become a virtual Center of Excellence in Embedded Systems Design. This is mainly achieved through tight integration between the central players of the European research community. These teams have already established a long-term vision for embedded systems in Europe, which advances the emergence of Embedded Systems as a mature discipline.

The research effort aims to integrate topics, teams, and competencies, through an ambitious and coherent research programme of research activities which are grouped into 4 Thematic Clusters: “Modelling and Validation”, “Software Synthesis, Code Generation, and Timing Analysis”, “Operating Systems and Networks”, “Platforms and MPSoC”. “Transversal Integration” covering both industrial applications and design issues aims for integration between clusters.

The NoE has a very dynamic International Collaboration programme, interacting at top levels with the best research centers and industrial partners in the USA: (NSF, NASA, SRI, Boeing, Honeywell, Windriver, Carnegie Mellon, Vanderbilt, Berkeley, UPenn, UNC Chapel Hill, UIUC, etc) and in Asia (Tsinghua University, Chinese Academy of Sciences, Seoul National University, East China Normal University, etc).

ArtistDesign also has a very strong tradition of Summer Schools and Graduate Schools (http://www.artist-embedded.org/artist/-Schools-.html), and major workshops (http://www.artist-embedded.org/artist/-Workshops-and-Seminars,29-.html).

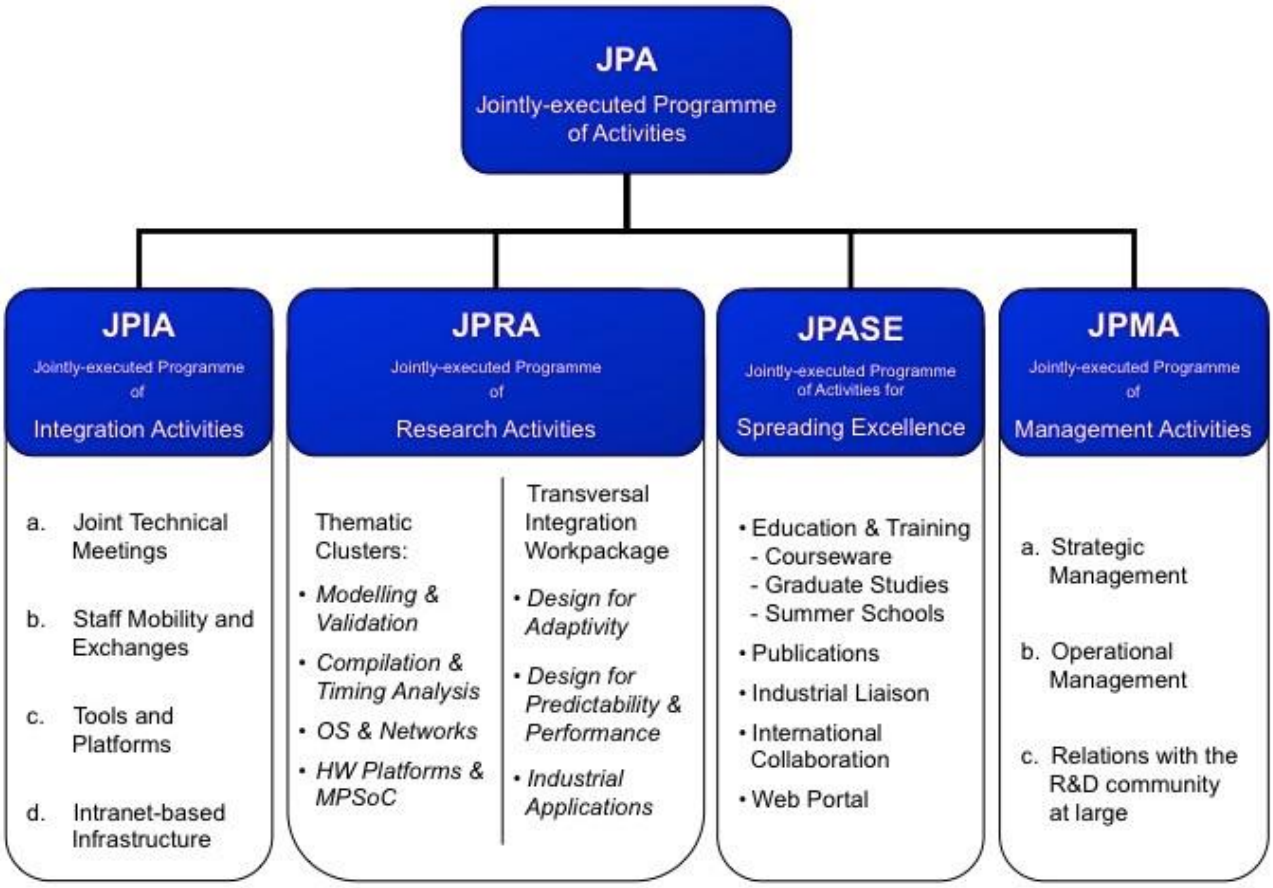
ArtistDesign builds on existing international visibility and recognition, to play a leading role in structuring the area.

The Scientific Coordinator for the ArtistDesign European Network of Excellence is Joseph Sifakis (VERIMAG Laboratory). The Technical Coordinator is Bruno Bouyssounouse (VERIMAG Laboratory).

b. Joint Programme of Research Activities (JPRA)

The ArtistDesign NoE implements a Joint Programme of Activities, composed of:

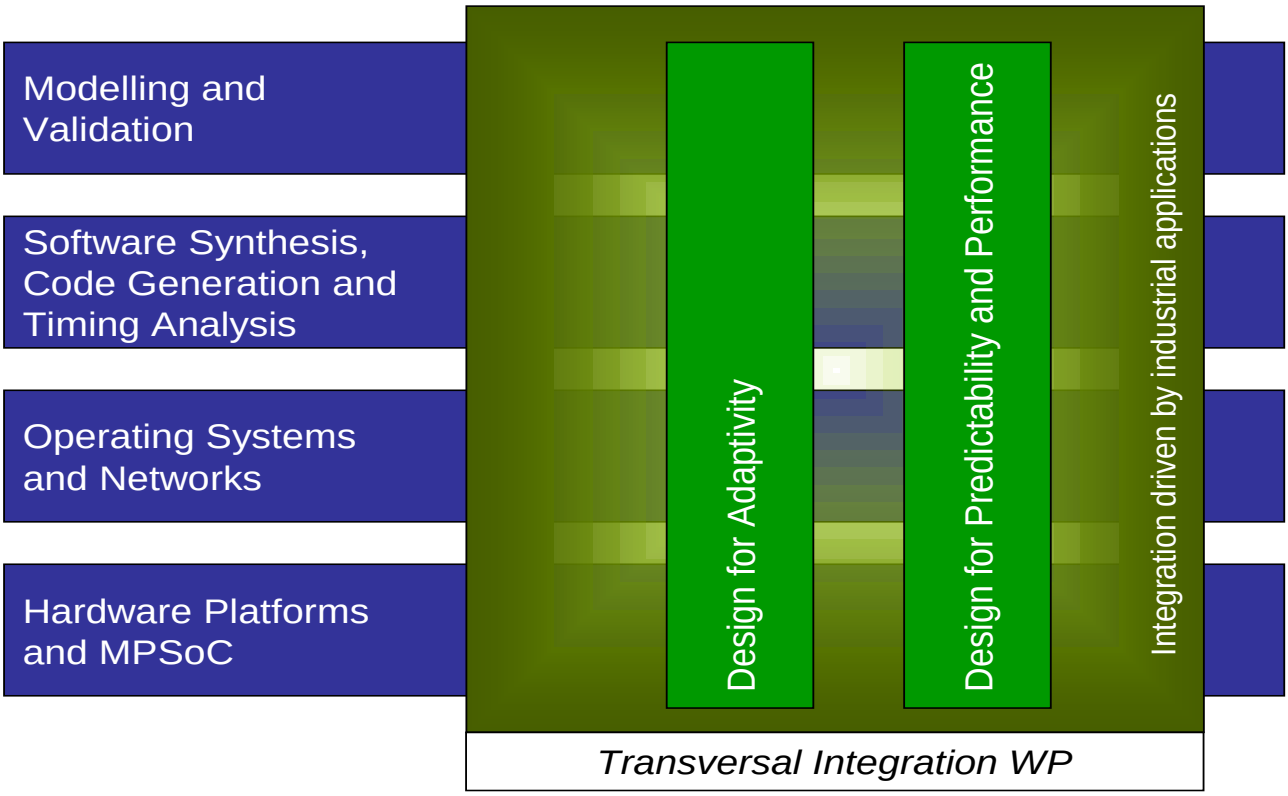
- **Joint Programme of Integration Activities (JPIA)**
  including joint technical meetings, staff mobility and exchanges, sharing research tools and platforms, and an intranet-based communication structure.
  These activities promote horizontal integration of geographically dispersed teams – each excellent in one or more topics -, and vertical and trans-disciplinary integration of traditionally separated topics. All these activities will have long-lasting effects, well beyond the duration of the initial EC funding.
- **Joint Programme of Research Activities (JPRA)**
  promote excellence and integration via either the Thematic Cluster activities, or the Transversal Integration activites.
  Integration may These activities are expected to move the state of the art forward, and have a real impact on work done in other teams, for both research and development.
- **Joint Programme of Activities for Spreading Excellence (JPASE)**
  allow excellence to spread from the JPRA and JPIA activities, to the larger embedded systems community.
  These usually take the form of workshops, schools, seminars, and publications (books, course materials, etc). Spreading excellence activities also allow the Artist2 partners to gain useful contacts and information from outside the NoE.
- **Joint Programme of Management Activities (JPMA)**
  plan, organize, direct and monitor the integrated effort to efficiently achieve the technical objectives within the ArtistDesign constraints of time schedule and budget.



The JPRA is composed of intra and inter-cluster research activities on cutting-edge topics in embedded systems design. While the main bulk of financing for these activities is taken up by outside programmes (Integrated Projects, National Programmes, Industrial Contracts, etc), the ArtistDesign NoE finances the extra burden due derived from integrating these into a single coherent research programme.

Thus, the essential ingredient within ArtistDesign is the JPRA, which motivates the participating research teams far more than the actual financing, which is tiny in comparison with the overall research aims. It is completed by the Joint Programme of Integrating Activities (JPIA), and the Joint Programme of Activities for Spreading Excellence (JPASE), and overseen by the Joint Programme of Management Activities (JPMA).

The structure of the research activities reflects the following decomposition of the embedded systems design flow.
This design flow is composed of the following cooperating activities, starting with component based modeling and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality.
Accordingly, we have structured the area of embedded systems design into the following topics.



Modeling and Validation. Unlike other computer systems, embedded systems are strongly connected with a physical environment. A scientific foundation for embedded systems must therefore deal simultaneously with software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based. The overall objective of this activity is develop model and component based theories, methods, and tools that establish a coherent family of design flows

spanning the areas of computer science, control, and hardware. The activity brings together the most important teams in the area of model and component based design in Europe.

SW Synthesis, Code Generation and Timing Analysis. There is a continuing demand for higher performance of information processing, which stimulates using a growing amount of parallelism (including using multiple processors). This trend affects the design of embedded systems. We address issues related to multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces. Such processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors.

Timing analysis is also affected by the trend toward the new platforms. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Also, timing analysis beyond the single processor is required. Hence, timing analysis will also consider the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors.

Operating Systems and Networks. We investigate how current real-time operating systems have to be extended or modified to support emerging real-time embedded systems characterized by a high degree of complexity, highly variable resource requirements and parallel processing such as multicores. Most embedded systems are often characterized by scarce resources in terms of processing power, memory, space, weight, energy, and cost.

Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, whilst guaranteeing isolation properties. Also, to support dynamic applications with variable resource requirements or to cope with unpredictable resource availability, feedback control techniques for resource management at the operating system and application level are also investigated.

Hardware Platforms and MPSoC Design. While hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application environments is much less clear. The consequence is fragmentation: while many research teams are working on one or more of these domains, there is little communication and integration, this leads to duplication of results and overall slow progress. The teams involved in this activity have a wide-ranging research experience which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ArtistDesign will help the participants to the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion.

Design for Adaptivity. An embedded hardware-software system is adaptive, if it can modify its behavior and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is a cross-cutting system characteristic that affects both hardware and software. At the software-level adaptivity is mainly concerned with flexible and adaptive resource scheduling, e.g., CPU time scheduling. At the hardware-level adaptivity includes both adaptation of operation modes, e.g., supply voltage and clock frequency, processor instruction sets, and dynamic management of hardware resources, e.g., processing elements and memory.

Design for Predictability and Performance. Many applications have strict requirements on timing, and limited resources (memory, processing power, power consumption, etc.). All systems also have increasing demands on (average) performance, which has motivated the introduction of features such as caching, pipelining, and (now becoming very prominent) multiprocessor platforms. Almost all such efficiency-increasing features drastically increase variability and decrease analyzability of response-times, etc. and thus have a detrimental effect on predictability. Since the introduction of new architectural features is inevitable, it is important to: a) develop technology and design techniques for achieving predictability of systems built on modern platforms, and b) investigate the trade-offs between performance and predictability.

Integration Driven by Industrial Applications. To have a strong impact on industry and society at large, the results of the Thematic Clusters need to be harmonized in an overall design flow that can sustain the embedded design chain from conception of the product to its implementation. The design chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g.,Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics). Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, the system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company.

c. Joint Programme of Integration Activities (JPIA)

The JPIA activities promote integration of geographically dispersed team sand have long lasting effects:

Joint Technical Meetings. Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

Staff Mobility and Exchanges. This is essential for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. Mobility is justified by and refers to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.

Tools and Platforms. A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalization on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

d. Jointly-executed Programme of Activities for Spreading Excellence (JPASE)

ArtistDesign is progressively creating a European embedded systems design community and spreading the "Artist culture" in all major research institutions.
To ensure that the next generation of researchers will continue in this direction we, as a consortium, devote a great deal of effort to Spreading Excellence, in both academic and industrial circles. Furthermore, through our links with both core and affiliated partners, we actively set up permanent links between industry and public research, based on existing partner collaborations with major industrial players in the area.
The JPASE activities are intended to spread excellence and structure the community at large. They are planned by the Strategic Management Board, and are implemented by ArtistDesign core and affiliated partners.
The NoE will leverage on its members and teams, who play a main role in the organization of world-class scientific events, to disseminate results in the area. We expect that the NoE's structured and authoritative dissemination will have a strong effect on the community as a whole, for orienting and creating synergy for research.

e. Managing the Network of Excellence (JPMA)

We believe that the current two-tiered Management structure - dividing the management amongst cluster leaders and the Strategic Management Board composed of both cluster leaders and a limited number of other selected prominent core partners – has been the right one for managing such a large research entity. It has provided the right combination of flexibility and accountability, while leaving room for innovation and evolution.

This management structure is reproduced with adaptations in the ArtistDesign NoE. The adaptations reflect the greater cohesion between partners, and move to capitalize on and strengthen the integration achieved in Artist2.

3. Core of the report for the period: Project objectives, work progress and achievements, project management

a. Project objectives for the period

The ArtistDesign NoE is the visible result of the ongoing integration of a community.
The central objective for ArtistDesign is to build on existing structures and link, to become a virtual Centre of Excellence in Embedded Systems Design. This is achieved through tight integration between the central players of the European research community. Also, the consortium is smaller, and integrates several new partners. These teams have already established a long-term vision for embedded systems in Europe, which advances the emergence of Embedded Systems as a mature discipline.

ArtistDesign is becoming the main focal point for dissemination in Embedded Systems Design, leveraging on well-established infrastructure and links. It will extend its dissemination activities, including Education and Training, Industrial Applications, as well as International Collaboration. ArtistDesign will establish durable relationships with industry and SMEs in the area.

ArtistDesign builds on existing international visibility and recognition, to play a leading role in structuring the area.

The research effort aims to integrate topics, teams, and competencies, grouped into 4 Thematic Clusters: "Modeling and Validation", "Software Synthesis, Code Generation, and Timing Analysis", "Operating Systems and Networks", "Platforms and MPSoC". "Transversal Integration" covering both industrial applications and design issues aims for integration between clusters.

b. Work progress and achievements during the period

i. Modelling Activity and the Validation Activity

Both research activities with the cluster – the Modelling Activity and the Validation Activity – have progressed substantially within the fourth year, and with significant synergy between proposed modelling formalisms and methods and validation techniques they support:
The work on Component Modeling and Compositional Validation involved several partners that produced significant results on compositional modelling and verification:

Results on modelling can be summarized as follows:

- Composition frameworks for behaviour and properties of heterogeneous systems such as assume/guarantee reasoning, interface automata, modal transition systems as well composition frameworks for tool integration based on meta-models and model-transformations have been consolidated and applied to case studies.
- Resource modelling techniques applied to design space exploration, multi-core scheduling, performance evaluation and derivation of distributed implementations from global specifications.
- Quantitative modelling techniques for weighted automata, priced timed automata and quantitative communication models.

Results on validation can be summarized as follows:

- Quantitative Validation covering a wide range of techniques for WCET analysis, schedulability analysis, frequency analysis of timed automata, analysis of parametric quantitative models, and analysis of resource consumption using energy- and price-extensions of timed automata. These techniques use new notions of metrics and robustness.
- Cross-Layer Validation focusing on model-based testing techniques such conformance testing of real-time systems using time- and data abstractions, asynchronous testing and test-case generation for embedded Simulink, incremental testing of composite systems as well as runtime monitoring.

In addition to these results, the Cluster has endeavoured a considerable integration effort for connecting tools, joint meetings, open workshops and joint publications.

ii. Software Synthesis, Code Generation and Timing Analysis

In year 4, we have seen a further proliferation of the basic techniques studied by this cluster. The importance of using multi-processor systems has been continuing to grow. Any session on programming multi-cores and multi-processor systems is filled with people. Fortunately, ArtistDesign is active in this area.
The work on software synthesis and code generation focused on the development of tools and resource-aware compilation. We developed two tools for mapping applications to multi-core or

multi-processor platforms (RWTH Aachen, IMEC). Our work on resource-aware compilation has continued with new results on energy efficiency and thermal behavior control as well as with fundamental machine-learning techniques for optimized code generation.

In program flow analysis, MDH and Tidorum have made advances towards increased soundness by developing an advanced relational value analysis that takes possible overflows and wraparounds into account. This is important for small embedded systems, where wraparounds are common
Additional activities include the organization of an international workshop on Software Synthesis (http://www.artist-embedded.org/artist/-WSS-11-.html) and development of new educational material on software synthesis, compilers and timing analysis in the second edition of the textbook on embedded systems by P. Marwedel.

The work on timing analysis and timing predictability has progressed significantly in two directions. The first focuses on enforcing predictability through determinism. It produced new and industrially relevant results on cache analysis and ache-aware memory allocation that have been taken up by commercial tools such as aiT from Absint. The second takes a probabilistic approach and relies on randomization to make timings on micro-level independent. Very promising initial results has been obtained.
Advances in hybrid WCET analysis methods, which include elements of measurements and testing, have been made (MDH, York, TU Vienna). Such timing models can be used to provide worst-case timing estimates early as well as small but appropriate sets of test vectors for tasks with very large input sets, and evaluation of coverage metrics for test-data generation.

Finally, the Cluster has achieved increased integration of timing analysis tools and compilation tools (TU Dortmund, TU Vienna).

iii. Operating Systems and Networks

The work developed by the cluster involved several partners that produced significant results summarized as follows:

The work on operating systems and middleware focuses on resource reservation and predictability. We developed an implementation of a real-time scheduler in the Linux kernel, with a support for resource reservation. We also developed a programming framework to support resource reservation of concurrent real-time applications on multi-core platforms, considered by Ericsson for software development in next generation cell phones. Finally, we proposed a comprehensive taxonomy for the resources currently used in embedded real-time systems.
Our work on predictability includes cache-aware analysis and scheduling for safety-critical applications, In collaboration with the Cluster on Compilers and Timing analysis.
The Cluster also developed a middleware and communication protocol for teams of mobile robots that are self-reconfigurable and provide efficient support to intensive interactions and which have been adopted by several teams in the RoboCup Middle Size League.
The work on networks includes two toolsets. One for the design, analysis, configuration and deployment of dense WSNs, the other is the MAST (Modelling and Analysis Suite for Real-Time Applications), which was enhanced with more networking components and analysis, namely for switched networks such as AFDX. Also a number of communication protocols and tools, developed for improving predictability and adaptivity in (industrial) networked embedded systems.

The cluster teams have been involved in many European projects, had strong interaction with industry and disseminated their work through active participation in world class conferences, workshops and schools.

iv. Hardware Platform and MPSoC Design

The Cluster has continued its efforts to establish an integrated modelling and design methodology that can take into account predictability and resource-awareness with focus on efficiency. This work has benefited from fruitful collaboration with the Cluster on Modelling and Validation and Timing Analysis as well as from the transversal activities on design from adaptivity and predictability.
Main results can be summarized as follows:

- Fault tolerant distributed embedded systems: We have developed results for handling both processor and communication faults in distributed real-time systems for automotive applications, based on CAN or FlexRay communication.
- Performance analysis methods: TU Braunschweig and ETH Zurich have developed very original and relevant results. They have collaborated to establish a method for coupling the tools SymTA/S and MPA. Relying on different analysis techniques each of the two tools can be individually used to evaluate the performance of embedded real-time systems. The interface developed for tool coupling now allows combining the strengths of the two tools. Evaluations have been jointly performed and the work resulted in joint publications.
- MPSoC design: Major activities on MPSoC design have focused on application parallelization, platform mapping, memory hierarchy management, application scenario exploitation, and run-time resource management, including reconfigurable systems. The outcome of these 4 years was the development of related tools, tool integration in tool chains in collaboration with several ArtistDesign partners, and highly referenced publications.
- Energy harvesting: We have developed new node level scheduling techniques (UNIBO and ETHZ) as well as network level routing algorithms (DTU), and have demonstrated that these techniques can lead to considerable extensions of the lifetime of the network. One specific outcome is the founding of the company WISPES srl (Wireless Self-Powered Electronic Systems) that aims at providing technologies and devices able to add wireless communication and local computation to the customer's monitoring and sensing activities.
- Temperature and energy aware optimization: EPFL has developed a novel online thermal management policy based on dynamic voltage and frequency scaling for high-performance 3-D systems with liquid cooling. The approach is able to gain up to 50% as compared to current state-of-the-art thermal control techniques.

Finally, the Cluster has an impressive record of joint publications, invited talks, analysis and design tools and industrial collaborations.

v. Design for Adaptivity

The work done includes numerous highlights:

- Scheduling analysis: Efficient and effective scheduling analysis for fixed priority systems has been developed that takes into account tasks arriving and leaving the system. Furthermore, a new method for allocation and scheduling of parallel tasks in soft-real time systems (multimedia decoding) in the presence of post-silicon, process and ageing induced variability in a nominally homogeneous target multi-core platform has been developed.
- Memory: Dynamically adaptable memory architectures for supporting dynamic real-time process loads have been developed.

- Collaboration frameworks: An adaptable cooperation-based framework for networked embedded systems with heterogeneous nodes has been developed, allowing constrained devices to cooperate with more powerful (or less congested) neighbours, to meet allocation requests and handle stringent constraints, opportunistically taking advantage of global resources and processing power.

- Service adaptation: Techniques have been developed for adapting the service request handling behaviour to the specific requirements of the services in Service Oriented Architectures (SOA). CPU contracts are used to ensure sufficient computation time for dealing with services with special requirements.

- Run-time resource management: An adaptive resource manager for distributed embedded systems aimed at multimedia applications, e.g., broadcast management systems, was developed. Considerable savings in power consumption, hardware cost and system size were reported in an industrial case study. Parallel to this a QoS based adaptive resource management system for homogeneous multicore platforms was developed.

- Run-time analysis: A distributed approach for in-system run-time performance analysis of embedded systems, complemented by a framework enabling access control and runtime-optimization through the use of distributed algorithms.

- Sensor networks: New approaches to adaptive energy management of energy harvesting system using solar cells have been developed. Based on a prediction of the future available energy, the application parameters are adapted in order to maximize the utility in a long-term perspective.

- Control techniques: A new method for optimizing the timing parameters of real-time control tasks in resource-constrained embedded systems has been derived. Also, new feedback scheduling techniques and new event-driven sampling mechanisms have been proposed.

- Adaptivity in networks: Here various ways of adapting a communication channel to varying application requirements or environmental conditions to enhance the efficiency of medium utilization have been proposed. For controlled access networks with isolated virtual channels the guaranteed bandwidth and latency can be adapted online using the Flexible Time-Triggered (FTT) paradigm on switched Ethernet, either with COTS switches (FTT-SE protocol) or enhanced ones (FTT-enabled switch).

- Programmable hardware: A new type of ultra-fault-tolerant FPGA named the eDNA architecture has been conceived all the way from development of the concept, to the implementation of a prototype, to test in a space related case study NASA JPL.

- WCET analysis: Parametric WCET bounds, where the WCET bound depends on the values of certain inputs, can be used in adaptive real-time systems where the scheduling of tasks adapts to external factors such as varying data sizes affecting the running times of tasks. A general method for parametric WCET analysis, which combines a number of advanced symbolic techniques including relational abstract interpretation, counting of integer points in polyhedra, and parametric integer programming has been developed and implemented in the WCET analysis tool SWEET.

- Reference architectures: A reference architecture for automotive embedded systems that addresses the needs for flexible and automatic run-time reconfiguration has been proposed. The research focus was the development of technical support in terms of middleware services for a closed adaptation of distributed embedded systems. In addition to the

reference architecture an information model of the control parameters that represent the target system configuration alternatives, environmental parameters, and internal conditions has been defined and a functional design has been performed.

vi. Design for Predictability and Performance

The Predator project has made strong progress in its attempt to reconcile Predictability with Performance. The integration of the AbsInt timing-analysis tool aiT with the WCET-aware compiler of TUDortmund is described separately. Another recent achievement of the project concerns the determination of context-switch costs, which provides support for schedulability analysis for preemptive scheduling strategies. Insights into the predictability properties of architectural features have found their way into the embedded-systems industry, e.g., as a result of collaboration in European projects. These insights, however, are still at odds with trends at the processor manufacturers' side. Suppliers of time-critical embedded systems cannot find platforms with the required predictability properties on the market.

The trends to multi-core platforms presents a significant challenge to the building of predictable and performant systems, and there is still significant hesitation to migrating embedded systems to multi-cores. Significant advances on isolation and analysis techniques have been made (to a large extent by ARTIST-Design partners): progress is made, e.g., in the area of deterministic access protocols and controllers for shared resources such as buses or memory. However, the worst-case delay used in safe approximations is still often too high to be acceptable.

A good collection of insights was gathered at the PPES workshop, organized by ARTIST-Design, jointly with Predator and Merasa, as a satellite event of DATE 2011 in Grenoble. Overviews about architecture and software issues were given, e.g. including a survey on predictability and performance requirements in avionics systems, and a template for, partly analytically, partly intuitively; estimating the predictability of hardware features was presented.

During year 4, development of support for the MARTE standard (initiated during ARTIST2), led by U. Cantabria, has provided increased support for scheduling and code generation. The work on integration between timing analysis tools has matured: several of the leading timing analysis tools have been integrated by efforts in the All-Times project (described in the report on Timing analysis).
A notable trend during Year 4 has been the work on reconciling predictability with performance, developing techniques for optimizing performance along several dimensions (e.g., combing WCET with average-case timing). Work in this direction (by Bologna, ETHZ, Linköping, Trento) has considered different forms of multi-objective optimization of embedded software; such possibilities also exist in the WCC compiler. Another increasingly important topic has been to make scheduling and timing analysis robust to inaccuracies in assumptions about, e.g., execution times, interferences, etc.
Work on the integration of timing analysis and compilation, in the context of the WCC compiler, aimed at removing some of the earlier restrictions. The work started at TU Dortmund considering WCET-aware basic block reordering has been finished. Unconditional branches are avoided and the prediction of conditional branches is supported by the developed techniques. A genetic approach applies evolutionary algorithms considering the WCET of the program to optimize as fitness value with the costs of high optimization times. Thus, an integer-linear programming-based approach has been developed which determines the optimal order of basic blocks and also takes the branch prediction into account [PKFM11]. Furthermore, WCET-aware cache locking and code positioning has been improved. The integration and enhancement of a framework for the static analysis of software and hardware as announced in last year's report has been advanced. The extension of

WCC's native analysis capabilities allows for novel approaches especially in the domain of multitask- and multicore-aware compilation. A much higher degree of control over system states directly affected by optimization decisions can thus be achieved. The primary effort was made in the direction of tightening timing estimations and the evaluation and improvement of cache analysis techniques with a focus on improving compiler optimizations [KFM11].
http://ls12-www.cs.tu-dortmund.de/research/activities/wcc

vii. Industrial Integration

This activity groups a set of industrial interactions and collaborations with ArtistDesign teams. The long-term goal is to understand industrial design methodologies and identify the research results that could be applied in these methodologies.

The activities include both technical achievements and dissemination work on the following: General Frameworks for system-level design; Applications to the Automotive Sector; Applications to Chip Design; Applications to Buildings; Applications to Wireless communication technology; Timing Analysis and Predictability; Other Applications.

The level of energy at the meetings organized to foster industrial integration was excellent. This theme is of increased interest to the European community in response to energy conservation concerns.

c. Project management during the period

The consortium management is carried out by the ArtistDesign Strategic Management Board (http://www.artist-embedded.org/artist/-Strategic-Management-Board,938-.html): Joseph Sifakis – chair (UJF/VERIMAG), Luis Almeida (Univ Porto), Karl-Erik Årzén (Lund), Luca Benini (Bologna), Albert Benveniste (INRIA), Bruno Bouyssounouse (UJF/VERIMAG), Alan Burns (York), Giorgio Buttazzo (Pisa), Tom Henzinger (IST Austria), Bengt Jonsson (UPPSALA), Kim Larsen (Aalborg), Jan Madsen (DTU), Peter Marwedel (TU Dortmund), Alberto Sangiovanni (TRENTO), Lothar Thiele (ETH Zurich), Reinhard Wilhelm (Saarland University).

Day to day management of the NoE is carried out by the ArtistDesign office: The Scientific Coordinator is Joseph Sifakis; the Technical Coordinator is Bruno Bouyssounouse, the Administrative, Legal and Financial Coordinator is Olivier Guérard.

The management tasks include (but are not limited to):

- Organize the technical work and meetings
- Ensure that work progresses on track
- Organize, collect and finalize the technical reporting
- Organize, collect and finalize the financial and administrative reporting
- Organize the Spreading Excellence Activities (see the deliverable), and implement the main ones (others are implemented by the partners).
- Take care of management issues (evolution of the budget, changes to the consortium, etc).

The management achievements include:

- A successful Year 4 (all of the points above).

Problems that have occurred

- No particular problems occurred over the course of year 4

Changes in the consortium

- Partner n°33 UNIV PORTO became partner n°35 Universidade do Porto.

Project Meetings, Dates, Venues

The following section is detailed in tthe JPASE: Spreading Excellence D4-(2.0)-Y4.

Project planning and status

The project has fully achieved its objectives and technical goals for the period.
All milestones had been reached for the fourth year and all deliverables had been produced.

Impact of possible deviations from the planned milestones and deliverables, if any

There were no significant deviations from the planned milestones or deliverables.

Any changes to the legal status of any of the beneficiaries, in particular non-profit public bodies, secondary and higher education establishments, research organisations and SMEs;

During Year 4, there were no changes in legal status for any of the beneficiaries.

Development of the Project website

The following section is an extract from the JPASE: Spreading Excellence D4-(2.0)-Y4.

ArtistDesign Web Portal

Objectives and Background Information

The ArtistDesign Web Portal is a major tool for Spreading Excellence within the Embedded Systems Community. Its aim is rather ambitious: to be the focal point of reference for events and announcements of interest to the embedded systems community.
The web portal disseminates information about contacts (ArtistDesign core and affiliated partners), the ArtistDesign JPA activities, as well a fairly thorough set of links to sites of interest to the embedded systems community.
As can be seen, a great deal of effort has been put into the web site, both for ergonomics / graphical quality, as for the contents.
The web site includes several features that help keep it coherent and up to date:

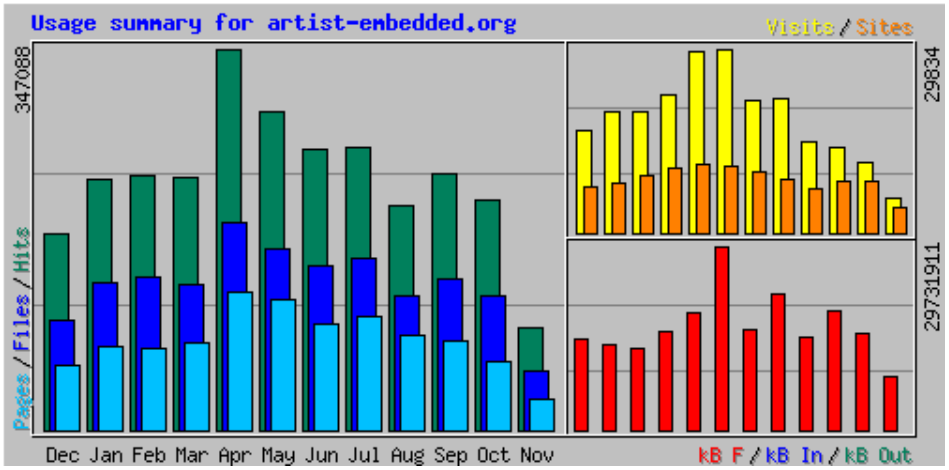
Authorised users (principally, the ArtistDesign partners) can access the back end of the site to modify and update information directly. The changes are immediately visible on the site, which greatly streamlines the updating process.
It's possible to track changes and go back to previous versions of individual web pages.
Events are automatically sorted by date, and transferred to 'Past Events'. When appropriate.
Structural information (hierarchy of pages) is maintained automatically.
Ergnomics are set for the entire site. The "look and feel" of the site is always homogeneous thoughout the site. It's possible to change these ergonomics, and these changes are applied homogeneously throughout the site, via automated machanisms.

Structure

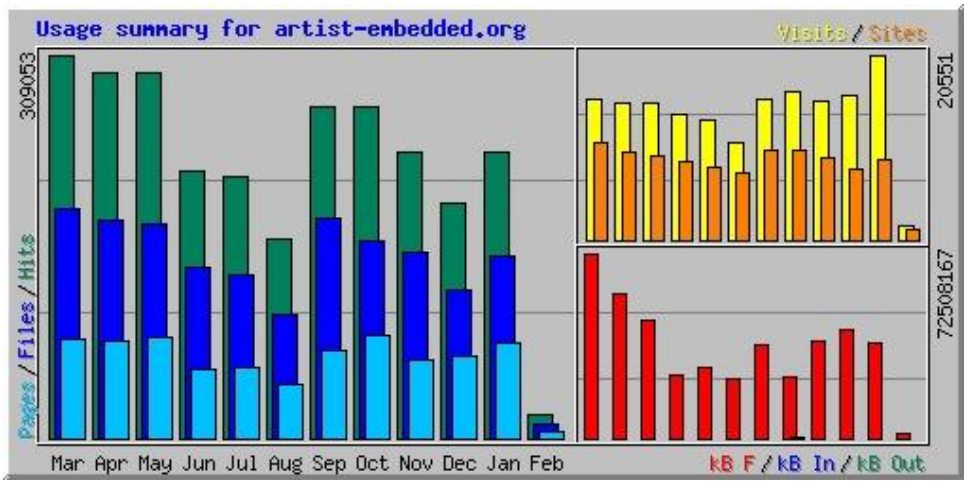
The structure of the ArtistDesign web site is visible on the Site Map: http://www.artist-embedded.org/artist/spip.php?page=plan). Analysis of Visits to the Portal

Number of Visits Overall

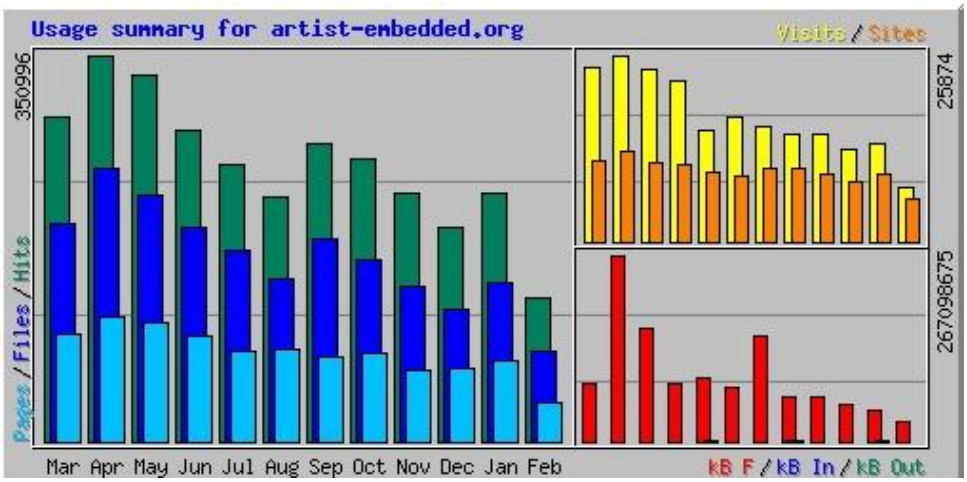
Year 1

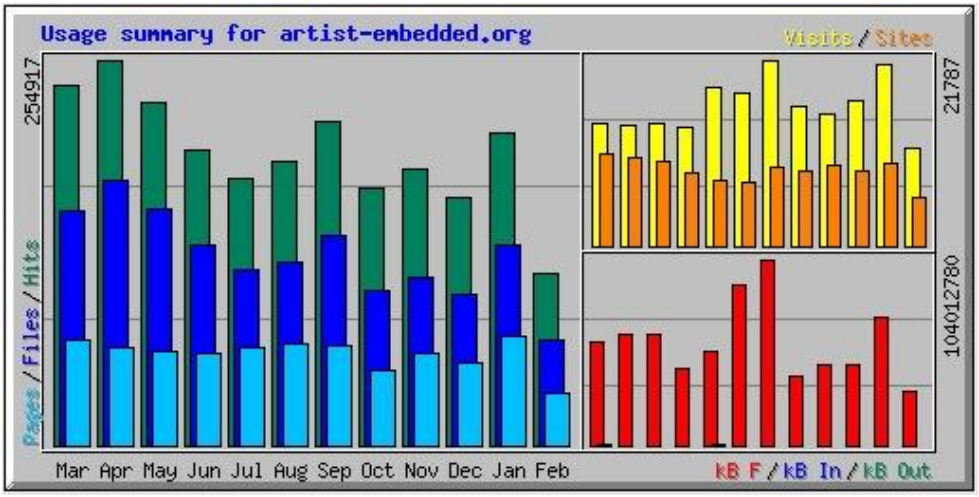


Year 2



Year 3





The main conclusion from this analysis is that visits to the site are largely driven by the ARTIST events organised (workshops, conferences, schools), and that this drives visits to the other sections: "Embedded Systems Links", and "Research and Integration".

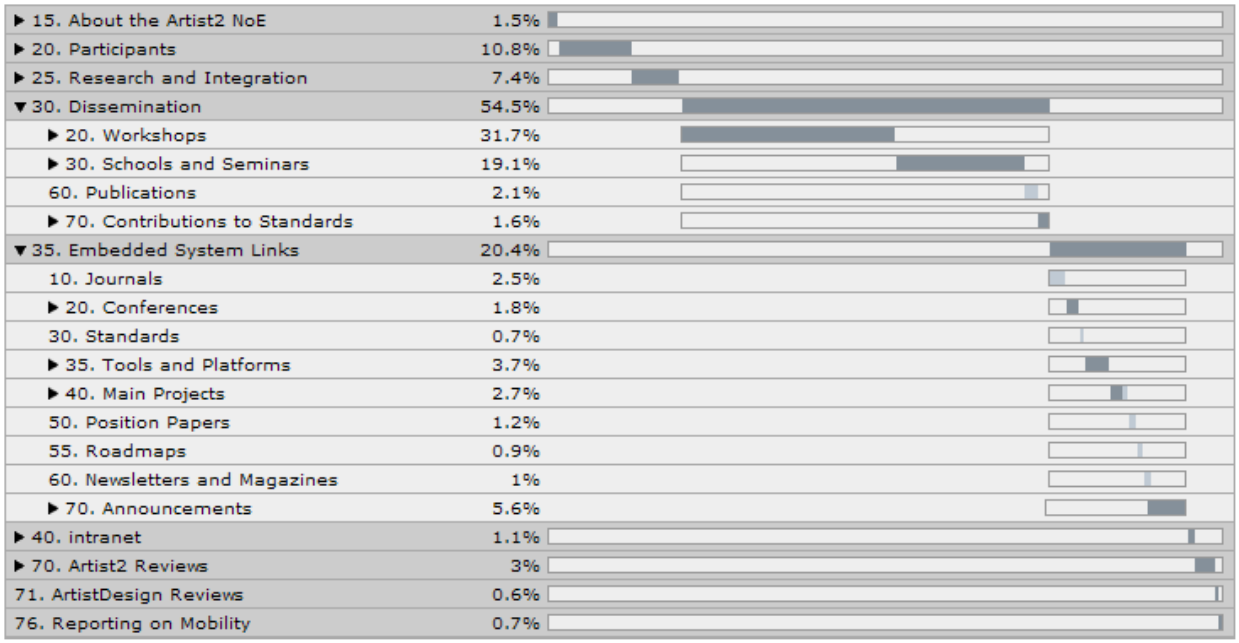
Yearly variations do not necessarily imply that the portal has had less impact. For example, if key information (eg: the program or registration or venue) is missing from a workshop page, then it can logically be expected that visitors will return often, generating *more* traffic for what is, finally, *lower* impact and usability.

It is important to note that a deep analysis of the pertinence and effectivity of the web portal would need to go beyond the numerical analysis provided here. The real impact of a website is in whether or not the members of the community find the information relevant, and how it helps them in their daily tasks.

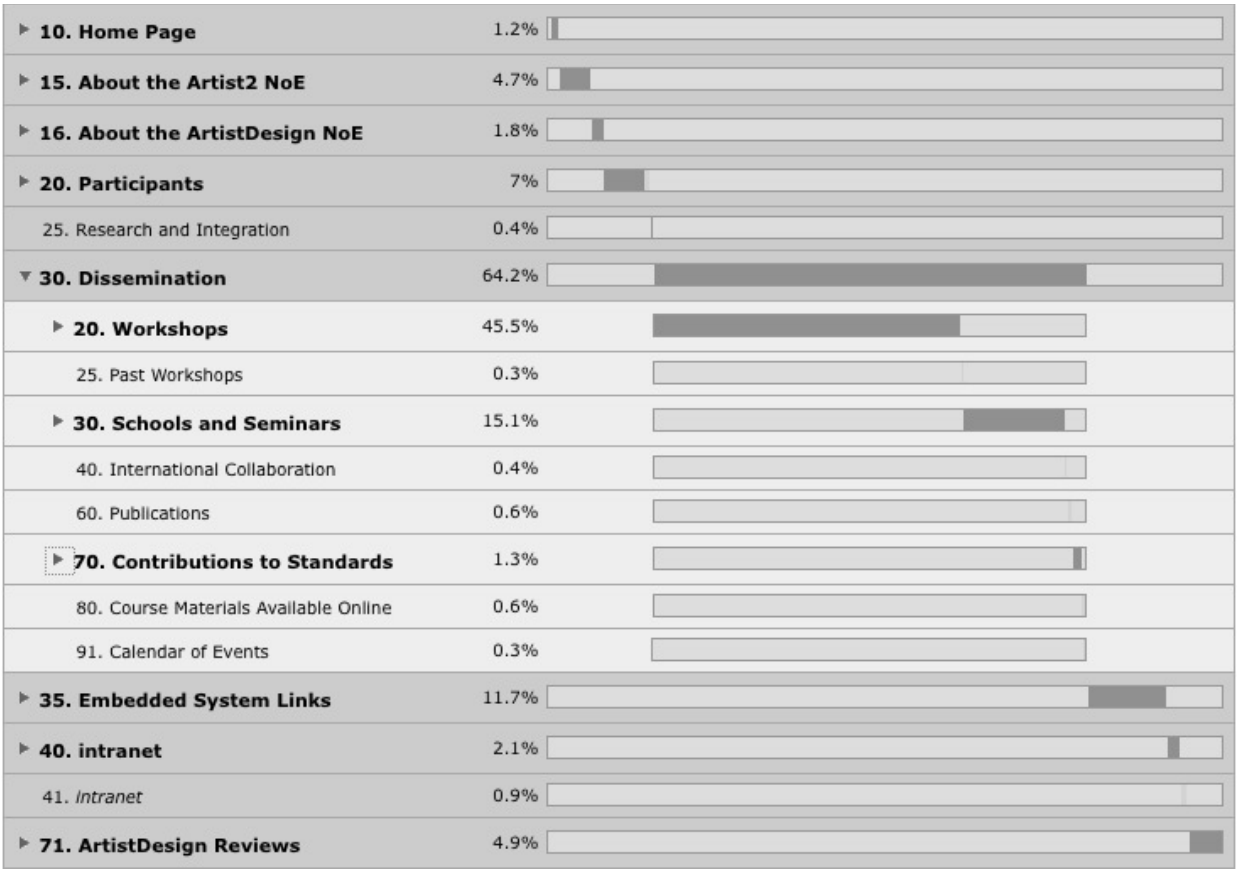
Visits Distribution within the site

The tables below show the distribution of visits to the various parts of the portal.

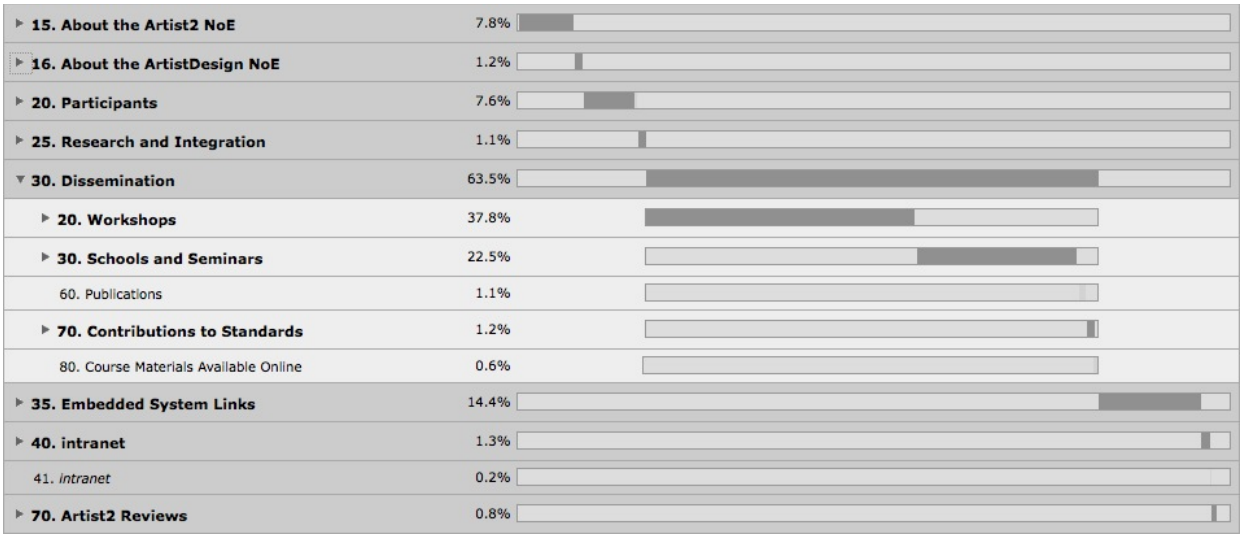
Year 1



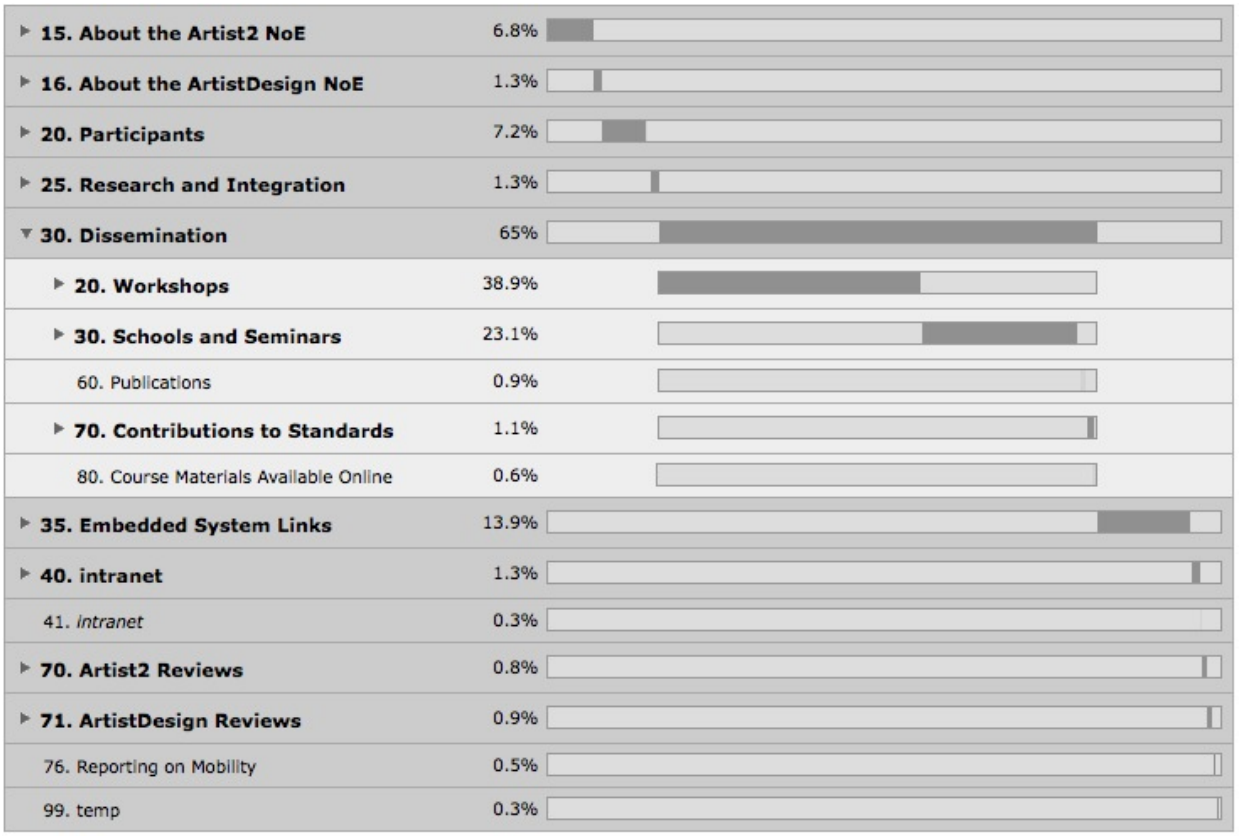
Year 2



Year 3


15. About the Artist2 NoE 7.8%
16. About the ArtistDesign NoE 1.2%
20. Participants 7.6%
25. Research and Integration 1.1%
30. Dissemination 63.5%
20. Workshops 37.8%
30. Schools and Seminars 22.5%
60. Publications 1.1%
70. Contributions to Standards 1.2%
80. Course Materials Available Online 0.6%
35. Embedded System Links 14.4%
40. intranet 1.3%
41. intranet 0.2%
70. Artist2 Reviews 0.8%

Year 4


15. About the Artist2 NoE 6.8%
16. About the ArtistDesign NoE 1.3%
20. Participants 7.2%
25. Research and Integration 1.3%
30. Dissemination 65%
20. Workshops 38.9%
30. Schools and Seminars 23.1%
60. Publications 0.9%
70. Contributions to Standards 1.1%
80. Course Materials Available Online 0.6%
35. Embedded System Links 13.9%
40. intranet 1.3%
41. intranet 0.3%
70. Artist2 Reviews 0.8%
71. ArtistDesign Reviews 0.9%
76. Reporting on Mobility 0.5%
99. temp 0.3%

4. Deliverables and milestones tables

a. Deliverables

WP0: Joint Programme of Management Activities (JPMA)		
Floralis	D1-(0.1)-Y4	Periodic Report
UJF/Verimag	D2-(0.2)-Y4	Project Management Report *(the sum of the 5 chapters below)*
UJF/Verimag	D2-(0.2a)-Y4	ch. 1 - Executive Summary and Overview
Aalborg	D2-(0.2b)-Y4	ch. 2 - Modelling and Validation
Dortmund	D2-(0.2c)-Y4	ch. 3 - SW Synthesis, Code Generation and Timing Analysis
Pisa	D2-(0.2d)-Y4	ch. 4 - Operating Systems and Networks
DTU	D2-(0.2e)-Y4	ch. 5 - Hardware Platforms and MPSoC Design
WP1: Joint Programme of Integration Activities (JPIA)		
UJF/Verimag	D3-(1.0)-Y4	Integration Activities Report
WP2: Joint Programme of Activities for Spreading Excellence (JPASE)		
UJF/Verimag	D4-(2.0)-Y4	Spreading Excellence Report
WP3: Modeling and Validation (JPRA)		
UJF/Verimag	D5-(3.1)-Y4	Modelling
Aalborg	D6-(3.2)-Y4	Validation
WP4: Software Synthesis, Code Generation and Timing Analysis (JPRA)		
Dortmund	D7-(4.1)-Y4	Software Synthesis, Code Generation
Malardalen	D8-(4.2)-Y4	Timing Analysis
WP5: Operating Systems and Networks (JPRA)		
Pisa	D9-(5.1)-Y4	Resource-aware Operating Systems
York	D10-(5.2)-Y4	Scheduling and Resource Management
Univ. Porto	D11-(5.3)-Y4	Real-Time Networks
WP6: Hardware Platforms and MPSoC (JPRA)		
Bologna	D12-(6.1)-Y4	Platform and MPSoC Design
DTU	D13-(6.2)-Y4	Platform and MPSoC Analysis
WP7: Transversal Integration (JPRA)		
Lund	D14-(7.1)-Y4	Design for Adaptivity
Uppsala	D15-(7.2)-Y4	Design for Predictability
		Building Timing Predictable Embedded Systems (unplanned, extra deliverable - PDF only)
Trento	D16-(7.3)-Y4	Integration Driven by Industrial Applications

b. Milestones

Table 2. Milestones - Year 4

Milestone N°	Milestone name	Due achievement date from Annex 1	Achieved Yes/No	Actual / Forecast achievement date	Comments
M-Integr-Y4	Integration through EU centers of excellence	T0+48	**Yes**	Actual achievement date	Cf. Deliverable D3-1-0-Y4_Integration_Activities
M-Educ-Y4	Education Y4	T0+48	**Yes**	Actual achievement date	Cf. Deliverable D4-2-0-Y4_Spreading_Excellence
M-Web-Y4	Web Y4	T0+48	**Yes**	Actual achievement date	Cf. Deliverable D4-2-0-Y4_Spreading_Excellence
M-IntlCollab-Y4	International Collaboration Y4	T0+48	**Yes**	Actual achievement date	Cf. Deliverable D4-2-0-Y4_Spreading_Excellence

5. Explanation of the use of the resources

For the last year of the project, there is no significant financial deviation to take into account.

Amounts claimed on personnel cost are closely linked with the effort in terms of man month claimed in the project. Some partners did not declare any personnel costs with any adjustments planned retrospectively.

The following table indicates the costs claimed by partners per type of expenditures.

ARTISTDESIGN - ESTIMATED ELIGIBLE COSTS PER TYPE OF EXPENDITURES Y4+ADJ							
N°	Participant	Manpower	Travel (*please provide details)	Other costs	Other costs (WP2)	Overheads	Total
1	FLORALIS	23 890 €		3 603 €	123 842 €	5 499 €	**156 833 €**
2	UJF	176 676 €	1 289 €		56 €	351 534 €	**529 555 €**
3	Aachen	21 310 €				12 786 €	**34 096 €**
4	Aalborg		5 160 €	4 467 €		5 897 €	**15 524 €**
5	Aveiro						0 €
6	Bologna	11 606 €	19 364 €	6 699 €		22 601 €	**60 270 €**
7	TUBS						**0 €**
8	Cantabria	22 788 €	17 535 €	3 033 €	3 020 €	27 826 €	**74 202 €**
9	CEA	15 714 €	9 097 €			7 773 €	**32 583 €**
10	DTU	34 787 €	582 €		7 159 €	21 222 €	**63 750 €**
11	Dortmund	36 503 €	3 595 €	966 €		24 638 €	**65 702 €**
12	EPFL	7 159 €	0 €	17 €		4 306 €	**11 482 €**
13	ESI	8 767 €	253 €			5 412 €	**14 432 €**
14	ETH Zurich	0 €	1 319 €			792 €	**2 111 €**
15	IMEC	75 400 €	24 €			71 935 €	**147 359 €**
16	INRIA	30 405 €	1 871 €		7 704 €	15 590 €	**55 570 €**
17	TUKL	30 321 €	14 260 €	312 €		26 741 €	**71 634 €**
18	KTH	43 730 €	18 961 €	3 035 €		20 709 €	**86 435 €**
19	Linköping	2 802 €	5 981 €			5 269 €	**14 052 €**
20	ULund	33 047 €	3 403 €	135 €	0 €	21 951 €	**58 536 €**
21	MDH	18 000 €	4 228 €	1 079 €		13 984 €	**37 292 €**
22	OFFIS	3 139 €	10 471 €	0 €	0 €	8 166 €	**21 776 €**
23	Parades						0 €
24	Passau	15 800 €	7 600 €	0 €	0 €	14 050 €	**37 450 €**
25	SSSA-Pisa	8 515 €	8 736 €	10 475 €		16 636 €	**44 362 €**
26	Porto	5 419 €			408 €	3 251 €	**9 078 €**
27	Saarland	24 700 €	5 000 €	0 €	0 €	17 820 €	**47 520 €**
28	PLU-Salzburg						**0 €**
29	Uppsala	1 005 €	720 €	0 €		1 035 €	**2 760 €**
30	Vienna	6 105 €	11 866 €			10 782 €	**28 753 €**
31	York						**0 €**
32	IST Austria	20 457 €	6 586 €			16 225 €	**43 268 €**
35	Unv Porto	21 220 €	5 610 €		5 767 €	16 098 €	**48 696 €**
34	TRENTO	28 164 €	5 561 €			15 181 €	**48 906 €**
	TOTAL	**727 429 €**	**169 072 €**	**33 821 €**	**147 955 €**	**785 709 €**	**1 863 986 €**

Please note that the second "other costs" box is related to specific costs and sponsorship to the spreading excellence activity (WP2).
Details are provided in the JPASE deliverable Spreading Excellence D4-(2.0)-Y4.

Floralis, co organizer of the Summer School in Aix les Bains (France) received money from the fees registration. The amount of receipts is 50 923€ excluded VAT and does not appear in the table above. According to the financial rules of FP7 projects, these receipts had been declared in FormC for the Year 4. An adjustment on Y2 receipts needs to be submitted. Receipts had been previously declared included VAT.

Please note that there are missing figures related to expenses on Y4.
Due to the date of the review (before the official end of the project, some partners just can't send their cost statement.)

The following table provides details on the different work packages with explanations on the tasks performed related to the costs claimed above:

ARTISTDESIGN - YEAR 4			
Table - COMMENTS ON WORK carried out			
Participants	**WPs**	**person months**	**Comments**
Partner 1 Floralis	**WP00**	6,00	**Legal, Administratvie and Financial Coordination of the project** + organization of the Artistdesign Summer school
	WP02	0,00	expenses related to the "spreading excellence" activity.
TOTAL		**6,00**	
Partner 2 UJF	WP00		**Scientific and Technical coordinators of the project** - Joint Programme of Management Activities (JPMA)
	WP01		Joint Programme of Integration Activities (JPIA)
	WP02		Joint Programme of Activities for Spreading Excellence (JPASE)
	WP03		Modeling and Validation (JPRA)
	WP04		Software Synthesis, Code Generation and Timing Analysis (JPRA)
	WP05		Operating Systems and Networks (JPRA)
	WP06		Hardware Platforms and MPSoC (JPRA)
	WP07		Transversal Integration (JPRA): "Design for Adaptivity", "Design for Predictability", " Integration Driven by In
TOTAL		**0,00**	
Partner 3 Aachen	WP04	5,00	MAPS compiler for MPSoC platforms
TOTAL		**5,00**	
Partner 4 Aalborg	WP01	0,00	
	WP02	0,00	
	WP03	0,00	
	WP07	0,00	
TOTAL		**0,00**	
Partner 6 Bologna	WP01	1,00	Personnel: cost of 1 full professor; Travel expenses: participation to meetings with Verimag, CEA LETI, ST in Grenoble and to the review Meeting in Brussels.
	WP02	0,95	Personnel: costs of 1 full professor and 2 grants for research; Travel expenses: participation to Biostec 2011 in Rome, to DAC 2011 in San Diego, to ETMEC 2011 in Maui, to the Summer school Artistdesign in
	WP06	0,00	Consumables: purchase of electronic material; Other costs refer to a reimbursement for a seminars.
TOTAL		**1,95**	
Partner 7 TUBS	WP01		
	WP02		
	WP06		
	WP07		
TOTAL		**0,00**	
Partner 8 Cantabria	WP01		Contribution to Project Meetings, organization of workshops and conferences
	WP02		Organization of IRTAW-15 workshop, Organization of Workshop on Real-Time System Models for Schedulability Analysis
	WP05		Joint research and dissemination of scheduling theory, real-time operating systems, and real-time
	WP07		Real-time component-based design platform, and contribution to OMG standards
TOTAL		**0,00**	

Partner 9 CEA	WP02	0,22	Workshops organisation: UML&FM2011, ACES 2011 and UML & AADL 2011.
	WP03	13	Work on a framework for designing real-time systems in order to apply component-based design pattern for supporting MoCC as defined in the MARTE specification
	WP06	1	Work on resource dynamic management in the context of parallel architecture.
TOTAL		**14,22**	
Partner 10 DTU	WP01	1,95	Coordination between research projects, arranging events and meetings
	WP02	1,00	Organization of program for CODES+ISSS 2011 as part of ESWeek; Organizing and teaching on ARTIST Summer School in China 2011; Organizing Industry Workshop on safety-critical systems; Embedded Systems position paper for danish industry; Tutorial on microfluidic biochips at ESWeek; Participating in
	WP06	0,43	Coordinating and writing the MPSoC deliverables; MPSoC design and programming; Modeling and analysis of heterogeneous systems; Microfluidic biochips
	WP07	2,00	Adaptive Systems: Self-organizing and self-healing bio-inspired hardware architecture for safety-critical
TOTAL		**5,38**	
Partner 11 Dortmund	WP01	0,00	Interaction across clusters
	WP02	0,63	Workshop management, handling of textbook
	WP04	6,00	Cluster coordination, integration and research on worst case execution time (WCET) aware compilation
	WP07	1,00	Benchmarking for worst case execution time (WCET) aware compilation
TOTAL		**7,63**	
Partner 12 EPFL	WP02	1,00	Research visit, collaboration and organization with Prof. Luca Benini
	WP03		(i) Analysis of clock distribution networks in 3-D ICs (ii) Development of analytic thermal models for vertically integrated systems (iii) Design automation tools for MPSoC and 2D/3D NoC-based systems (iv) Optimization techniques for thermal management of 3-D MPSoC (v) 3-D monolithic integration *As a part of WP6: Hardware Platforms and MPSoC
TOTAL		**1,00**	
Partner 13 ESI	WP01	0,10	
	WP03	0,10	
	WP07	0,40	
TOTAL		**0,60**	
Partner 14 ETH Zurich	WP01	0,00	
TOTAL		**0,00**	
Partner 15 IMEC	WP01	4,81	
	WP04	1,50	
	WP05	1,00	
	WP06	2,00	
	WP07	1,25	
TOTAL		**10,56**	
Partner 16 INRIA	WP01		
	WP03		
	WP07		
TOTAL		**0,00**	
Partner 17 TUKL	WP01	0,50	travel expenses: Fohler: RTSS 2010 San Diego, Artist Meeting Brussels, Research Meeting Houston/USA,ECRTS & Artist Meeting Lund/Sweden, Artist Meeting Bologna/Italy, Artist Meeting Pisa/Italy; Schorr: Artist Meeting Bologna, Summer School Trient/Italy; Pereira: Artist Meeting Bologna/Italy, Summer School Trient/Italy; Ferreira: Artist Meeting Bologna/Italy. Anderson: Reimbursement of travel expenses for
	WP02	0,50	
	WP05	3,00	Partner in the OS, Scheduling, and Networks cluster. Mixed Criticality on TT, Resource Management on
	WP07	3,00	Partner in ActivityDesign for Adaptivity. Adaptive Resource Management Framework, Adaptive Control of Vi
TOTAL		**7,00**	
Partner 18 KTH	WP06	1,20	Performance modeling and contact based design methodology for NoCs.
TOTAL		**1,20**	
Partner 19 Linkoping	WP01		Travel expenses: Project meeting Brussels February, CPS Week Chicago April, Project meeting Zurich April, RASDAT 2011 & DELTA 2011 Conferences, January.
	WP06	4,30	1. Continued the work on temperature modelling and extended the earlier elaborated temperature models to multicore systems. 2. Fault modelling of the communication infrastructure aiming at the synthesis of fault tolerant communication over FlexRay buses for automotive applications.
	WP07	1,50	1. Temperature aware and energy efficient design of real-time embedded systems. The emphasis was on In the issue of leakage energy optimization through temperature aware idle time distribution. 2. Security aware optimisation of Distributed Embedded Systems.
TOTAL		**5,80**	

Partner 20 Ulund	WP05		Partner in the OS and Networks cluster. Coordinated research on event-based control and co-design of
	WP07	7,00	Leader for the Design for Adaptivity transversal activity. Organized workshop, editing deliverable, preparing review, setting up wiki, Coordinated research on adaptivity in embedded systems. Joint work with TUKL on adaptive resource management, with the aim to
TOTAL		**7,00**	
Partner 21 MDH	WP01		Travel expenses: review and general assembly in Brussels, TA activity meetings in Brussels, Porto
	WP02		organization WCET workshop
	WP04		Coordination TA activity, Research on WCET analysis for explicitly parallel programs, early WCET analysis
	WP07		Research on parametric timing analysis for adaptive systems
TOTAL		**0,00**	
Partner 22 OFFIS	WP03	0,50	Activities related to topics Model-based engineering of critical embedded systems, contract-based design, development platform for critical systems engineering covering interoperability concepts. Travel details: - Feb 22-24; Brussels; Bernhard Josko; ArtistDesign Year3 Review; 1085,55€ - Dec 1-3, 2012; Braunschweig; Hardi Hungar; Workshop FORMS/FORMAT2010; 484,24 € - Feb. 16-18; Dagstuhl; Hardi Hungar; Seminar MBEES2011; 397,38€ - March 26 - Apr 2; Rome; Werner Damm; Work together with A. Sangiovanni Vincentelli on contract-based defign; 1608,86 € - Apr. 1-4; Dagstuhl; Hardi Hungar; Workshop Science and Engineering of Cyber Physical Systems; 165,35 €
	WP07	0,00	Continous deliberations on industrial design processes for critical systems engineering and establishment of a reference technology platform for critical systems engineering with large companies (Automotive, Aerospace); Dedicated workshops with individual partners on critical systems engineering; co-organisation of SafeTRANS Industrial Days on Reference Technology Plaftforms for Critical System Design and on Certified Design Processes for Multi-core Target Architectures. Travel Details:
TOTAL		**0,50**	
Partner 24 Passau	WP01		Travel expenses for attending workshops & conferences on automatic parallelization and embedded systems. Research on extending the polyhedral model to the embedded domain (Accelerators: FPGA/GPGPU) PARTICIPATIONS AND PRESENTATIONS: - CGO 2011: Christian Lengauer, Armin Größlinger, Andreas Simbürger - HIPEAC 2012: Armin Größlinger, Andreas Simbürger - SCOPES 2011: Andreas Simbürger
	WP04	5,81	
	WP07		
TOTAL		**5,81**	
Partner 25 SSSA PISA	WP02	0,50	Organization of the Graduate Courses on Real-Time Kernels for Microcontrollers, Pisa, June 13-17, 2011.
	WP05	0,50	Contributions to the maintenance of the operating systems and tools used by other partners. Advertisement
TOTAL		**1,00**	
Partner 26 PORTO	WP01	0,50	Participation in the General Assembly and Review Meeting and contributions to the year 4 tuning of objectives of concerned clusters and transversal activities.
	WP02	1,50	Organization of ECRTS 2012, Visit by Kai Huang
	WP05	2,75	Contributions to the 3 activities, namely in efforts concerning multiprocessor scheduling, QoS and resource management, cluster-tree wireless sensor networks, and energy management; Travel: Meeting in conjunction with ECRTS11 PC meeting; CPS Week11 conference; RTN11 workshop; Meetings with other partners; For 2012 (the activity was extended) - Visit to Pisa, PhD examination, Talk
TOTAL		**4,75**	
Partner 27 SAARLAND	WP04	3,50	
TOTAL		**3,50**	
Partner 28 PLU SALZBURG	WP01		
	WP02		
	WP03		
	WP07		
TOTAL		**0,00**	
Partner 29 UPPSALA	WP01		
	WP02		
	WP03		
	WP07		
TOTAL		**0,00**	

Partner 30 VIENNA	WP00	0,07	Reporting, Financial Management
	WP01	1,23	Meetings at WCET, DATE, ECRTS, WORNUS, RTSS; work on open timing-analysis platform
	WP02	1,24	Direction of WCET workshop; organisation of RTSS; presentations at meetings (WCET, WORNUS)
	WP04	0,02	open timing-analysis platform definition and prototype; coverage metrics for measurement-based WCET analysis; prefetch memory architecture
	WP07	0,24	timing analysis and flow-fact generation; time-predictable memory hierarchies; T-CREST proposal on time-predictable multi-core architectures
TOTAL		**2,80**	
Partner 31 YORK	WP01	0,00	
	WP04	0,00	
	WP05	0,00	
	WP07	0,00	
TOTAL		**0,00**	
Partner 32 IST Austria	WP03	4,74	Modeling and Validation (JPRA);
TOTAL		**4,74**	
Partner 35 Univ Porto	WP01	1,34	Joint work with Mallorca on dependability in adaptive systems; joint work with Aveiro and Malardalen on hierarchical scheduling within Ethernet switches; Joint work with Bilbao and Cantabria on topology
	WP02	0,83	Co-organization of RTN 2011 (sponsoring of keynote and organizers); co-organization of APRES 2011 (sponsoring of keynote, organizers and proceedings); lecture in the Summer School in China; course in
	WP05	1,67	Coordination of the RT Networks activity within the OS and Networks cluster. Organization of NeRES 2011. Setting up wiki. Further developments in the FTT framework (scaling and virtualization);
	WP07	0,94	Partner in the Adaptivity activity. Development and analysis of adaptive mechanisms in hierarchically scheduled Ethernet switches, in beacon management for target tracking sensor networks and in real-time
TOTAL		**4,78**	
Partner 34 TRENTO	WP01	4,22	Travel: Brussels meeting and review for Roberto Passerone and Alberto Sangiovanni-Vincentelli, travel for Alberto Sangiovanni-Vincentelli to Artist summer school
	WP03	1,82	Multiviewpoint modeling, meta-models, modal interfaces, heterogeneous composition, contract models,
	WP07	0,78	Summer school on energy, special section on robustness at SIES 2011
TOTAL		**6,82**	

The following tables show the consumption of manmonth by WP over the four years of the project. It also shows clearly the Y4 consumption.
(Until the 31st of March, 2012, those figures are not finalized.)

WP0 Management of the consortium

		TOTAL	Partner 1 FLORALIS	Partner 2 UJF	Partner 30 Vienna
WP0	Y1:	7,29	6,93	0,36	
	Y2:	7,70	6,49	1,11	0,10
	Y3:	12,64	9,20	3,30	0,14
	Y4:	6,07	6,00		0,07
	Planned WP total:	41,00	34,00	6,50	0,50

The rate of consumption of manmonth for this WP is 82 %.

WP1 Jointly-executed Programme of Integration Activities (JPIA)

		TOTAL	Partner 2 UJF	Partner 4 Aalborg	Partner 5 Aveiro	Partner 6 Bologna	Partner 7 TUBS	Partner 8 Cantabria	Partner 10 DTU	Partner 11 Dortmund	Partner 12 EPFL	Partner 13 ESI	Partner 14 ETH Zurich	Partner 15 IMEC	Partner 16 INRIA	Partner 17 TUKL	Partner 21 MDH	Partner 25 SSSA PISA	Partner 26 Porto	Partner 28 PLU Salzburg	Partner 29 Uppsala	Partner 30 Vienna	Partner 32 IST Austria	Partner 35 UnivdoPorto	Partner 34 TRENTO
WP1	Y1:	17,30	2,38		1,47	0,50		0,01		0,10	0,10	0,41	1,20	5,04	0,75			2,00	2,35	0,45		0,54			
	Y2:	25,16	7,09		0,48	0,50	0,50	0,26		1,00	0,50		3,00	5,04	0,60		2,20		2,00		0,30	1,14	0,05	0,50	
	Y3:	36,52	7,65	11,75			0,50	2,94	0,80	1,00	0,50	0,08		5,00				0,50	0,50	0,10	0,10	1,00		1,50	2,60
	Y4:	15,65				1,00			1,95			0,10		4,81		0,50			0,50			1,23		1,34	4,22
	Planned WP total:	161,45	19,50	6,50	1,95	6,00	2,50	2,50	3,00	3,00	1,50	2,50	11,00	20,00	2,50		6,50	6,00	8,50	2,50	2,50	4,50	1,00	4,00	10,00

The rate of consumption of manmonth for this WP is 59%.

WP2 Joint Programme of Activities for Spreading Excellence (JPASE)

		TOTAL	Partner 2 UJF	Partner 5 Aveiro	Partner 6 Bologna	Partner 7 TUBS	Partner 8 Cantabria	Partner 9 CEA	Partner 10 DTU	Partner 11 Dortmund	Partner 12 EPFL	Partner 14 ETH Zurich	Partner 15 IMEC	Partner 16 INRIA	Partner 17 TUKL	Partner 19 Linkoping	Partner 20 Ulund	Partner 21 MDH	Partner 23 Parades	Partner 25 SSSA PISA	Partner 26 Porto	Partner 27 Saarland	Partner 28 PLU Salzburg	Partner 29 Uppsala	Partner 30 Vienna	Partner 32 IST Austria	Partner 35 UnivdoPorto
WP2	Y1:	9,07	2,35	0,83	0,50		0,10	0,60		0,30	0,10		1,55	0,52					0,06	1,00	0,50	0,25	0,13		0,28		
	Y2:	22,95	10,31	0,38	0,50	1,00	0,74	0,15		2,00	0,05	1,00	1,56			0,55	0,25	0,70			1,41			0,50	1,37	0,05	0,43
	Y3:	18,35	7,20			1,00		0,33		2,00			2,00							1,00	0,50		0,50	1,50	1,92		0,40
	Y4:	8,37			0,95			0,22	1,00	0,63	1,00				0,50					0,50	1,50				1,24		0,83
	Planned WP total:	31,86	12,50	1,21	1,00	1,00	0,84	0,75		2,30	0,15	1,00	3,11	0,52		0,55	0,25	0,70	0,06	1,00	1,91	0,25	0,13	0,50	1,65	0,05	0,43

The rate of consumption of manmonth for this WP is 185%

WP3 Thematic Cluster: Modeling and Validation (JPRA)

		TOTAL	Partner 2 UJF	Partner 4 Aalborg	Partner 9 CEA	Partner 12 EPFL	Partner 13 ESI	Partner 16 INRIA	Partner 22 OFFIS	Partner 23 Parades	Partner 28 PLU Salzburg	Partner 29 Uppsala	Partner 32 IST Austria	Partner 34 TRENTO
WP3	Y1:	6,75	2,59		1,60	0,50		0,75	0,50	0,25	0,56			
	Y2:	28,05	5,60	13,06	3,70	0,25	0,69	1,50	0,50			2,50	0,25	
	Y3:	22,99	8,61	3,00	2,00	1,00	0,20	1,30	0,50		1,00	0,50	2,20	2,68
	Y4:	20,16			13,00		0,10		0,50				4,74	1,82
	Planned WP total:	68,25	16,00	13,00	9,50	2,00	2,50	5,50	3,00	0,25	2,50	6,50	1,50	6,00

The rate of consumption of manmonth for this WP is 115%

WP4 Thematic Cluster: SW Synthesis, Code Generation and Timing Analysis (JPRA)

		TOTAL	Partner 2 UJF	Partner 3 Aachen	Partner 11 Dortmund	Partner 15 IMEC	Partner 21 MDH	Partner 24 Passau	Partner 27 Saarland	Partner 30 Vienna
WP4	Y1:	11,76		2,00	1,00	1,87	3,00	0,76	2,00	1,13
	Y2:	23,13		6,00	6,30	1,92	1,80	1,60	4,50	1,01
	Y3:	24,09	2,09	3,00	6,30	2,00			6,00	4,70
	Y4:	18,33		5,00	6,00	1,50		5,81		0,02
	Planned WP total:	68,00		8,00	18,50	8,00	7,50	7,50	14,50	4,00

The rate of consumption of manmonth for this WP is 114%

WP5 Thematic Cluster: Operating Systems and Networks (JPRA)

		TOTAL	Partner 2 UJF	Partner 5 Aveiro	Partner 8 Cantabria	Partner 15 IMEC	Partner 17 TUKL	Partner 20 Ulund	Partner 25 SSSA PISA	Partner 26 Porto	Partner 35 UnivdoPorto
WP5	Y1:	9,43		1,87	1,53	0,88			2,00	3,15	
	Y2:	7,29		0,54	1,18	0,84		0,25		4,00	0,48
	Y3:	13,37	1,94		3,03	1,00			3,00	2,50	1,90
	Y4:	8,92				1,00	3,00		0,50	2,75	1,67
	Planned WP total:	35,41		2,41	6,50	3,50		2,50	6,00	10,00	4,50

The rate of consumption of manmonth for this WP is 111%

WP6 Thematic Cluster: Hardware Platforms and MPSoC Design (JPRA)

		TOTAL	Partner 2 UJF	Partner 6 Bologna	Partner 7 TUBS	Partner 9 CEA	Partner 10 DTU	Partner 14 ETH Zurich	Partner 15 IMEC	Partner 18 KTH	Partner 19 Linkoping
WP6	Y1:	19,91		1,25	2,50		6,00	3,75	2,31		4,10
	Y2:	39,18		19,50	2,00	2,30	6,00	3,00	2,28		4,10
	Y3:	19,65	1,94	0,66	1,00	1,00	2,80	5,95	2,00		4,30
	Y4:	8,93				1,00	0,43		2,00	1,20	4,30
	Planned WP total:	81,00		21,00	8,50	4,50	16,00	14,00	9,00		8,00

The rate of consumption of manmonth for this WP is 109%

WP7 Transversal Integration (JPRA)

		TOTAL	Partner 2 UJF	Partner 4 Aalborg	Partner 5 Aveiro	Partner 6 Bologna	Partner 7 TUBS	Partner 8 Cantabria	Partner 9 CEA	Partner 10 DTU	Partner 11 Dortmund	Partner 12 EPFL	Partner 13 ESI	Partner 14 ETH Zurich	Partner 15 IMEC	Partner 16 INRIA	Partner 17 TUKL	Partner 19 Linkoping	Partner 20 Ulund	Partner 21 MDH	Partner 23 Parades	Partner 25 SSSA PISA	Partner 26 Porto	Partner 27 Saarland	Partner 28 PLU Salzburg	Partner 29 Uppsala	Partner 30 Vienna	Partner 32 IST Austria	Partner 35 UnivdoPorto	Partner 34 TRENTO
WP7	Y1:	17,13	0,84		0,63	1,25	1,25	3,34	0,24		0,11	0,10	0,83	2,00	1,31			1,40		1,00	1,12	1,00	0,20		0,13		0,38			
	Y2:	21,16	2,34		0,10	6,00	1,50				1,00	0,05	0,47	1,00	1,32			1,40	0,50	0,50			0,35	0,50		2,00	0,75	0,05	0,33	1,00
	Y3:	27,83	5,87	2,00		0,44	1,00	4,20			1,00		0,40	3,60	1,00	0,70		1,50				0,50	0,46		1,00	1,00	1,16		1,00	1,00
	Y4:	18,11								2,00	1,00		0,40		1,25		3,00	1,50	7,00								0,24		0,94	0,78
	Planned WP total:	88,35	9,50	2,00	0,73	7,50	5,00	5,50	2,00	2,00	3,00	0,50	3,50	5,00	5,00	2,00		3,00	2,50	2,50	1,12	3,00	2,50	2,50	0,50	3,00	3,00	2,00	2,50	3,00

The rate of consumption of manmonth for this WP is 96%.

At a project level, 97% of planned manmonth had been consumed over the 4 years of the project.

6. Financial statements – Form C and Summary financial report

A separate financial statement from each beneficiary (FormC) is available on NEF.

A summary financial report which consolidates the claimed Community contribution of all the beneficiaries is provided here (it takes into account Y4 cost + adjustment):

Cost declared Year 4		RTD	MGT	OTHERS	TOTAL
1	FLORALIS	0	33 000	123 842	156 842
2	UJF/Verimag	487 555	42 000	0	529 555
3	Aachen	34 096	0	0	0
4	Aalborg	15 524	0	0	15 524
6	Bologna	60 270	0	0	60 270
7	TUBS	0	0	0	0
8	Cantabria	71 182	0	3 020	74 202
9	CEA	32 583	0	0	32 583
10	DTU	56 591	0	7 159	63 750
11	Dortmund	65 702	0	0	65 702
12	EPFL	11 482	0	0	11 482
13	ESI	14 432	0	0	14 432
14	ETH Zurich	2 111	0	0	2 111
15	IMEC	147 359	0	0	147 359
16	INRIA	47 866	0	7 704	55 570
17	TUKL	71 634	0	0	71 634
18	KTH	86 435	0	0	86 435
19	Linköping	14 052	0	0	14 052
20	ULund	58 536	0	0	58 536
21	MDH	37 292	0	0	37 292
22	OFFIS	21 776	0	0	21 776
24	Passau	37 450	0	0	37 450
25	SSSA-Pisa	44 362	0	0	44 362
26	Porto	8 670	0	408	9 078
27	Saarland	47 520	0	0	47 520
28	PLU-Salzburg	0	0	0	0
29	Uppsala	2 760	0	0	2 760
30	Vienna	28 753	0	0	28 753
31	York	0	0	0	0
32	IST AUSTRIA	43 268	0	0	43 268
35	Uporto FEUP	42 929	0	5 767	48 696
34	TRENTO	48 906	0	0	48 906
	total	**1 641 096**	**75 000**	**147 900**	**1 829 900**

Please note that Floralis received money from the registration on the ArtistDesign summer school 2011. It does not appear in the table above.

Additional details on "other direct costs" (mainly travel expenses) had been provided here:

Partner n°6 Bologna

Travel costs refer to participation to CADS 2010 in Teheran, to a meeting with the University of Pisa in Pisa, to a meeting with STM in Lyon, to ArtistDesign Cluster meeting 2010 in Leuven, to Summer School 2010 in Autrans, to UBICOMM 2010 in Florence, to GLSVLSI 2010 in Providence, to meetings with ST in Grenoble, to DATE 2011 committee in Turin, to Artistdesign Cluster meeting 2010 in Leuven.

Partner n°4 Aalborg

04/09/2011	Aix-Les-Bains - France - Artist Summer school	Kim Guldstrand	€ 1 125,00
06/08/2011	Beijing / Shanghai China. Artist Summer School	Kim Guldstrand	€ 1 838,00
02/02/2011	Brussels - Belgium. Artist Design Review	Kim Guldstrand	€ 1 293,00
27/06/2010	Paris - France,	Alexandra David	€ 904,00

Partner n°8 Cantabria

Who	Place	Date	Why	Price
Michael González Harbour	Brussels (Belgium)	23-24/02/2011	The ArtistDesign Y3 General Assembly	680,85 €
Julio Medina	Grenoble (France), Lund	18-25/03/2011	Conf. M-BED Grenoble 18/03/11, ECRTS in Lund (Sued	3 583,12 €
Iria Estevez (Univ. Carlos III Madrid)	Santander (Spain)	07-08/02/2011	ArtistDesign Time Software Workshop in Santander	345,44 €
Rafael Zamorano (Univ. Politécnica Madrid)	Santander (Spain)	07-08/02/2011	ArtistDesign Time Software Workshop in Santander	258,54 €
José Ismael Ripoll (Univ. Polit. Valencia)	Santander (Spain)	07-08/02/2011	ArtistDesign Time Software Workshop in Santander	510,74 €
Vicente Brocal	Santander (Spain)	07-08/02/2011	ArtistDesign Time Software Workshop in Santander	251,18 €
J. Emilio Salazar Marsá (Univ. Polit.Madrid)	Santander (Spain)	07-08/02/2011	ArtistDesign Time Software Workshop in Santander	172,84 €
Mª Soledad García Valls (Univ. Carlos III, Ma	Las Vegas (USA)	09-12/01/2011	ICCE 2011	2 167,12 €
Prof. Pablo Basanta (Univ. Carlos III, Madrid)	Las Vegas (USA)	09-12/01/2011	ICCE 2011	2 100,91 €
Iria Estevez (Univ. Carlos III Madrid)	Las Vegas (USA)	09-12/01/2011	ICCE 2011	2 043,57 €
Michael González Harbour	Edinburgh (UK)	20-24/06/2011	The Ada Connection Conference	1 389,89 €
Julio Medina	Orlando (USA)	19-28/09/2011	OMG Technical Meeting	2 475,28 €
Juan Rivas	Aix-Les-Bains (France)	04-09/09/2011	ARTIST Summer School Europe 2011	466,37 €
Miguel Tellería	Aix-Les-Bains (France)	04-09/09/2011	ARTIST Summer School Europe 2011	399,89 €
José Javier Gutierrez (colaborador)	Porto (Portugal)	10-11/11/2011	NeRES 2011	689,38 €
				17 535,12 €

Partner n° 10 DTU

Month	Participants	Purpose	Place		Cost DKK	Cost EUR
September 2010	Jan Madsen			WP0	-832	-111,93
February	Jan Madsen	Artist Design Review	Brussels, B	WP0	2543	342,10
February	Jan Madsen	Artist Design Review	Brussels, B	WP0	2618,38	352,24
June	Jan Madsen	TPC Meeting, San Diego	San Diego, USA	WP 2	12872,43	1731,68
June	Jan Madsen	TPC Meeting, San Diego	San Diego, USA	WP 2	8127	1093,29
August	Jan Madsen	Artist Summerchool, Beijing	Beijing, China	WP 2	13750	1849,73
August	Jan Madsen	Artist Summerchool, Beijing	Beijing, China	WP 2	3162,83	425,48
October	Jan Madsen	CODES + ISSS 2011	Taipei, China	WP 2	11094	1492,43
November	Jan Madsen	TPC Meeting, Zurich	Zurich, CH	WP 2	2361	317,62
November	Jan Madsen	TPC Meeting, Zurich	Zurich, CH	WP 2	1848,2	248,63
Total travel cost registered in 2011					57544,84	7741,28

Partner n° 11 Dortmund

Person	Place	Date	Net Amount
Seeker	Edinburgh	01.-31.01.11	466,41
Marwedel	Brüssel	23.-25.02.11	176,77
Holsti	Brüssel	23/02/11	495,35
Marwedel	St. Goar	27.-29.06.11	561,48
Holsti	Porto	04.-07.07.11	605,19
Marwedel	Peking	05.-11.08.11	1 290,11

Partner n°17 TUKL

travel expenses: Fohler: RTSS 2010 San Diego, Artist Meeting Brussels, Research Meeting Houston/USA,ECRTS & Artist Meeting Lund/Sweden, Artist Meeting Bologna/Italy, Artist Meeting Pisa/Italy; Schorr: Artist Meeting Bologna, Summer School Trient/Italy; Pereira: Artist Meeting Bologna/Italy, Summer School Trient/Italy; Ferreira: Artist Meeting Bologna/Italy. Anderson: Reimbursement of travel expenses for a workshop at KL.

Partner n°19 Linkoping

Petru Eles	Project meeting Brussels February 23	1 005 €
Petru Eles	CPS Chicago April 10	2 697 €
Petru Eles	Project meeting Zurich April 27	548 €
Breeta Sengupta	RASDAT 2011 & DELTA 2011	1 730 €

Partner n°22 OFFIS

Travel details:

- Feb 22-24; Brussels; Bernhard Josko; ArtistDesign Year3 Review; 1085, 55€
- Dec 1-3, 2012; Braunschweig; Hardi Hungar; Workshop FORMS/FORMAT2010; 484, 24 €
- Feb. 16-18; Dagstuhl; Hardi Hungar; Seminar MBEES2011; 397, 38€
- March 26 - Apr 2; Rome; Werner Damm; Work together with A. Sangiovanni Vincentelli on contract-based defign; 1608,86 €
- Apr. 1-4; Dagstuhl; Hardi Hungar; Workshop Science and Engineering of Cyber Physical Systems; 165, 35 €
- March 14-16, 2012; Dresden; Bernhard Josko; ArtistDesign Year 4 Review; 700€ (estimated)
- Apr. 10-16; Chicago; Werner Damm; Cyber Physical Systems Week; 5310, 53€

Partner n°25 PISA

331,50	Dott. Franchino in Porto for Workshop Neres 9-11/11/11
337,22	Dott. Marinoni in Torino for AICA 2011 15-17/11/11
365,00	Dott. Della Vedova in Tolosa for RTNS 2010 1-5/11/10
522,80	Prof. Buttazzo in Lund for ECRTS 2011 18-20/03/11
548,98	Dott. Facchinetti in Tolosa for RTNS 2010 1-5/11/10
573,33	Prof. Buttazzo in Chicago for RTAS 2011 6-18/04/11
1 135,06	Prof. Buttazzo in Bruxelles for Review Artist Design 3 22-27/02/11
1 882,00	Prof. Buttazzo in San Diego for RTSS 2010 27/11/10-5/12/10
3 040,26	Prof. Buttazzo in Chicago for Seminario Urbana oltre conf. RTAS 2011

Partner n°30 Vienna

Travel reason	Date	Place	Who	Price
Review meeting, Project workshop	22.-24.02.2011	Brussels, Belgium	Peter Puschner	600,17
DATE 2011 Conference (Session chair); Networkin	14.-16.03.2011	Grenoble, France	Peter Puschner	1 029,01
PC meeting	18.-20.03.2011	Lund, Sweden	Peter Puschner	603,09
ISORC, WORNUS workshop	25.03.-01.04.2011	New Port Beach, USA	Peter Puschner	2 399,99
ECRTS conference	04.-09.07.2011	Porto, Portugal	Benedikt Huber	942,14
ECRTS conference	04.-08.07.2011	Porto, Portugal	Peter Puschner	1 453,84
RTCSA conference	25.08.-02.09.2011	Toyama, Japan	Michael Zolda	1 771,77
ARTIST Summer School	03.-10.09.2011	Aix-les-Bains, France	Benedikt Huber	1 076,36
PC meeting (DATE 2012)	02.-03.11.2011	Zürich, Switzerland	Peter Puschner	489,41
DATE 2012 Conference, Review meeting	March 2012	Dresden, Germany	Peter Puschner	1 500,00

Partner n°32 IST Austria

Datum	Text	An Kategorie Code	Betrag
28/02/2011	ToHe_T_Brussels240211 flight ArtistDesign	TRAVEL	332,45
31/03/2011	ToHe_T_Brussels240211 flight	TRAVEL	140,00
31/03/2011	ToHe_T_Brussels240211 flight	TRAVEL	50,00
31/03/2011	ToHe_T_Brussels240211 parking	TRAVEL	28,50
31/03/2011	ToHe_T_Brussels240211 Taxi	TRAVEL	45,00
31/03/2011	ToHe_T_Brussels240211 Taxi	TRAVEL	45,00
31/03/2011	ToHe_T_Saarbrücken010411 train ETAPS	TRAVEL	64,00
31/03/2011	ToHe_T_Saarbrücken010411 flight	TRAVEL	292,75
31/03/2011	ToHe_T_Saarbrücken010411 train	TRAVEL	95,00
06/04/2011	ToHe_T_Saarbrücken010411 public transp.	TRAVEL	4,80
15/09/2011	DaZu_T_Marktoberd.020811 train	TRAVEL	95,70
15/09/2011	DaZu_T_Marktoberd.020811accom.	TRAVEL	680,00
30/09/2011	DeNi_T_Taiwan091011 flight EMSoft	TRAVEL	1 211,81
26/09/2011	Raluca Halalai Visit QEST 2011 flight, train	TRAVEL	254,72
26/09/2011	Raluca Halalai Visit QEST 2011 accom. + meals	TRAVEL	160,80
30/09/2011	Sriram Rajamani visit IST, taxi	TRAVEL	63,00
24/10/2011	DeNi_T_Taiwann091011 tranps. ES Week	TRAVEL	87,88
24/10/2011	DeNi_T_Taiwann091011 accom. + meals	TRAVEL	224,04
24/10/2011	DeNi_T_Taiwann091011 visa fee	TRAVEL	37,00
07/10/2011	Gregor Goessler Visit IST 09/2011 flight, publ. tr	TRAVEL	417,83
13/12/2011	Serdar Tasiran Visit IST 11/2011 flight+accom	TRAVEL	386,67
30/12/2011	Swen Jacobs Visit IST 12/2011 transp.	TRAVEL	330,30
26/09/2011	UdBo_T_Bergen140911 Flight,transp.	TRAVEL	425,14
26/09/2011	UdBo_T_Bergen140911 accom. + meals	TRAVEL	264,20
26/09/2011	UdBo_T_Bergen140911 accom. + meals	TRAVEL	-264,20
26/09/2011	UdBo_T_Bergen140911 Flight,transp.	TRAVEL	-425,14
31/01/2012	J. Gehrke Visit IST 12/2011	TRAVEL	219,24
31/01/2012	Jan Otop Visit IST 01/2012 train, bus	TRAVEL	119,05
13/03/2012	ToHe_T_Dresden flight	TRAVEL	900,00
13/03/2012	ToHe_T_Dresden ArtistDesign Meeting hotel	TRAVEL	300,00
			6 585,54

Partner n°35 Universidade do Porto

RTD Travel					
1550,28	Mario Sousa	RTSS 2011	Vienna, Austria	29nov-2dec201	work in progress towards a network resource manager based on Linux-TC
773,51	Luis Almeida	Dagstuhl Seminar	Dagstuhl, Germany	2-4nov2011	participation in the Dagstuhl Seminar on Cyber-Physical Systems
510	Moris Behnam	ETFA 2011	Toulouse, France	5-8sept2011	work on the MTU configuration in FTT-SE
560	Luis Oliveira	Artist Summer School in Europe	Aix-les-Bains, France	4-9sept2011	attendance
643,05	Luis Oliveira	RoboCupSymposium	Istambul, Turkey	5-11jul2011	work on self-synchronization in ad-hoc networks of mobile robots and its impact in relative localization
363,48	Farahnaz Yeke	SIES 2011	Vasteras, Sweden	15-17jun2011	work in progress towards scaling FTT-SE to large networks
476,48	Luis Almeida	DATE 2011	Grenoble, France	14-18mar2011	Chairing the E1 topic on Real-Time, Networked and Dependable Systems
733,62	Luis Almeida	ArtistDesign Y3 Review	Brussels, Belgium	22-24feb2011	participation