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on Design for Embedded Systems

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1. Final publishable summary report

1.1 Executive summary

The ArtistDesign NoE is the visible result of the ongoing integration of a community.

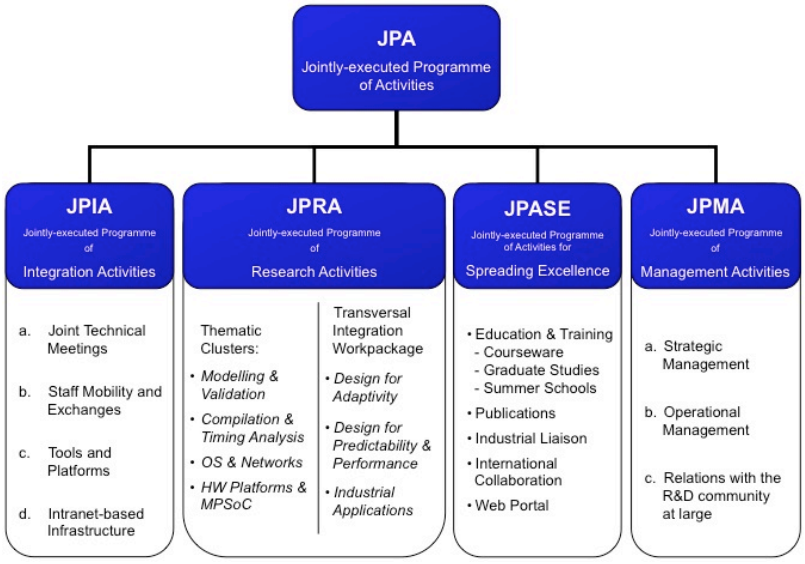
ArtistDesign has been a driving force for federating the European research community in Embedded Systems Design. It brought together 31 of the best research teams as core partners, 15 Industrial and SME affiliated Industrial partners, 25 affiliated Academic partners, and 5 affiliated International Collaboration partners who participate actively in the technical meetings and events.

The central objective for ArtistDesign has been to build on existing structures and links forged since 2001, to become a virtual Centre of Excellence in Embedded Systems Design. This was achieved through tight integration between the central players of the European research community. These teams have already established a long-term vision for embedded systems in Europe, which advances the emergence of Embedded Systems as a mature discipline.

ArtistDesign built on existing international visibility and recognition, to play a leading role in structuring the area.

The research effort integrated topics, teams, and competencies, grouped into 4 Thematic Clusters: “Modelling and Validation”, “Software Synthesis, Code Generation, and Timing Analysis”, “Operating Systems and Networks”, “Platforms and MPSoC”. “Transversal Integration” covering both industrial applications and design issues aims for integration between clusters.

The NoE had a very dynamic International Collaboration programme[2], interacting at top levels with the best research centers and industrial partners in the USA: (NSF, NASA, SRI, Boeing, Honeywell, Windriver, Carnegie Mellon, Vanderbilt, Berkeley, UPenn, UNC Chapel Hill, UIUC, etc) and in Asia (Tsinghua University, Chinese Academy of Sciences, Seoul National University, East China Normal University, etc).



ArtistDesign also had a very strong tradition of Summer Schools and Graduate Schools[3], and major workshops[4].

ArtistDesign has built on existing international visibility and recognition, and played a leading role in structuring the area. It has provided a significant evolutionary step for integrating the leading embedded systems design research teams - both in terms of impact on the overall structuring and lasting integration within the consortium and more generally within the area in Europe.

1.2 Summary description of project context and objectives

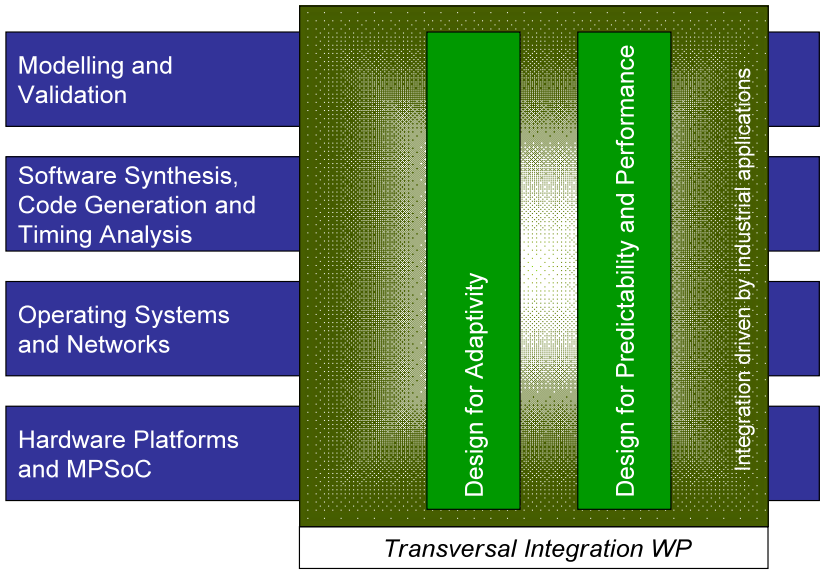
1.2.1 Structure and Vision for the Research Effort

The NoE was composed of intra and inter-cluster research activities on cutting-edge topics in embedded systems design. While the main bulk of financing for these activities was taken up by outside programmes (Integrated Projects, National Programmes, Industrial Contracts, etc), the

[2] http://www.artist-embedded.org/artist/-International-Collaboration,1050-.html
[3] http://www.artist-embedded.org/artist/-Schools-.html
[4] http://www.artist-embedded.org/artist/-Workshops-and-Seminars,29-.html

ArtistDesign NoE financed the extra effort derived from integrating these into a single coherent research programme.

Thus, the essential ingredient within ArtistDesign was the JPRA, which motivated the participating research teams far more than the actual financing, was tiny in comparison with the overall research aims. It was completed by the Joint Programme of Integrating Activities (JPIA), and the Joint Programme of Activities for Spreading Excellence (JPASE), and overseen by the Joint Programme of Management Activities (JPMA).



This design flow was composed of the following cooperating activities, starting with component-based modelling and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality. Accordingly, we have structured the area of embedded systems design into the following topics.

1.2.2 Joint Programme of Research Activities (JPRA): Thematic Clusters

- Modelling and Validation. Unlike other computer systems, embedded systems are strongly connected with a physical environment. A scientific foundation for embedded systems must therefore deal simultaneously with software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based. The overall objective of this activity was to develop model and component-based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. The activity brings together the most important teams in the area of model and component based design in Europe.
- SW Synthesis, Code Generation and Timing Analysis. There was a continuing demand for higher performance of information processing, which stimulates using a growing amount of parallelism (including using multiple processors). This trend affects the design of embedded systems. We address issues related to multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces. Such processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Timing analysis was also affected by the trend toward the new platforms. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Also, timing analysis beyond the single processor was required. Hence, timing analysis will also consider the timing of communication. The overall objective was to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors.
- Operating Systems and Networks. We investigate how current real-time operating systems have to be extended or modified to support emerging real-time embedded systems characterized by a high degree of complexity, highly variable resource requirements and parallel processing such as multicores. Most embedded systems are often characterized by scarce resources in terms of processing power, memory, space, weight, energy, and cost. Hence, another objective was to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, whilst guaranteeing isolation properties. Also, to support dynamic applications with variable resource requirements or to cope with unpredictable resource availability, feedback control techniques for resource management at the operating system and application level are also investigated.

- Hardware Platforms and MPSoC Design. While hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application environments was much less clear. The consequence was fragmentation: while many research teams are working on one or more of these domains, there was little communication and integration, this leads to duplication of results and overall slow progress. The teams involved in this activity have a wide-ranging research experience, which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ArtistDesign will help the participants to the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion.

1.2.3 Joint Programme of Research Activities (JPRA): Transversal Integration Activities

- Design for Adaptivity. An embedded hardware-software system was adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity was increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity was a cross-cutting system characteristic that affects both hardware and software. At the software-level adaptivity was mainly concerned with flexible and adaptive resource scheduling, e.g., CPU time scheduling. At the hardware-level adaptivity includes both adaptation of operation modes, e.g., supply voltage and clock frequency, processor instruction sets, and dynamic management of hardware resources, e.g., processing elements and memory.
- Design for Predictability and Performance. Many applications have strict requirements on timing, and limited resources (memory, processing power, power consumption, etc.). All systems also have increasing demands on (average) performance, which has motivated the introduction of features such as caching, pipelining, and (now becoming very prominent) multiprocessor platforms. Almost all such efficiency-increasing features drastically increase variability and decrease analyzability of response-times, etc. and thus have a detrimental effect on predictability. Since the introduction of new architectural features was inevitable, it was important to: a) develop technology and design techniques for achieving predictability of systems built on modern platforms, and b) investigate the trade-offs between performance and predictability.
- Integration Driven by Industrial Applications. To have a strong impact on industry and society at large, the results of the Thematic Clusters need to be harmonized in an overall design flow that can sustain the embedded design chain from conception of the product to its implementation. The design chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics). Today, there was stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There was a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company.

1.2.4 Joint Programme of Activities for Spreading Excellence (JPASE)

The JPIA activities promote integration of geographically dispersed teams and have long-lasting effects:

- Joint Technical Meetings. These aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.
- Staff Mobility and Exchanges. This is essential for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. Mobility is justified by and refers to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.
- Tools and Platforms. A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

  The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

  ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

  Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

1.2.5 Joint Programme of Activities for Spreading Excellence (JPASE)

The NoE's actions for Spreading Excellence have been at 3 levels:

- Targeted towards affiliated partners Affiliated partners are not core members in the consortium, but receive support for travelling to ArtistDesign meetings, and actively contribute to the implementation of the Joint Programme of Activities (JPA). These affiliated partners include industrial, SME, academic, and international collaboration affiliates.
- Targeted towards the scientific and technical community in the large This is achieved mainly bottom-up through the organisation of scientific events, publications, distribution of tools and components, industrial partnerships (not funded by ArtistDesign), education; and through the ArtistDesign web pages.
- Targeted towards students A particular focus has been placed on the ARTIST Summer Schools this year – with a truly outstanding programme of lecturers, and the innovation of providing the lectures in video form on the Artist website.

1.3 Description of the main S&T results / foregrounds

The main Scientific and Technical results are organized according to the cluster /activity structure described earlier.

1.3.1 Thematic Cluster: Modelling and Validation

Both research activities with the cluster – the *Modeling Activity* and the *Validation Activity* – have progressed substantially within the four years of the project, and with significant synergy between proposed modeling formalisms and methods and validation techniques they support:

Within the sub-activity *Component Modeling,* the main focus was on defining and composing models with heterogeneous semantics. We considered rich models including non-functional issues, architectures and assumptions on the environment (contracts) and corresponding modeling and/or synthesis environments. Some of the most visible achievements on modeling have been obtained by collaboration in multi-partner projects that mostly have evolved from collaborations within ARTIST. In particular, the European projects ACROSS, ATTEST (1 and 2), CESAR, COMBEST and

SPEEDS have been set up due to collaborations in ARTIST and have come up with important results.

Within the sub-activity *Resource Modeling,* we studied the design of resource-constrained systems, where the resource can be quantitative (e.g. energy consumption) or not (e.g. shared memory access). In particular, we considered here problems related to scheduling and resource allocation, to Design Space Exploration and to modeling for performance. The methods and tools developed by the cluster partners have been applied to real-world applications, for example the thermal behavior of an MRI scanner and printers, the Salzburg Helicopter platform, and energy regulation for intelligent buildings.

Within the sub-activity *Quantitative Modeling,* we specifically focussed on design frameworks for quantitative modeling. We have mainly focused on timing and probabilities, but also on multi-valued evaluation. We have in particular also considered the extraction of quantitative properties from non quantitative models, as well as models and theories for non-usual “quantities” such as evolvability, extendability, flexibility and robustness There was an important focus on synthesis.

Within the sub-activity *Compositional Validation* the main focus has been on methods for deriving non-functional properties from properties of their components, with the purpose of developing scalable compositional techniques for performance analysis and verification. Also validation methods based on abstractions and refinements for quantitative models have been developed.

Within sub-activity *Quantitative Validation.* the focus was on design frameworks for quantitative modeling, in particular Markov models, timed automata, priced timed automata, memory models involving stacks and queue and linear hybrid. A main achievement has been the wealth of algorithmic techniques allowing for efficient and scalable validation of formalism whose expressive power was previously out of reach. A particular scalable technique which has emerged is that of statistical model checking which allows several performance properties of very rich models to be established on the basis of simulation *up to a desired level of confidence.*

Within the sub-activity *Cross-Layer Validation* a substantial line of results have been obtained with respect to improved schedulability analysis and WCET analysis supporting multiprocessor and multi-core applications. The methods include WCET analysis and schedulability analysis addressing mixed-criticallity systems including tool implementation using model checking, as well as introduction new task models (e.g. Digraph based) allowing for more scalable and efficient schedulability analysis. Main results within *Cross-Layer Validation* concerns automatic controller synthesis from various rich game models (timed and probabilistic) with possible partial obsevability, and with a number of industrial successful application already having been achieved (e.g. the automatic synthesis of climate control in pig-stable, and synthesis of optimal control of hydraulic pumps). This shows that the distance from fundamental theoretical breakthroughs to industrial impact may be very short. Also, a number of results have been obtained with respect to conformance testing of non-functional properties based on quantitative model. Finally, within the theory of timed automata substantial effort has been made towards the analysis of their robustness: i.e. to what extent does the realization of the model on a non-perfect platform preserve properties already established.

Note that the cluster has organised relatively few closed ARTIST meetings, but we considered more interesting to meet at the margin of conferences and workshops organised by the cluster partners or collaborators from other ARTIST clusters. The organisation activities of the cluster and the intervention of cluster memebers as invited speakers of conferences and summer schools have been quite consequent, as can be seen from the list provided in the activity reports of the cluster.

1.3.2 Thematic Cluster: Software Synthesis, Code Generation and Timing Analysis

The cluster made good progress in all the areas of its scope and also contributed to overlapping and neighboring areas.

For code generation, upcoming MPSoCs were considered to be the major challenge. When the network started, appropriate tools were hardly visible. Given the novelty of the aims and goals, we could not expect to be able to just integrate existing tools. Instead of starting the development of tools from resources of the network, we focused on interfacing the relevant researchers and to reach out to specialists beyond the network, including non-European partners. During the lifetime of the

network, several new tools for this problem were designed, each one with a slightly different goal. At the end of 2011, several tools are available: including DOL (ETH Zürich), Daedalus (Univ. Leiden and Amsterdam), MAPS (RWTH Aachen), Mnemee (IMEC, Dortmund, TU Eindhoven and others), SystemCodesigner (Univ. Erlangen Nuremberg), Hopes (Seoul National University) and a tool from the City University of Hong Kong. In addition, many initiatives support the development of software for multi-core processors. In total, the scene has changed significantly since the proposal of this network was written.

Resource-aware compilation has also seen a good amount of attention. In particular, energy-aware compilation has become one particular aspect of saving energy and has been linked to green computing. In this sense, it has become included in a mega-trend.

While the problem of mapping applications to MPSoCs is not yet completely solved, the next problem in code generation has popped up. General purpose computing on graphical processing units (GPGPU) has been found to offer dramatic potential for an increased performance. Researchers at TU Dortmund have also demonstrated that GPGPU also leads to the corresponding savings in consumed energy (more precisely, in the amount of electrical energy converted into heat). However, GPGPU programming can be rather cumbersome and advanced code generation techniques are required to get around this issue. This does very naturally lead to the necessity for synergies between high performance computing and code generation for embedded systems.

Software synthesis is based on techniques which synthesize software from models in a model-based design environment. Software synthesis, if compared to manually written software, has the potential of providing safer software at a reduced development time. Techniques for software synthesis have been proposed in different communities, not all of which could be included as partners of our cluster. Therefore, we focused on attracting these communities to our workshop on software synthesis. This approach worked well. In 2011, we attracted top researchers to the workshop. More communication between these researchers is still required. We expect more research to be performed in this area in the future.

The cluster has also made good progress advancing the state of the art in timing analysis and timing predictability. In this area, we have achieved significant results for single-core systems with single or multiple tasks. For multi-processor systems, important design principles for ensuring timing predictability have been formulated and are being evaluated. Work on more pragmatic, test-based methods has also progressed significantly.

One of the key achievements is the integration of timing analysis and compilers. In cooperation with AbsInt and Saarland University, TU Dortmund has implemented the WCET-aware compiler WCC. WCC incorporates a tight integration of timing analysis into compiler optimizations. The potential for making standard optimizations WCET-aware has been explored in depth. It turned out that the largest potential is in exploiting the memory hierarchy. It was demonstrated that scratchpads offer a large potential for WCET-improvements, but even WCET-aware register allocation can contribute toward WCET-efficiency. Recent extensions include code generation beyond the TriCore architecture, the support of multi-processing and multi-processors as well as multiple objectives.

The level of collaboration between partners was significant. In addition to collaborative research, tools and prototypes have been developed and tools are integrated. This level of integration is indicative of the successful collaborative structure of the cluster.

In year 1, many teams have analyzed the requirements and started to work. In year 2, initial versions of tools became available. In year 3, these tools have started to see wide-spread use. This use has continued in year 4. Also, several teams extended their scope well beyond the classical code synthesis, code generation and timing analysis areas. Resource aware design, energy efficiency, timing predictability and multi-cores are now found in several application areas and ArtistDesign stimulated this spreading of techniques.

1.3.3 Thematic Cluster: Operating Systems and Networks

The work produced by the cluster since the start of the NoE was excellent. The major benefit of the ArtistDesign NoE was to act as a large research forum, where groups with different expertise had the possibility to interact and collaborate for addressing challenging research problems in the

complex domain of embedded systems. Such a collaborative work produced the following significant results:

- Challenging research issues. Different collaborations took place within the cluster that allowed exploiting complementary expertize available among the partners to address complex problems and propose interesting solutions. This can be assessed by the large number of joint papers produced by the cluster members. Some of the most relevant results achieved so far include:
  - The implementation of a real-time scheduler in the Linux kernel, with a support for resource reservation.
  - A programming framework to support resource reservation of concurrent real-time applications on multi-core platforms, considered by Ericsson for software development in next generation cell phones.
  - The integration of cache-aware analysis and limited-preemptive scheduling (together with the Cluster on Compilers and Timing Analysis) to increase predictability as well as efficiency of safety critical applications. The work has been carried out in collaboration with Airbus (for avionic applications) and Bosch (for automotive systems).
  - The toolset to design, analyse, configure and deploy dense WSNs, in part built within the ARTEMIS EMMON project, including the Open-ZB ZigBee protocol stack and the Z monitor.
  - A middleware and communication protocol for teams of mobile robots that are self-reconfigurable and provide efficient support to intensive interactions and which have been adopted by several teams in the RoboCup Middle Size League.
  - The MAST suite (Modelling and Analysis Suite for Real-Time Applications), which was enhanced with more networking components and analysis, namely for switched networks such as AFDX;
  - A number of communication protocols and tools, developed for improving predictability and adaptivity in (industrial) networked embedded systems.
  - The development of a comprehensive taxonomy for the resources currently used in embedded real-time systems.
- European projects. Several European projects started thanks to the integration activities triggered by ArtistDesign. Examples are FRESCOR; ACTORS, PREDATOR, IRMOS, MORE, INTERESTED, FlexWARE, MADES, S(o)OS, iLAND, RT-MODEL, and HI-PARTES.
- Bridge between Industry and Academia. Several contacts with the industry have been established within ArtistDesign, which contributed to reduce the huge gap existing between the theoretical work carried out in the university and the applications developed by the companies. Example of industries that collaborated with the cluster include Airbus, Bosch, Magneti Marelli, General Motors, Ericsson, Philips, Microchip Technology, Alcatel Lucent, Telecom. A significant effort has been made by the cluster to precisely define a common language between industry and academia.
- Dissemination. The cluster members were deeply involved in the organization of first class conferences and workshops all over the world to disseminate the achieved results. Example of conferences include RTSS, RTAS, ECRTS, CPS Week, RTCSA, ETFA, RTNS, HSCC, Ada Europe, DATE, EmSOFT. From the educational side, a large number of graduate courses, summer schools, workshops, and training laboratory activities have been organized to disseminate the knowledge of the cluster to graduate and PhD students.

1.3.4 Thematic Cluster: Hardware Platform and MPSoC Design

Over the 4 years periode, the MPSoC cluster has continued its efforts to establish an integrated modelling and design methodology that can take into account predictability and efficiency constraints. A major topic has been to involve all current layers with a particular emphasis on a resource-aware design trajectory. In this effort, we have focused on multi- and many-core platforms

and platforms for distributed networked systems. A particular challenge has been to include and handle the concequences of new technological developments, such as 3D chip integration, variability, microfluidic components, and wireless sensors (e.g. for Cyber Physical Systems).

Within multicore SoC architectures the major themes are predictability, Network-on-Chip, programming models and resource awareness. The activities related to predictability have resulted in a better understanding of the subject of shared resource interference in multiprocessor systems, where the competition for e.g. a shared memory leads to a “feedback” on the task timing that breaks the predominant analysis approaches (in which the task timing is investigated in isolation). Open issues and possible improvements on the modelling and analysis approaches of multi-core systems with shared resources have been indentified and discussed with members of the Timing Analysis Cluster. Solutions have been presented that allow circumnavigating this problem in a formal performance analysis. Furthermore, efforts on the applicability of formal scheduling theory to realistic foreseeable industrial architectures (e.g. in the automotive domain) have been investigated. Applying formal methods to realistic use cases generally increases the user acceptance of formal analysis methods. Collaboration among partners has resulted in a number of analysis tools to analyse resource usage and timeliness. A new direction within on-chip network structures is the use of 3D structures that allows the stacking of cores. These new structures need to be captured by the design and analysis tools. A particular challenge is to capture thermal effects, allowing for temperature-aware design methods and tools. Another new research direction for NoC, has been the addressing of fault-tolerance for both transient and wear-out faults. Effort in understanding how to program multicore SoC has been investigated. This covers both programming models and how to use the parallel architectures to support adaptivity, including task distribution and migration. It also includes activities related to memory architechtures and on-chip memory management, resulting in new domain specific memory allocation techniques. There has been an increased focuse on the definition of runtime services for dynamic resource allocation and power management in the context of non-stationary system workloads, which has lead to the definition and design of a software runtime layer for the management of many-core systems. There has been an increasing interest in heterogeneous modelling at the system level which allows for both simulation and formal analysis and a new framework, the ForSyDe multi-MoC (Model of Computation) framework, has been included as one of the new platforms provided by the cluster. Finally, initial exploration of new emerging biochip platforms has been explored. It is expected that one of the next integration steps for SoC is to include capabilities for biochemical analysis and “computation”.

Within distributed architectures the major themes are reliability and fault-tolerance, and resource awareness, in particular energy. The activities related to fault-tolerance have resulted in new techniques where hardware and software tolerance techniques are combined and where hard real-time and soft real-time tasks can coexist gauranteing that hard real-time task will meet their deadlines in case of faults, while soft real-time tasks will experience a graceful degradation. The focus of the resource awareness has focused on the design of wireless sensor networks powered by energy harvesters. Emphasis has been on both node level energy awareness and network level (system level) energy awareness. Results have shown that dynamic adaptation can result in significantly extended lifetime of wireless sensor networks. Modelling and QoS optimization of control applications is a new area of focus which had lead to very interesting work, with good publications.

1.3.5 Transversal Integration activity: Design for Adaptivity

During the four years of ArtistDesign significant results have been achieved in a number of areas of relevance for adaptivity in embedded systems. The majority of the work falls within the general area of adaptive resource management, in particular of CPU resources, but significant work has also been performed in the areas of adaptive networking and adaptive hardware.

A short summary of the some of the highlights of the work can be found below:

- **Scheduling analysis**: Efficient and effective scheduling analysis for fixed priority systems has been developed that allows adaptivity, in the sence of tasks arriving and leaving the system, to be accommodated. The emphasis of this work is to maximise the utilisation of the available resources by adapting near optimal algorithms. Additionally, a new method for allocation and scheduling of parallel tasks in soft-real time systems (multimedia decoding) in

the presence of post-silicon, process and ageing induced variability in a nominally homogeneous target multi-core platform has been developed. In this context an efficient online policy for meeting timing constraints with minimum energy has been proposed and demonstrated.

- **Memory**: Adaptable memory architectures based upon scratchpads for supporting dynamic real-time process loads have been developed, where the control of when data is moved can change with the actual dynamic behaviour of the application.
- **Collaboration frameworks**: An adaptable cooperation-based framework for networked embedded systems with heterogeneous nodes has been developed, which allows constrained devices to cooperate with more powerful (or less congested) neighbors, to meet allocation requests and handle stringent constraints, opportunistically taking advantage of global resources and processing power. Service allocation is performed by time-bounded distributed QoS-aware services, which are able to trade-off computation time and resource usage for the quality of achieved results.
- **Service adaptation**: Techniques have been developed for adapting the service request handling behaviour to the specific requirements of the services in Service Oriented Architectures (SOA). CPU contracts are used to ensure sufficient computation time for dealing with services with special requirements. The framework, which also supports multicore hardware, runs of top of a modified version of the Linux kernel that provides CPU budgets. Related to this techniques have been developed in order to perform quality compositions of services at design and execution time as a means for adaptation of, and decision making on, which services/components to use and how.
- **Run-time resource management**: An adaptive resource manager for distributed embedded systems aimed at multimedia applications, e.g., broadcast management systems, was developed. Considerable savings in power consumption, hardware cost and system size were reported in an industrial case study. Parallel to this a QoS based adaptive resource management system for homogeneous multicore platforms was developed. The approach is based on partitioned CBS bandwidth servers in combination with control and optimization techniques and is executing on top of Linux. The approach is mainly developed for soft real-time applications, e.g. multimedia, modelled with dataflow networks, but has also been applied to feedback control applications. The latter approach has also been extended to network-based video streaming applications (MPEG-2 and MPEG-4) as well as has been ported to Android.

  Related to the above a new method for synthesizing adaptive controllers for real-time applications has been developed. Here algorithms are parameterized by quality levels which impact the QoS and the execution times. The controller computes optimal values of the quality levels online, i.e. values that allow the highest QoS while meeting the real-time constraints. To cope with uncertain execution times a fine-grained controller that is constantly adapting the chosen quality levels depending on the actual time and on a combination of average and worst-case estimates of the execution times is used.
- **Run-time analysis**: A distributed approach for in-system run-time performance analysis of embedded systems has been developed. The embedded analysis engine is complemented by a framework that enables access control and runtime-optimization through the use of distributed algorithms that allow the usage of self-configuration services for self-protecting real-time systems.
- **Sensor networks**: New approaches to adaptive energy management of energy harvesting system using solar cells have been developed. Based on a prediction of the future available energy, the application parameters are adapted in order to maximize the utility in a long-term perspective. A formal model of the corresponding optimization problem has been formulated. The problem is solved using multiparametric programming to precompute the application parameters offline for different environmental conditions and system states. Related to this an optimal algorithm has been derived for scheduling the tasks within the sensor nodes that jointly handles constraints from both the energy and time domain. This is combined with an admittance test that decides for arbitrary task sets, whether they can be scheduled without

deadline violations. The latter is based on the concept of energy variability characterization curves (EVCC) which captures the dynamics of various energy sources.

- **Control techniques**: A new method for optimizing the timing parameters of real-time control tasks in resource-constrained embedded systems has been derived. Also, new feedback scheduling techniques and new event-driven sampling mechanisms have been proposed. The latter results show that adaptive and non-periodic sampling schemes are an interesting new technique for meeting the demands imposed by modern embedded systems.
- **Adaptivity in networks**: Here various ways of adapting a communication channel to varying application requirements or environmental conditions to enhance the efficiency of medium utilization have been proposed. For controlled access networks with isolated virtual channels the guaranteed bandwidth and latency can be adapted online using the Flexible Time-Triggered (FTT) paradigm on switched Ethernet, either with COTS switches (FTT-SE protocol) or enhanced ones (FTT-enabled switch). For uncontrolled access networks, e.g., wireless networks, a method based on a TDMA round that adapts its phase to escape away from interfering traffic while restructuring the round in a dynamic number of slots equal to the current number of active nodes has been developed.
- **Programmable hardware**: A new type of ultra fault tolerant FPGA named the eDNA architecture has been conceived all the way from development of the concept, to the implementation of a prototype, to test in a space related case study NASA JPL.
- **WCET analysis**: Parametric WCET bounds, where the WCET bound depends on the values of certain inputs, can be used in adaptive real-time systems where the scheduling of tasks adapts to external factors such as varying data sizes affecting the running times of tasks. A general method for parametric WCET analysis, which combines a number of advanced symbolic techniques including relational abstract interpretation, counting of integer points in polyhedra, and parametric integer programming has been developed and implemented in the WCET analysis tool SWEET.
- **Reference architectures**: A reference architecture for automotive embedded systems that addresses the needs for flexible and automatic run-time reconfiguration has been proposed. The research focus was the development of technical support in terms of middleware services for a closed adaptation of distributed embedded systems. In addition to the reference architecture an information model of the control paramaters that represent the target system configuration alternatives, environmental parameters, and internal conditions has been defined and a functional design has been performed.

1.3.6 Transversal Integration activity: Design for Predictability and Performance

During the 4 years of ArtistDesign, the technological development in the predictability area has been rather remarkable. Before the start of ArtistDesign, the state-of-the-art was roughly that WCET calculations for some classes of uniprocessors was reasonable well understood, that uniprocessor scheduling was a mature topic. However, many important challenges concerning advanced dynamic architectural and software features, as well as handling of multicores, were not at all well understood. A point of reference is the survey paper by Thiele and Wilhelm (Real Time Systems 28(2-3), 2004).

Research at UNIBO targets methods for realizing predictable and efficient non-preemptive (execution) schedules for multi-task applications in the presence of uncertainties with respect of execution durations. Hard real-time guarantees are provided with limited idle time insertion, by exploiting a hybrid off-line/on-line technique known as Precedence Constraint Posting (PCP). This approach does not require probability distributions to be specified, relying instead on simple and cheaper-to-obtain information (bounds, average values). The method has been tested on synthetic applications/platforms and compared with an off-line optimized Fixed Priority Scheduling (FPS) approach and a pure on-line FIFO scheduler; the results are very promising, as the PCP schedules exhibit good stability and improved average execution time (14% on average, up to 30% versus FPS and up to 40% versus the FIFO scheduler).

One of the key achievements is the integration of timing analysis and compilers. In cooperation with AbsInt and Saarland University, TU Dortmund has implemented the WCET-aware compiler WCC.

WCC incorporates a tight integration of timing analysis into compiler optimizations. The potential for making standard optimizations WCET-aware has been explored in depth. It turned out that the largest potential is in exploiting the memory hierarchy. It was demonstrated that scratchpads offer a large potential for WCET-improvements, but even WCET-aware register allocation can contribute toward WCET-efficiency. Recent extensions include code generation beyond the TriCore architecture, the support of multi-processing and multi-processors as well as multiple objectives.

Another important development is the gradual increase in understanding how to achieve predictability for multicore systems. One of the key issues here is to achieve temporal isolation between logically independent activities. Techniques have been developed for achieving isolation concerning cache utilization (e.g., page colouring, static cache solutions), and for accessing shared buses (e.g., TDMA-like schemes). There has been major progess in terms of analysing the predictability of memory access in multi-core systems. Analysis methods have been developed by combining analytical (real-time calculus) and state-based (timed automata) models. This way, the scalability towards larger application scenarios and more complex computer architectures has been improved. Nevertheless, the scalability of the analysis techniques needs to be improved. Furthermore, some of the proposed solutions are not readily supported by the most common currently available architectures.

A new trend has also emerged towards specific programming languages for time predictability, jointly with dedicated architectures. PRET-C is an example of such languages; it extends C with synchronous constructs to express multi-threading, communication with the environment, pre-emption, and logical ticks (in a manner similar to ESTEREL). Thanks to the synchronous abstraction, PRET-C provides communication through shared variables, such that communications are both deterministic and guaranteed to avoid race conditions. PRET-C can be either executed on a traditional processor, or on a dedicated processor called ARPRET and inspired by the so called reactive processors (processors that were specially tailored to execute ESTEREL programs). The latter solution provides better performances.

1.3.7 Transversal Integration activity: Industrial Integration

Each of the ArtistDesign Thematic Clusters (WP3-WP6) is important per se for advancing the state-of-the-art in embedded system design. However, if we wish to have a strong impact on industry and society at large, the results of the thematic clusters have to be harmonized in an overall design flow that can sustain the industrial embedded design chain from conception of the product to its implementation.

The chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI, Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics).

Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, the system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company. The benefits of these flows and methods are obvious as they provide shorter time to market and better quality designs but require a will of the industrial segment to work together towards this goal. In the automotive domain, Autosar is an excellent step in that direction. Other industrial segments are less cohesive in searching for a unified approach to design. In addition, society concerns such as energy, health and environment conservation, are offering new business opportunities for emerging technologies such as wireless sensor networks. The difficulty in these new opportunities resides in lack of standards and of experience with new communication concepts and, last but not least, in security.

We believe that all the thematic clusters bring something important to all industrial segments, but we need to pay attention to the way the results obtained by the clusters are formulated. Integration is a matter of modelling and providing interfaces that guarantee that the properties of the components are maintained after integration. Integration takes two forms: an horizontal one where different IPs coming from different companies or from different design groups in the same company have to be assembled; a vertical one, where the requirements are clearly and possibly formally communicated from a higher level player to a lower level one and where the information about the capabilities and limitations of the IPs are unambiguously communicated from the lower level to the higher level. The ultimate goal of this activity is to provide the “meta rules” according to which the design transformations are carried out and interfaces are built and hence to provide strong guidance to the clusters to make their results more relevant and applicable. Understanding the roles and dynamics of an existing, well-established, vertical industrial segment is a complex task. We could only imagine the complexity of industrial segments that are coming together in these years. While we do target some industrial domain to be the driver for this activity, we understand that our research is going to be more relevant and better quality if we can distil some common traits of these domains and work with those to choose at a later date which particular chains to address.

The transversal activity hence has two prongs:

- to dive into particular vertical industrial segments and package design methods out of the thematic cluster results for the segments;
- to identify some important common features among verticals and work towards developing methods to address these topics.

We note that the two concerns that are also part of the Transversal JPRAs (predictability and adaptability) are common to almost all industrial concerns: For this reason, they provide a framework to start the work on integration driven by industrial applications. Predictability has been a goal since the beginning of the modern industry: predicting the capabilities of existing components allows companies to come to market faster with new products and prevents taking dead ends; predicting the effort needed to develop parts of the design and their correct integration prevents early recalls and associated costs. The faster is the dynamics of the industry, the more important is to have predictability in design.

Adaptability is the property of a design to be adapted to changing environments and working conditions. Reconfigurability, programmability, dynamic restructuring are all facets of adaptability. Novel approaches to communication could benefit greatly from adaptability. In fact, much research is being carried out to design devices that could sense available bandwidth and adapt the communication protocol to the most convenient band at the time.

We believe that it will be eventually easier to compose the vertical design industrial flows once these two sub-flows have been examined and results obtained. In addition, being generic concerns they do not require effort from the academic partners to understand the modus operandi of entire industrial segments and offer a shorter time to results.

The vertical industrial segment motivated prong will begin by bringing up-to-speed the largest possible number of participants to the logic of the design chain by organizing workshops for discussion with the participants to the chain.

We proposed at the onset of the activity to target Automotive, Nomadic and Health Applications as potential vertical segments where we have a range of maturity from well-established (automotive) to emerging (health). At the 2008 meeting in Rome of the ArtistDesign partners, the three vertical markets of interest were identified as:

Automotive/avionics since we noted a strong similarity in the overarching issues faced by these two industrial segments that are driven by safety concerns and have to consider distributed implementations;

Health applications with particular emphasis on equipment design and manufacturing and a new thrust in the use of emebedded system design methodologies to synthetic biology;

Energy efficient buildings, a novel field of great interest to the European Community as well as to the rest of the world as 30% of energy consumption is considered to be in commercial buildings.

These applications address an established area of excellence of European Industry where international competition is fierce, an area of growth where again European Industry has a strong position but where the dynamics are fast and new applications are envisioned in strategic areas such as elderly care, and a new area with great potential where energy conservation concerns are going to place a great political emphasis. In addition, we believe that synthetic biology is going to have a fundamental role for the foreseeable future in the definition of new organisms to foster the creation of new drugs as well as new materials. Given the nature of this work, the main participants in the cluster are the groups that have industrial vocation such as ESI, OFFIS, and IMEC.

1.4 Main events and publications organised

The ArtistDesign High-level Events were intended to gather together the very best world-leading experts from academia and industry, to discuss progress on the state of the art, relevant work directions.

The complete lists of events organised are available here:

- **Schools and seminars** http://www.artist-embedded.org/artist/-Schools-and-Seminars,59-.html
  The NoE organized 22 specific schools and seminars.
  This does not include those organised under the earlier Artist2 NoE.
- **International Collaboration events**
  http://www.artist-embedded.org/artist/-International-Collaboration,82-.html
  These are events having a significant impact beyond Europe's borders.
- **Workshops** http://www.artist-embedded.org/artist/-Workshops,29-.html
  (some overlap with the international collaboration events)
- **Education** http://www.artist-embedded.org/artist/-Transversal-topics-in-Embedded-.html

The most important events were the ARTIST Summer Schools in Europe, China, and South America, as described below.

1.4.1 ARTIST Summer Schools in Europe (2009 2010 2011)

http://www.artist-embedded.org/artist/-ARTIST-Summer-School-Europe-2011-.html

The ArtistDesign European Network of Excellence on Embedded Systems Design has organized the 5th through 7th edition of it's highly successful "ARTIST Summer School in Europe" series - funded by the European Commission. These yearly schools on embedded systems design, initiatied in the first ARTIST project, were meant to be exceptional in terms of both breadth of coverage and invited speakers.

These were the largest such schools in the world for embedded systems design (120 participants in 2010), and each year gathered some of the top researchers from Europe, the USA, and Asia.

The schools brought together some of the best lecturers from Europe, USA and China in a 6-day programme, and was a fantastic opportunity for interaction. The 2011 edition was held in beautiful Aix-les-Bains, near Grenoble - France.

1.4.2 ARTIST Summer Schools in China (2009 2010 2011)

http://www.artist-embedded.org/artist/-ARTIST-Summer-School-in-China-2011-.html

The ArtistDesign European Network of Excellence on Embedded Systems Design has organized the highly successful "ARTIST Summer School in China" series - funded by the European Commission. 2011 was the sixth edition of these yearly schools on embedded systems design.

The school was open in priority to Chinese students. We believe that this will open opportunities for collaboration with Chinese research teams. The school offers a full week consisting of in-depth tutorials on state-of-the-art techniques for the design and analysis of embedded systems given by leading experts.

We aimed to provide a forum for young professors, lecturers, researchers, postgraduates (advanced master and PhD students) working in embedded systems as well as engineers from industry with practical background with the development of embedded systems.

Participants were selected according to their CVs submitted to the organization committee. Programme and Lecturers Top European lecturers from the ArtistDesign European Network of Excellence will provide a world-class programme.

1.4.3 ARTIST Summer Schools in South America (2009 2010 2011)


http://www.artist-embedded.org/artist/-ARTIST-SummerSchool-SouthAmerica-.html (2009)

http://www.artist-embedded.org/artist/-ARTIST-Summer-School-South-America-.html (2010)

The ARTIST Summer School in South America has strengthened the cooperation between Europe and South America in the area of embedded systems, both at educational and research levels. For this purpose, the goal of the school is to provide state-of-the-art courses on embedded systems oriented towards advanced students and young researchers. It should also provide a pleasant atmosphere for research-related discussions among the participants.

1.4.4 Publications

The ArtistDesign community is extremely active in publishing in scientific journals and conferences, and these seem seem to be a reliable measure of integration and building excellence between the

partners. In the annual deliverables on Spreading Excellence, there are approximately 80 pages of references to joint papers published in leading journals by the partners over the course of the NoE.

1.5 Impacts on Key Conferences

The ArtistDesign NoE has had a very significant impact on the main international conferences in the area, most specifically :

- ES Week (http://www.esweek.org/) – The vast majority of General Chairs for ES Week in the last 10 years have been members of the ArtistDesign NoE.
- CPS Week (http://www.cpsweek.org/) – CPS Week is the main research conference for Embedded Systems in the USA. The level of interaction has been fantastic.
- RTSS (http://www.rtss.org/) - RTSS is a major conference in the area, which has been continuously organized by ARTIST members since the start of the NoE.

A fairly complete reference to all active conferences in the area is available on the EMSIG webiste: http://emsig.embedded-systems-portal.org/links/es-conferences/

1.6 Other Impacts

Dissemination efforts were structured arounf the Joint Programme of Activities for Spreading Excellence (JPASE) part of the NoE's workplan. Our actions for Spreading Excellence were at 2 levels:

- *Targeted towards affiliated partners* Affiliated partners are not core members in the consortium, but receive support for travelling to ArtistDesign meetings, and actively contribute to the implementation of the Joint Programme of Activities (JPA). These affiliated partners include industrial, SME, academic, and international collaboration affiliates.
- *Targeted towards the scientific and technical community in the large* This is achieved mainly bottom-up through the organisation of scientific events, publications, distribution of tools and components, industrial partnerships (not funded by ArtistDesign), education; and through the ArtistDesign web pages.
- *Targeted towards students* A particular focus has been placed on the ARTIST Summer Schools this year – with a truly outstanding programme of lecturers, and the innovation of providing the lectures in video form on the Artist website.

Regarding Scientific events, we distinguish between conferences and workshops, schools, and high-level events mainly for International Collaboration.

1.6.1 Tools and Components

The ArtistDesign community plays a leading role in the distribution of software tools and components, on verification/validation tools. Some tools are distributed free of charge, such as UPAAL, IF. Others are commercialised, such as AbsInt, SymTA/S. For many other tools used in the platforms, and shared between the Artist partners, a common dissemination policy has not yet been defined.

1.6.2 Industrial Liaison

ArtistDesign has a wide array of affiliated industrial and SME partners (see the Thematic and Transversal Activity deliverables). Most of these partners have participated in some way in the ArtistDesign technical meetings and the overall effort. There is strong, high-level industry participation through the various Spreading Excellence events organised by ArtistDesign. Our active involvement in the European Technology Platform ARTEMIS also could have a significant and long-term impact.

We believe that the strong involvement of four main ArtistDesign partners in the SPEEDS Integrated Project has a very positive impact on progress in the state of the art, in component-based embedded systems engineering.

1.6.3 Affiliated partners

Affiliated partners are not core members in the consortium, but receive support for travelling to ArtistDesign meetings, and actively contribute to the implementation of the Jointly-executed Programme of Activities (JPA). These affiliated partners include industrial, SME, academic, and international affiliates.

1.6.4 Interaction with the Scientific and Technical Community in the Large

Interaction with these other scientific communities is achieved mainly bottom-up through the organisation of scientific events, publications, distribution of tools and components, industrial partnerships (not funded by ArtistDesign), education; and through the ArtistDesign web pages.

Our sponsoring policy aims specifically at enforcing integration of existing scientific events in the area. This is sought in particular through the Embedded Systems Week (http://www.esweek.org/), in which we play a crucial role.

Another concrete example is our action within the DATE conference (http://www.date-conference.com/), in which we are working to shift the emphasis towards becoming the central European conference on embedded systems design, in collaboration with the ARTEMIS European Technology Platform.

Regarding Scientific events, we distinguish between conferences and workshops, schools, and high-level events mainly for International Collaboration.

The ARTIST community now clearly leads the initiatives for organizing the most significant conferences in the area. In Europe, it has a very strong presence in the DATE conference, which is becoming the main conference on embedded systems within Europe. Over the past 10 years, 9 general chairs of DATE have been leading ARTIST members.

Artist partners are also active members of the ACM's SIGBED, and the IEEE's upcoming Special Interest Group on Embedded Systems currently being set up. Artist members actively work for structuring international events on embedded systems.

1.6.5 International Collaboration

International Collaboration has been one of the central activities pursued within ARTIST since 2003, and is described in detail in this document.

All of the recurring ARTIST International Collaboration events have continued and been expanded within ArtistDesign in 2011. Further details about the schools are available in the section "Organisation of Schools".

1.6.6 Industrial Liaison

ArtistDesign has a wide array of affiliated industrial and SME partners, as described in the deliverables' "Affiliated Partners" sections. Most of these partners participate in some way in the ArtistDesign technical meetings and the overall effort. There is strong, high-level industry participation through the various Spreading Excellence events organised by ArtistDesign.

Our active involvement in the European Technology Platform ARTEMIS also could have a significant and long-term impact. Several ArtistDesign partners, including VERIMAG, BOLOGNA, OFFIS and TU Vienna, are actively involved in the ARTEMIS ETP. The ArtistDesign Strategic Management Board was actively consulted for finalizing the 2011 release of the ARTEMIS Strategic Research Agenda.

In addition, each ArtistDesign partner has an outstanding track record for interaction with industry. Globally, the ArtistDesign consortium has a very strong impact on European R&D in embedded systems. This impact is visible via the achievements in Integrated Projects and STREPs (see below).

1.6.7 Sustainable integration: transfer of selected ARTIST activities to EMSIG

Some of the more important initiatives within the Spreading Excellence effort will continue through the newly-created EMSIG (Embedded systems Special Interest Group: http://emsig.embedded-

systems-portal.org/) chaired by Peter Marwedel, TU Dortmund. EMSIG is created within EDAA (http://www.edaa.com/) the permanent structure that handles the DATE conference. Most notably, it aims to:

- leverage on the ArtistDesign NoE results
- help to structure the Embedded Systems Design community
- identify areas of future research and development
- interact on a high level with industry, funding agencies, and other world-class structures
- support the advancement of state of the art embedded systems design approaches
- facilitate the exchange of ideas and knowledge in embedded systems design
- provide visibility and dissemination (eg: web hosting for events), projects
- support the creation of project consortia
- spread knowledge in embedded systems design
- support the application of embedded systems technology

Shift to the EMSIG website is ensured, by providing links within the NoE website to the equivalent sections on the EMSIG website, and a permanent link on all the NoE website's pages (indicated in red) points to the EMSIG website. We will also make regular announcements to the worldwide Embedded Systems community about EMSIG's activities, and referring to ARTIST NoE as needed.

The ARTIST Summer School is also continuing beyond ARTIST, with support from Nano-Tera (EPFL): http://emsig.embedded-systems-portal.org/links/summer-schools#1027

The integration achieved between tools developed by the ARTIST partners will also provide a basis for continuing integration in the longer term.

1.6.8 Publications / impacts on conferences

These include :

- The DATE conference (http://www.date-conference.com/), which has drawn a very large proportion of its General Chairs from the ARTIST NoE's prominent members.
- The CPSWeek conference (http://www.cpsweek.org/), with very tight links to the NoE
- Prof. Peter Marwedel's authoritative book "Embedded Systems Design" (http://www.springer.com/engineering/circuits+%26+systems/book/978-94-007-0256-1) This is part of a larger book series at Springer on Embedded Systems: http://www.springer.com/series/8563?detailsPage=titles

1.6.9 ArtistDesign Web Portal

The ArtistDesign Web Portal was a major tool for Spreading Excellence within the Embedded Systems Community. Its aim was rather ambitious: to be the focal point of reference for events and announcements of interest to the embedded systems community.

The web portal disseminates information about contacts (ArtistDesign core and affiliated partners), the ArtistDesign JPA activities, as well a fairly thorough set of links to sites of interest to the embedded systems community.

As can be seen, a great deal of effort has been put into the web site, both for ergonomics / graphical quality, as for the contents.

The web site includes several features that help keep it coherent and up to date:

Authorised users (principally, the ArtistDesign partners) can access the back end of the site to modify and update information directly. The changes are immediately visible on the site, which greatly streamlines the updating process.

It's possible to track changes and go back to previous versions of individual web pages.

Events are automatically sorted by date, and transferred to 'Past Events'. When appropriate.

Structural information (hierarchy of pages) was maintained automatically.

Ergnomics are set for the entire site. The "look and feel" of the site was always homogeneous thoughout the site. It's possible to change these ergonomics, and these changes are applied homogeneously throughout the site, via automated machanisms.

1.7 ArtistDesign vision for the Future

While significant progress has been achived during the lifetime of the ArtistDesign NoE, huge amounts of research work are still needed. This work has to be seen in the context of a growing number of products and systems which are based on the integration of information processing and the environment. Emphasizing the physical aspects of the environment, such systems can be called cyber-physical systems (CPS). Models of cyber-physical systems are expected to be more comprehensive than those of current embedded systems, since they will also comprise models of the environment. Such models will also need to take a closer look at the interface between the analog and the digital world, since the state of the art in this area still leaves many issues open. For example, control theory needs to take a closer look at the implications of discretization.

Verification needs to take a closer look at the implications imprecise measurements of physical quantities and the resulting imprecision for meeting specifications. Verification techniques for hybrid systems will also have to be extended. Due to the complexity of future systems, formal verification techniques are required. Neverthesless, powerful simulation capabilities for complex systems are also required.

Future systems will have to be designed from components. Otherwise, required time-to-market, safety- and reliability targets cannot be met. Compositional design is therefore mandatory for future design methodologies. Compositional design has to be complemented by synthesis techniques. Synthesis techniques can replace error-prone techniques for example for software design.

Major applications can be expected in the transportation, energy, fabrication, health, smart home, military and consumer sectors. In the past, many concepts could be applied to a large variety of application areas. Future work will also have to look closer at the particular features of the different application areas. In particular, safety and security constraints may be different for these areas.

A large number of future systems will go beyond the integration of physics and information processing. Biophysical systems and physical chemistry will also be integrated with information processing, leading to a fresh look at varios aspects of science.

A reduction of the conversion of various form of energy into thermal energy is expected to remain a mega-trend. It will impact all levels and phases of product design and use. Increasing prizes of gas and oil and restricted availability of raw materials will have an impact on the entire life cycle of CPS products.

Achieving predictable timing is expected to remain an issue, particularly in the presence of multi-core systems and best-effort oriented communication.

The design of future CPS has to take requirements of the users and the community into account. The consideration of technical feasibility has to be complemented by a detailed analysis of the needs of the society. Implications on communities and the environment have to be considered. Safety, security and privacy will be difficult to guarantee in distributed environments with billions of devices of all kinds. Dependability is expected to grow in importance, due to the increasing dynamism and openness of embedded and cyber-physical systems. Increasing fault-rates of hardware components, resulting from decreasing feature sizes, will contribute to this growth. The increasing complexity of systems will also provide a challenge for the design, verification, test and operation of systems. It will be necessessary for systems to achieve a certain level of error resilience, possible resulting from self-organization.

The competitiveness of companies around the globe will depend crucially on the availability of the know-how and skills related to such CPS. The importance of CPS has already been recognized in many parts of the world. In the US, the National Science Foundation (NSF) has started a large project in the area. China is also investing heavily into CPS. For the ArtistDesign community, it will be essential to retain its momentum in order not to loose grounds against these younger initiatives. Also, it will be important continue the close cooperation established in the ArtistDesign network. Without such cooperation, there would be the danger of a new fragmentation. Such cooperation is likely to become more transcontinental than it has been ever before. Mechanisms for supporting transcontinental cooperation also also needed.