Year 4 Review
Dresden, March 16th, 2012

Cluster

Achievements and Perspectives :

Software Synthesis, Code Generation and Timing Analysis

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TU Dortmund

High-Level Objectives

- Limitations of increasing clock speeds any further
  ☞ focus on using MP platforms, in particular MPSoCs
  - increased importance since proposal writing
  - industrially relevant for many sectors (automotive, consumer, ..)

  Different from situation for PCs / data centres: Multiple applications, heterogeneous processors, and multiple objectives
- Efficient design
  - e.g. energy efficiency, especially relevant for portable devices
- Software synthesis also in the scope
  - e.g. workshops on software synthesis
- Coordination with other projects

High-Level Objectives and Vision

- Timing predictability becoming a major issue
  - especially for cyber-physical systems
  - including industrial sectors such as automotive, avionics, railways
  - increasing importance during lifetime of the project
- MP platforms pose threats to timing predictability;
  - develop MP/MPSoC design principles for maximal predictability
  - develop models/methods for timing analysis of parallel software
  - no sound timing-analysis method exists for available MP designs
- Partners contribution to transversal clusters
  (e.g. for predictability: WCC)

All objectives are expected to be very important in the future as well.

Integration Achieved

in the area, in Europe

- Established community working on mapping to MPSoCs
- Linked experts working on various aspects of software synthesis
- Strengthened cooperation of timing analysis community
  - Several joint projects
  - Tool vendors heavily involved
- TU Dortmund demonstrated the integration of compilers and timing analysis and can be considered leading this research area.
- Resulting tools can be interfaced to standard industrial tools since we are using standard languages (e.g. C)

Building Excellence

- Rheinfels workshop, St. Goar, June 2008/09/10/11
- TA meetings, Tutorials, Summer schools, Teaching at ALARI
- WESE, WSS, WCET Workshop, WCET Challenge, ...
- Publications: 80 (20 joint)
- Textbook, slides, video recorded lectures (http://ls12-www.cs.tu-dortmund. de/daes/daes/mitarbeiter/prof-dr-peter-marwedel/embedded-system-text-book/slides/slides-2011.html)

Language	First Edition (first printing)	First Edition (second printing)	Second Edition
English	 Kluwer 2003 Downloads	 Springer 2006 Downloads	 Springer 2011 Downloads
German	 Springer 2007 Downloads	 Springer 2007 Downloads	(in preparation)
Chinese 中文	 Science Publishers 2007 Downloads 勘误表		Contract signed last week
Macedonian македонски јазик	 Ad Verbum АД ВЕРБУМ 2010 Downloads		
Greek ελληνική γλώσσα			(in preparation)

Quantified information (as requested)

- Contract with Chinese publisher to publish 3000 copies signed last week
- ~500 physical copies and ~1400 e-books sold in 2011
- 1150 slides
- 9 hrs 50 mins of recorded lectures
- 2060 accesses to videos between May 2011 and Jan. 26th, 2012

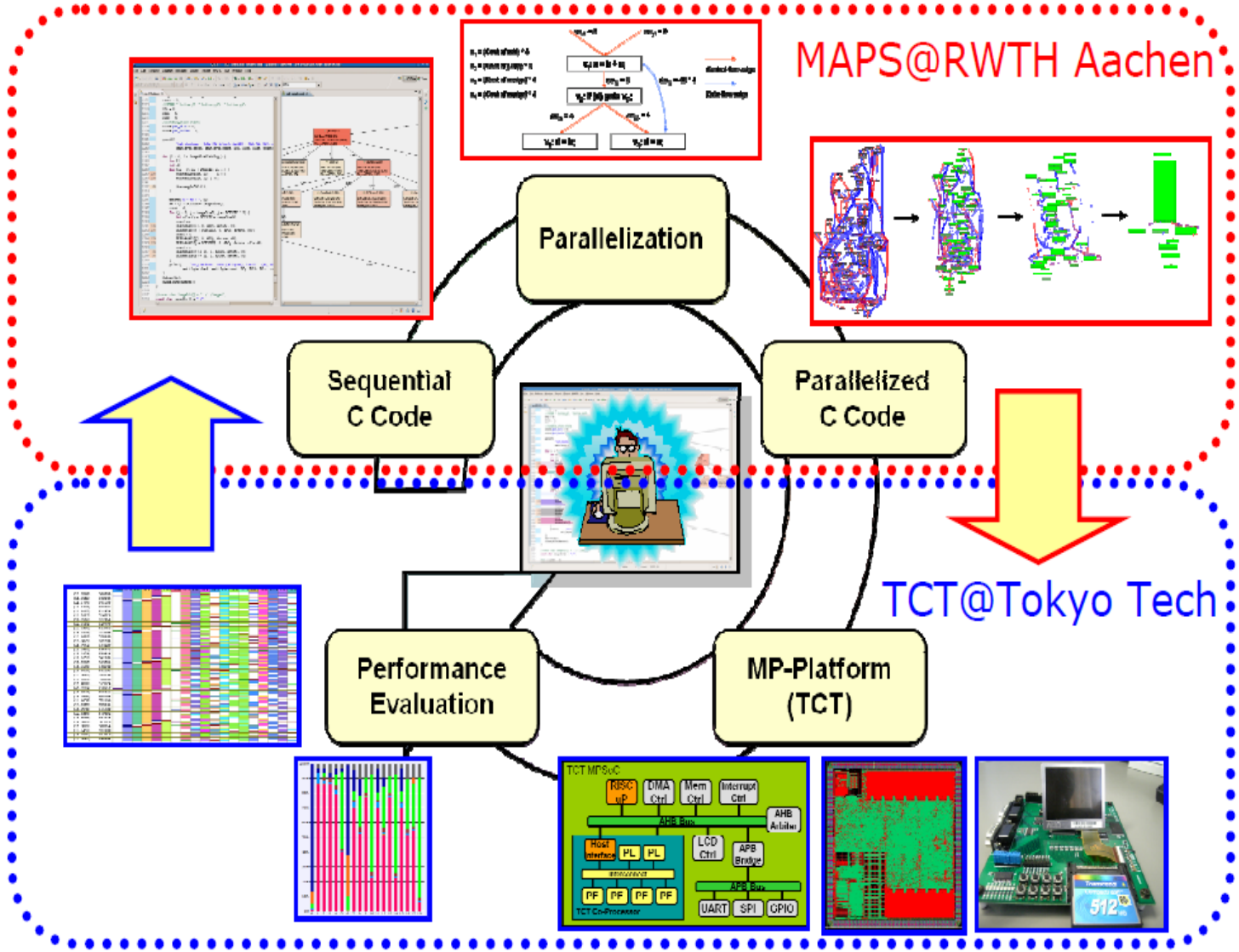
Author	Title	Published	Citations
Wayne Wolf	Computers as components: Principles of Embedded Computing Design	2001 & 2008	387
Frank Vahid	Embedded System Design: A Unified hardware/software introduction	2002	306
Peter Marwedel	Embedded System Design (1st & 2nd ed.)	2003 & 2011	276
Daniel Gajski	Embedded System Design: Modeling, Synthesis and Verification	2009	34
Edward Lee	Introduction to Embedded Systems: A Cyber-Physical Systems Approach	2011	14

Scientific Highlights: Mapping to MPSoCs

Several tools for mapping applications to MPSoCs have become available

- MAPS (RWTH Aachen)
  Huawei has consulted RWTH Aachen to develop a 3-years technology roadmap on their MPSoC programming flow. The roadmap was tailored to future directions for Huawei wireless products.
- MPMH/Mnemee-Integration (IMEC, Dortmund, Eindhoven, Athens)
- SystemCoDesigner (U. Erlangen-Nuremberg)
- Daedalus (U. Leiden)
- HOPES (Seoul National University)

MAPS-TCT Framework



Rainer Leupers, Weihua Sheng: MAPS: An Integrated Framework for MPSoC Application Parallelization, *1st Workshop on Mapping of Applications to MPSoCs, Rheinfels Castle*, 2008

Found the interest of users …

MAPS

MUG 2011

1st MAPS User Group Workshop

September 28-29, 2011

UMIC Research Centre, Aachen, Germany

Software Analysis & Transformation

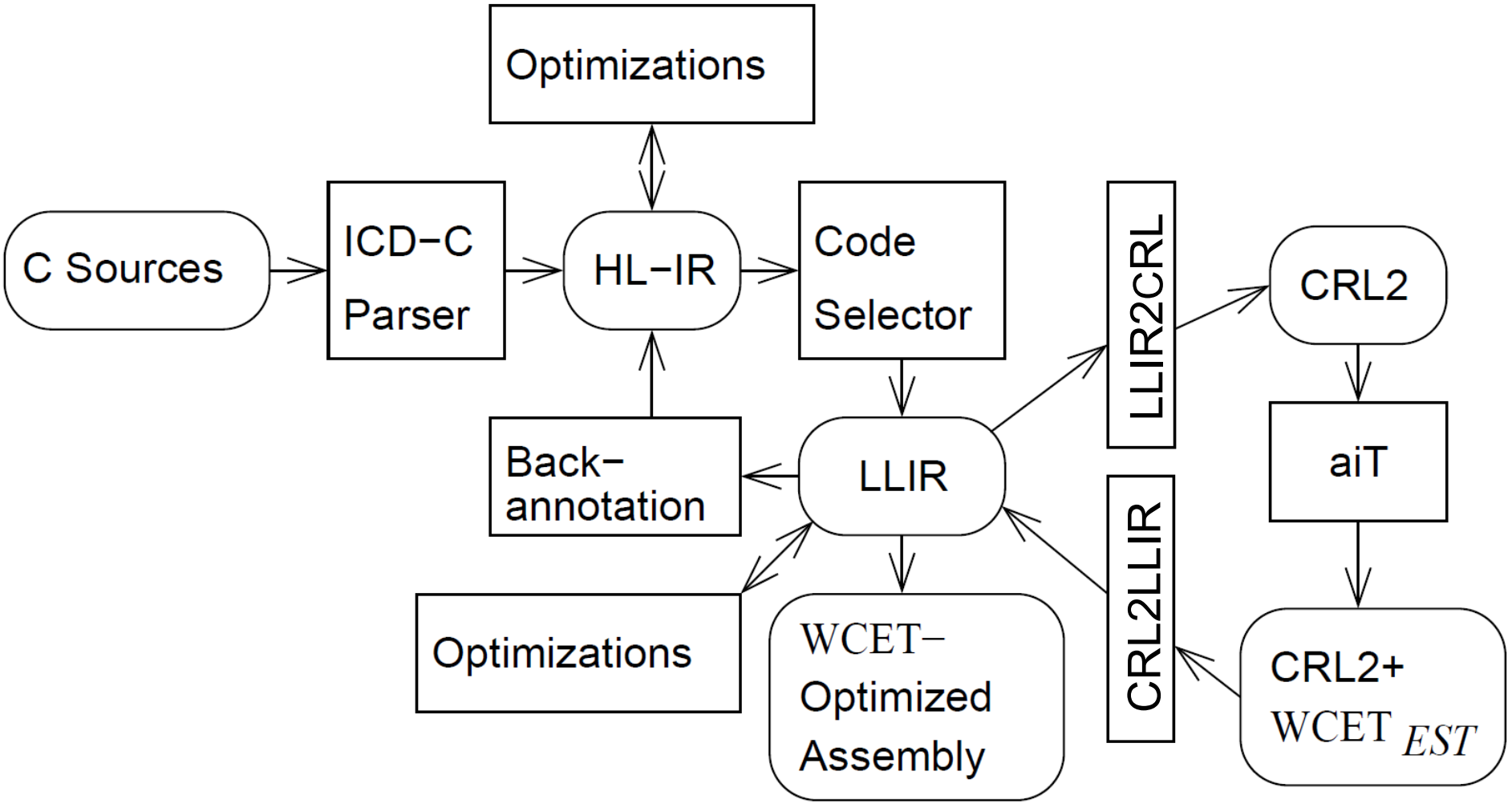
IMEC

- MH parallelization assistant

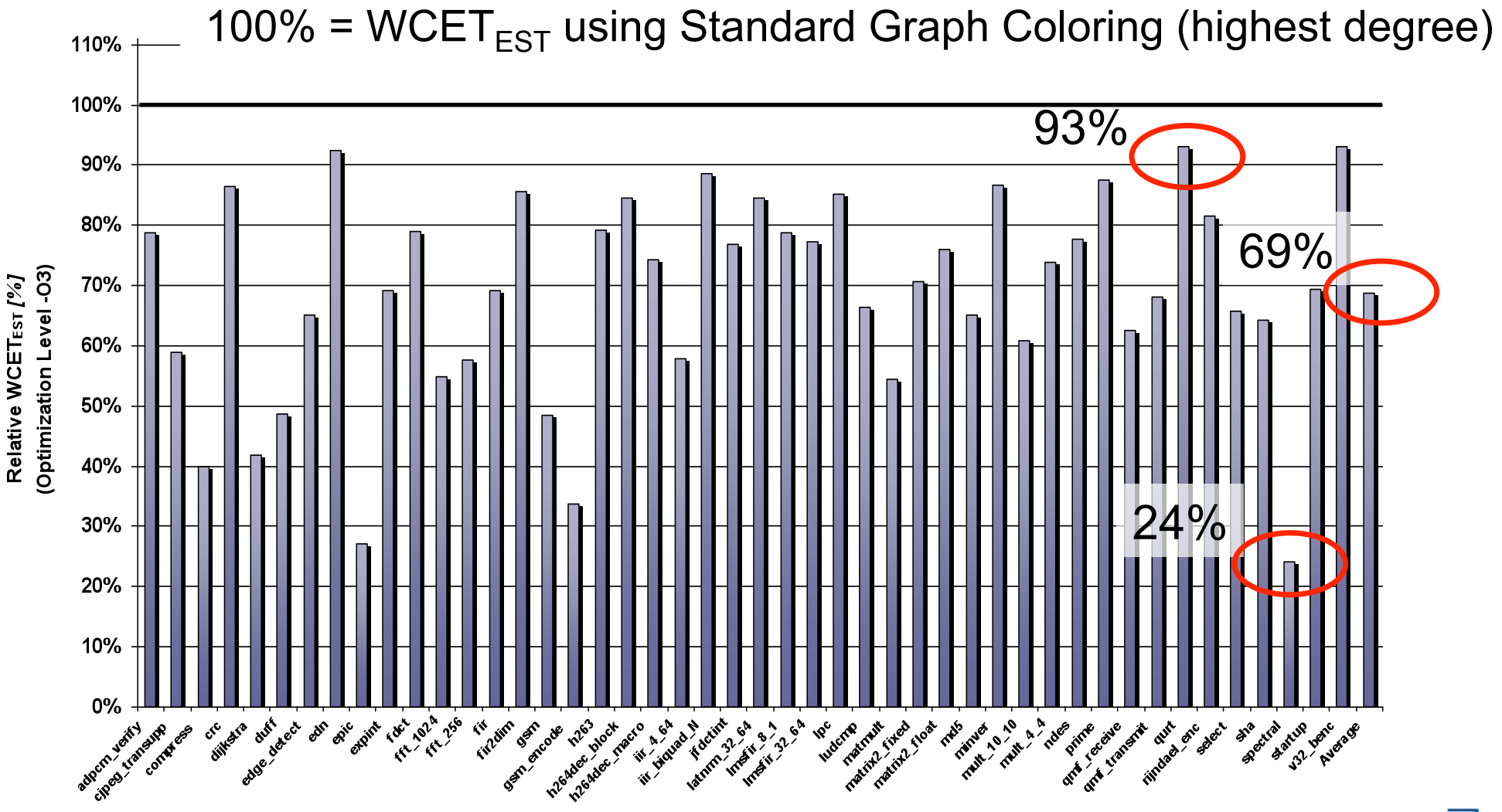
U. Passau

- Establishment of the polyhedron model for loop parallelization with several entries in the Encyclopedia of Parallel Computing, September 2011
- First steps of making the polyhedron model multicore-ready (polly.llvm.org)
- Moving the polyhedron model further towards practical embedded systems

Structure of WCC (WCET-aware C-compiler)



Register Allocation

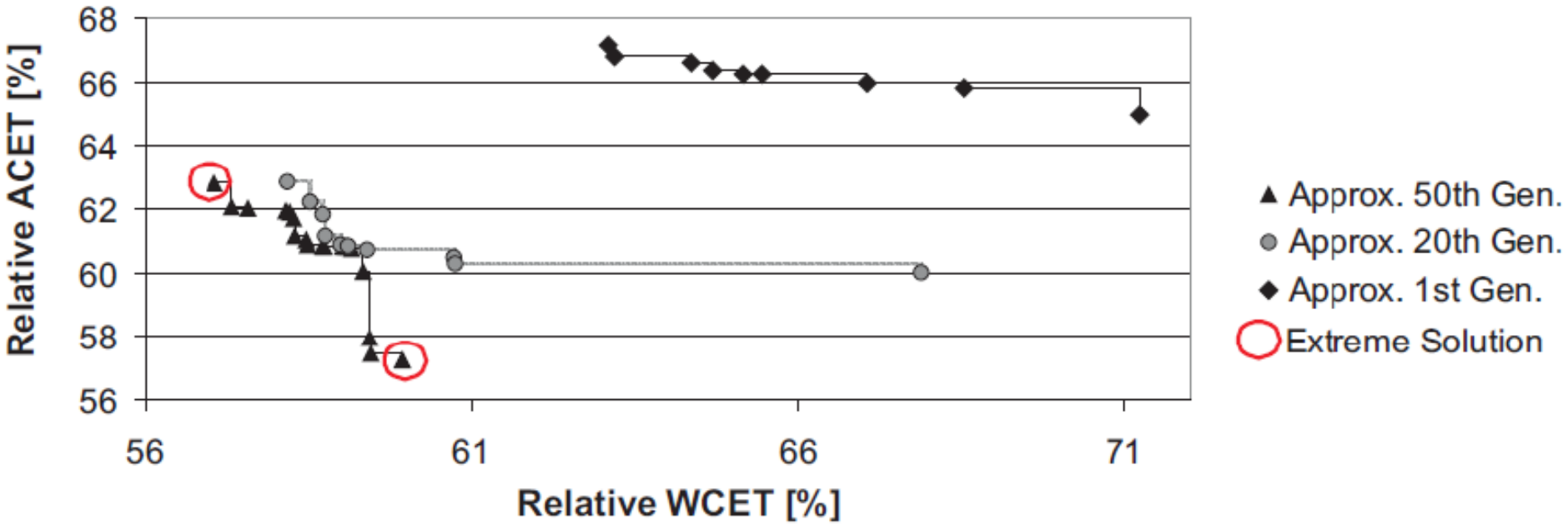


[H. Falk]

WCET-aware SPM allocation

- Setup
  - Bosch Democar: Runnable: IgnitionSWCSync
    Part of task actuator
    activated every 90° of crankshaft angle ☞ time-critical
  - WCET-aware SPM allocation of program code by WCC, including fully automated WCET analyses using aiT and solution of the ILP for SPM allocation
  - WCET reduced to about 50%, compared to gcc.
- ☞ PREDATOR project partners Bosch & Airbus interested in WCC

Timing Analysis and Compiler Techniques



Automatic Pareto-optimal trade-off between WCET, ACET (and code size)

- ***Result:*** trade-off WCET ↔ ACET reveals that (for the considered standard optimizations) WCET performs similar to ACET; achieved WCET and ACET reductions are very similar

Software Synthesis

3 Workshops on Software Synthesis;
program of the 3rd workshop:

- Shuvra Bhattacharyya:
  Software Synthesis from Dataflow Graphs: State of the Art and Emerging Trends
- Kaushik Ravindran and Hugo Andrade:
  From Streaming Models to Hardware and Software Implementations
- Marco di Natale:
  From analysis to optimization in the deployment of real-time distributed functions in modern automotive systems
- Rajeev Alur: Interfaces for control components
- Nicolas Halbwachs:
  Code generation from synchronous languages - a short survey

Software Synthesis (2)

1 call for a special journal issue of the journal on Industrial Informatics covering the workshop on software synthesis and MAP2MPSoCs

- 9 papers submitted
- 3 papers finally accepted:
  - Soonhoi Ha et al. (SNU)
  - Rainer Leupers et al. (RWTH Aachen)
  - Jan Madsen et al. (TU Denmark)
- Conclusion
  - Accepted papers came from ArtistDesign members or affiliates
  - Scope of both workshops covered
  - Low acceptance ratio (☞ not a very mature area?)

Comments on special issues, as requested

Scientific Highlights: Timing Predictability

- Cooperation with OS cluster strengthened
- Cache-aware scheduling (U. Saar, SSSA)
  - soundly estimating the cache-related preemption delay
- Timing analysis for multi-core systems with caches
- ICT project PREDATOR clarified many issues in the domain of predictable architectures:
  - defined predictable cores
  - clarified the significance of the interference on shared resources
- Research on the trade-off between average-case performance and worst-case predictability supported by Deutsche Forschungsgemeinschaft
- L. Thiele, R. Wilhelm: Architectural Aspects of Deriving Performance Guarantees, Tutorial at ISCA 2010

Scientific Highlights: Timing Analysis

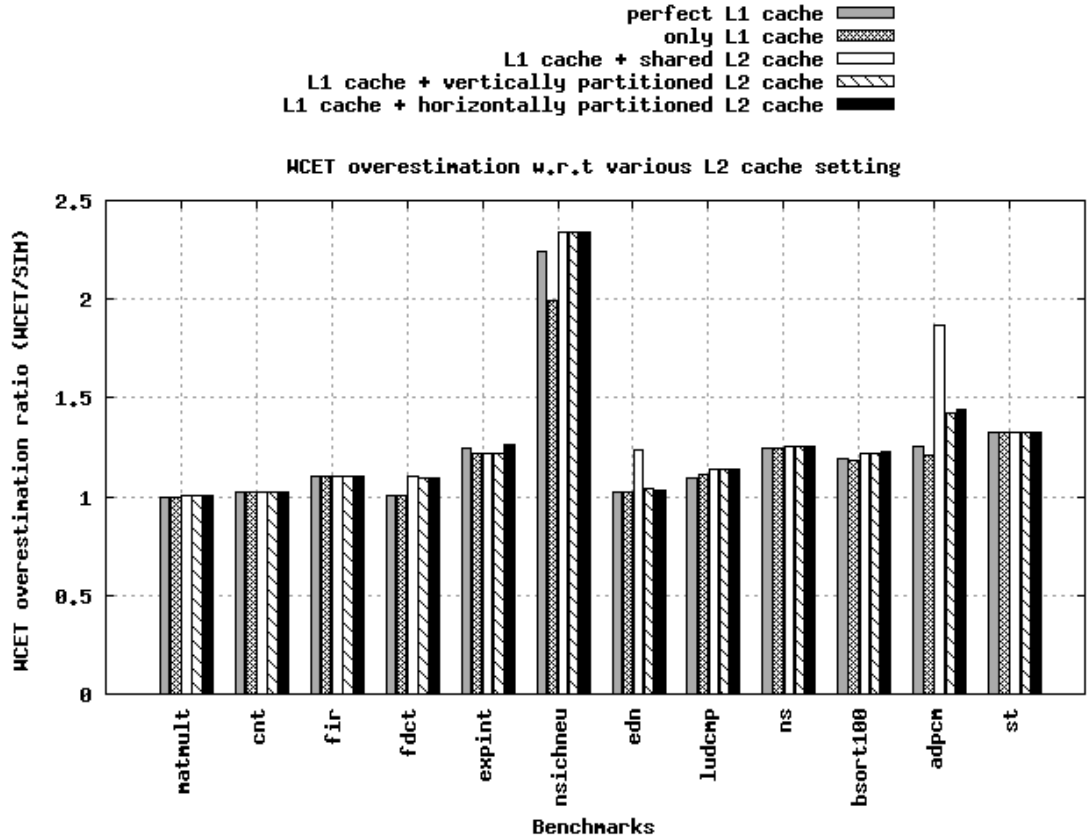
Main significant results in timing analysis:

- Foundational issues (predictability)
- Design principles for timing-predictable systems
- New & improved methods for timing analysis:
  - First analyses for multi-core
  - Novel cache analyses
  - Parametric WCET analysis
  - Measurement/hybrid methods: identification of timing models

Special issue of Journal of Systems Architecture on WCET Analysis (Volume 57, Issue 7, 2011)

Scientific Highlights: WCET Analysis for Multi-Cores

- A unified WCET analysis framework for multi-cores
- Assumes TDMA bus scheduling. Can deal with shared caches, and modern processor core features (exhibiting timing anomalies)



Scientific Highlights: Cache Analysis

- Cache analysis by a combination of abstract interpretation and model checking
- **Cache analysis**: classify memory accesses as hit/miss/unknown, needed for WCET analysis
- **Abstract interpretation** (AI) yields a scalable but somewhat imprecise analysis
- **Model checking** (MC) can give potentially very precise results, but has scalability problems
- **Idea**: First analyze by AI, then refine imprecise parts with MC. Keep complexity of MC under control by restricting its use to where it makes a difference
- Experiments show very good improvements of resulting WCET estimate

Joint Technical Meetings (1)

- Course: Retargetable Compilation, *Lugano, CH, Feb. 16-19 & 23-25, 2011*
- Tutorial: Mnemee design flow: a framework for memory management and optimization of static and dynamic data in MPSoC system, *ARCS 2011*
- Tutorial: MPSoC hardware/software architectural and design challenges/ solutions, *DATE 2011, Grenoble, France, March 15th, 2011*
- Industrial Workshop Bringing Theory to Practice: Performance and Predictability in Embedded Systems, *Grenoble, France, March 18, 2011*
- Workshop: Software & Compilers for Embedded Systems (SCOPES) 2011, *St. Goar, Germany – June 27-28, 2011*
- Meeting: 4th Workshop on Mapping Applications to MPSoCs, 2011 *St. Goar, Germany – June 28-29, 2011*
- Workshop: 11th International Workshop on Worst-Case Execution Time Analysis, 2011, *Porto, Portugal – July 5th, 2011, in connection with ECRTS 2011*
- Keynote: Energy-Efficient Embedded Computing, Energy-Aware Computing (EACO) Workshop, *Bristol, United Kingdom – July 13-14, 2011*
- Tutorial: Embedded System Foundations of Cyber-Physical Systems ARTIST Summer School in China 2011
- Workshop: 1st MAPS User Group Workshop (MUG 2011) *Aachen, Germany – September 28-29, 2011*

Joint Technical Meetings (2)

- Workshop: 7th Workshop on Embedded Systems Education, 2011
  Taipei, Taiwan – October 13th, 2011
- Workshop: 3rd Workshop on Software Synthesis, 2011
  Taipei, Taiwan – October 14th, 2011
- Tutorial: Energy modeling: Workshop of Collaborative research center SFB 876,
  Lüdenscheid, Germany, Oct. 20th, 2011
- Keynote: Parametric WCET Analysis
  Nordic Workshop of Programming Theory
- Visiting researcher: Prof. Reinhard Wilhelm (Saarland University)
  Team visited: IRIT, Université Paul Sabatier Grenoble, November 2011
- Team visited: Programming languages Lab at TU Vienna, November 2010
- Visiting Researcher: Mihail Asavoaie is a PhD student at University Al. I. Cuza of Iași, Team visited: Compiler Design Lab, Saarland University, November 2011
- Visiting researcher: Vitor Rodrigues, University of Porto
  Team visited: Compiler Design Lab, Saarland University
- Visiting researcher: Jan Gustafsson, Mälardalen University
  Team visited: Peter Puschner's real-time research group at TU Vienna, Austria
- Visiting student: Volker Seeker (Technical University of Berlin)
  Team visited: Björn Franke (University of Edinburgh)

Tools and Platforms

- aiT
  - commercial timing analysis tool, used in industry
- MAPS (MPSOC Application Programming Studio)
  - applied to real life processors, demonstrated to industry
- WCC: WCET-aware compiler
  - evaluated by Bosch
- MH, LooPo: parallelization assistants
- Bound-T, SWEET, Chronos: Timing analysis tools
- Cosy, ICD-C: Compiler design tool suites

Resulting tools can be interfaced to standard industrial tools since we are using standard languages (e.g. C)

Lasting Impacts

Future interaction beyond the end of the NoE

- Continuation of joint SCOPES and MAP2MPSOC WS (e.g. at Rheinfels on May 15th/16th, 2012)
- Continuation of WESE (e.g. @ ESWEEK 2012, Tampere)
- Continuation of Workshop on Software Synthesis
- Continuation of WCET WS, and WCET challenges
- Availability of tools like aiT, MAPS, LooPo, MH, ICD-C
- Running SIG of EDAA on Embedded System Design (Summer school, web site)
- Several joint projects (e.g. between ETH and SNU)
- COST Action proposal on timing analysis
- Contribution to education (e.g. textbook on ES)
- Results exploited in other projects (SFB 876, SPP1500,)
- Industrial exploitation through AbsInt, ICD, Rapita, …

Final Overall Assessment

Mapping of applications to MPSoCs

- Established discussion forum, experts are cooperating (e.g. joint paper at ESWEEK 2011)
- Availability of tools with different focus: MAPS, DOL, SystemCoDesigner, HOPES, etc.

Software Synthesis

- Linked experts, published papers at *IEEE Trans. on Industrial Informatics*, contribution to book on papers at ESWEEK 2011

Efficient Design: Continued as a side-track

Final Overall Assessment

Timing Analysis

- Many new insights in timing analysis for multi-core
- Need to push results on multi-cores to industry
- Continue to keep up with technology (both HW and SW)
- Need to further strengthen ties with other relevant communities

Contribution to global activities (education, summer school, transversal activities)

Recommendation:

- continuation of workshops
- applications for joint projects
- membership in ArtistDesign SIG of EDAA
- (supported) projects!