SEVENTH FRAMEWORK PROGRAMME
Challenge 3: Components, systems, engineering
ICT-2007.3.3 Embedded systems design

Grant agreement for: **Network of Excellence (NoE)**

Annex I - "Description of Work"

Project acronym: **ArtistDesign**
Project full title: **ArtistDesign – Design for Embedded Systems**

Grant agreement no.: 214373
Coordinating persons: Joseph Sifakis (Scientific Coordinator) – UJF/VERIMAG
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List of Beneficiaries:
UJF Filiale (France), Université Joseph Fourier Grenoble 1 (France), Rheinisch-Westfaelische Technische Hochschule Aachen (Germany), Aalborg Universitet (Denmark), Universidade de Aveiro (Portugal), Alma Mater Studorium - Universita di Bologna (Italy), Technische Universitaet Braunschweig (Germany), Universidad de Cantabria (Spain), Commissariat à l'Energie Atomique (France), Danmarks Tekniske Universitet (Denmark), Universitaet Dortmund (Germany), Ecole Polytechnique Fédérale de Lausanne (Switzerland), Embedded Systems Institute (Netherlands), Eidgenoessische Technische Hochschule Zuerich (Switzerland), Interuniversitair Micro-Electronica Centrum VZW (Belgium), Institut National de Recherche en Informatique et Automatique (France), Technische Universitaet Kaiserslautern (Germany), Kungliga Teknika Hogskolan (Sweden), Linköpings Universitet (Sweden), Lunds Universitet (Sweden), Maelardalens Hoegskola (Sweden), Offis E.V. (Germany), Project on Advanced Research of Architecture and Design of Electronic System (Italy), Universitaet Passau (Germany), Scuola Superiore di Studi Universitari e di Perfezionamento Sant'Anna (Italy), Instituto Superior de Engenharia do Porto (Portugal), Universitaet des Saarlandes (Germany), Universitaet Salzburg (Austria), Uppsala Universitet (Sweden), Technische Universitaet Wien (Austria), University of York (United-Kingdom).

Detailed table is available in section A.1.3.

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1 (coordinator)	UJF FILIALE	FLORALIS	France
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7	TECHNISCHE UNIVERSITAET BRAUNSCHWEIG	TUBS	Germany
8	UNIVERSIDAD DE CANTABRIA	CANTABRIA	Spain
9	COMMISSARIAT À L'ENERGIE ATOMIQUE	CEA	France
10	DANMARKS TEKNISKE UNIVERSITET	DTU	Denmark
11	UNIVERSITAET DORTMUND	DORTMUND	Germany
12	ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE	EPFL	Switzerland
13	EMBEDDED SYSTEMS INSTITUTE	ESI	Netherlands
14	EIDGENOESSISCHE TECHNISCHE HOCHSCHULE ZUERICH	ETH Zurich	Switzerland
15	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM VZW	IMEC	Belgium
16	INSTITUT NATIONAL DE RECHERCHE EN INFORMATIQUE ET AUTOMATIQUE	INRIA	France
17	TECHNISCHE UNIVERSITAET KAISERSLAUTERN	TUKL	Germany
18	KUNGLIGA TEKNIKA HOGSKOLAN	KTH	Sweden
19	LINKÖPINGS UNIVERSITET	LINKOPING	Sweden
20	LUNDS UNIVERSITET	ULUND	Sweden
21	MAELARDALENS HOEGSKOLA	MDH	Sweden
22	OFFIS E.V.	OFFIS	Germany
23	PROJECT FOR ADVANCED RESEARCH OF ARCHITECTURE AND DESIGN OF ELECTRONIC SYSTEMS	PARADES	Italy
24	UNIVERSITAET PASSAU	PASSAU	Germany
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28	UNIVERSITAET SALZBURG	PLU-SALZBURG	Austria
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Part A

A.1. Budget Breakdown and Project Summary

1.1. Overall budget breakdown for the project

Partner n°	organisation short name	Estimated eligible costs (whole duration of the project)			TOTAL A+B+C	Requested EC contribution
		RTD (A)	MNGT (B)	Other (C)		
1	Floralis	349 €	248 400 €	484 956 €	733 705 €	733 530 €
2	UJF/Verimag	285 417 €	66 600 €	15 578 €	367 595 €	296 239 €
3	Aachen	119 762 €	0 €	0 €	119 762 €	89 822 €
4	Aalborg	191 922 €	0 €	0 €	191 922 €	143 942 €
5	Aveiro	163 404 €	0 €	2 400 €	165 804 €	124 953 €
6	Bologna	219 350 €	0 €	0 €	219 350 €	164 513 €
7	TUBS	138 048 €	0 €	1 472 €	139 520 €	105 008 €
8	Cantabria	148 996 €	0 €	0 €	148 996 €	111 747 €
9	CEA	133 226 €	0 €	0 €	133 226 €	99 920 €
10	DTU	246 778 €	0 €	6 400 €	253 178 €	191 484 €
11	Dortmund	255 016 €	0 €	4 000 €	259 016 €	195 262 €
12	EPFL	143 996 €	0 €	0 €	143 996 €	107 997 €
13	ESI	102 228 €	0 €	0 €	102 228 €	76 671 €
14	ETHZ	164 492 €	0 €	0 €	164 492 €	123 369 €
15	IMEC	296 771 €	0 €	0 €	296 771 €	222 577 €
16	INRIA	104 812 €	0 €	0 €	104 812 €	78 609 €
17	Kaiserslautern	122 552 €	0 €	6 400 €	128 952 €	98 314 €
18	KTH	216 416 €	0 €	3 200 €	219 616 €	165 512 €
19	Linköping	136 159 €	0 €	0 €	136 159 €	102 119 €
20	Lund	97 518 €	0 €	3 200 €	100 718 €	76 339 €
21	Malardalen	119 762 €	0 €	6 400 €	126 162 €	96 222 €
22	OFFIS	78 368 €	0 €	0 €	78 368 €	58 776 €
23	Parades	153 342 €	0 €	1 528 €	154 870 €	78 199 €
24	Passau	91 428 €	0 €	0 €	91 428 €	68 571 €
25	Pisa	212 163 €	0 €	0 €	212 163 €	159 122 €
26	Porto	122 552 €	0 €	0 €	122 552 €	91 914 €
27	Saarland	209 302 €	0 €	0 €	209 302 €	156 977 €
28	Salzburg	78 368 €	0 €	4 466 €	82 834 €	63 242 €
29	Uppsala	131 258 €	0 €	0 €	131 258 €	98 444 €
30	Vienna	117 872 €	0 €	0 €	117 872 €	88 404 €
31	York	309 610 €	0 €	0 €	309 610 €	232 206 €
	Total	**4 911 237 €**	**315 000 €**	**540 000 €**	**5 766 237 €**	**4 500 000 €**

1.2. Project Summary

Proposal acronym:	**ArtistDesign**
Proposal acronym and full title:	**ArtistDesign – Design for Embedded Systems**
Strategic objectives addressed:	**Challenge 3: Components, systems, engineering** **ICT-2007.3.3 Embedded systems design**

The ArtistDesign NoE is the visible result of the ongoing integration of a community, that emerged through the ARTIST FP5 Accompanying Measure and that was organised through the ARTIST2 FP6 NoE.

The central objective for ArtistDesign is to build on existing structures and links forged in ARTIST2, to become a virtual Centre of Excellence in Embedded Systems Design. This will be mainly achieved through tight integration between the central players of the European research community. Also, the consortium is smaller, and integrates several new partners. These teams have already established a long-term vision for embedded systems in Europe, which advances the emergence of Embedded Systems as a mature discipline.

ArtistDesign will become the main focal point for dissemination in Embedded Systems Design, leveraging on well-established infrastructure and links, such as a web portal and newsletter. It will extend its dissemination activities, including Education and Training, Industrial Applications, as well as International Collaboration. ArtistDesign will establish durable relationships with industry and SMEs in the area, especially through ARTEMISIA/ARTEMIS.

ArtistDesign will build on existing international visibility and recognition, to play a leading role in structuring the area.

The research effort aims to integrate topics, teams, and competencies, grouped into 4 Thematic Clusters: “Modelling and Validation”, “Software Synthesis, Code Generation, and Timing Analysis”, “Operating Systems and Networks”, “Platforms and MPSoC”. “Transversal Integration” covering both industrial applications and design issues aims for integration between clusters.

ArtistDesign has defined a four-year workprogramme, with a strong commitment to integration and sustainability. To achieve the aims, the estimated support from the EC is approximately 4.5 Million Euros. This support is a very small proportion of the overall investment by the core partners.

1.3. List of Beneficiaries

Beneficiary number*	Beneficiary name	Beneficiary short name	Country
1 (coordinator)	UJF FILIALE	FLORALIS	France
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Part B

B.1. Concept and Objectives, Progress Beyond the State of the Art, S/T Methodology and Work Plan

Objective: To build on previous integration, and become a virtual Centre of Excellence in Embedded Systems Design:
- Achieve tight integration between the central players of the European research community
- Establish durable relationships with industry and SMEs in the area, especially through ARTEMISIA/ARTEMIS
- Become the main focal point for dissemination, via ARTIST competencies and infrastructure
- Build on existing international visibility and recognition, to play a leading role in structuring the area.

1.1. Concept and Project Objectives

Main Idea 1

Embedded systems are essential to ensuring a leading position for Europe in key industrial sectors services. This is well-recognized in the ICT FP7 priorities, and through the ARTEMIS ETP under construction.

About Embedded Systems

Embedded Systems are components integrating software and hardware jointly and specifically designed to provide given functionalities. These components may be used in many different types of applications, including transport (avionics, space, automotive, trains), electrical and electronic appliances (cameras, toys, television, washers, dryers, audio systems, and cellular phones), power distribution, and factory automation systems.

The extensive use of embedded systems and their integration in everyday products marks a significant evolution in information science and technology. An important requirement for their proliferation is seamless integration with their environment while respecting real-world constraints such as hard deadlines, reliability, availability, robustness, power consumption, and cost.

Embedded systems are deployed in the physical environment, and as such they have a continuous interaction with it. This gives rise to a number of specific characteristics, which play a role in structuring the technical domain, and for determining the relevant areas of research and industrial development:

Economic Stakes for Europe

Embedded systems are of strategic importance in modern economies. They are used in mass-market products and services, where value is created by supplying either functionality or quality. Functionality is defined as the service rendered to the user. Quality for a given functionality characterizes extra-functional properties of the product or service, such as performance, or dependability. For instance, a cellular phone offers functionality for mobile communication, while quality is characterized by audio fidelity, battery life, and durability.

Embedded technologies confer advantages to system and service developers, in generating added value and enhancing competitivity. The relative weight of software in the value of embedded systems is constantly increasing. Software allows new, complementary services, and differentiation, which brings competitive advantages.

Embedded technologies are the fastest growing sector in Information Technologies.

Europe currently has leading positions in sectors where embedded technologies are central to growth. These sectors currently include avionics, automotive, space, consumer electronics, smart cards, telecom devices, energy distribution, and railway transport. It is anticipated that they will also include distributed services such as e-Health and e-Banking.

In particular, Europe is well-positioned in avionics and space. In the automotive sector, European manufacturers and their suppliers enjoy a leading technological advantage for engine control, and emerging technologies such as brake by wire and drive by wire. Railway signalling in Europe relies on embedded systems, and allows faster, safer, and heavier traffic. Embedded technologies will be extensively used to make energy distribution more flexible, especially in view of the coming market liberalization. Embedded technologies are strategic for the European telecommunication sector, which is also well-positioned. Finally, Europe is well-positioned for e-Services (e-Banking, e-Health, e-Training).

The FP6/FP7 Perspective - ARTEMIS

Embedded systems have already been one of the priorities in FP6. The European Commission, as well as the member states, is increasingly interested in reinforcing the R&D effort in this area. This is attested by:

- The launching of large R&D projects, focused on design and validation techniques in countries such as Sweden (Uppsala, Mälardalen) and Germany (AVACS, VeriSoft projekt);
- The creation of specialised research institutes, such as the Embedded Systems Institute in Eindhoven, the Centre for Embedded SW Systems in Aalborg;
- National Research Programmes on Embedded Systems, and in particular the creation of “competitivity poles”, that federate the efforts of the main players in the area, at a regional level. Amongst these, 3 poles are strongly focused on embedded systems (Systematic, Aerospace Valley, Minalogic);
- Creation of Networks of Excellence (ARTIST2, HiPEAC, HyCon).

The ArtistDesign core partners have been actively involved in leading all these initiatives.

In FP7, several indicators show the clear willingness to make Embedded Systems a top priority for Europe. This is reflected by the significantly increased overall budget of the ICT programme. It is also confirmed by the creation of the ARTEMIS Joint Technology Initiative (JTI), set up to reinforce European R&D in embedded systems. ARTEMIS governance will involve representatives from 3 stakeholders: the European Commission, member states, as well as representatives from corporate industry, SMEs, and Public Research Organisations. These are organised within the ARTEMISIA association.

As the leading Network of Excellence focusing on design for embedded systems, ArtistDesign will have a close working relationship with ARTEMIS and ARTEMISIA. A liaison group composed of ArtistDesign members having responsibilities within ARTEMISIA will be set up to manage interaction. This will concern contributions to the ARTEMIS Strategic Research Agenda (SRA), and the Working Group on Innovation Environment.

Beyond the applied research and development activities driven by its industrial stakeholders, it is essential for the long-term success of ARTEMIS to have an environment supporting upstream research driven by the academic community in the large (universities and research institutes).

Leveraging on existing links between the ArtistDesign NoE leadership and ARTEMIS, ArtistDesign NoE will actively promote structuring within the academic community for effective and efficient interaction with industry via ARTEMISIA.

Main Idea 2

Embedded systems design is an emerging scientific discipline, mobilizing a large international community, around a set of fundamental challenging and multi-disciplinary problems. For this discipline to emerge, a considerable focused research effort by the best teams is needed.

Current Scientific Foundations for Systems Design, and their Limitations

Design for Systems in General: Systems design is the process of deriving, from requirements, a model from which a system can be generated more or less automatically. A model is an abstract representation of a system. For example, software design is the process of deriving a program that can be compiled; hardware design, the process of deriving a hardware description from which a circuit can be synthesized. In both domains, the design process usually mixes bottom-up and top-down activities: the reuse and adaptation of existing component models; and the successive refinement of architectural models in order to meet the given requirements.

Design for Embedded Systems: An embedded system is an engineering artefact involving computation that is subject to physical constraints. The physical constraints arise through two kinds of interactions of computational processes with the physical world: (1) reaction to a physical environment, and (2) execution on a physical platform. Accordingly, the two types of physical constraints are reaction constraints and execution constraints. Common reaction constraints specify deadlines, throughput, and jitter; they originate from the behavioural requirements of the system. Common execution constraints put bounds on available processor speeds, power, and hardware failure rates; they originate from the implementation requirements of the system. Reaction constraints are studied in control theory; execution constraints, in computer engineering. Gaining control of the interplay of computation with both kinds of constraints, so as to meet a given set of requirements, is the key to embedded systems design.

The design of embedded systems requires a holistic approach that integrates essential paradigms from hardware design, software design, and control theory in a consistent manner. We postulate that such a holistic approach cannot be simply an extension of hardware design, nor of software design, but must be based on a new foundation that subsumes techniques from both worlds. This is because current design theories and practices for hardware, and for software, are tailored towards the individual properties of these two domains; indeed, they often use abstractions that are diametrically opposed.

Main Challenging Issues

We need methods and tools for the cost-effective design of systems of guaranteed quality and performance. These should focus on the overall system as the combination of software and hardware interacting with its environment. A key issue is the joint design of both hardware and software to determine tradeoffs between cost and quality and performance.

Embedded systems design raises difficult, fundamental research problems which are at basis of an emerging theory that will bring together Informatics and Physics. Informatics is founded on models and theory that ignore physical time. Existing models and paradigms such as automata, algorithms, computability and complexity theory adopt an abstract "logical" view of time which is difficult to link to physical time. Existing theory does not provide a basis for predicting the dynamic behaviour of application software on a given platform.

We believe that the challenge of designing embedded systems offers a unique opportunity spanning the spectrum from theoretical foundations to engineering practice. To begin with, we need a mathematical basis for systems modelling and analysis which integrates both abstract-machine models and transfer-function models in order to deal with computation and physical constraints in a consistent, operative manner. Based on such a theory, it should be possible to combine practices for critical systems engineering to guarantee functional requirements, with best-effort systems engineering to optimize performance and robustness.

The theory, the methodologies, and the tools need to encompass heterogeneous execution and interaction mechanisms for the components of a system, and they need to provide abstractions that isolate the sub-problems in design that require human creativity from those that can be automated. This effort is a true grand challenge: it demands paradigmatic departures from the prevailing views on both hardware and software design, and it offers substantial rewards in terms of cost and quality of our future embedded infrastructure.

Need for Critical Mass and Excellence

Embedded Systems Design is a multi-disciplinary area. Its development requires integration of contributions from different topics, and thus critical mass. This is visible in large research centres in the USA, which play a leading role in the area. For example, the excellent position held by UC Berkeley on wireless sensor networks has been made possible by bringing together competencies in architectures, compilers, and telecommunication.

Given the hard problems to be addressed for the emergence of this discipline, it is essential to have, in addition to critical mass, the best possible teams from the contributing topics. Furthermore, the effort needs to be properly structured and motivated to succeed.

ArtistDesign gathers the right critical mass, with the best European teams. Furthermore, most of these teams have participated in ARTIST2, and have already built up momentum and shown their willingness and commitment to collaborate, around a coherent and ambitious workprogramme.

1.2. Progress beyond the State of the Art

1.2.1. Theory Methods and Tools for Embedded Systems Design

Design flow involves topics leading from initial requirements to a final implementation satisfying them. The objective is to study specific needs for these design activities, as well the possibility of integrating them in a coherent design flow.

We distinguish four essential topics, for which existing techniques should be adapted and extended

Modelling and Validation: Modelling is an essential activity in the design flow. For embedded systems, we need formal modelling techniques that take into account the characteristics of a system's external and execution environments. Furthermore, these techniques should support component-based construction for heterogeneous components to be applicable throughout the design process. For embedded systems, validation focuses on testing and verification of non functional properties, including performance and dependability.

Software Synthesis, Code Generation and Timing Analysis: These are interrelated topics, for which strong integration should be sought. The aim is to study and implement resource-aware synthesis and code generation techniques. These techniques allow the generation of an implementation meeting given user requirements from a functional description of an application (e.g. application software) and a model of a target platform. Timing analysis techniques are needed for building accurate platforms models, used by code generation tools. In particular, they provide estimates about the dynamic characteristics of the platforms e.g.; worst case or best case execution times.

Real-Time Operating Systems Scheduling and Networks: The aim is to develop theory methods and tools for new real-time software infrastructures, for the execution and communication between embedded applications. The main problems include adaptive resource management and dependability techniques, in particular to improve robustness to deviations from nominal conditions.

Platforms and MPSoC Design: The aim is implementation of complex applications on multi-core HW platforms. It raises a number of problems for ensuring predictability and efficiency. These include adaptive techniques for resource management, and the study of reliable programming models for multi-core architectures.

Integrating these results in a coherent design flow is the main scientific and technical objective of the ArtistDesign NoE. This integration will be achieved for design flows ensuring given essential properties such as adaptivity, predictability, dependability, etc. In a specific Workpackage, for each of these properties, we will examine how to combine results in the topics above. Additionally, validation of this integration work will be guided by comparison and analysis of design flows in automotive, multi-media, healthcare, applications.

1.2.2. Strengthening Scientific and Technological Excellence through Integration

Through the integration of high-quality scientific teams, achieve the emergence of embedded systems design as a discipline, and the corresponding structured scientific community.

ArtistDesign will integrate the European research community in embedded systems design by implementing a long-term research vision for embedded systems in Europe.

The ambition is to compete on the same level as equivalent centres in the USA (Berkeley, Stanford, MIT, Carnegie Mellon), for both the production and transfer of knowledge and competencies, and for the impact on industrial innovation. ArtistDesign will create a research pipeline with continuous production of top research results. It will proactively invest in research groups to ensure competitivity at an international level.

This objective will be achieved by integration around a Joint Programme of Activities, aiming to create critical mass from selected European teams.

The partners' international standing, research and teaching programmes in the field, the technologies they have developed and possess, and their leading presence in international scientific events prove their excellence. The Joint Programme of Activities will integrate the partner institutions mainly by promoting close collaboration and massive researcher exchanges between partners and thus start an "ARTIST culture" within the network.

The long-term ambition is the emergence of Embedded Systems Design as a mature discipline through research projects, integration of communities, education.

1.2.3. Spreading Excellence in Embedded Systems Design

The NoE's influence is greatly expanded through its affiliated partners, who actively participate in the technical work and act as a relay to the greater Embedded Systems Design community. We expect that more affiliated partners will join the project and that the NoE's impacts will continue to grow with time. With this number of excellent people working on the same goals, the visibility of the European research effort in embedded systems design will be worldwide. This will progressively create a European embedded systems design community, and spread the "ARTIST culture" in all major research institutions.

To ensure that the next generation of researchers will continue in this direction, ArtistDesign will devote a great deal of effort to spreading our knowledge in education and training. We will establish a vision for Education and Training in embedded systems by promoting reference curricula and training for industrial engineers.

Activities such as joint PhDs between partners, courseware, textbook publications, summer schools, and seminars, will all serve to attract students and young researchers to our research field.

A specific effort will be devoted to spreading excellence to industry. All the core partners have strong and lasting collaborations with major industrial players in the area. It is vital for the partners to see the industrial know-how and techniques evolve, through the integration of state of the art results. Concretely, this transfer to industry will be through shared PhDs with affiliated industrial partners, by opening the NoE's platforms to industry, and through a strong participation of the partners in Integrated Projects, STREPS, etc. It is worth noting the degree of collaboration between ArtistDesign partners for building Integrated Projects in the area (e.g.: SPEEDS, DECOS, ASSERT, SHAPES).

ArtistDesign will actively work to promote and enable the transfer of partners' results through participation in industrial projects, and training (schools, on-site, etc.). We will represent and promote the highest level of research competence and provide a network that taps into the highest levels of competence. The NoE will analyze and communicate industrial needs to research.

Finally, through the key participation of core partners in ARTEMIS/ARTEMISIA, the NoE will actively contribute to maintaining strong links between Public Research Organisations and Corporate Industry, and SMEs in the area.

ArtistDesign will build up and reinforce existing links between the European embedded systems design community and main international (outside Europe) players in the area. Through the International Collaboration activities in ARTIST FP5 and the ARTIST2 NoE, we have set up regular activities such as:

- High-level meetings (e.g.: in collaboration with the NSF) that gather together international experts from industry and academia to analyse the state of the art and identify promising work directions.
- International workshops on top-priority topics, such as timing analysis, and component-based design, as well as workshops on education.
- International schools in China, and South America, to promote European research results in emerging economies and reinforce our visibility as well as to draw top students.

ArtistDesign will continue to organize these types of events, to reinforce international visibility and recognition. We will go a step further, to develop an International Collaboration programme in embedded systems, involving the main non-European centres of excellence in embedded systems design.

The ArtistDesign NoE will extend the portal initiated in ARTIST2, by adding services for interaction with the embedded systems community in the large. It will act as a repository of knowledge in the area, including courseware, information about standards, methods and tools, research publications and results. This web portal will be made available within the NoE core and affiliated partners, and also to other parties according to modalities to be defined.

This repository will be the reference for the embedded systems design community. It will build on the existing ARTIST2 Portal, and offer information about workshops, conferences, schools and seminars, international collaboration, publications, course materials available online, etc..

As was done at the start of ARTIST2, ArtistDesign will hold a press conference to announce the start of the NoE. This is described in further detail in section B.1.3.5 “WP2 Description – JPASE”.

The NoE will also publish a high-quality newsletter to disseminate pointers to events, innovative results, high-level interviews, and other information useful to the community.

1.2.4. Long-term Integration

This section provides the global Indicators for Integration, expressed as high-level objectives, which will deeply and qualitatively change the degree of integration between academic entities in the area.

Embedded systems design is a multidisciplinary area requiring competences from hardware engineering, operating systems and networks, programming and compilation, modelling and software engineering, control engineering. The ArtistDesign NoE gathers together leading European teams from all these areas.

The experience within ARTIST2 has shown that integration is a long-term process. Nonetheless, it has been possible within a 3-year timeframe to achieve durable integration between European teams working on topics such as Control and Adaptive Real Time, Timing Analysis and Execution Platforms, Modelling and Validation.

This durable integration is also visible through an organised community that has a concerted action for structuring the area, through joint workshops, conferences, schools and publications.

ArtistDesign will continue and extend these activities, both quantitatively and qualitatively. In setting up the consortium, we have sought the right balance between critical mass, excellence, and commitment from the core partners.

- *Critical Mass*
  It was essential to gather a sufficient number of partners, to achieve a fair coverage of the main topics in the area, as well as to have the capacity to impact the European research landscape. Nonetheless, to ensure efficiency, we have limited the number of core partners, based on previous experience. At the same time, our impact is amplified through the large number of affiliated academic, SME, industrial and international collaboration partners.
- *Excellence*
  The ArtistDesign core partners include the main European leading teams, as attested by their leadership in their respective areas, as well as their strong involvement in national and European projects and initiatives.
- *Commitment*
  The majority of the ArtistDesign core partners were already involved as core partners in the ARTIST2 NoE. They have demonstrated a high degree of investment to achieve the workprogramme objectives, by committing the resources needed, which are an order of magnitude larger than those provided by the NoE financing. We estimate that the effort for implementing the JPA is roughly 10 times the financial contribution for integration.

The momentum and willingness of the consortium to continue working together are very strong. This is a good indication that integration will be sustained even after the end of the contract. ArtistDesign will leverage on the initial results of the ARTIST2 NoE, to achieve a durable structuring effect on European research in a variety of respects:

1. The NoE will extend the *integration of academic research*. Clustering around an emerging coherent theoretical embedded systems design framework contributes to the unification of the scientific community. This unification will be reinforced through measures for overcoming the inherent contextual, cultural, and disciplinary diversity – through implementation of the JPA (schools, joint workshops, etc.).
2. We intend to work towards integration between the recently funded IST STREP projects, that have a strong level of ARTIST involvement and leadership:
   - ACTORS - Adaptivity and Control of Resources in Embedded Systems
   - ALL-TIMES - Integrating European Timing Analysis Technology
   - COMBEST - COMponent-Based Embedded Systems design Techniques
   - PREDATOR - Design for Predictability and Efficiency
   - Quasimodo - Quantitative System Properties in Model-Driven Design of Embedded Systems.
   - MNEMEE
   - EMUCO Embedded Multi-Core
   - JEOPARD - Java Environment for Parallel Realtime Development

Over the course of Year 1, we will identify possible synergies between these projects, and the ArtistDesign NoE, and restructure the effort accordingly. This work could lead to a proposal for modifying the ArtistDesign Joint Programme of Activities at the end of Year 1.

The idea is very attractive, and fully supported by the consortium. We would use a part of the NoE's resources to ensure the best possible integration between the results of the projects. Nonetheless, its implementation requires prior investigation, to ensure that such a possible coordination would not hamper these projects, and have an overall positive impact.

3. ArtistDesign will impact *R&D activities from an organizational perspective*. The NoE will explicitly aim to create a context, an infrastructure and a culture for embedded systems design. This will be achieved via the JPA activities, and also by the growing community spirit generated.
   More specifically, to ensure a durable structuring, and coordination of the embedded systems design community, the NoE actively works in the following directions:
   - Exploitation and improvement of the existing Web Portal and Intranet for disseminating information and coordination R&D activities.
   - Continue efforts to reinforce the Embedded Systems Week, and to place embedded systems design at the heart of the DATE conference. We will pursue interaction with scientific organizations in the area (e.g.: ACM, IEEE, Euromicro, DATE), to further structure the scientific event landscape.
   - Work and interaction with and within ARTEMIS/ARTEMISIA will be pursued, to ensure tight interaction between the academic and industrial components of the embedded systems design community.
   - A very promising perspective we are currently investigating is in setting up a European Institute of Technology (EIT), on Embedded Systems. Funding for EITs is planned within IST FP7. Our community is well-positioned for this, in terms of credibility, critical mass, excellence and organizational infrastructures. Naturally, competition for these funds is fierce. Nonetheless, we are convinced that, if Embedded Systems are selected for funding, that our community will be at the heart of an EIT on this topic.
   - To ensure the sustainability of the community beyond the ArtistDesign funding period, it is important to set up a lasting coordination structure. A solution to be explored would be through a specific ARTEMISIA Working Group.
     As a fallback solution, we could alternately set up the *ArtistInstitute* as a non-profit organization. In complement to coordinating the community, it would provide interaction and collaboration with the European large companies and SMEs in Embedded Systems, leveraging on its network of top European researchers.
4. ArtistDesign will have structural impact on European education in Embedded Systems Design, by:
   - Integrating state of the art knowledge into the curricula, and accelerating the convergence towards unified multi-disciplinary approaches.
   - Promoting approaches, techniques, which are well-adapted to meeting current and future industrial needs.

1.3. S/T Methodology and Associated Work Plan: Joint Programme of Activities (JPA)

1.3.1. Overall Strategy and General Description

We present an overview of the JPA breakdown, and the way in which the different types of Activities cooperate to achieve the overall objective.

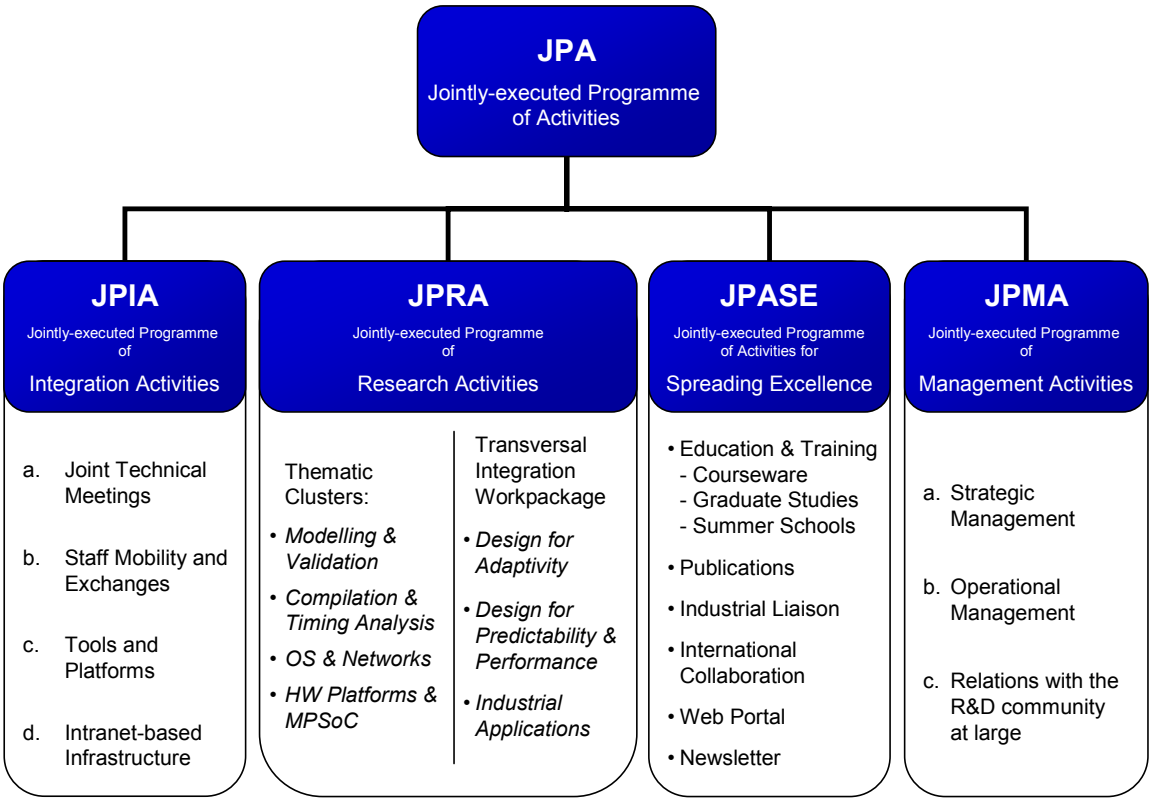
Overview

ArtistDesign will act as a *Virtual Centre of Excellence*, composed of a set of virtual teams, called *clusters*. Each cluster gathers together selected teams from partners, to create the critical mass and expertise in one of the essential topics for embedded systems design.

Each cluster acts as a scientific team, with a specific workplan, and it also participates in global Integration activities, as specified in the *Joint Programme of Activities* (JPA). Each cluster has one or more scientific leaders, who lead the team and coordinate the effort.

A founding principle of the ArtistDesign NoE is integration around a common set of essential research topics, which may evolve over the lifetime of the NoE. This concept was initiated in the ARTIST2 NoE, and refined in ArtistDesign.
An essential new structural feature is the Transversal Integration workpackage having far greater independence (separate leaders and independent budget). We expect this to lead to continued integration between the topics.
Each cluster has affiliated partners, serving as relays to the community. These affiliated partners, as well as external parties sharing ArtistDesign's objectives may receive funding and participate in the ArtistDesign Activities according to rules to be defined.

The Joint Programme of Activities is structured as follows:



To enhance the readability of the proposal, we have preserved this structure (and the corresponding reference numbers) wherever possible throughout the document. This diagram can be used as a reference to understand the relative positions between the different Activities.

All the Activities will be monitored to check their relative success or failure. Evaluation will rely on internal mechanisms. The overall success criteria for the NoE will be the emergence of a European scientific community on embedded systems design, with strong interaction with industry, and internationally recognized excellence.

All the activities are open to the ArtistDesign Affiliated partners. These are not core partners in the consortium, but receive support for travelling to ArtistDesign meetings, and actively contribute to the implementation of the Joint Programme of Activities (JPA). These affiliated partners include industrial, SME, academic, and international affiliates. We will continue to apply the ARTIST2 procedure for joining ArtistDesign as affiliated partners, described here: http://www.artist-embedded.org/artist/Becoming-an-Affiliated-Partner.html

The breakdown for the Jointly-executed Programme of Activities (JPA) is the following:

Jointly-executed Programme of Management Activities (JPMA)

In order to ensure correct integration and coordination of activities, and coordination between the partners, the Consortium will carry out a Joint Programme of Management Activities (JPMA). It includes:

Strategic Management
The Strategic Management Board (SMB) plays a key role in ensuring ongoing integration at 3 levels: I) within the cluster; II) between clusters; III) with the larger European Embedded Systems Design community.

Operational Management
is ensured by the ArtistDesign Office, and the Executive Management Board (composed of the Cluster Leaders). The ArtistDesign Office ensures that all aspects of the NoE are running smoothly, and that progress is made towards the overall NoE objectives. It is composed of the Scientific Coordinator, the Technical Coordinator, and the Legal, Administrative and Financial Coordinator.

Relations with the R&D community at large
The NoE has a very strong presence within the embedded systems design community, at all levels. High-level interaction with the main institutions and bodies such as ARTEMIS/ARTEMISIA, professional organisations such as ACM TECS, NSF, DARPA, large conferences, are ensured and supported by various members of the Strategic Management Board, and the Scientific and Technical Coordinators.

Jointly-executed Programme of Integrating Activities (JPIA)

Each ArtistDesign research activity will have work within both the JPIA and the JPRA workpackages. The JPIA Activities are carried out on a global, NoE level, transcending the clusters. They form the supporting background for integration of the NoE, and are executed in phase and in interplay with the JPRA research activities. For instance, funds for staff mobility will be allocated taking into account the needs for research.

The activities listed here will promote integration of geographically dispersed teams. All these activities will have long-lasting effects, well beyond the duration of the initial EC funding.

These activities include Joint Technical Meetings, Staff Mobility and Exchanges, Tools and Platforms, and an Intranet-based Infrastructure for Communication and Collaboration.

- **Joint Technical Meetings**
  Joint Technical meetings aim to present, discuss and integrate the ongoing work, and exchange points of view with other teams. They also serve to identify future work directions.

- **Staff Mobility and Exchanges**
  This is essential for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. Mobility should be justified by and refer to involvement in an activity from the JPRA or JPIA, or one of the following: co-funded scholarships with industry; exchange of students and personnel within the consortium.
  These measures are indicative – ArtistDesign will take the appropriate steps and incentives to ensure integration through mobility.

- **Tools and Platforms**
  A research platform is composed of competencies, resources, and tools targeting specific technical and scientific objectives around a chosen topic. These are at the state-of-the-art, and are made available to the R&D community for experimentation, demonstration, evaluation, and teaching.

  The research platforms, tools and facilities are an essential tool for implementing the JPIA. They will lay the groundwork for the JPRA, allowing common research to occur and capitalisation on research results. Platforms are used as the basis for transfer of research results to industry. They allow teaching practical knowledge of the concepts and techniques.

  ArtistDesign platforms are not defined from scratch – they integrate the results of long-term efforts, and are meant to be durable, evolving with the state of the art. The partners are committed to durability, and have invested significant resources into their development. The construction of ArtistDesign has provided the opportunity to assemble existing pieces into a rationally-structured set of platforms, covering the area of embedded systems design.

  Some of the ArtistDesign platforms have international visibility, and the ambition is for these to serve as world-wide references in their respective topics.

  Joint Management of the Knowledge Portfolio:
  We believe that ArtistDesign has an enormous potential in Tools and Platforms. We will set up a repository for managing and disseminating the participating team's IPR, including tools, software and hardware IPs. This repository will be used for dissemination purposes, as well as for marketing the partner's achievements. These dissemination efforts will be completed through technical meetings and presentations.

- **Intranet-based Infrastructure for Communication and Collaboration**
  To overcome the physical, cultural, and topic distances between teams, the ARTIST2 NoE has already set up a common infrastructure for communication and collaborative work between teams. This infrastructure will be further refined within ArtistDesign.

Jointly-executed Programme of Activities to Spread Excellence (JPASE)

These activities serve as a relay between the NoE and the international embedded systems design community at large. They are managed at the NoE level, and are mostly not specific to any cluster. The JPASE activities are planned by the Strategic Management Board, and are implemented by the Executive Management Board and the ArtistDesign Office.

The JPASE activities consist of the following:

- **Education and Training**
  Even if the Education and Training activities are open to the community at large, the first beneficiaries will be the NoE participants. The NoE will have a strong policy for encouraging education within its ranks. These activities play a double role:
  - They work to integrate teams and viewpoints by serving as incubators for developing integrated curricula and materials. To capitalise on these activities over time, the insights gained from one event (e.g.: a summer school) will be applied to subsequent events.
  - They serve to disseminate results and spread excellence well beyond the partners and affiliated partners of ArtistDesign.
- **Publications in Conferences and Journals**
  This will be implemented through publication in the main conferences on Embedded Systems Design of the area, as well as the active participation for the organization and management of these events.
- **Industrial Liaison**
  This consists of actions oriented towards affiliated industrial partners, to transfer results follow and get feedback on the research and integration activities in the JPA (JPRA, JPIA).
- **International Collaboration**
  These activities will play a dual role: showcase the participants' results, and reinforce the NoE's leadership role worldwide. They will also collect relevant information about evolution of the state of the art outside Europe.
- **Web Portal**
  This will play a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large. The web portal will be an essential mechanism for achieving integration and recognition.

Jointly-executed Programme of Research Activities (JPRA)

This section describes the JPRA Activities that are decided and executed jointly within ArtistDesign. There are two types of Activities within the JPRA: “Joint Research”, and “Tools and Platforms”.

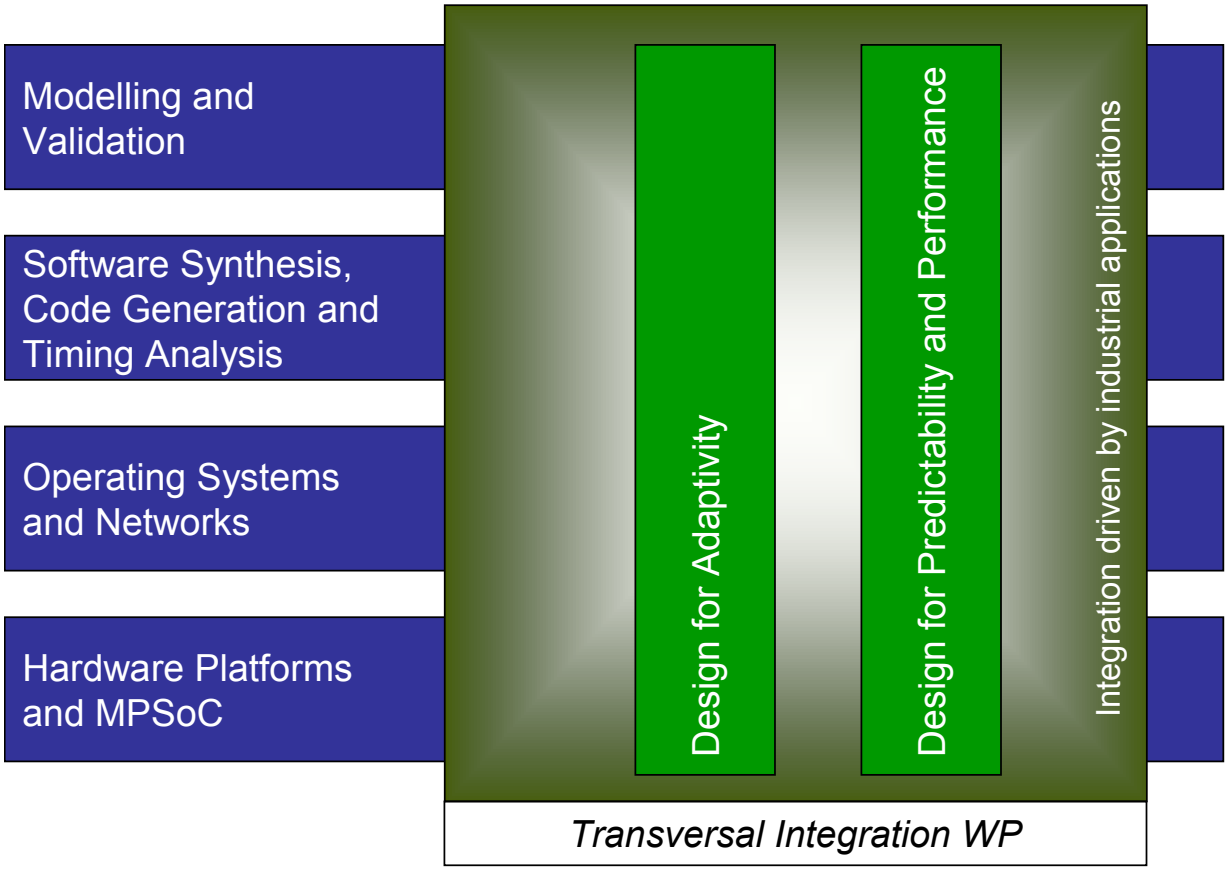
The JPRA is structured into 4 **Thematic** (horizontal) Clusters, and a Transversal Integration workpackage.

Clusters are autonomous entities, with specific objectives, teams, leader(s), and a dedicated yearly budget.

The set of Thematic Clusters cover all the main topics in Embedded Systems Design. The Activities in the Transversal Integration workpackage focus on Design methodologies, with specific objectives (Predictability, Adaptivity).

Each cluster may have one or several Activities, as appropriate.

The detailed descriptions of the “NoE Integration” research activities are provided below.



1.3.2. Timing of Workpackages and their Components

All Workpackages are active throughout the 4-year period.

1.3.3. Workpackage List / Overview

The anticipated structure of the area reflects the following decomposition of the embedded systems design flow.

The embedded systems design flow is composed of the following cooperating activities, starting with requirements capture and leading to implementation. These activities must be well coordinated, and supported by tools and methods to ensure satisfactory levels of productivity and quality. Accordingly, we have structured the area of embedded systems design into the following topics.

WP N°	WP title	Type of activity	Lead partic no.	Lead partic. short name	Person months	Start month	End month
WP0	Jointly-executed Programme of Management Activities (JPMA)	MGT	1	Floralis	51	1	48
WP1	Jointly-executed Programme of Integration Activities (JPIA)	RTD	1	UJF/ VERIMAG	327	1	48
WP2	Jointly-executed Programme of Activities for Spreading Excellence (JPASE)	OTHER	1	Floralis	106,75	1	48
WP3	Thematic Cluster: Modeling and Validation • *Activity: Modelling* • *Activity: Validation*	RTD	4	Aalborg	87,25	1	48
WP4	Thematic Cluster: Software Synthesis, Code Generation and Timing Analysis (JPRA) • *Activity: Software Synthesis, Code Generation* • *Activity: Timing Analysis*	RTD	10	Dortmund	79,25	1	48
WP5	Thematic Cluster: Operating Systems and Networks (JPRA) • *Activity: Resource-Aware OS* • *Activity: Scheduling & Resource Mgt* • *Activity: Embedded RT Networking*	RTD	24	SSSA-Pisa	73	1	48
WP6	WP6: Thematic Cluster: Hardware Platforms and MPSoC (JPRA) • *Activity: Platform and MPSoC Design* • *Activity: Platform and MPSoC Analysis*	RTD	13	DTU	80,5	1	48
WP7	Transversal Integration (JPRA) • *Activity: Design for Adaptivity* • *Activity: Design for Predictability and Performance* • *Activity: Integration Driven by Industrial Applications*	RTD	22	PARADES	109	1	48
	TOTAL				913,75		

1.3.4. Deliverables List

Del. no.	Deliverable name	WP no.	Nature	Dissem. level	Delivery date (proj.)
WP0: Joint Programme of Management Activities (JPMA)					
D-0.1-Y*n*	Project Management Report	WP0	**R**eport	**RE**stricted	
D-0.1-Y*n*	Project Activity Report	WP0	**R**eport	**RE**stricted	
WP1: Joint Programme of Integration Activities (JPIA)					
D-1.0-Y*n*	Integration Activities Report	WP1	**R**eport	**PU**blic	
WP2: Joint Programme of Activities for Spreading Excellence (JPASE)					
D-2.0-Y*n*	Spreading Excellence Report	WP2	**R**eport	**PU**blic	
WP3: Thematic Cluster: Modeling and Validation (JPRA)					*All these deliverables will be due at:*
D-3.1-Y*n*	Modelling Report	WP3	**R**eport	**PU**blic	
D-3.2-Y*n*	Validation Report	WP3	**R**eport	**PU**blic	
WP4: Thematic Cluster: Software Synthesis, Code Generation and Timing Analysis (JPRA)					
D-4.1-Y*n*	Software Synthesis, Code Generation	WP4	**R**eport	**PU**blic	T0+12
D-4.2-Y*n*	Timing Analysis	WP4	**R**eport	**PU**blic	T0+24
WP5: Thematic Cluster: Operating Systems and Networks (JPRA)					
D-5.1-Y*n*	Resource-Aware Operating Systems	WP5	**R**eport	**PU**blic	T0+36
D-5.2-Y*n*	Scheduling and Resource Management	WP5	**R**eport	**PU**blic	
D-5.3-Y*n*	Embedded Real-Time Networking	WP5	**R**eport	**PU**blic	T0+48
WP6: Thematic Cluster: Hardware Platforms and MPSoC Design					
D-6.1-Y*n*	Platform and MPSoC Design	WP6	**R**eport	**PU**blic	
D-6.2-Y*n*	Platform and MPSoC Analysis	WP6	**R**eport	**PU**blic	
WP7: Transversal Integration (JPRA)					
D-7.1-Y*n*	Design for Adaptivity	WP7	**R**eport	**PU**blic	
D-7.2-Y*n*	Design for Predictability	WP7	**R**eport	**PU**blic	
D-7.3-Y*n*	Industrial Integration	WP7	**R**eport	**PU**blic	

Where *n=1,2,3,4* for each end-of-year project review.

1.3.5. Workpackage Descriptions

WP0 Description - JPMA

WP number	0		**Start date or starting event:** T0 *(start of the project)*				
WP Title	**Jointly-executed Programme of Management Activities (JPMA)**						
Activity type	MGT *Management of the consortium*						
WP Leader	Liliane Pereira Bahia & Olivier GUERARD (Floralis)						
Participant number	1	2					
Participant short name	Floralis	UJF/VERIMAG					
Person-months per participant	37,50	13,50					

Objectives
The NoE Management organization is carried out through three activities: Strategic Management, Operational Management and Relations with the R&D Community at large.

Description of work

The Management Workpackage includes the Strategic Management and Operational Management activities. Floralis acts jointly with UJF/VERIMAG.

- Strategic Management
  - Yearly plenary meetings, at T0, T0+12, T0+24, T0+36, T0+48 will be organised, to plan the work in detail.
- Operational Management
  - Operational management implements the yearly plenary meeting decisions, and the setting up the infrastructure.
- Relations with the R&D Community at large
  - Direct interaction and relations with the community in the large are mainly handled by the ArtistDesign Office. The main strategic directions and orientations are decided the Strategic Management Board.

Deliverables

D-0.1-Y1 Project Management Report
D-0.1-Y1 Project Activity Report

D-0.1-Y2 Project Management Report
D-0.1-Y2 Project Activity Report

D-0.1-Y3 Project Management Report
D-0.1-Y3 Project Activity Report

D-0.1-Y4 Project Management Report
D-0.1-Y4 Project Activity Report

To ensure correct integration and coordination of Activities, and coordination between the partners, the Consortium will carry out a Joint Programme of Management Activities (JPMA). It includes 3 activities: Strategic Management, Operational Management, and Relations with the R&D Community at large.

Strategic Management

The ArtistDesign Strategic Management Board handles the major decisions of the NoE, in phase with the formal reviews of the European Commission (initial project kick-off, and annual reviews for JPA reporting and updating). The Strategic Management Board is composed of the following persons:
Joseph Sifakis (UJF/VERIMAG) - chair, Bruno Bouyssounouse (UJF/VERIMAG), Tom Henzinger (EPFL), Kim Larsen (Aalborg), Peter Marwedel (Dortmund), Reinhardt Wilhelm (Saarland), Giorgio Buttazzo (SSSA-Pisa), Alan Burns (York), Luis Almeida (Aveiro), Jan Madsen (DTU), Lothar Thiele (ETH Zurich), Luca Benini (Bologna), Karl-Erik Årzén (ULund), Bengt Jonsson (Uppsala), Alberto Sangiovanni Vincentelli (PARADES), Ed Brinksma (ESI), Albert Benveniste (INRIA)

Operational Management

The ArtistDesign Operational Management is carried out by the Executive Management Board and the ArtistDesign Office, acting in tight collaboration. The respective roles of these two bodies are:

- The Executive Management Board is a representative subset of the Strategic Management Board, where each cluster is represented by one leader. It meets on a roughly monthly basis, either via phone conference, or in person. It is composed of: *Joseph Sifakis (UJF/VERIMAG) - chair, Bruno Bouyssounouse (UJF/VERIMAG), Tom Henzinger (EPFL), Kim Larsen (Aalborg), Peter Marwedel (Dortmund), Giorgio Buttazzo (SSSA-Pisa), Jan Madsen (DTU), Karl-Erik Årzén (ULund), Bengt Jonsson (Uppsala), Alberto Sangiovanni Vincentelli (PARADES), Ed Brinksma (ESI).*
- The ArtistDesign Office ensures day-to-day management, including scientific, technical, legal, administrative, and financial activities. The Scientific Coordinator is Joseph Sifakis (UJF/VERIMAG). The Technical Coordinator is Bruno Bouyssounouse (UJF/VERIMAG). The legal, administrative and financial coordinators are Liliane Pereira Bahia and Olivier GUERARD (Floralis).

The ArtistDesign operational management implements the major decisions taken by the Strategic Management Board, and reports to it. It includes responsibility for the JPA, and monitors progress on a scientific and technical level. It validates the technical reports produced to the European Commission. The Executive Management Board submits proposals to the Strategic Management Board.

Relations with the R&D Community at large

Direct interaction and relations with the community in the large are mainly handled by the ArtistDesign Office. The main strategic directions and orientations are decided the Strategic Management Board.

The main effect of this activity is in coordinating and implementing the Jointly Executed Programme for Spreading Excellence (JPASE).

Relations with the R&D community at large are organized mainly bottom-up, through the organisation of scientific events, publications, distribution of tools and components, industrial partnerships (not funded by ArtistDesign), education; and through the ArtistDesign web pages.

Our policy aims specifically at enforcing integration of existing scientific events in the area, as was done in ARTIST2. An example is our participation in setting up the Embedded Systems Week. For sponsoring scientific events, we will apply the procedures developed in the ARTIST2 NoE (http://www.artist-embedded.org/artist/Allocating-JPASE-Funds.html).

WP1 Description - JPIA

WP number	1				**Start date or starting event:** T0 *(start of the project)*					
WP Title	**Jointly-executed Programme of Integration Activities (JPIA)**									
Activity type	RTD *Research and Technological Development*									
WP Leader	Bruno Bouyssounouse (UJF/VERIMAG)									
Participant number	2	3	4	5	6	7	8	9	10	11
Participant short name	UJF/VERIMAG	Aachen	Aalborg	Aveiro	Bologna	TUBS	Cantabria	CEA	DTU	Dortmund
Person-months per participant	19,50	8,25	9,25	6,00	15,25	9,50	10,25	9,00	7,25	17,25
Participant number	12	13	14	15	16	17	18	19	20	21
Participant short name	EPFL	ESI	ETH Zurich	IMEC	INRIA	TUKL	KTH	Linkoping	ULund	MDH
Person-months per participant	9,75	12,75	17,00	20,25	7,25	8,25	14,75	9,25	7,25	8,25
Participant number	24	25	26	27	28	29	30	31	22	23
Participant short name	Passau	SSSA-Pisa	Porto	Saarland	PLU-Salzburg	Uppsala	Vienna	York	OFFIS	PARADES
Person-months per participant	6,00	14,50	8,25	14,25	5,25	9,25	8,25	21,25	1	12.75

Objectives

The aim is to promote the integration of geographically dispersed teams. All these activities will have long-lasting effects, well beyond the duration of the initial EC funding.

Description of work

These activities include Joint Technical Meetings, Staff Mobility and Exchanges, Tools and Platforms, and an Intranet-based Infrastructure for Communication and Collaboration, as described in detail below.

Deliverables

Each deliverable is a report on the activity's work, provided yearly.

D-1.0-Y1 Integration Activities Report

D-1.0-Y2 Integration Activities Report

D-1.0-Y3 Integration Activities Report

D-1.0-Y4 Integration Activities Report

Joint Technical Meetings

This an indicative list of Joint Technical meetings planned by the ArtistDesign Thematic Clusters, and the Transversal Integration workpackage.

The ***Modelling and Validation*** cluster will hold an annual meeting at Embedded Systems Week. Each meeting will have two parts: an open scientific part (organized as the Workshop on Foundations and Applications of Component-based Design in conjunction with the ACM Conference on Embedded Software), and a closed organizational part. The meetings will be combined for both activities of the cluster. At each meeting, depending on the theme, we will invite selected people from other clusters.

The ***Software Synthesis, Code Generation and Timing Analysis*** cluster will organise the following meetings on Software Synthesis, Code Generation:

- The *Spring Activity meeting* typically takes place at the DATE conference. Its aim is to report on initial results generated for the work scheduled at the fall meeting. It is checked whether the goals set in the fall meeting are still met. If necessary, corrective actions are taken.
- The *Fall Activity meeting* will check the results of the previous year (if any) and to verify that the goals of the activity have been met. Also, this meeting is used to plan and schedule the work to be performed in the following year (if any). The partners use this meeting to schedule joint work and to make sure that overlaps are taken into account.
- The partners will typically attend the *SCOPES* workshop (http://www.scopesconf.org). The SCOPES workshop is the key event in Europe dedicated toward compilers for embedded processors. Many of the partners will actually be involved in organising the SCOPES workshop.
- Other meetings will be held between a subset of the partners. They will be centred on sub-topics of the activity, such as compilation for MPSoCs. They will be organized on a case to case basis.

It will also organise the following meetings on Timing Analysis:

- Joint meeting with the HW Platform & MPSoC and OS/Network clusters to discuss the topic of predictable MPSoC architectures, integrated timing analysis for time-triggered SoC, and operating systems design to support timing predictability. There will be a joint meeting with the Modelling & Validation cluster to discuss the possible connections between timing analysis on code level and timing analysis on model level.
- There will be an average of three internal meetings per year: spring, summer, and fall. The summer meeting will typically be co-located with the annual WCET Analysis Workshop, which typically is attended by most partners. Some internal meetings may be combined with the SS/CG part, as has happened within ARTIST2.
- The *WCET Tool Challenge* of ARTIST2 will be continued within ArtistDesign. This is a bi-annual event, where different timing analysis tools are evaluated with respect to different criteria on a well-defined set of benchmarks.

The ***Operating Systems and Networks*** cluster will organize the following meetings:

1. An inter-cluster meeting to discuss open issues for component-based operating systems to define features to be implemented and problems to be solved.
2. An activity meeting focusing on resource management to initiate the process of producing taxonomy of system resources and the analysis techniques available to manage their use.

3. A meeting on adaptive resource management at the operating system, network, programming language level co-organized with the Design for Adaptivity transversal activity.
4. A meeting to discuss the real-time scheduling algorithms for multi-core that should be recommended for standards, e.g. POSIX, Ada and Java.

The ***Hardware Platforms and MPSoC*** plans a joint technical meeting of the activity twice a year at one of the partner sites. Affiliated members and industry will be invited to discuss the current state of integration and future challenges.

In addition, we plan the joint organization of special workshops, tutorials and summer schools on MPSoC.

Especially for meetings with 'adaptivity vertical cluster': Define common terminology (run-time/design-time, online/offline, adaptive/self-adaptive, compile time/execution time, calibration/reconfiguration, etc.)

Besides these general meetings, there will be one-to-one meetings between the cooperating partners on specific issues and challenges. They should lead to joint tools and/or publications.

The ***Transversal Integration*** workpackage will organize the annual technical meetings on Integration Driven by Industrial Applications, Design for Adaptivity in Embedded Systems, and Design for Predictability.

Staff Mobility and Exchanges

This is an essential activity for integration within the NoE, including mobility of students and/or researchers, between core teams, or between core teams and affiliated teams. To encourage exchange between core teams and affiliated industrial teams, specific scholarships co-funded with industry will be set up.

Mobility should be justified by and refer to involvement in an activity from the JPRA or JPIA.

Tools and Platforms

The role of Tools and Platforms in the overall strategy of the NoE is described in Section B.1.2.1.

Intranet-based Infrastructure for Communication and Collaboration

The aim of this infrastructure is to ensure smooth collaboration and exchange of information between the ArtistDesign core and affiliated partners. This is also a tool for monitoring the progress of the work by the ArtistDesign Office and boards. Furthermore, selected information from the intranet may be used for dissemination purposes, through the web portal, as decided by the NoE management.

We will leverage on the existing ARTIST2 intranet infrastructure. It provides mailing list services, web publishing for events, internal communication services, templates for deliverables and presentations, standard sets of logos for ArtistDesign branding, directories of contact information.

All these features will continue to be developed and extended, within ArtistDesign.

WP2 Description – JPASE

WP number	2	**Start date or starting event:** T0 *(start of the project)*
WP Title	**Joint Programme of Activities for Spreading Excellence (JPASE)**	
Activity type	OTHER	
WP Leader	Bruno Bouyssounouse (UJF/Verimag)	

Participant number	1	2	3	4	5	6	7	8	9	10
Participant short name	Floralis	UJF/VERIMAG	Aachen	Aalborg	Aveiro	Bologna	TUBS	Cantabria	CEA	DTU
Person-months per participant	8,50	2,25	2,50	2,75	3,25	4,75	3,00	3,25	2,75	2,25
Participant number	11	12	13	14	15	16	17	18	19	20
Participant short name	Dortmund	EPFL	ESI	ETH Zurich	IMEC	INRIA	TUKL	KTH	Linkoping	ULund
Person-months per participant	5,25	3,00	4,00	5,25	6,25	2,25	2,50	4,50	2,75	1,50
Participant number	21	23	24	25	26	27	28	29	30	31	22
Participant short name	MDH	PARADES	Passau	SSSA-Pisa	Porto	Saarland	PLU-Salzburg	Uppsala	Vienna	York	OFFIS
Person-months per participant	2,50	4,00	1,75	4,50	2,50	4,25	1,50	2,75	2,50	6,50	1.50

Objectives

These activities are intended to spread excellence and structure the community at large. They are managed at the NoE level, and are mostly not specific to any cluster. The JPASE activities are planned by the Strategic Management Board, and are implemented by the Executive Management Board and the ArtistDesign Office.

Description of work

The JPASE activities consist of:

- Education and Training
- Publications in Conferences and Journals
- Industrial Liaison
- International Collaboration
- Web Portal

Deliverables

Each deliverable is a report on the activity's work, provided yearly.

D-2.0-Y1 Spreading Excellence Report
D-2.0-Y2 Spreading Excellence Report
D-2.0-Y3 Spreading Excellence Report
D-2.0-Y4 Spreading Excellence Report

ArtistDesign will leverage on the worldwide visibility of the ARTIST2 NoE. It is progressively creating a European embedded systems design community and spreading the “Artist culture” in all major research institutions.

To ensure that the next generation of researchers will continue in this direction we, as a consortium, will devote a great deal of effort to Spreading Excellence, in both academic and industrial circles. Furthermore, through our links with both core and affiliated partners, we will actively set up permanent links between industry and public research, based on existing partner collaborations with major industrial players in the area.

The JPASE activities are intended to spread excellence and structure the community at large. They are planned by the Strategic Management Board, and are implemented by ArtistDesign core and affiliated partners.

The NoE will leverage on its members and teams, who play a main role in the organisation of world-class scientific events, to disseminate results in the area. We expect that the NoE’s structured and authoritative dissemination will have a strong effect on the community as a whole, for orienting and creating synergy for research.

Education and Training

We distinguish between Global, and Thematic Education and Training activities.

Global Education and Training Activities

- Courseware – The NoE has the ambition to serve as a resource and point of reference for the area, including by collecting and disseminating course materials for teaching embedded systems design.
- Graduate Studies – The NoE will provide support for selected graduate studies programmes, as the means for training engineers and researchers in embedded systems design.
- Summer Schools – The NoE will actively support and participate in summer schools and seminars in embedded systems design.
- International Workshop on Embedded Systems Education – We will continue this series of international workshops, started in ARTIST2. York has accepted to lead this activity.
- Implement a high-visibility International Summer School. The ArtistDesign NoE will organise each year a high-visibility international Summer School, drawing top European lecturers in Embedded Systems Design. The audience is researchers, PhD students, and engineers. The following group of core partners will lead this activity: Luca Benini (Bologna), Giorgio Buttazzo (SSSA-Pisa), Petru Eles (Linkoping), Kim Larsen (Aalborg), Peter Marwedel (Dortmund).
- Training Engineers – Many partners are already active in this area, such as IMEC, EPFL, ESI, and Aalborg’s CSI. The ArtistDesign NoE will provide logistical, financial dissemination through the Web Portal and newsletter.

Thematic Education and Training activities

The *Modelling and Validation* cluster aims at organizing a yearly PhD-school disseminating the most promising, state-of-the-art techniques from partners of the cluster or other clusters. Similar schools were previously held in Nässlingen, Sweden (2005) and Trento, Italy (2007).

The fourth edition of the international summer school on MDD for DRES is scheduled for September 2008 (http://www.mdd4dres.info/).

The *Software Synthesis, Code Generation and Timing Analysis* cluster partners have frequently taught or will teach at summer schools, including the ARTIST spring school in China in 2006, the ARTIST2 MOTIVES summer school in 2005 and spring school in 2207, the ACASES summer school in 2006 and 2007 (see http://www.hipeac.net/summerschool) and the Kubiq summer school of the network on knowledge discovery in ubiquitous systems in 2006 and 2008. This effort will be continued and it can be expected that the partners will teach at least two summer schools per year.

Partners at the University of Dortmund have published an introductory book on “embedded system design” (this is also the title). The book is used for embedded system education on all (inhabited) continents. It can serve as an initial guideline for designing embedded system curricula.

Partners at the University of Dortmund and Aachen jointly are contributing towards education and training at ALARI (Lugano, see http://www.alari.ch). There, they are jointly holding a course on retargetable compilers and embedded processor design. They are also both teaching in the “Embedded Programmable System Design” course organized by EPFL in September (see http://www.mead.ch/htm/ch/EPSD-Program.html). This course typically has a very good set of industrial attendees.

Aachen is also contributing to the teaching program of the Thai German Graduate School (TGGS) and provides EDA tool trainings and support for its research partners. Furthermore, Aachen will continue to offer tool trainings to other teams interested in embedded processor and MPSoC design and compilers (such as LISATek).

There will be training workshops on timing analysis and time-predictable MPSoC architectures.

The *Operating Systems and Networks* cluster will organise Graduate Courses, summer schools, and tutorials on Real-Time Systems Development, OSEK Compliant Real-Time Kernels, Real-Time Distributed Systems and Networks, Real-Time Control, and Adaptive Resource Management.

They will also develop an educational kit for embedded systems, based on Microchip dsPIC technology, consisting of a number of modules that can easily be composed depending on specific application purposes. We plan to develop a set of libraries to simplify the access to the hardware devices (sensors, servomotors, wireless modules) and a number of sample real-time control applications that can be easily replicated by the users.

The idea is to build a community within ARTIST to develop: tools for design and development embedded systems; libraries to simplify the access to the hardware devices (sensors, servomotors, wireless modules); a number of sample real-time control applications that can be easily replicated by the users.

The *Hardware Platforms and MPSoC* cluster will integrate other European research groups and industry into the activities as associated partners. Examples are ESI (Embedded Systems Institute, Eindhoven), STM Research Division. In addition, we will involve major research groups in US and Asia, for example Rajesh Gupta (UC San Diego - US), Jan Rabaey (UC Berkeley - US), Preete Panda, Duoli Zhang, Masaharu Imai (Osaka Uni. - Japan), Hiroto Yasuura (Kyushu Uni. - Japan), Tsuyoshi Isshiki (Tokyo - Japan), Anshul Kumar (IIT Delhi - India), M. BalaKrishnan (IIT Delhi - India).

Sharon Hu, Univ. Notre Dame, USA, academic affiliate will include its solutions to work optimization.

Publications in Conferences and Journals

The ArtistDesign consortium is very active in publishing in scientific journals and conferences, as attested by the list of significant publications by the partners' teams.

Here is also an indicative list of conference and journals, in which the ArtistDesign partners publish on a regular basis, per cluster. In most of these, the ArtistDesign partners play a leading role, as organisers, members of the programme committees and editorial boards.

The *Modelling and Validation cluster* participates in organising ACM Symposium on Embedded Software (EMSOFT), ACM Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES), ACM Transactions on Embedded Systems, Formal Methods in System Design, IEEE Conference on Quantitative Evaluation of Systems (QEST), IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), IEEE Real-Time Systems Symposium (RTSS), International Conference on Computer Aided Verification (CAV), International Conference on Concurrency Theory (CONCUR), International Conference on Dependable Systems and Networks (DSN), International Conference on Formal Modeling and Analysis of Timed Systems (FORMATS), International Conference on Hybrid Systems -Computation and Control (HSCC), International Conference on Computer Safety, Security, and Reliability (SAFECOMP), International Conference on Tools and Algorithms for the Construction and Analysis of Systems (TACAS), Real-Time Systems Journal.

Partners in the "*Software Synthesis, Code Generation and Timing Analysis*" activity typically publish at the following conferences and in the following journals: Design, Automation and Test in Europe (DATE); Design Automation Conference DAC); Asia-South Pacific Design Automation Conference (ASPDAC); Embedded System Week, comprising the ISSS/CODES and CASES conferences, and ESTIMEDIA, CASA and WASP workshops; Workshop on Software and Compilers for Embedded Systems (SCOPES); ACM Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES); Journal on Design Automation of Embedded Systems (DAEM); IEEE Transactions of CAD (TCAD); IEEE Transactions on VLSI (TVLSI); ACM Transactions on Embedded Computing Systems (TECS); ACM Transactions on Design Automation of Electronic Systems (TODAES); Journal of Embedded Computing (JEC); Real-Time Systems Symposium (RTSS); Euromicro Conference on Real-Time Systems (ECRTS); Journal of Real-Time Systems.

The "*Operating Systems and Networks"* cluster members will publish in international conferences, such as ECRTS, RTSS, RTAS, EmSoft, ETFA, WFCS, RTNS, SIES. They will also edit Special Issues in journals such as: IEEE Transactions on Computers; Real-Time Systems; ACM Transactions on Embedded Computing; IEEE/IES Transactions on Industrial Informatics.

The "*Hardware Platforms and MPSoC*" members' results and progress shall be demonstrated at the annual DATE university booth. Together with the industrial and affiliated partners workshops will be organized where the progress is shown to industrial tool users. This will foster the discussion between industrial designers and the partners. At least one common tutorial at a major event shall be proposed. Several joint papers are planned explaining the integrated tools and methods. Publications and demonstrations will show new ways to use the new tools in the context of industrial design. The results shall be used in further more design oriented projects with industrial partners. The results shall be presented at major educational events, such as the annual MPSoC summer school. Last not least, the new methods shall be included in the embedded systems curriculum.

In addition, we intend to establish a summer school on MPSoC which will be targeted primarily towards PhD students. Last not least, the new methods shall be included in the embedded systems curriculum.

The "*Industrial Liaison*" cluster members, which include all the ArtistDesign partners, have a very strong degree of interaction with major industrial companies in the area.

The NoE will leverage on its members and teams, who are strongly implicated in collaboration with industry, to organize and structure industrial relations, and develop mutually beneficial interactions. Furthermore, through Industrial Liaison, ArtistDesign will receive useful feedback about the relevance of work directions and priorities.

We will follow the approach initiated in the ARTIST2 NoE, which organized high-level technical meetings open to industry, such as "Beyond Autosar", "ARTIST2 meeting on Integrated Modular Avionics". ArtistDesign will organize similar technical meetings, to present and discuss its views and results, as well as their adequacy with respect to emerging industrial needs.

Furthermore, ArtistDesign will seek a tight interaction with the Artemis community, through the **Artemisia Liaison Task Force**. This is composed of the following prominent ArtistDesign members, also active in ARTEMIS/ARTEMISIA: Luca Benini, Ed Brinksma, Werner Damm, Jean-Luc Dormoy, Rudy Lauwereins, and Joseph Sifakis. Amongst these, 3 are elected members of the ARTEMIS Steering Board. Joseph Sifakis is the chair of ARTEMISIA's Chamber B.

ArtistDesign partners will be encouraged to join ARTEMISIA.

The ArtistDesign has more than 25 industrial affiliated partners. The list of industrial affiliated partners and their roles is provided in the description of WP3. They serve as an efficient relay for transferring the JPRA research results to the wider industrial community, as they actively participate in the technical work and meetings.

The ArtistDesign "*International Collaboration*" activities will allow ArtistDesign to be visible internationally, and to monitor the evolution of the state of the art in the area worldwide. This ArtistDesign activity will build on the very successful ARTIST FP5 and ARTIST2 NoE International Collaboration activities organised in 2002-2006.

In ArtistDesign, we will continue in this direction. The objective is now to launch joint projects between IST and equivalent funding agencies, such as NSF, DARPA. Another objective is to reach the same level of dialogue with funding agencies in Asia.

The NoE will leverage on past ARTIST FP5 & FP6 experience in International Collaboration, and also on its members' and teams' contacts, to promote a structured approach to International Collaboration, particularly with the USA and Asia.

The International Collaboration workplan consists of Global International Collaboration Activities, organized by the NoE management, and Thematic International Collaboration activities, organized by the clusters.

Overall, the ArtistDesign NoE will define processes for interaction between the European R&D community, and the main international players in the area, including research institutions, professional organisations (ACM, IEEE), standardisation bodies (e.g.: OMG, IEEE), large consortia, funding agencies (e.g.: NSF, DARPA).

- Ensure awareness of European research about main research trends and to benefit from advances occurring in other parts of the world.
- Disseminate European know-how in the area, thus influencing trends beyond Europe's borders.
- Enhance the attractivity of Europe for top students and researchers.

International Collaboration should fit into a global win-win strategy for achieving the participants' long-range aims. Examples of activities include:

- **High-level meetings** gathering top representatives from industry, funding agencies, and research, to discuss avenues for International Collaboration, including on R&D

and standards e.g. IST/NSF Workshop on Component-based Engineering (Paris, June 05).

- International Collaboration **Working Groups** for exploring possible avenues for research and education in a chosen topic and producing white papers and reports e.g. joint EU/US Working Groups: on Timing Validation, Adaptive Real-Time Systems for Dynamic Applications, Semantic Platform for Hard Real Time (2002 – 2003).
- Organization and sponsoring of international conferences and schools, to disseminate recent research results, and promote the emergence of embedded systems as a discipline e.g. Embedded Systems Week, New Jersey, October 2005.
- International Collaboration **Publications**.
- **Joint international projects**. Set up joint collaborative projects e.g. Columbus project or extend existing projects, by allotting them an extra budget.

International Collaborations is implemented mainly in collaboration with the USA, building on existing links between IST and the US funding agencies (mainly NSF).

ArtistDesign will leverage on and extend the successful International Collaboration activities initiated in the ARTIST2 NoE. These include an annual Summer School in China (http://www.artist-embedded.org/artist/-Artist2-UNU-IIST-School-in-China-.html) and Latin America (http://www.artist-embedded.org/artist/-First-European-SouthAmerican-.html), yearly high-level meetings with the NSF (http://www.artist-embedded.org/artist/Joint-US-EU-TEKES-workshop.html), and yearly International Workshops on Education (http://www.artist-embedded.org/artist/WESE-06-Embedded-Systems-Education.html).

Web Portal

The ArtistDesign Web Portal, complemented by the ArtistDesign Newsletter, is a major tool for Spreading Excellence within the Embedded Systems Community. It aims to be the focal point of reference for events and announcements of interest to the embedded systems community.

This will play a key supporting role for collaboration and Integration, such as interaction between clusters, management information, such as scholarships, internal events, and progress of the work. The web portal will also be used to disseminate any relevant information to the community at large. We believe the web portal will be an essential mechanism for achieving integration.

It will act as a repository of knowledge in the area, including courseware, information about standards, methods and tools, research publications and results. This web portal will be made available within the NoE core and affiliated partners, and also to other parties according to modalities to be defined.

This repository will be the reference for the embedded systems design community. It will build on the existing ARTIST2 Portal, which includes several features that help keep it coherent and up to date:

- Authorised users (principally, the ARTIST2 partners) can access the back end of the site to modify and update information directly. The changes are immediately visible on the site, which greatly streamlines the updating process.
- It's possible to track changes and go back to previous versions of individual web pages.
- Events are automatically sorted by date, and transferred to 'Past Events'. When appropriate.
- Structural information (hierarchy of pages) is maintained automatically.
- Ergonomics are set for the entire site. The "look and feel" of the site is always homogeneous throughout the site. It's possible to change these ergonomics, and

these changes are applied homogeneously throughout the site, via automated mechanisms.

The ArtistDesign Web Portal will offer information about:

- **Workshops, Conferences, Schools and Seminars**
  Provide information about the main scientific events in the area, and in particular those organised by ArtistDesign.
- **International Collaboration**
  Advertise the ArtistDesign International Collaboration events, and provide pointers to the most visible International Projects (either about significant projects outside Europe, or joint International Collaboration projects.
- **Publications**
  Publications from core partners, with emphasis on Position Papers, White Papers, etc. that may have a particularly deep impact.
- **Course Materials Available Online**
  The web portal will centralize course materials from as many sources as possible, to make them available to the general public.

With respect to the ARTIST2 web infrastructure, the following improvements and extensions will be implemented:

- Intranet
  - **Web-based Reporting**
    The initiative started in Y3 of ARTIST2 will be generalized, so that wherever possible, the partners will be able to report on advancement using a web-based interface.
  - **Group Workspace**
    We will investigate possibilities for implementing group workspace services, such as shared files, shared calendars, etc.
- Web Portal
  - **Calendar of Events**
    A calendar-based view of events in the area will be implemented.
  - **Interface with Google Maps**
    An interface based on Google Maps would be provided, showing where the main activities per topic are located. This would cover labs in Europe as well as our International Collaboration partners.
  - **Announcements archive**
    The current ARTIST Mailing List would be expanded, to include automatic archiving, and availability via the ARTIST Web Portal.

Communication to the general press

ArtistDesign core partners have a strong tradition of communication to the general press.

As was done at the start of ARTIST2, ArtistDesign will hold a press conference to announce the start of the NoE, and to disseminate information about:

- the overall structure and objectives of the NoE
- the ArtistDesign Consortium, including contact points
- the expected impacts for the general public
- the strategic interests for the ArtistDesign partners

Newsletter

As was initiated within ARTIST2, the ArtistDesign NoE will publish a high-quality newsletter (latest issue: http://www.artist-embedded.org/artist/Artist2-Newsletter,438.html).

WP3 Description - Modeling and Validation

WP number	3	**Start date or starting event:** T0 *(start of the project)*				
WP Title	**Thematic Cluster: Modeling and Validation (JPRA)**					
Activity type	RTD *Research and Technological Development*					
WP Leader	Kim Larsen (Aalborg)					
Participant number	2	4	9	12	13	16
Participant short name	UJF/VERIMAG	Aalborg	CEA	EPFL	ESI	INRIA
Person-months per participant	17,50	11,50	6,50	9,75	6,50	6,50
Participant number	18	22	23	28	29	
Participant short name	KTH	OFFIS	PARADES	PLU-Salzburg	Uppsala	
Person-months per participant	6,50	3,00	6,50	6,50	6,50	

Objectives Establish a coherent body of modelling formalisms that support the component-based design and automatic analysis of embedded systems.

Description of work

Activity "Modeling" will focus on :

- Component modelling
  the study of composing models with heterogeneous semantics based on their interfaces
- Resource modelling
  the study of mapping abstract models to resource-constrained implementation platforms
- Quantitative modelling - the study of models that quantify timing, uncertainty, and reliability constraints

Activity "Validation":

- Compositional validation
  the design of verification algorithms and tools that scale by combining results about individual components of a complex system
- Quantitative validation - the design of verification algorithms and tools for stochastic, real-time, and hybrid systems
- Cross-layer validation - the design of algorithms and tools for the synthesis and verification of implementations from specifications. Lectures and publications at workshops, conferences, and journals. Integration of different modelling and verification tools.

Deliverables

Each deliverable is a report on the activity's work, provided yearly.

D-3.1-Y1 Modelling Report
D-3.2-Y1 Validation Report
D-3.1-Y2 Modelling Report
D-3.2-Y2 Validation Report
D-3.1-Y3 Modelling Report
D-3.2-Y3 Validation Report
D-3.1-Y4 Modelling Report
D-3.2-Y4 Validation Report

Overall Objective

The sheer complexity of future embedded devices seriously challenges current development practice; new, integrated and scalable methods are urgently needed. The use of *model-driven* and *component-based* approaches are seen as a way of obtaining dependable embedded implementations with high performance and with reduced time and cost.

Embedded systems involve monitoring and control of complex physical objects or phenomena using a number of dedicated hardware and software components often within a networked solution. Therefore, the use of models, analysis techniques and supporting tools span the areas of control theory, computer science, hardware, networks and even mechatronic all well established research areas which however – by and large – have been developed independently. This has the unfortunate consequence that it often becomes impossible to state, not to mention validate, overall properties of an embedded system.

Overall objectives of the cluster are:

1. Establish a coherent family of modelling formalisms spanning the areas of computer science, control, hardware and networks covering all aspects of embedded systems.
2. Development and combination of efficient means for analysis of models including simulation, testing, static analysis, model-checking, run-time verification, monitoring, diagnosability, controller synthesis.
3. Emphasis on support for compositional methodologies in terms of allowing new complex systems to be assembled from already constructed and validated components.
4. Realization of coherent tool chain obtained by adjusting and combining the models and tools from the different research areas. This will provide the basis for a cost-efficiency development process allowing for early design-space exploration and verification as well as reduce the sizeable amount of final testing-time and –cost.
5. Interaction with the Activities in the Transversal Integration workpackage on validating the formalisms and tools through real industrial development projects and case studies.

Indicators for Integration

Interactions planned between partners include:

- Connections to SPEEDS; UPPAAL & RAPTURE & MODEST; Metropolis and HDL (Giotto); UPPAAL & IF; ARTS & UPPAAL (from simulation to verification); TrueTime.
- 10 Joint publications between partners/year
- 2 open workshops / year
- Connections between tools of partners; joint meetings.

JPRA Activity: "Modeling"

Core Teamleaders

Tom Henzinger (EPFL - Switzerland)*;* Kim Larsen (Aalborg - Denmark), Alain Girault (INRIA - France); Martin Törngren (KTH - Sweden) *;* Werner Damm (OFFIS - Germany); Christoph Kirsch (PLU-Salzburg - Austria); Bengt Jonsson (Uppsala - Sweden); Joseph Sifakis (UJF/VERIMAG - France) Sébastien Gérard (CEA - France); Ed Brinksma (ESI - Netherlands); Alberto Sangiovanni-Vincentelli (PARADES - Italy)

Affiliated Teamleaders

Pierre Wolper (CFV - Belgium)*;* Yiannis Papadopolous (Hull - United-Kingdom); Simin Nadjm-Tehrani (Linkoping - Sweden); Marta Kwiatkowska (Oxford - United-Kingdom)*;* Henrik Lönn (Volvo Technology - Sweden); Johan Lilius (Turku Centre for Computer Science, and Deparment of Information Technologies, Åbo Academi – Finland); Jan-Friso Groote, Jos Baeten, Henk Corporaal (Eindhoven University of Technology); Mariëlle Stoelinga, Boudewijn Haverkort, Pieter Hartel (University of Twente); Arie van Deursen, Arjan van Gemund, Henk Sips (Delft University of Technology); Joost-Pieter Katoen (Aachen - Germany); Christel Baier (Dresden - Germany); Francois Laroussinie (LSV Cachan - France); Roberto Passerone (University of Trento - Italy); Tiziano Villa (Verona - Italy)

Policy Objective

Unlike other computer systems, embedded systems are strongly connected with a physical environment. A scientific foundation for embedded systems must therefore deal simultaneously with software, hardware resources, and the physical environment, in a quantitative manner. In order to gain independence from a particular target platform, embedded system design must be model-based. In order to scale to complex applications, embedded system design must be component-based. The overall objective of this activity is develop model and component based theories, methods, and tools that establish a coherent family of design flows spanning the areas of computer science, control, and hardware. The activity brings together the most important teams in the area of model and component based design in Europe.

Background

An important class of model-based methodologies is those based on a synchronous execution model. The synchronous languages, such as Lustre, Esterel, and Signal, embody abstract hardware semantics (synchronicity) within different kinds of software structures (functional; imperative). Implementation technologies are available for several platforms, including bare machines and time-triggered architectures. Other model-based approaches are built around a class of popular languages exemplified by Matlab Simulink, whose semantics is defined operationally through its simulation engine. Originating from the design automation community, SystemC also chooses synchronous hardware semantics, but allows for the introduction of asynchronous execution and interaction mechanisms from software (C++). Implementations require a separation between the components to be implemented in hardware, and those to be implemented in software; different design-space exploration techniques provide guidance in making such partitioning decisions. More recent modelling languages, such as UML and AADL, attempt to be more generic in their choice of semantics and thus bring extensions in two directions: independence from a particular programming language; and emphasis on system architecture as a means to organize computation, communication, and constraints.

Model-based design relies on the separation of the design level from the implementation level, and is centred around the semantics of abstract system descriptions rather than on the implementation semantics. Design often involves the use of multiple models that represent different views of a system at different levels of granularity. Usually design proceeds neither strictly top-down, from the requirements to the implementation, nor strictly bottom-up, by integrating library components, but in a less directed fashion, by iterating model construction, model analysis, and model transformation. Some transformations between models can be automated; at other times, the designer must guide the model construction. While the compilation and code generation for functional requirements is often routine, for non-functional requirements, such as timing, the separation of human-guided design decisions from automatic model transformations is not well understood. Indeed, engineering practice often relies on a trial-and-error loop of code generation, followed by test, followed by redesign (e.g., priority tweaking when deadlines are missed).

We believe that existing model-based approaches will ultimately fall short, unless they can draw on new foundational results to overcome the current weaknesses of model-based design, such as the lack of analytical tools for computational models to deal with physical constraints and quantitative metrics; and the difficulty to automatically and compositionally transform non-computational models into efficient computational ones. This leads us to the key needs for a better understanding of component modelling, resource modelling, and quantitative modelling.

Technical Description: Joint Research

The joint research falls into the following three sub-activities.

Sub-activity A: Component Modeling
Large embedded software systems are developed by distributed teams belonging to a number of different organizations. This calls for methods and techniques that split the design into smaller sub-systems and clarify the responsibilities for each participant. Theories of interfaces and contracts are needed to support these requirements and encompass functional, performance, resource, and reliability viewpoints. Additionally, we need to deal with the ability to integrate component-based system engineering within model-driven approaches. That means at least to work on refinement issues with regard to the component paradigm in order to benefit its full power with model-driven processes which are basically iterative design processes.

We currently have a dichotomy between operational and transformational modelling approaches. Operational means automata-based: these approaches work on a component level, and have been successful in model checking, protocol verification, and code generation. Transformational means stream-based: these approaches work on the system level, and have been successful in performance analysis. While operational approaches have difficulties to scale to systems, transformational approaches suffer a loss of precision. We plan to develop techniques for bridging and combining both approaches.

Sub-activity B: Resource Modeling
Embedded software design differs from other software design in that behavioural properties must be reconciled with resource constraints. This is best done within models that permit the exploration of trade-offs between multiple dimensions, such as functionality, reliability, performance, and resource consumption. This ability must be carefully balanced against the need to separate concerns as much as possible. We expect different formalisms to be appropriate for different purposes, such as time-power trade-offs in power-constrained computing. The relevant dimensions (e.g., time and power) must then be captured within interfaces (sub-activity A) in order to support component-based design.

Complex embedded systems are built around specific distributed architectures and networks (e.g., Arinc, CAN, and FlexRay). Efforts have been undertaken to abstract such architectures as Models of Computation and Communication (MoCC): time-triggered, event-triggered, loosely time-triggered, etc. Research must further study these MoCCs to clarify their relationships, invent new ones with new interesting features, identify their basic building blocks, and find out how generic services can be built on top of them.

Sub-activity C: Quantitative Modeling
Many classical formalisms are Boolean: a temporal specification is either satisfied or not satisfied; a real-time deadline is either met or not met. This type of worst-case reasoning is not helpful in practical situations, where a system designer has to choose from a number of alternatives, none of them perfect, but some better than others. We propose to further develop quantitative theories of executable systems, together with rational criteria for making design decisions. In such theories, Boolean-valued system properties are replaced by real-valued rewards (or costs), and Boolean-valued refinement relations are replaced by real-valued similarity metrics.

Quantitative models are also required for modelling stochastic behaviour, real-time behaviour, and hybrid (mixed discrete-continuous) behaviour. Our current models for such systems (Markov processes; timed automata; hybrid automata) tend to be brittle and overly sensitive towards arbitrarily small numeric perturburances. We need robust models for stochastic, timed, and hybrid systems.

Four-Year Work Programme

We expect the following results from the three sub-activities:

Sub-activity A: Component Modeling
We will focus on heterogeneous models of computation and communication (MOCCs), as well as interfaces and contracts for components. We plan to relate various existing models at a semantic level. Based on these insights, we plan to develop methods and tools for consistently combining heterogeneous models and their properties. We will derive property preserving transformations between different classes of models, e.g., between stream-based analytical models and automata-based executable models. In particular, we will develop code generation techniques from application models to models of various target platforms.

In the first 18 months, the core partners will perform the following tasks:

- EPFL will develop rich interface theories for component-based design. Such interfaces expose non-functional information about components, such as resource consumption and reliability metrics. The interfaces will support algorithms for compatibility checking and refinement.
- Aalborg will work on compositionality for real-time systems: in the first 18 months, it will develop on a compositional method for networks of timed automata and timed temporal logic (timed modal mu-calculus). Also, a timed extension of the interface theory based on modal I/O transition systems will be developed.
- INRIA will provide a generic algebra of contracts setting assumptions, promises, and responsibilities; meaning of a set of contracts attached to a component; an algebra of components, across viewpoints (functional, performance, resource, and safety; and a generic contract manipulation engine implementing the above algebra and submitting proof and/or synthesis obligations to viewpoint specific engines.

- INRIA will propose a language for COTS-based design (Components-Off-The-Shelf), able to express the real-time properties of the components and the interactions between the components. In particular, this language will give to user the possibility to express mandatory interactions (uncontrollable) and optional interactions (controllable). An incremental adaptor synthesis method will also be proposed, in order to solve the incompatibilities between the components, based on discrete-controller synthesis techniques.
- INRIA plans to define a contract-based module language using Polychrony as model of computation. This task contributes to the effort on algebras for interfaces and contracts by considering the symbolic, relational model of time of the polychronous model of computation as a possible viewpoint instance. The polychronous model of computation will be used to express the assumptions and guarantees of possibly heterogeneous and foreign components. The language will use these contracts to construct proof obligations, and to assess the consistency of the modelled architecture. The proof obligations will take the form of abstract Signal specifications; they will be given to Polychrony's built-in static analyzer or model-checker for the purpose of validation. Also constructed from contracts will be an executable Signal specification, to schedule the execution of the heterogeneous components. This will provide a means for automatically constructing a system-level simulator given the modular, contract-based description of an architecture.
- KTH will develop embedded systems ontology as a basis for systems design, and as a means to integrate domain models (Simulink, UML, and AADL) and analysis techniques (such as model checking, safety analysis, and timing analysis). The ontology will be captured as a UML-profile. The ontology will be used as a framework for relating and mapping different concerns and modelling techniques. Transformations to selected UML models, Simulink, and reliability/safety models will be developed. In developing embedded systems, a number of different behavioural models are needed, at different levels of abstraction, including environment models and embedded systems internal models for nominal as well as abnormal system behaviour, all involving different models of computation and communication. The enrichment of the ontology to cover behavioural models of different types and their relations will be investigated.
- KTH will further develop the ForSyDe modelling framework. ForSyDe combines the operational and the transformational modelling approach in that its elements, the processes, are modelled as automata, and they communicate with each other via streams. It plans to extend ForSyde to cover all major MOCCs from untimed to continuous time. This will allow the modelling of heterogeneous systems that consist of continuous time, discrete time, synchronous time, and untimed sub-systems. It will also develop concepts and techniques to model adaptivity in a systematic way at the system level. Reconfigurability and programmability are special cases of adaptivity.
- OFFIS will work on a tool-independent meta-model for heterogeneous rich component models allowing the specification of non-functional characteristics, which will be used as the basic for analysis techniques. It will in particular work on concepts related to a safety viewpoint, to provide a contract-based compositional framework for safety analysis.
- PARADES in collaboration with University of Trento will develop heterogeneous modelling techniques using conservative approximations to guarantee system properties. We also plan to develop techniques for transformation of models based on the concept of a common semantic domain. Further, we plan to implement these techniques in the form of translators in an appropriate executable framework, such as Metropolis, to mediate communication and scheduling between the different models. We also plan to develop tools for checking compatibility and substitutability for contracts and interfaces. Finally, we plan to investigate ways of synthesizing a contract given a context and a global specification. This work will naturally interface with the work of UJF/VERIMAG, INRIA, ETH Zurich, ESI and PLU-Salzburg.

- PLU-Salzburg plans to enhance the existing support of Giotto semantics in the exotask system. Giotto is a real-time programming language for the design and implementation of portable and efficient control software. For example, there is a prototypical implementation of helicopter flight control software in Giotto. However, the current system only performs low-level flight control and lacks high-level functionality such as flight navigation and data collection, which is necessary for fully autonomous flight. A key problem that needs to be addressed in the current system is therefore a broader design of the exotask modelling, validation, and scheduling components. Non-trivial real-time applications such as fully autonomous flight typically consist of a variety of challenging sub-problems that require an integration of modelling and programming semantics at potentially different levels of abstraction. While low-level aspects that require deterministic timing such as flight control can readily be expressed in Giotto, more high-level aspects such as flight navigation and data collection may be modelled more naturally in other models. Since the exotask system is specifically designed to be extensible by pluggable schedulers, other models may easily be integrated.
- Uppsala will develop techniques for transformations between operational automata formalisms and more abstract (stream-based) formalisms for expressing functional, timing, and resource properties. This is a basis for connecting component specifications and system-level properties in a compositional and scalable way.
- UJF/VERIMAG will investigate relations between sub-classes of component-based systems in the BIP modelling framework. This framework allows the representation of a system as a point in a three-dimensional space: Behaviour x Interaction x Priority. The main idea is to study transformations relating classes of systems e.g. untimed and timed systems, event triggered and data triggered, synchronous and asynchronous. These transformations and their properties will be used to characterize Models of Computation studied by other teams (INRIA, PARADES, and EPFL).
- CEA will investigate, on the basis of the Marte standard, the possibility to define a MoCC design workbench which could provide a full framework for specifying and designing MoCCs and their relationships for dealing with heterogeneous models. CEA will also provide an associated formal framework to specify heterogeneous system by defining structuring mechanisms of MoCCs.
- ESI will work on frameworks for heterogeneous modelling based on its industrial collaborations with a.o. ASML, NXP and Philips Medical Systems. In particular we will address the scalability and the use approximate abstractions to overcome complexity. We will work with other teams (Aalborg, EFPL, OFFIS, PARADES) to see how different MoCCs perform in this respect.

Sub-activity B: Resource Modeling

We will focus on incorporating resource constraints into MOCCs, and on architecture exploration. We plan to explore modelling techniques that encompass resource (memory, time, power) constraints at various abstraction levels. Based on these techniques, we will develop implementation mappings that preserve high-level resource assumptions. We will develop compositional techniques for reasoning about resources, and design-space exploration techniques for the quantitative comparison of different architectures with respect to their resource demands.

In the first 18 months, the core partners will perform the following tasks:

- Aalborg will work on MPSoC modelling: In the first 18 months, together with the Execution Platform cluster, it will investigate efficient modelling of multi-processor systems-on-chip using the timed automata based formalisms of UPPAAL.

- EPFL will develop a theory of component interfaces that expose resource information, and compatibility checking for such interfaces; implementation mappings that preserve high-level resource assumptions; and compositional proof rules about resources.
- INRIA will study, design, and implement architectures based on communication-by-sampling. Within the SynDEx tool and associated AAA methodology, resource models will be taken as input in order to optimize distributed scheduling using quantitative data. Besides, Simulink models will be compiled into Lustre in order to give a precise semantics to Simulink models. Then deployment techniques of Simulink models onto communication-by-sampling architectures will be studied, thanks to their prior translation into Lustre. This code generation scheme shall be suited to Simulink models as general as possible, in particular models involving control tasks both with periodic clocks and triggered by sporadic events.
- KTH will develop approaches for dynamic modelling of network and communication resources will be developed. Design of networked control protocols using cross-layer optimization techniques will be pursued, considering trade-offs between event-triggered and time-triggered control techniques. Architectural design of embedded systems takes place on different levels of abstraction, and can concern a number of different qualities of concern (e.g. cost, performance, reliability and flexibility) as well as strategic engineering concerns. A number of techniques have been proposed over the years, including decision and exploration techniques. The decisions can be qualitative (e.g. ATAM) and/or quantitative (figures of merits, different approaches to weighting of qualities, or pareto-optimal techniques). KTH intends to develop a survey and comparison of different approaches and to place them in the context of embedded systems design.
- OFFIS will develop hierarchical architectural abstraction models for system architectures as a basic for design space exploration with refinements.
- PARADES will pursue design-space exploration with quantitative comparisons; automatic mappings of functionality to implementations; and multi-processing architecture modelling using common semantic domains. We also plan to run case studies of architectural exploration in the context of software defined radios using multiprocessor and DSP architectures. We plan to verify part of this exploration by implementing the software in the real architecture. We further plan architecture exploration of other constrained systems, such as wireless sensor nodes.
- PLU-Salzburg plans to add support for reliability modelling to the Giotto/HTL portion of the exotask system. HTL is a hierarchical coordination language that supports refinement of timing and data dependency aspects of real-time tasks. The key result is that any concrete HTL program is schedulable if it refines a schedulable abstract HTL program. Checking schedulability of abstract programs may be simpler than of concrete programs, and checking refinement is simpler than checking schedulability. Reliability modelling in HTL should support similar refinement relations. For example, a concrete HTL program should be implementable on a given architecture with a given reliability if it refines an abstract HTL program that can be implemented on that architecture and that reliability.
- Uppsala will develop techniques for expressing the correlation between resource and timing properties, both at a detailed operational level, and at an abstract system level. Transformations from system level descriptions to operational level can be used to derive implementations from abstract specifications.
- UJF/VERIMAG will also investigate code generation techniques for BIP models taking into account user requirements and the characteristics of the target platform. We will study code generation techniques for multi-thread and distributed implementation of specific classes of systems, in particular for timed systems (collaboration with EPFL and PLU-Salzburg on Giotto).

- CEA will provide a method and its related tools for modelling both software and hardware resources in order to foster simulation of embedded systems.
- ESI will investigate how budget-based design techniques can be combined with quantitative modelling formalisms to deal with resource constraints such as memory, processing power and energy consumption.

Sub-activity C: Quantitative Modeling

We will focus on the robust modelling of embedded systems, in particular the robust modelling of stochastic, timed, and hybrid systems using quantitative data about probabilities, time, and sensor values, both in nominal behaviour and under stress, faults, and disturbances. For this purpose we will study quantitative metrics for the comparison of systems. This will be done in a way that bridges the gap with the use of metrics in control. Based on such metrics, we will develop estimation and approximation theories for embedded systems, as well as compositional techniques for reward and cost sensitive design. We will also design formalisms for specifying and checking long-run average properties of systems. We will use these formalisms for computing and estimating quantities such as power consumption, timing, and cost of a given application model relative to different implementation choices.

In the first 18 months, the core partners will perform the following tasks:

- Aalborg will extend the modelling formalisms of UPPAAL Cora (priced timed automata) to allow for multiple costs in order that optimality and safety may be addressed in multi-priced setting. The use of priced timed automata in capturing energy and memory consumption of MPSoC systems. Also, probabilistic extensions of priced timed automata will be developed.
- EPFL will develop (bi)simulation metrics for discrete, real-time, and hybrid systems; languages and algorithms for specifying, checking, and comparing stochastic properties; and assume-guarantee methods for reasoning about rewards (or costs).
- INRIA will bridge the gap with the use of metrics in control. This shall allow the precise comparison of several automatic control systems designs. Furthermore, techniques involving the combination of Boolean and numerical control (i.e., hybrid systems) will be experimented and implemented in the NBac tool. In this manner, we expect to be able to combine complex Boolean control with linear numerical behaviour.
- KTH will define metrics for architectural design and use them as a basis for the architectural exploration. We also aim at developing a system-on-chip (SoC) and network-on-chip performance specification and analysis method that is based on network calculus and the concept of contracts between tasks and the SoC infrastructure. This method will allow to statically analyze the performance of complex, multi core SoCs with sufficient accuracy. Moreover, it will allow to compose complex SoCs from simpler sub-systems by making performance properties composable as well. In the first 18 months KTH will develop a formalism for expressing QoS contracts between IPs, processors and task on one hand and interconnect and the memory architecture on the other hand. These contracts will be based on network calculus, as developed by Cruz, LeBoudec, and others. It will allow to statically derive delay bounds for individual transactions, streams of transactions, and task periods. Furthermore, it will allow to dimension buffers, communication and memory capacity of the SoC infrastructure.
- PARADES will study the estimation and computation of quantities, such as power, timing, and costs associated with implementations. The estimated quantities will be related to implementation choices, and the simulation of system evolutions will be constrained by the estimated quantities.
- Uppsala will develop techniques for expressing long-term resource and timing properties of components, both average properties and regular "deviations".

- CEA will define model transformations to go from design model based on specific MoCC to schedulability analysis model conformed to the Marte standard.
- ESI will work on industrial-scale modelling of performance and dependability requirements, especially hard and soft real-time behaviour. Special attention will be to analysis and model-based validation (testing).

JPRA Activity: "Validation"

Core Teamleaders

Kim Larsen (Aalborg - Denmark); Joseph Sifakis (UJF/VERIMAG - France); Tom Henzinger (EPFL - Switzerland); Thierry Jéron (INRIA - France); Werner Damm (OFFIS - Germany); Ed Brinksma (ESI - Netherlands); Wang Yi (Uppsala - Sweden); Christoph Kirsch (PLU-Salzburg - Austria); Alberto Sangiovanni-Vincentelli (PARADES - Italy); Martin Törngren (KTH – Sweden)

Affiliated Teamleaders

Marius Minea (Institute e-Austria Timisoara, Romania); Christophe Gaston (CEA); Roberto Passerone (Trento – Italy); Jean-Francois Raskin (CVF – Belgium); Joost-Pieter Katoen (Aachen – Germany); Holger Hermanns (Saarlandes U – Germany); Christel Baier (Dresden – Germany); Francois Laroussinie (LSV Cachan – France), Peter Eriksson (ABB Robotics - Sweden).

Policy Objective

The objective is to address the growth in complexity of future embedded products while reducing time and cost to market requires methods allowing for early exploration and assessment of alternative design solutions as well as efficient methods for verifying final implementations. This calls for a range of model-based validation techniques ranging from simulation, testing, model-checking, compositional techniques, refinement as well as abstract interpretation. The challenge will be in designing scalable techniques allowing for efficient and accurate analysis of performance and dependability issues with respect to the various types of (quantitative) models considered. The activity brings together the leading teams in Europe in the area of model-based validation.

Background

By far the most common validation technique applied in embedded industrial today is based on rather ad-hoc and manual (hence quite error-prone) testing. Given that some 30-50% of the overall development time and cost are related to testing activities it is clear that the impact of improved validation technologies is substantial. Given this current industrial practice the academic state-of-the-art has a lot to offer. In particular the cluster combines the efforts and skills on of the individual leading researchers in Europe into a world-class virtual team for advancing the state-of-the-art and industrial take-up of model-based validation techniques.

Whereas validation techniques for assessing functional correctness have reached a certain level of maturity and industrial acceptance, there is a need for mature validation techniques addressing quantitative aspects (e.g. real-time, stochastic and hybrid phenomena) being accessible from within industrial tool-chains. Thus, particular effort should be made to transfer of validation methods and tools to industry, including integration of the techniques developed into existing tools.

Technical Description: Joint Research

The joint research falls into the following three sub-activities

A Compositional validation:
The complexity of a given analysis method is not only determined by its accuracy (and issues addressed) but mainly by the sheer size of the model analysed measure in number of components, tasks, variables, etc. In order to achieve methods which scale to the need of industry *compositionality* is paramount. That is, it should be possible for composite models to be interrelated and properties to be inferred only by consideration of the components of the models and their interfaces. In the presence of composite models with heterogeneous components – in particular involving components where quantitative aspects are considered – this is a challenge that has not yet been dealt with satisfactory.

B Quantitative validation:
Whereas functional validation addresses issues concerning logical correctness with respect to stated temporal specifications, quantitative validation takes the quantitative aspects into account. For embedded systems applied in safety-critical applications hard real-time guarantees are often imperative. For embedded systems in less critical applications performance and QoS are often more important properties: in this case the quantitative validation should return a value as to the "quality" of the model with respect to a given relevant metric, e.g. expected energy consumption pr time-unit. The quantitative aspects to be dealt with involve real-time, stochastic and hybrid phenomena.

C Cross-layer validation
During the design trajectory, the software engineer will create, refine and make use of several models of the same system focusing on different aspects and varying in terms of level of abstraction. A natural requirement is the possibility to interrelate these models and in particular to transfer properties established of one (early) model to properties guaranteed to hold of other (later) models without any additional effort.

Techniques for validating the conformance between design models and executing code (on particular platforms) are particular important. This includes considerations of (robust) methods for automatic code generation as well as methods for synthesizing controllers from plant models and control objectives.

In order for validation methods to be industrial applicable it is essential that existing (or third-party) code may be dealt with. Here software verification techniques (combining static analysis and model checking) need to be extended to involve quantitative aspects.

We expect the following results of the three sub-activities:

A Compositional validation
Aalborg will work on Modal I/O interfaces enriched with timing and recourse information; Abstractions and refinements with congruence properties; Timed version of Compositional Backwards Reachability method; Quotient method extended to timed and hybrid systems.

EPFL will develop algorithms for assume-guarantee checking the compatibility of component interfaces that expose resource constraints such as real time and power consumption.

Aalborg will work towards quantitative extensions of the Modal I/O Interface Theories including methods for checking consistency, refinements and compatibility. Also algorithmic support using UPPAAL TIGA will be pursued.

The exotask system currently supports so-called Giotto/HTL semantics. Giotto and HTL are real-time programming languages for the design and implementation of portable and efficient control software. For example, there is a prototypical implementation of helicopter flight control software in HTL and the exotask system. PLU-Salzburg plan to work on techniques that support compositional scheduling of all parts necessary for fully autonomous flight.

One focus of the OFFIS activities will be on compositional safety analysis techniques. For the safety viewpoint, OFFIS will develop methods and tools for using HRC models to determine their failure propagation behaviour. In particular, it will be possible to identify the impacts of failures on safety critical states and to identify failures as causes for given safety critical states. The provided safety characterization of a component allows to define different failure propagations depending on the (assumptions about the) environment of the component. The safety assumptions that will be developed in this context, allow for a concise annotation of components with the safety relevant details of the environment they are sensitive to. Based on these descriptions the analysis to be developed will be able to compute cause-consequence pairs for the given environmental conditions.

ESI will focus on validation frameworks that allow the combination of analytical techniques from different disciplines (software, hardware, control), in particular on the system level.

CEA will define a framework for symbolic execution of models of heterogeneous systems as a basis for compositional testing or model checking activities. The definition of a compositional methodology for testing will also be addressed.

PARADES will define in collaboration with UC Berkeley the verification component of the Metropolis II framework. The verification algorithms in the framework will include formal verification of interfaces, of successive refinement relations and joint execution of operational and denotational descriptions.

B Quantitative validation

Aalborg will work on efficient algorithmic methods for synthesizing optimal *infinite* schedules from priced timed automata models. Also optimality issues in multi-priced settings will be pursued in collaboration with LSV Cachan. Together with Aachen symbolic algorithms for analysing *probabilistic* priced timed automata will be developed in order that QoS guarantees for soft-real time systems maybe given

EPFL will collaborate with INRIA on providing and analyzing algorithms for checking quantitative reliability measures of implementations. EPFL will work with Oxford on algorithms for verifying stochastic systems.

As part of the modelling activity, PLU-Salzburg plan to add support for reliability modelling to the Giotto/HTL portion of the exotask system. In particular, PLU-Salzburg plan to work on validating reliability constraints in a hierarchical fashion, which will involve checking adequate notions of abstract reliability and extensions of the existing refinement relations in HTL.

Uppsala will develop approximation algorithms to trade for the efficient computation of quantitative metrics and abstract properties of components, which are precise enough for compositional reasoning of timing and resource constraints. The developed techniques will be integrated in UPPAAL and TIMES.

ESI will work on model-based real-time test generation and test coverage analysis, especially in combination with the TorX tool.

INRIA will work on model-based test selection for models with data, using symbolic techniques guided by approximate analysis. These analyses, together with dynamic partitioning will also found research on coverage based test selection. Combination of control and diagnosis will also be explored for the improvement of selection and precision of verdicts. The techniques will be integrated in the STG symbolic test selection tool, using the Nbac tool for approximate analysis.

PARADES will work on methods for reliability and performance assessment at multiple levels of abstractions in the Metropolis framework.

C Cross-layer validation

Aalborg and Uppsala will work together with CFV on generating robust and correct code from timed automata based models.

EPFL and PLU-Salzburg will collaborate on generating compositional, reliable code from time-triggered coordination languages in the Giotto family.

EPFL and Aalborg will work with CFV and LSV (and others?) on solving infinite, stochastic, and timed games for component synthesis and interface compatibility checking.

Uppsala will develop techniques for transformations between operational automata formalisms and more abstract transformational (stream-based) formalisms for automatic code generation from design models, preserving timing and resource constraints.

OFFIS will work on deployment architecture synthesis. Starting point of the exemplified automatic generation of deployment architectures are task level specifications which are refined to a concrete implementation on a given hardware architecture while guaranteeing timing and resource constraints. The synthesis of deployment architectures will be driven by an optimisation procedure which is used to yield proper implementations with respect to potentially multiple optimisation objectives, like bus utilisation, memory consumption, cost, etc. The deployment techniques will allow multi-objective optimisation on industrial-sized systems. The classes of supported architectures deal with complex distributed heterogeneous architectures (different types of busses and ECUs, nearly arbitrary network topologies).

ESI will work on multi-layer performance analysis and design-space exploration techniques as well as predictable refinement and synthesis for multi-processor platforms. This will be done jointly with the JPRA Activity: “Design for Predictability and Performance”.

PARADES will work on automatic mapping of functional requirements on distributed platforms characterized by heterogeneous components and hierarchical communication infrastructures.

WP4 Description - SW Synthesis, Code Generation and Timing Analysis

WP number	4		**Start date or starting event:** T0 *(start of the project)*					
WP Title	**Thematic Cluster: SW Synthesis, Code Generation and Timing Analysis (JPRA)**							
Activity type	RTD *Research and Technological Development*							
WP Leader	Peter Marwedel (Dortmund)							
Participant number	3	11	15	21	24	27	30	31
Participant short name	Aachen	Dortmund	IMEC	MDH	Passau	Saarland	Vienna	York
Person-months per participant	7,50	19,00	7,50	7,50	7,50	15,25	7,50	7,50

Objectives: Provide software synthesis, code generation and timing analysis tools which are required for modern embedded architectures and MPSoCs in particular.

Description of work

Activity "Software Synthesis, Code Generation :

- Software Synthesis
  The potential of software synthesis techniques starting from non-imperative specification styles will be analysed and options for their extension for MPSoC programming will be examined.
- Code generation
  There will be an analysis of the need and the potential of extending compilers for compiling for MPSoCs.

Activity "Timing Analysis":

- Timing analysis of MPSoCs
  Classical timing analysis will be extended toward MPSoCs.
- Non-standard timing analysis approaches
  Approaches based on timed automata and restricted parallel programming models will be explored

Partners will also contribute toward the transversal activity where they will focus on predictability and adaptivity.

Deliverables

Each deliverable is a report on the activity's work, provided yearly.

D-4.1-Y1	Software Synthesis, Code Generation Report
D-4.2-Y1	Timing Analysis Report
D-4.1-Y2	Software Synthesis, Code Generation Report
D-4.2-Y2	Timing Analysis Report
D-4.1-Y3	Software Synthesis, Code Generation Report
D-4.2-Y3	Timing Analysis Report
D-4.1-Y4	Software Synthesis, Code Generation Report
D-4.2-Y4	Timing Analysis Report

Overall Objective

There is a continuing demand for higher performance of information processing. This growing demand stimulates using a growing amount of parallelism (including using multiple processors), due to limitations of increasing clock speeds any further. This trend also affects the design of embedded systems. Hardware platforms, containing connected processors, are becoming increasingly parallel. Actually, there are various kinds of connectivity. In multi-processors in a system on a chip (MPSoC), processors are tightly connected and communication is fast. In other cases, networked processors may be less tightly connected and communication may be slower. In this project, we would like to address the issues resulting from the use of multiple processors, in particular in the form of multiple heterogeneous processors on a chip, also containing memory hierarchies and communication interfaces.

These processors can only be exploited if (sets of) applications can be efficiently mapped to heterogeneous processors. Mapping techniques can be either based on task graphs or on sequential applications. The latter require the use of automatic parallelization techniques. In this cluster, we want to provide at least partial solutions to the problem of mapping specifications of embedded systems to networks of embedded processors. These networks will be characterized by different speed parameters reflecting the communication and memory architectures. These parameters will be considered during the mapping. We will focus on mappings from simple sequential code from C or C-like languages. However, we will also look at the generation of code from other specifications, being based, for example, on MATLAB or UML. Such languages could simplify the mapping since such specifications might be inherently parallel (and also more appropriate for embedded systems). In general, mapping techniques will be indispensable for using future architectures.

Timing analysis is also affected by the trend toward the new platforms. Timing analysis has to cope with the kind of memory hierarchies found in MPSoCs. Also, timing analysis beyond the single processor is required. Hence, timing analysis will also consider the timing of communication. The overall objective is to provide safe timing guarantees for systems consisting of local memories hierarchies and multiple processors.

Partners in this cluster will also participate in the activities of the Activities of the Transversal Integration workpackage, where they will address adaptivity and predictability of complex systems comprising MPSoCs. Predictability will also be addressed in the cooperation between partners of the two activities of this cluster.

It is understood that the current project can only help integrating work that provides potential solutions.

Indicators for Integration

Interactions planned between partners include:

- There will be an integration of techniques developed by the high-performance computing community and the compiler for embedded systems community. There will be at least one tool flow demonstrating the advantages of combining these approaches. There will be examples demonstrating the power of the integrated techniques for MPSoCs. The activity will make compilation techniques available to the MPSoCs activity.
- There will be at least one timing analysis tool integrated with an experimental compiler, optimizations within this compiler consider multiple objectives (including worst case execution times) and a detailed set of results demonstrating the advantages and limitations of such an integration will be available.
- The partners will organize at least one open, internationally visible workshop on software generation, compilers and timing analysis per year.

- The partners involved in the cluster will publish at least four joint papers per year.

JPRA Activity: "Software Synthesis, and Code Generation"

Core Teamleaders

Peter Marwedel (Dortmund - Germany); Arnout Vandecappelle (IMEC - Belgium); Christian Lengauer (Passau - Germany); Rainer Leupers (Aachen - Germany)

Affiliated Teamleaders

Joseph van Vlijmen (Ace – Amsterdam / Netherlands); Björn Franke (University of Edinburgh); Sabine Glesner (TU Berlin); Paul Kelly (Imperial College, London); Alain Darte (ENS, Lyon); Marco Bekooij, Ruben van Royen (NXP – Eindhoven /Netherlands); Bart Kienhuis (Compaan Design B.V. – Leiden /Netherlands)

Policy Objective

Top-level experts have been selected for the activity. Their publication record, their reputation in industry and their links to leading colleagues clearly demonstrate that world-class experts have been selected for the core teams. In order to achieve the required critical mass without increasing the number of partners beyond a manageable number, affiliated partner are added. These affiliated partners complement the work done by the core partners.

Background

Significant effort on automatic parallelization has been spent in the context of high-performance computing. Due to this effort, automatic parallelization has become feasible provided certain assumptions about the applications are met. The same results are not yet available for embedded systems. For embedded systems, the situation is different in various respects. MPSoCs, for example, are characterized by communication speeds which are comparable to the speeds of larger on-chip memories. As a result, communication based on the message-passing interface (MPI) is completely ill-designed, since it uses memory buffers extensively. Also, embedded system applications are different from general purpose or high-performance computing. They are typically more "well-behaved" in that features like recursion, dynamic loop bounds, dynamic memory allocation, pointers, dynamic class loading etc. are much less frequent, simplifying the analysis. However, heterogeneity of processing elements, real-time constraints, streaming data, limited communication resources and energy awareness impose additional restrictions.

Software generation has evolved to a level where compilers are key components, but not the only components that are useful for generating executable code. New models of computations such as data-flow based models aim at avoiding the well-known disadvantages of imperative programming styles. Software synthesizers generate imperative code from abstract specifications such as Matlab, or Kahn process networks. It can also be expected that the link between software engineering and embedded systems will become stronger. Hence, trends like the use of UML-based system models do have to be respected as well. For the above models, code is synthesized from specifications in non-imperative languages.

Existing compilers represent very valuable software components which cannot be easily replaced by new methods. Many companies hesitate to replace their existing proven compilers by less well-debugged research results.

There is a growing gap between the speed of processors and the speeds of memories, even for larger on-chip memories of MPSoCs. Memory hierarchies are introduced to ease the problems resulting from this gap. Currently available memory hierarchies are typically designed to provide a good average-case performance. However, methods for increasing the average-case performance often deteriorate the worst-case performance and the timing predictability. Hence, timing predictability is becoming a key bottleneck for high-performance embedded systems and the memory system is a key source of unpredictability. Furthermore, memory hierarchies have not been designed for an efficient use of the available energy. In general, the link between memory architectures and compilation techniques is rather weak.

Technical Description: Joint Research

Compilation techniques for MPSoCs cannot be developed from scratch since the problems to be solved are very challenging. The current project will certainly not provide enough resources to develop completely new techniques. Fortunately, we can build upon compilation techniques for high-performance computing. Using the limited resources, we plan to establish a link between the high-performance computing and the embedded system domain. Integration activities will comprise an in-depth analysis of the applicability of techniques designed in one domain to the other domain. For this purpose, it is very essential that the proposed project includes enough expertise in different areas of applications. Knowledge about hardware architectures would not be sufficient to really check the applicability of the techniques. The University of Passau will be a link to the high-performance community. Cooperation with core partners and selected affiliates will be used to check which of the existing techniques can be employed in embedded systems and which extensions are needed. The partners propose to start with an intensive **road-mapping workshop** about 6 months after the start of the project. The workshop should involve a major number of key players in the area. Other clusters of the network include prominent experts on software synthesis (Benveniste, Halbwachs). They will be invited to contribute their view. Invitations will also not be limited to members of the network. 12 months after the start of the project, a detailed roadmap should be available. The roadmap will complement the available HiPEAC “High-Performance Embedded Architecture and Compilation Roadmap” in many ways: it will be more dedicated toward embedded MPSoCs, will involve a larger set of contributors, will be more focussed on compilation issues and will provide more details concerning the steps to be taken. This roadmap will be used to guide further integration work. It is expected that a major effort will be required to design a proper integration. After 24 months, the design of the integration work should be complete. Later, available automatic parallelization techniques will be integrated to close identified gaps in the tool support. After 36 months, the implementation of the integrated tools should be complete. After 48 months, an evaluation of the integration should be available.

In order to make the results available to as many designers as possible, tools will be based on pre-pass compilation whenever feasible. This way, the mapping of applications to MPSoCs can be added to many existing, proven tool flows. Investments into compilers can be protected, the development effort can be reduced and the focus on new optimization techniques can be increased. The key advantage of pre-pass optimizers is their applicability in a large number of tool chains. Such tool chains may be using a compiler from a family of compilers (such as gcc) or specially designed compilers. Pre-pass compilers can easily support a family of compilers without any modification and different compilers with only few modifications. They reflect the fact that the limited resources of a network of excellence are not sufficient for revolutionizing the way, software is generated in practice. Pre-pass optimisers do already exist for memory-architecture aware compilation and program parallelization. IMEC and partners at the Universities of Dortmund, Passau, and Edinburgh have significant experience with the design of pre-pass optimizers. Post-pass optimizers provide target-specific optimizations which can be applied to code generated by different compilers for the same target platform. They are expected to play a minor role.

Memory architectures will also be very important for the mapping to networked processors. Indeed, the mapping of applications to processing elements may be significantly affected by the connectivity of the memories. Hence, optimized mappings to memories have to be considered as well. Such techniques should provide optimization techniques taking several objectives into account.

The members of this activity will also contribute to the Activities of the Transversal Integration workpackage, focussing on predictability and adaptivity issues.

Technical Description: Tools and Platforms

The overall goal of using tools and platforms is to make efficient use of the available manpower and to avoid a duplication of efforts and the lack of interoperability. Avoiding the duplication of efforts implies that interoperability of existing tools and new tools should be one of the key goals.

Hence, wherever feasible, existing tools such as the gcc family of compilers as well as proprietary compilers (e.g. from ACE) should be considered as building blocks. gcc in particular will be a key tool that will be employed as a back-end tool for pre-pass optimizers for parallelization.

In certain cases, the development of compilers for new architectures or compilers meeting new criteria (such as retargetability or support for multiple objective functions) is necessary. In those cases, existing standard compiler development platforms will be used. In order to provide continuity with respect to ARTIST2, ACE will continue to employ and develop the COSY compiler platform as a vehicle for coherent research on compilers.

ICD-C (see http://www.icd.de/es) will be used as a platform for selected source to source transformations.

LooPo (http://www.fim.uni-passau.de/cl/loopo/, M. Griebl)
The loop parallelizer LooPo may have uses in the automatic parallelization of nested loop programs for MPSoCs. It can convert sequential C or Fortran loops, or also recurrence equations, into parallel C code.

aiT will be the primary platform for all work related to timing analysis.

The focus will be on compiling for C. SystemC will be used as the key language for describing system models, where feasible. XML will be used for representing information which cannot be described in any of the other languages.

JPRA Activity: “Timing Analysis”

Core Teamleaders

Reinhard Wilhelm (Saarland - Germany)*;* Björn Lisper (MDH - Sweden); Peter Puschner (Vienna - Austria); Guillem Bernat (York – United-Kingdom)

Affiliated Teamleaders

Christian Ferdinand (AbsInt - Germany); Niklas Holsti (Tidorum - Finland)

Policy Objective

The activity gathers the most prominent groups in the timing analysis area. They have all previously worked together in the ARTIST2 NoE, and therefore have well established links. The theme of the activity, timing analysis of MPSoC systems, is basically a new field

scientifically, and also very timely from an application perspective as MPSoC and Multicore architectures rapidly are becoming mainstream. A research effort in this area will thus establish European dominance in a field that rapidly is becoming very important.

ArtistDesign also provides a close to perfect environment for this research due to the relevant competence in other activities and clusters, such as the compiler groups in the local cluster, and the MPSoC cluster.

Background

All the partners in this activity have participated in the NoE ARTIST2. They developed a common tool architecture, interfaces between tools, and exchanged tool components. They have created a WCET Tool Challenge, executed the first time in 2006, to evaluate the existing commercial tools and academic prototypes. The Tool Challenge will be executed every second year with improved conditions and more challenging benchmarks.

Technical Description: Joint Research

Traditional timing analysis has three parts: the flow analysis, which finds constraints on the possible program flows, the low-level analysis, which applies hardware timing models to obtain timing estimates for short execution paths, and the calculation which combines the result of the two previous analyses to obtain an estimate of the WCET for the full code.

Timing analysis on code level has so far dealt almost exclusively with sequential programs running in isolation. For MPSoC and multicore architectures, these assumptions will no longer be valid: tasks might be parallel, and different tasks will run in parallel on different sets of cores. Timing analysis of parallel code, running on parallel hardware, is a new research area, and the aim of this activity is to initiate research in this area. Due to the novel nature much of the research, at least for the first 18 months, will have the nature of initial investigations, paving the way for future in-depth research.

Some research problems:

- Flow analysis has to be extended from single-threaded programs to multi-threaded programs with possible synchronization between threads.
- Current low-level analysis is restricted to synchronous processor models: only [Thesing06] has modelled processor periphery. Hardware modelling must be extended to include asynchronous systems including, ultimately, full MPSoC and multicore architectures.
- New WCET calculation methods must be invented, which take into account that several interacting threads may have to complete before a task has completed.
- Methods to handle common resources must be devised. For single-processor systems, interference between tasks through shared resources like caches can be dealt with on the scheduling level, by bounding the number of preemptions and calculating a maximal timing penalty. For parallel processors, common resources can potentially be accessed at any time by totally unrelated activities. This renders traditional scheduling theory useless to estimate costs from interference with other tasks running in parallel.

Some ideas how to tackle the research problems are given below:

For flow analysis, there are several possibilities. One is to consider restricted parallel programming models, like Bulk Synchronous Programming, which have been developed in the parallel programming area in order to ease the task of parallel programming. These programming models have simple cost models, which should translate into more predictable timing models. Another possibility may be to use timing analysis to derive a Timed Automaton modelling the parallel code, and use the TA to analyze its synchronization properties. A third possibility is to use information from a parallelizing compiler. Such compilers sometimes use internal representations describing the computation in an abstract way, like an explicit task graph, or a polyhedral index set for sets of loop body executions, which is allocated and scheduled. The compiler then actually has considerable knowledge about where and when different computations are performed, which could be used to help predict the timing.

For low-level analysis, the necessary hardware modelling should start with a formal specification of the architecture, and be based on sound methods of abstraction, analysis, and transformation. The attainable accuracy of the models will be critically dependent on the hardware architecture: thus, research is necessary to find suitable MPSoC architectures which are amenable to timing analysis.

The calculation methods will depend on the program execution model. Thus, research to find appropriate such methods will be strongly connected to the flow analysis research.

The common resources problem is a matter of both hardware and system design. As for low-level analysis, research into MPSoC architecture and systems is necessary to reduce the interference between tasks. In particular on-chip networks and memories are crucial components which have to be designed to allow predictable timing. A hypothesis is that the ability to dynamically partition the resources, like assigning different parts of the network to different tasks, is helpful in this regard.

In the first 18 months, we foresee the following activities and potential results:

1. Derivation of timing models from MPSoC designs given in a language like Verilog or VHDL.
2. Meetings with researchers in Timed Automata (Modelling & Validation Cluster) to discuss the possible connections between timing analysis on code level and timing analysis on model level. Possible outcome: a report describing one or several combined approaches to the problem of analyzing parallel software with respect to timing properties such as WCET.
3. An investigation whether restricted models for parallel programming can make the problem of WCET analysis easier to solve for programs adhering to these models. Possible outcome: a survey of potentially interesting parallel programming models, with an assessment of their respective amenability to WCET analysis.
4. A joint activity with the MPSoC cluster, where TA expertise is fed back to MPSoC architecture level. Task: to identify features of MPSoC architectures that are critical to the predictability of timing properties, and to suggest possible designs which make the architectures more predictable with respect to these properties. Evident targets are shared resources like on-chip networks and shared memories. Possible outcome: a report describing the problem and some possible solutions, with their respective pros and cons.

WP5 Description - Operating Systems and Networks

WP number	5		**Start date or starting event:** T0 *(start of the project)*					
WP Title	**Thematic Cluster: Operating Systems and Networks (JPRA)**							
Activity type	RTD *Research and Technological Development*							
WP Leader	Giorgio Buttazzo (SSSA-Pisa)							
Participant number	5	8	15	17	20	25	26	31
Participant short name	Aveiro	Cantabria	IMEC	TUKL	ULund	SSSA-Pisa	Porto	York
Person-months per participant	7,00	10,25	3,50	10,25	3,00	15,25	10,25	13,50

Objectives Establish the fundamental basis of a new real-time software technology that can provide a more efficient and predictable support at the operating system and network level to the development of future embedded systems, characterized by high complexity, dynamic behaviour and distributed organisation.

Description of work

Activity "Resource Aware Operating Systems":

- Component-based operating systems, to optimize the use of resources and increase softwYalization techniques to abstract the available resources into a set of independent devices providing temporal and spatial isolation.

Activity "Scheduling and Resource Management ":

- Taxonomy of system resources and the analysis techniques available to manage their use - build up an understanding of the tradeoffs between architectural (static) choices and run-time dynamic adaptability.

Activity "Real-Time Networks":

- Timeliness analysis in the frameworks of Networked Embedded Systems, Wireless Sensor Networks and Mobile Ad-hoc Networks particularly under the dynamic behaviour arising from load variations, topology changes, adaptation to the environment or other reconfigurations;
- Efficient temporal partitioning and isolation mechanisms to provide integrated global resource management within distributed embedded systems;
- Energy-consumption reduction in networking, particularly in wireless sensor networks and mobile devices in general, both from device and system perspectives;
- Systematic and progressive replacement and/or extension of wired with wireless networking technologies, from embedded control applications to multimedia systems.

Deliverables
Each deliverable is a report on the activity's work, provided yearly.

D-5.1-Y1	Resource-Aware Operating Systems Report
D-5.2-Y1	Scheduling and Resource Management Report
D-5.3-Y1	Embedded Real-Time Networking Report
D-5.1-Y2	Resource-Aware Operating Systems Report
D-5.2-Y2	Scheduling and Resource Management Report
D-5.3-Y2	Embedded Real-Time Networking Report
D-5.1-Y3	Resource-Aware Operating Systems Report
D-5.2-Y3	Scheduling and Resource Management Report
D-5.3-Y3	Embedded Real-Time Networking Report
D-5.1-Y3	Resource-Aware Operating Systems Report
D-5.2-Y3	Scheduling and Resource Management Report
D-5.3-Y3	Embedded Real-Time Networking Report

Overall Objective

The high level objective of this cluster is to build the fundamental basis of a new real-time software technology that can provide a more efficient and predictable support to the development of future embedded systems, characterized by high complexity dynamic behaviour and distributed organisation. In particular, the new software technology should:

- support scalability to facilitate the porting of control applications to different platforms;
- simplify the management of resources to control the growing complexity and distribution of embedded systems;
- take advantage of parallel processing platforms, such as multicores, in order to satisfy timing and adaptivity requirements;
- be light-weight to optimize the usage of scarce resources in tiny embedded computing devices;
- increase programming flexibility, for specifying functional and performance requirements to simplify test and verification;
- enable run-time reconfigurability and functionality updates to deal with the dynamics and ubiquitous nature of the supporting computing infrastructure;
- increase programming productivity, by raising the level of abstraction of the resource management services;
- increase system adaptivity to react to environmental changes, still providing a sufficient level of performance;
- be robust to tolerate transient and permanent overload conditions due to wrong design assumptions or unpredictable changes.

Such features would have a concrete impact on European industry to reduce time to market, and improve software reliability and testability. To support industry in such a transition phase, new tools, algorithms and kernel mechanisms must be also provided. In this respect, this cluster is playing an active role, acting as a bridge between the academic and the industrial world, especially in the domain of consumer electronics, robotics, industrial automation, telecommunications, and the so called cyber-physical systems.

A means to achieve such a goal is to develop a research platform for real-time systems to share competencies, resources, and tools targeting at the development of applications, such as control systems, with performance and timing requirements. The use of a shared platform is essential for experimenting new real-time software technology, including novel scheduling algorithms, resource management techniques, communication paradigms, energy-aware policies and overload handling approaches to increase robustness and predictability. A shared platform also facilitates the transfer of research results to industry, as it allows teaching practical knowledge of concepts and techniques. In addition, several solutions can be developed and tested in parallel in different partner sites, allowing the evaluation of the most appropriate approach for specific applications.

Specific research topics addressed in this cluster are related to operating systems and networks, with particular emphasis on scheduling and resource management, including energy-aware strategies and exploitation of parallelism in multicores.

Integration activities will be carried out through different means, including student exchanges between specific partners, joint theses, joint publications, joint software implementation, workshops, working groups, and common European projects already active in the cluster, such as FRESCOR, ACTORS, and PREDATOR.

New theoretical results produced within this cluster will appear in a set of joint publications that will be submitted to high quality international conference proceedings and journals. Based on previous results, at least 10 joint publications will be produced every year by the cluster.

From a practical point of view, the individual contributions each team will be integrated and tested using a shared platform, the Shark operating system, which has been developed under the ARTIST2 project. In fact, Shark has a modular structure that allows different users to develop new scheduling algorithms and new resource management policies independently of other kernel mechanisms. Under Shark, the same application can be tested under different scheduling policies and resource management protocols, without changing the source code. Moreover, the algorithms can be dynamically selected by the user at system initialization through a configuration file. This feature cannot be found in today's operating systems. Finally, it complies with the POSIX standard, PSE51 profile, so facilitating the porting of a real-time application developed for different operating systems and platforms.

Cluster Leader

Giorgio Buttazzo (SSSA-Pisa - Italy)
Advanced scheduling methodologies and overload management)

Other core team leaders, Roles

Luis Almeida (Aveiro – Portugal)
Dynamic reconfiguration in distributed embedded systems

Eduardo Tovar (Porto – Portugal)
Wireless Sensor Networks, Multiprocessor Scheduling, QoS-Aware Computing, Tiny OSs

Michael Gonzalez Harbour (Cantabria, Spain)
Flexible Scheduling Framework, Distributed Real-Time Systems

Alan Burns (York – United-Kingdom)
Advanced scheduling and resource modelling and management

Gerhard Fohler (TUKL – Germany)
Real-time resource management and media processing

Karl-Erik Årzén (ULund – Sweden)
Adaptive control methods for real-time systems

Affiliated team leaders, Roles

Ivo De Lotto (University of Pavia – Italy, Affiliated to SSSA-Pisa)
Energy-aware management and real-time sensory processing.

Lucia Lo Bello (University of Catania – Italy, Affiliated to SSSA-Pisa)
RT networks and scheduling.

Hermann Haertig (University of Dresden – Germany, Affiliated to TUKL)
Micro-kernel- and hypervisor-based systems

Jean-Dominique Decotignie (Swiss Center for Electronics and Microtechnology (CSEM) – Switzerland, Affiliated to TUKL)
Networks.

Alejandro Alonso (Technical University of Madrid – Spain, Affiliated to Cantabria)
QoS resource management, high integrity systems

Marisol García Valls (Carlos III University of Madrid – Spain, Affiliated to Cantabria)
Memory management in Real-Time Java middleware, dynamic reconfiguration architectures in distributed real-time systems.

Alfons Crespo (Technical University of Valencia – Spain, Affiliated to Cantabria)
Real-Time memory management, Virtualization of real-time kernels

Pau Martí (Technical University of Catalonia – Spain, Affiliated to ULund)
Feedback control and resource management

Julian Proenza (University of the Balearic Islands – Spain, Affiliated to Aveiro)
Fault-tolerance.

Stylianos Mamagkakis (IMEC – Belgium, Affiliated to York)
Run-time resource management.

Dirk Pesch (Cork Institute of Technology - Ireland, affiliated to Porto)
Adaptive wireless systems, wireless sensor networks

Paolo Gai (Evidence s.r.l. – Italy, Affiliated to SSSA-Pisa)
Operating systems and tools.

Guillem Bernat (Rapita Software - Affiliated to York)
Performance analysis tools.

Liesbeth Steffens (NXP – The Netherlands, Affiliated to TUKL)
Multimedia processing.

Johan Eker (Ericsson – Sweden, Affiliated to ULund)
Telecommunication systems.

Alberto Ferrari (PARADES, Italy, Affiliated to SSSA-Pisa)
Real-time operating systems

Indicators for Integration

Interactions planned between partners include:

- 10 Joint publications / year in international journals and proceedings related to real-time and embedded computing systems;
- Organization of joint educational activities on real-time operating systems and networks, like training courses, summer schools, or student competitions;
- Organization of 3 workshops / year for discussing new trends and solutions on operating systems and networks;

- Creation of a repository for relevant publications, algorithms, and libraries related to real-time operating systems.

JPRA Activity: "Resource-Aware Operating Systems"

Core Teamleaders

Giorgio Buttazzo (SSSA-Pisa - Italy); Luis Almeida (Aveiro – Portugal); Eduardo Tovar (Porto – Portugal); Michael Gonzalez Harbour (Cantabria, Spain); Alan Burns (York – United-Kingdom); Gerhard Fohler (TUKL – Germany)

Affiliated Teamleaders

Ivo De Lotto (University of Pavia – Italy, Affiliated to SSSA-Pisa); Paolo Gai (Evidence s.r.l. – Italy, Affiliated to SSSA-Pisa); Hermann Haertig (University of Dresden – Germany, Affiliated to TUKL); Pau Martí (Technical University of Catalonia – Spain, Affiliated to ULund); Alfons Crespo (Technical University of Valencia – Spain, Affiliated to Cantabria); Alejandro Alonso (Technical University of Madrid – Spain, Affiliated to Cantabria); Marisol García Valls (Carlos III University of Madrid – Spain, Affiliated to Cantabria)

Policy Objectives

The main objective of this activity is to investigate how current real-time operating systems have to be extended or modified to support emerging real-time embedded systems characterized by a high degree of complexity, highly variable resource requirements and parallel processing such as multicores. Most embedded systems are often characterized by scarce resources in terms of processing power, memory, space, weight, energy, and cost. Hence, another objective is to investigate kernel mechanisms that can efficiently manage the available resources, taking multiple constraints into account, whilst guaranteeing isolation properties. Also, to support dynamic applications with variable resource requirements or to cope with unpredictable resource availability, feedback control techniques for resource management at the operating system and application level will be investigated.

The impact on operating system standards (like RT-POSIX and OSEK) will also be taken into account. In fact, developing real-time applications and components using an interface compliant to a standard will promote portability to other compliant platforms and will challenge the current standard to be extended to better meet the needs of advanced applications with flexible resource requirements. We realize though that in specific application domains, significant performance advantages can be realized by optimizing software across layers, for example exploiting specific behaviour of a medium access control protocol. This is often the case in operating systems for sensor network platforms such as TinyOS or NanoRK. Such cross-layer design does not necessary contradicts operating system standards, but they do require other interfaces. Some partners in this activity are involved a few research and standardization efforts over such type of tiny operating systems.

Several of the partners of this activity are partners of the FRESCOR IST project, which has among its objectives the development of a framework that uses a contract model that can be used by applications to specify their requirements with respect to the flexible use of the processing resources in the system, both in regard to the resources that must be guaranteed if the component is to be installed into the system, and also on how the system can distribute any spare capacity that it has, to achieve the highest usage of the available resources. This framework is very open and can be used to provide support for QoS requirements, real-time, distribution, and new adaptive scheduling techniques. The partners of the NoE could use the FRESCOR framework as a common platform to integrate their different contributions and enhance its usefulness. The benefit of this framework is that it facilitates the integration effort, and it can be disseminated to industry as a complete solution that increases the level of abstraction as compared to the regular operating system services provided for embedded systems.

One of the partners in this activity will be involved on a national project (RESCORE) aiming at the development of real-time scheduling algorithms for multicores with a high utilization bound and low run-time overhead (few preemptions and low dispatching overhead). The algorithms developed are expected to be important inputs to researchers in operating systems and to standardization processes.

Industrial domains that will directly benefit of the results of this research include consumer electronics and telecommunications, for improving the functionality and the utilization of multimedia applications, automotive industry, to handle overload conditions that frequently occur in the microcontrollers embedded in the car, and industrial automation, where often robotics applications consists of several tasks with different criticality and timing constraints.

Other issues that will be considered in this activity are related to:

- microkernels and virtualization;
- component-based operating systems.
- hypervisor for embedded systems (UPVLC). A hypervisor is a small kernel running underneath the operating systems providing virtualisation features to hosted operating systems. It allows safe, parallel and independent deployment of multiple operating systems on single hardware while preserving hard real-time behaviour of one, or more, of the hosted operating system called domains or partitions. It is achieved by means of a temporal and spatial isolation.

Background

Although there is a large variety of real-time operating systems (RTOSs) varying in sizes, level of provided services, and efficiency, there are some common elements that can be found in most of them:

- An RTOS usually provides support for concurrent programming via processes or threads or both. Processes usually provide protection through separate address spaces, while threads can cooperate more easily by sharing the same address space, but with no protection.
- Real-time scheduling services are provided because this is one of the keys to obtaining a predictable timing behaviour. Most current RTOS's provide the notion of a scheduling priority, usually fixed, as for the moment there are few systems providing deadline-driven or other dynamic-priority scheduling.
- Although some RTOS designed for high-integrity applications use non preemptive scheduling, most support preemption because it leads to smaller latencies and a higher degree of utilization of the resources.

- The OS has to support predictable synchronization mechanisms, both for events or signal and wait services, as well as for mutual exclusion. In the later case some way of preventing priority inversion is required because otherwise very improbable but also very long delays may occur. The common mechanism used to prevent priority inversion is the use of some priority inheritance protocol in the mutual exclusion synchronization services. Priority inversions must also be avoided in the internal kernel implementation; among other things this requires the use of priority queues instead of regular FIFO queues in those OS services where processes or threads may be queued waiting for some resource.
- The OS has to provide time management services with sufficient precision and resolution to make it possible for the application to meet its timing requirements.
- OS behaviour should be predictable, and so metrics of the response time bounds of the services that are used in real-time loops should be clearly given by the RTOS manufacturer or obtained by the application developer. These metrics include the interrupt latency (i.e., time from interrupt to task run), the worst case execution time of the system calls used in real-time loops, and the maximum time during which interrupts are masked or disabled by the OS and by any driver.

An RTOS is generally chosen not only for its real-time characteristics, but also for the middleware that is integrated in the RTOS, such as file system, communication stack, for its portability to different platforms (i.e., the board support packages that are provided), and for the associated cross-development environment.

A commercial RTOS is usually marketed as the run-time component of an embedded development platform, which also includes a comprehensive suite of (cross-) development tools and utilities and a range of communications options for the target connection to the host, in an Integrated Development Environment (IDE). Moreover, the vendor generally provides development support. For each successful open source RTOS there is also at least one commercial distributor that provides development tools and development support.

For many embedded-systems companies, the availability of development tools and support is a major requirement for choosing a particular RTOS. The quality of the overall package deal, including service and pricing strategy is often decisive in choosing a particular RTOS.

Development Tools
In addition to the general programming tools, such as (graphical) editors, compilers, source code browsers, high-level debuggers, and version control systems there are a number of tools specifically aiming cross development, and run time analysis. Advanced tools in this domain not only address development and analysis of the own application code, but also third-party code and the integration with the OS. Memory analyzers show memory usage and reveal memory leaks before they cause a system failure. Performance profilers reveal code performance bottlenecks and show where a CPU is spending its cycles, providing a detailed function-by-function analysis. Real-time monitors allow the programmer to view any set of variables, while the program is running. Execution tracers display the function calls and function calling parameters of a running program, as well as return values and execution time. Event analyzers allow the programmer to view and track application events in a graphical viewer with stretchable time scale, showing context switches, semaphores, message queues, signals, tasks, timers, etc. Simulators enable application development to begin before hardware becomes available, allowing a large portion of software testing to occur early in the development cycle.

Schedulability Analysis Tools
There are different commercially available schedulability analysis tools: TimeWiz from Time Sys Corporation, and RapidRMA from TriPacific are based on Rate Monotonic Analysis (RMA, a modelling and analysis approach for fixed priority systems) [Kle93]. SymTA/S - Symbolic Timing Analysis for Systems - is a system-level performance and timing analysis approach based on formal scheduling analysis techniques and symbolic simulation. These tools allow designers to test software models against various design scenarios and evaluate how different implementations might optimize the performance of their systems, and isolate and identify potential scheduling bottlenecks of both soft and hard real-time systems. There are also WCET analyzer tools: aiT, from AbsInt takes the pipelining and caching of modern processors into account when determining worst-case execution times; RapiTime is an analysis tool that determines worst-case execution times (WCET) for software components running on advanced microprocessors using path analysis techniques and statistical methods.

These tools benefit from the great success in real-time scheduling theory; results that were developed in the 70's and 80's, and are now well-established and part of the undergraduate curriculum world-wide. Considering the rapid increase in the use of multicores, it is desirable to also develop such tools for multicores. Unfortunately, concerning these, the scheduling theory in real-time scheduling is significantly lagging behind the single processing theory and significant basic research problems are still unsolved. There is however some fair expectation that schedulability analysis tools for multicores will be designed successfully in the near future and have large impact in some of the issues related to this activity.

Tiny operating systems such as TinyOS or Nano-RK are usually used in distributed ubiquitous systems. Tools for schedulability analysis of applications for such assemblies exist such as Avrora (from UCLA) or Tossim (from Berkeley). Although trying to engage a holistic view of the system (taking into account application tasks, OS and network specificities), there are still limitations on their use. Some partners in this activity have been addressing efforts related with making such tools available and practical.

Technical Description: Joint Research

The technical achievements expected will enable the development of resource efficient embedded systems for a broad scope of application domains, e.g., consumer electronics, automotive systems, industrial automation and sensor networks. These achievements, however, will require overcoming technical difficulties inherent to certain conflicting goals. For example, real-time techniques need a priori knowledge for providing guarantees while adaptive mechanisms will allow such knowledge to vary on-line. This variation will also complicate achieving safety and possibly other properties that are also commonly based on a priori knowledge. Moreover, resource usage imposes, many times, couplings and trade-offs between different tasks in the system, thus managing resources while considering such couplings to avoid undesired blocking and interference is another problem that will need to be overcome.

In order to solve these difficulties, we will make use of cutting-edge methodologies on which the involved groups are currently working on, such as flexible scheduling, flexible modes, dynamic QoS management and dynamic reconfiguration.

Microkernels and virtualization (Herman Haertig);
Microkernel-based systems are based on the idea that the highest hardware-level privileges should be constrained to the smallest possible inner core of systems, the microkernel. All other functionality is provided by user-level servers. Microkernels supporting legacy operating systems and their applications are sometime also called hypervisors. Such systems provide interesting benefits and challenges. One important, if not *the* most important, benefit lies in the additional security that such systems can provide: a successful

penetrator into a legacy operating system compartment in a microkernel-based system cannot harm other, highly critical parts of the system. This can be achieved if microkernels (such as L4/Fiasco) are designed to provide temporal and spatial separation and temporal, hard or statistical temporal guarantees. Among the challenges for such systems is the close interaction of inter-process communication with scheduling which requires a very carefully designed interface. Such questions will be studied in the project.

Hypervisor for embedded systems
The main open issues related to the hypervisor design are:

- Scheduling policies for domains
- Shared resources management
- Driver support
- Adaptation of new OS to work with a virtualised platform
- Deployment of multiple operating systems on multicore processor platform
- Security issues

Multicore embedded real-time systems (Paolo Gai);
Next generation RTOS must allow optimal off-line partitioning of the application source code on the different CPUs available on multicore heterogeneous systems, as well as on-line strategies for run-time migration with the objective of guaranteeing optimal usage of the CPUs available, with real-time response as well as minimization of power consumption.

Component-based operating systems
To optimize the use of resources and increase software portability on different platforms, it is highly desirable to compose the operating system using the functions strictly necessary for the application. To achieve this goal, it is crucial to design the operating system to be modular, so that each component can be independently developed from the others and can be replaced without changing the application.

Plan for the first 18 months

In the first 18 months we will mainly focus on the issue of component-based operating systems, defining the desired features and critical problems that need to be solved at the technical level. We will also address the problem of extending current RTOSs for uniprocessors to multicore devices, with the objective of making optimal usage of the CPUs available, as well as minimizing power consumption.

JPRA Activity: “Scheduling and Resource Management”

Core Teamleaders

Alan Burns (York - United-Kingdom); Giorgio Buttazzo (SSSA-Pisa - Italy); Luis Almeida (Aveiro - Portugal); Michael Gonzalez Harbour (Cantabria – Spain); Gerhard Fohler (TUKL - Germany); Karl-Erik Årzén (ULund- Sweden); Eduardo Tovar (Porto– Portugal); Stylianos Mamagkakis (IMEC)

Affiliated Teamleaders

Alfons Crespo (Technical University of Valencia – Spain, Affiliated to Cantabria); Marisol García Valls (Carlos III University of Madrid - Spain, Affiliated to Cantabria); Alejandro Alonso (Technical University of Madrid – Spain, Affiliated to Cantabria); Lucia Lo Bello - Technical University of Catania (Affiliated to SSSA-Pisa); Stylianos Mamagkakis (IMEC - Affiliated to York)

Policy Objective

The main objective of this activity will be the provision of models of embedded platform resources and policies, and the necessary analysis for undertaking the run-time scheduling of these resources and policies. A key scientific challenge is to link this resource-centred analysis with models of the application (and their resource usage policies) and the performance profiles of the hardware platform itself. Issues of temporality, safety, reliability and security can only be effectively addressed by an integration of these various abstract views of the overall system.

Seven promising approaches for providing this integration are:

- the use of search techniques to investigate architectural tradeoffs,
- the definition and use of virtual (unshared) resources,
- the use of reservations and contracts to allocate virtual resources,
- the use of coordination languages to integrate the use of different resource types,
- taking advantage of parallel processing platforms, such as multicores and FPGAs, in order to satisfy timing requirements,
- the application of self-adapting (feedback) resource allocation algorithms, and
- the recognition of the various time scales over which resource management must occur.

The nature of the scientific challenge should not be underestimated. Although very effective results for single resource (e.g. the processor) scheduling are available (and are used in industrial practice), for multiple resources there are no current applicable theories that have wide acceptability. Even for multi-processor SMP systems there is no consensus on the appropriate means of managing this resource.

The impact on operating system will be taken into account via interactions with Activity 1 of this cluster. In addition the management of the network resource(s) will be address via joint work with Activity 3.

The industrial domains that will directly benefit from the results of this research include consumer electronics (in particular the games industry and multimedia applications), the automotive and aerospace industries, and environmental electronics such as smart spaces.

Background

The platforms on which the next generation of embedded systems will be implemented will be radically different from those used in the current generation. The scale, performance, scope and applicability are all subject to significant enhancement. This presents the application developer and systems engineer with a number of fundamental challenges. At the centre of these challenges is the (effective) management of the platform's resources. Such platforms are likely to be multi-core (64 soon and 200+ by 2010); involve buses and networks of various capabilities and speeds (both off-chip and on-chip, i.e. NoCs); memories of various speeds; include specialised components such as MEMS, ASICs, DSPs, and ASIPs; are linked to a wide variety of sensors and actuators; are embedded in systems powered by batteries (for mobile applications); include areas of FPGA (which are capable of dynamic reprogramming); and may have input/output links to global web-based information systems (for cyber-physical systems). Applications will be multi-resource and configurable. They will want to make dynamic modifications to their behaviour to support adaptability and environmental change. For example, the level of parallelism may alter at run-time and lead to re-evaluation of how this parallelism is delivered, e.g. by a subset of the cores, by application specific processing elements of by reprogramming an area of FPGA.

The main objective of this activity is to investigate how this wide variety of platform resources can be abstracted, modelled and managed, and application-specific resource allocation policies defined. At run-time, near optimal performance is desirable, but so are levels of protection for high integrity applications and those that have security constraints. Effective run-time scheduling of multi-resource platforms is not currently achievable; new methods will need to be developed.

Technical Description: Joint Research

The technical achievements expected range from specific scheduling algorithms that cater for particular groups of resources, to a general purpose framework for addressing the broad problem of managing multiple resources for multiple applications on multiple time scales with multiple policies. It is expected that a means of abstracting, via a parameterised definition, the capability of each resource will be developed. A greater understanding of the distinctive roles of both static architectural tradeoffs and dynamic run-time adaptability will be obtained by both theoretical study and where possible the analysis of industrially relevant case studies.

The activity will focus on the techniques needed elsewhere in the NoE for predictability and adaptability. It will directly address the run-time techniques and analysis that will need to be supported by the OS and any network protocols.

The first 18 months will focus on producing taxonomy of system resources and the analysis techniques available to manage their use. One aspect of this taxonomy will be to survey the various forms of parallelism becoming available on current platforms; other topics will be the use of hierarchical scheduling, anytime approaches and communications. For mobile applications, energy is a key resource that is the subject of much research that will be surveyed. The final class of resources to be considered is that containing specialized components and external devices (and information sources)

It is expected that within 4 years, real-time scheduling algorithms for multicores with a utilization bound greater than 50% and few preemptions will be developed for sporadically arriving tasks. These results will be extended for arbitrary deadlines and for dealing with shared data structures. We expect these results to be as natural part of the undergraduate education as RM and EDF are today.

A key issue on reconfigurability is to not only ensure that the new mode is safe but also to ensure that the transition to the new mode does not violate timing requirements; this is often referred to as the mode change problem, and it is currently unsolved for multicores. Considering the current state-of-art in real-time scheduling in multicores, we expect this result on multicores to be available through the progress of ArtistDesign.

Dynamic memory management has been systematically avoided in real-time systems. One of the main reasons for this is the absence of deterministic allocators. Recently a new algorithm for dynamic memory allocation (TLSF) that solves this problem of the worst case bound whilst maintaining the efficiency of the allocation and deallocation operations has become available. This allows the reasonable use of dynamic memory management in real-time applications and permits consideration of dynamic memory as a first-class resource which can be used jointly with other resources in the schedulability of embedded systems. This integration of memory management and other resources is likely to develop over the next 18 months.

We also anticipate integration of the following research results:

1. SSSA-Pisa will investigate advanced scheduling methodologies for increasing the predictability of real-time systems characterized by a highly variable workload and execution requirements.

2. The University of Pavia (affiliated to SSSA-Pisa) will consider new methodologies for integrating overload management techniques with energy-aware strategies, in the context of small embedded systems for battery operated devices.
3. The real-time systems research group at York will contribute on advanced scheduling and resource management policies.
4. TUKL will work on the integration of offline and online scheduling for combining time triggered and event triggered methodologies in the same system and provide resource management methods for media processing.
5. Cantabria will focus on the integration of the resource management techniques developed by the other partners in the integrated framework for flexible resource management (FRESCOR). The group will also participate in the development of the Real-time POSIX operating systems standards and the OMG standard for Modelling and Analysis of Real-Time Embedded Systems (MARTE).
6. The team at Aveiro will be involved in the design and analysis of tools and mechanisms for supporting dynamic QoS management, mainly for distributed multimedia systems, flexible scheduling, dynamic reconfiguration, graceful degradation and survivability for distributed embedded control systems, particularly robots and vehicles.
7. The team at Porto will be involved in Scheduling on Multicores, QoS-Aware in Distributed and Collaborative Computing, Resource Management in Sensor Networks and general purpose abstract models and dynamic run-time adaptability with anytime approaches.
8. The team at the University of Dresden will be involved in building micro-kernel- and hypervisor-based systems as experimentation platforms.
9. The team at the Technical University of Valencia will be involved in providing real-time memory management OS support, and real-time kernel virtualization.
10. The team at the Technical University of Madrid will investigate on integrated resource management policies with emphasis on adaptability.
11. The team at the Carlos III University of Madrid will work on memory-based QoS management techniques to provide support for predictability in Real-Time Java middleware.
12. The team at the Technical University of Catalonia will work on the integration of feedback control and resource management techniques to provide adaptability to changing conditions on both resource and applications demands.
13. The team at the University of Catania will work on QoS-oriented scheduling and management of communication and processing elements in embedded platforms.

JPRA Activity: "Real-Time Networks"

Core Teamleaders

Luis Almeida (Aveiro – Portugal); Giorgio Buttazzo (SSSA-Pisa – Italy); Michael Gonzalez Harbour (Cantabria – Spain)*;* Alan Burns (York – United-Kingdom); Gerhard Fohler (TUKL – Germany); Eduardo Tovar (Porto– Portugal)

Affiliated Teamleaders

Hermann Haertig (University of Dresden - Affiliated to TUKL); Pau Martí (Technical University of Catalonia - Affiliated to ULund); Lucia Lo Bello (University of Catania - Affiliated to SSSA-Pisa); Julian Proenza (University of the Balearic Islands - Affiliated to Aveiro); Jean-

Dominique Decotignie (CSEM - Affiliated to TUKL); Marisol Garcia Valls (University Carlos III de Madrid, Affiliated to Cantabria); Dirk Pesch (Cork Institute of Technology - Ireland, affiliated to Porto)

Policy Objective

Looking at the current scenario in embedded systems we see a permanently growing role of networking, either to connect autonomous devices such as cell phones, PDAs, laptops and their peripherals, as well as to provide pervasive access to multimedia and telecommunication networks, to establish large-scale (geographical region, number of nodes) sensor networks, to support intelligence distribution in complex embedded systems, or even, at a small physical scale, to connect multiple processing cores in SoCs.

Along the past decades, several network communication protocols have been developed with new capabilities. From an ever increasing throughput and support for traffic classes (including guaranteed latency and jitter), to different topologies, integration of heterogeneous segments, extensive use of wireless technologies, openness to dynamic arrival and departures of nodes, openness to larger networks (such as the Internet), etc. If, on one hand, many problems have been solved, with a significant number of successful embedded applications that rely on networking services, on the other hand new problems appeared, or some old problems persist, that still require adequate solutions. Among these, a few areas deserve a particular reference for their enormous interest, namely the support for dynamic behaviours and run-time adaptability with provision of real-time and safety guarantees, the resilience to interference, intrusion, mobility and node crashes in wireless networks, the minimization of energy consumption in the communication process, scalability to large numbers of nodes, the integration with other resources in a distributed system, particularly the processors, efficient integration with distribution middleware, support for flexible application development paradigms such as service-oriented, and efficiency in micro-scale implementations, such as NoCs, considering physical area, throughput and energy.

This activity will address some of the issues referred above, within the frameworks of Networked Embedded Systems (NESs), Wireless Sensor Networks (WSNs) and Mobile Ad-hoc Networks (MANETs). Its main objectives are:

- to analyze what kind of timeliness guarantees can be achieved across those frameworks and which mechanisms can be devised to grant such guarantees, particularly under the dynamic behaviour arising from load variations, topology changes, adaptation to the environment or other reconfigurations;
- to foster the currently increasing integration levels within distributed embedded systems, by means of efficient temporal partitioning and isolation, integrated global resource management and flexible architectures;
- to pursue further energy-consumption reduction in networking, particularly in wireless sensor networks and mobile devices in general, both from device and system perspectives;
- to address the problems brought up by and devise solutions to the current trend towards the systematic and progressive replacement and/or extension of wired with wireless networking technologies, from embedded control applications to multimedia systems.

Background

This activity will address numerous research challenges in the frameworks of Networked Embedded Systems (NESs), Wireless Sensor Networks (WSNs) and Mobile Ad-hoc Networks (MANETs). Namely, energy-aware communication is turning out to become a major research challenge for WSNs, imposing innovative and efficient networking protocols that manage communications periodicity, nodes synchronization and transmitting power; QoS adaptation and the collaborative computing paradigms are challenges that will require protocol mechanisms that monitor instantaneous bandwidth usage, enforce minimum agreed QoS levels (e.g. through contracts and traffic policing) and leverage the access to free bandwidth (to increase QoS whenever possible); higher software integration in distributed embedded systems requiring integrated global resource management together with effective and efficient temporal partitioning (e.g., using hierarchical scheduling techniques), as well as flexible mapping between software and hardware architectures; replacement and/or extension of wired with wireless networking technologies, coping with more error-prone channels and security risks but profiting from simplified deployment and elimination of cabling.

Moreover, distributed sensing, actuation and cooperative computing involving small and tiny computing platforms appear as a basilar functionality in an ever crescent range of applications, including surveillance, environment and critical infrastructures monitoring, disaster recovery operations, distributed control, military operations, etc. The requirements imposed by these diverse applications necessarily imply different trade-off options on supported functionality, quality of service, efficiency, platforms, protocols, architectures, etc. In this area, we plan to elaborate on illustrative applications, on their requirements and on how these map into technology design issues.

Although the IT transformation in the 20th century appeared revolutionary, a bigger change is yet to come, exemplified by the Cyber-Physical Computer systems. Here, the computer systems do not only compute abstract quantities; they are tightly integrated and interacting with the physical environment by taking sensor readings and acting on its environment. Such systems require a rethinking in our concepts and given that the computers interact with their environment, the timing is of increasing importance. With the continuation of Moore´s law, these systems are increasing in size. For example, today networks with 1000 sensor nodes have been constructed for collaborative processing of physical information, and it is expected that networks with tens of thousands of nodes will be constructed within a few years. In the long-term future, we can expect that networks with millions of sensor nodes will be constructed. While, these sensor systems generate an enormous amount of sensor data, applications are typically only interested in a few sensor readings or an aggregated quantity of the sensor readings. This poses the challenge on how to combine all these sensor readings to useful aggregated quantities and to do this efficiently. Due to the large scale it is imperative that the time-complexity does not depend on the number of sensor nodes.

Finally, another challenge that will also be addressed is the efficient integration of network protocols into higher level middleware, e.g., to efficiently support properties like transparent distribution, true multicasting and publisher-subscriber interaction models. One specific middleware that will be considered is the contract-based framework that is being developed within the FRESCOR project, aiming at providing a uniform approach for the application to express its QoS and timing requirements with respect to any system resource. Our challenge will be to provide the required network services at the lowest possible levels of the architecture, to efficiently support the pursued virtual resource abstraction.

Notice that the use of wireless technologies, as openness in general, poses many challenges related to security, such as intrusion avoidance and tolerance as well as enforcement of data privacy. Despite their high importance, these challenges will not be addressed in this activity but awareness to them will allow following the relevant research results developed elsewhere.

Technical Description: Joint Research

The workprogramme for this activity includes the development of specific protocols to provide some level of timeliness guarantees and minimize energy consumption in WSNs and MANETs, protocols to enforce agreed QoS levels in NESs (wired/wireless) and also to support dynamic QoS management, dynamic reconfiguration and other run-time adaptation methods to achieve efficient resource usage and less expensive fault tolerance. Moreover, we expect to provide more efficient networking support for distribution middleware, with improved bandwidth usage and timeliness, as well as to virtual resource middleware, with improved temporal isolation between hierarchical partitions. Finally, we expect to provide adequate protocols for wireless-based NESs, capable of delivering the required QoS, comparable to that achieved with the wired counterparts but providing large benefits in terms of deployment and weight.

The first 18 months will focus on one side, on producing a taxonomy of WSNs and MANETs for time-sensitive applications, addressing the existing protocols, their features and limitations, as well as the respective middleware for application development. On the other side, a parallel thread of action will produce a taxonomy of flexibility in NES, addressing several perspectives of the concept, from design flexibility to configuration flexibility, operational flexibility etc, but also within the scope of real-time distributed applications with more or less criticality.

It is also foreseen the that joint research will be developed on: (i) the design distributed algorithms for computing basic operations in large-scale networked embedded sensor systems such that their time-complexity is independent of the number of sensor nodes and; (ii) showing their usefulness in the application areas of control of physical systems and sensor fusion (taking into account the dynamic nature of such communication infrastructures); and (iii) the support of Quality-of-Service (QoS) in wireless sensor networks (such as the ART-WiSe framework) with the additional goal to contribute to the standardization process on IEEE 802.15.4/ZigBee suite of protocols.

WP6 Description - Hardware Platforms and MPSoC Design

WP number	6		**Start date or starting event:** T0 *(start of the project)*					
WP Title	**Thematic Cluster: Hardware Platforms and MPSoC Design (JPRA)**							
Activity type	RTD *Research and Technological Development*							
WP Leader	Jan Madsen (DTU)							
Participant number	6	7	9	10	14	15	18	19
Participant short name	Bologna	TUBS	CEA	DTU	ETH Zurich	IMEC	KTH	Linkoping
Person-months per participant	13,75	9,25	4,50	9,25	16,00	9,25	9,25	9,25

Objectives

The purpose of this cluster is to integrate different view points and approaches to MPSoC design and programming. The cluster will consider the hardware architecture and software components in their interaction, investigate tools for accurate estimation of certain design parameters (power, performance), and provide the designer with adequate support for design space exploration and optimisation.

Description of work

The work of the cluster is partitioned into two activities.

The main scientific challenges addressed in the Activity *"Design" are* focused on how to map complex applications onto multi-core hardware platforms. This includes addressing allocation and scheduling issues like: scalability, flexibility, composability, predictability, design-time reduction and increased dynamism. The conceptual front-ends of application design flows are programming models and abstractions that must be efficiently supported by an application development environment that provides templates, components and libraries.

In the first 18 month of the project, the partners will focus on developing the formal and algorithmic frameworks required for design space exploration and optimization of highly-complex multicore platforms. The challenge with respect to the current state of the art is the high degree of concurrency in these systems, which enormously complicates the search for optimal design points. The other main challenge that will be tackled is the development of a more complete understanding of the interplay of design decisions related to different cost metrics, such as energy, reliability, predictability and cost.

The major focus of the activity on Platform *"Analysis"* is to establish a set of models and analysis methods that (a) scales to massively parallel and heterogeneous multiprocessor architectures, (b) is applicable to distributed embedded systems as well, (c) allows for the analysis of global predictability and efficiency system properties and (d) takes the available hardware resources and the corresponding sharing strategies into account.

Robustness to changes is particularly important for systems on chip since the cost of a redesign is high. So integration of methods and tools will be needed to be able to (1) define meaningful robustness metrics that reflect design tradeoffs (2) assess the robustness of a design based on such metrics. This integration will extend the world leading position of Europe in the field of scalable formal performance analysis to hardware platform and MPSoC design.

We will focus on methods that satisfy composability properties and to lift the component-based methods as known from software design to interfaces that talk about resource interaction. In addition, we are interested in adding run-time adaptivity to systems while using efficient run-time estimation methods combined with distributed finite horizon control methods. Again, the focus is on predictability AND efficiency. Here, we will use the expertise that is available at ETH Zurich (Lothar Thiele),and Bologna (Luca Benini). Hannu Tenhunen (KTH), Stylianos Mamagkakis (IMEC), Rolf Ernst (TUBS) will be involved in this activity.

Deliverables

Each deliverable is a report on the activity's work, provided yearly.

D-6.1-Y1	Platform and MPSoC Design Report
D-6.2-Y1	Platform and MPSoC Analysis Report
D-6.1-Y2	Platform and MPSoC Design Report
D-6.2-Y2	Platform and MPSoC Analysis Report
D-6.1-Y3	Platform and MPSoC Design Report
D-6.2-Y3	Platform and MPSoC Analysis Report
D-6.1-Y4	Platform and MPSoC Design Report
D-6.2-Y4	Platform and MPSoC Analysis Report

Overall Objective

The purpose of this cluster is to integrate different view points and approaches to MPSoC design and programming. Therefore, the work is based on existing and future hardware platforms and their expected properties as well as anticipated application domains. The cluster will consider the hardware architecture and software components in their interaction, investigate tools for accurate estimation of certain design parameters (power, performance) based on appropriate models for hardware and software components, and provide the designer with adequate support for design space exploration and optimisation.

The importance of resource awareness in embedded systems is growing very rapidly. One major aspect is predictability, in particular concerning the timing behaviour. With the growing software content in embedded systems, and the diffusion of highly programmable and re configurable platform, software is given an unprecedented degree of control on resource utilization. Therefore, the major focus of the combined activities is to establish a design methodology that (a) scales to massively parallel and heterogeneous multiprocessor architectures, (b) allows for predictable system properties and (c) uses the available hardware resources in an efficient manner. Promising approaches are based on increasing the adaptivity on various levels and on composable frameworks.

Indicators for Integration

Interactions planned between partners include:

- 10 Joint publications / year describing the results in terms of new methods and tools.
- Joint organization of workshops, tutorials, special sessions in international highly recognized conferences, e.g. EMSOFT, ISLPED, ISSS/CODES, DATE, DAC, and DSD. Yearly target is 1 workshop, 1 PhD course/school, 2-3 conference tutorials and special sessions.
- Integration of tools existing at the partner sites and definition of tool flows integrating tools from the different partners.

- Mobility, i.e. the number of PhD student and faculty exchanges. This integration activity will also introduce the concept of "student clusters", where more than two PhD students from different partners will work together in a single location.
- Impact on industrial practice in the area of MPSoC design and analysis. This objective will leverage student internships at associated industrial partner's sites.

JPRA Activity: "Platform and MPSoC Design"

Core Teamleaders

Luca Benini (University of Bologna - Italy); Lothar Thiele (ETH Zurich - Switzerland); Rolf Ernst (TUBS – Germany); Jan Madsen (DTU - Denmark); Petru Eles (Linkoping - Sweden); Stylianos Mamagkakis (IMEC - Belgium); Hannu Tenhunen (KTH - Sweden); Thierry Collette (CEA - France)

Affiliated Teamleaders

Dimitrios Soudris (DUTH - Greece); Salvatore Carta (UNICA – Italy); Roberto Zafalon (STMicroelectronics – Italy); Henrik Lönn (Volvo Technology Corporation - Sweden); Nigel Drew (FreeScale Semiconductors – United-Kingdom); Rune Domsteen (Prevas – Denmark); Karsten Nielsen (ICEpower Bang & Olufson – Denmark); ???(PAJ Systemteknik - Denmark)

Policy Objective

While there is wide consensus on the fact that hardware platforms for embedded applications will continue to be multi-core, with increasing degrees of parallelism, the evolution trajectory on programming models, design-time and run-time application environments is much less clear. The consequence is fragmentation: while many research teams are working on one or more of these domains, there is little communication and integration, this leads to duplication of results and overall slow progress. The teams involved in this activity have a wide-ranging research experience which covers all the key areas in MPSoC application specification mapping. The integration activity supported by ArtistDesign will help the participants to the cluster in strengthening the coherency of their approaches and focus on addressing complementary issues in a synergistic fashion. In particular, there will be an initial effort in reaching a common consensus on the most critical issues to be addressed, define common terminology and decide the operational strategy to address them in a collaborative fashion. The expected impact will be a faster and more consistently focused development of methods and tools in support of application development and mapping.

Background

The partners involved in this activity have very active ongoing cooperations on a number of topics. A non-exhaustive set of examples of background cooperation activities is given here.

IMEC, Bologna, University of Madrid and DUTH have ongoing collaboration on dynamic memory management optimizations at the system level for single processor systems, which they plan to extend in the domain of multiprocessor systems [1].

ETH Zurich and Bologna have ongoing collaborations on optimal management of smart sensor with energy harvesting capabilities. Wireless sensor networks are a very relevant example hardware platforms with very tight energy constraints. The limited battery lifetime can be extended indefinitely if the node is equipped with energy harvester that collect and store energy from the environment. However, given the erratic nature of environmental energy sources, the rate at which sensing, computation and storage operations can be performed should be dynamically adjusted to the energy availability using a closed-loop optimal control policy [3]

KTH and Bologna have cooperated on the development of optimal static mapping strategies for real-time biomedical application onto multi-core platforms [2]. This work has demonstrated that workload allocation is not sufficient to obtain energy-optimal mappings, as a very significant contribution to the power budget is spent in memory transfers. Hence synergistic memory and computation allocation approach is required.

Linkoping and Bologna have cooperated on allocation and scheduling policies for low power systems, where clock frequency and voltage setting are also degrees of freedom for optimization [4].

DTU and Linkoping have cooperated on optimisation of distributed embedded systems [5].

[1] David Atienza, Stylianos Mamagkakis, Francesco Poletti, Jose Manuel Mendias, Francky Catthoor, Luca Benini, Dimitrios Soudris: Efficient system-level prototyping of power-aware dynamic memory managers for embedded systems. Integration 39(2): 113-130 (2006)

[2]. Al Khatib, F. Poletti, D. Bertozzi, L. Benini, M. Bechara, H. Khalifeh, A. Jantsch, R. Nabiev. A multiprocessor system-on-chip for real-time biomedical monitoring and analysis: architectural design space exploration. Design Automation Conference 2006.

[3] C. Moser, L. Thiele, D. Brunelli, L. Benini, Adaptive power management in Energy Harvesting systems. Design Automation and Test in Europe 2007.

[4] Ruggiero M., Paci G., A. Guerri, D. Bertozzi, M. Milano, L. Benini, Andrei A., “A Cooperative, Accurate Solving Framework for Optimal Allocation, Scheduling and Frequency Selection on Energy-Efficient MPSoCS”, Proceedings of The IEEE International SOC Conference (SOCC), 2006.

[5] Traian Pop, Paul Pop, Petru Eles, Zebo Peng "Bus Access Optimisation for FlexRay-based Distributed Embedded Systems" Design, Automation, and Test in Europe Conference 2007

Technical Description: Joint Research

The main scientific challenges addressed in this activity are focused on how to map complex applications onto multi-core hardware platforms. This includes addressing allocation and scheduling issues like: scalability, flexibility, composability, predictability, design-time reduction and increased dynamism. The problem is complex and multi-faceted. On one hand, we have static (design/compile time) approaches, where applications are analyzed and optimal mapping decisions are taken before the platform is deployed in the field. On the other hand, we have dynamic, runt-time approaches where mapping decisions are taken online, and they are triggered by environmental and workload variations. While these approaches start from different premises, they should not be regarded as alternative, rather they are synergistic. Design time analysis and decisions can help in providing a good starting point for run-time adaptation; moreover off-line pre-computation can reduce the overhead of the online policies making them more reactive and less resource-hungry. One important requisite for any mapping strategy is to ensure predictability AND efficiency. Note that online adaptation is not adverse to predictability: if online adaptation is based on feedback control (e.g. finite horizon), it can be used to “stabilize” the system, and make it more robust (predictable) in response to environmental variations (e.g. temperature).

Another scientific challenge addressed in this activity is the development innovative reliable multicore programming models and architecture platform able to address computation and control oriented applications. One key building block is the development of efficient synchronization & communication abstractions that are required for successfully deploying MPSoCs in embedded application domains. Efficiency is inherently related to both power and performance; hence it is an energy metric. In embedded systems, productivity-enhancing abstractions are acceptable only if they do not compromise efficiency, so the focus is on how to enable fast development (debugging, tuning) without losing efficiency. It is also extremely important to take into account variability of both hardware fabrics and application workloads, which is deemed to rapidly increase. Hence, the concurrency management layer should provide means for dynamically managing workload variations, as well as hardware unpredictability sources.

In the first 18 month of the project, the partners will focus on developing the formal and algorithmic frameworks required for design space exploration and optimization of highly-complex multicore platforms. The challenge with respect to the current state of the art is the high degree of concurrency in these systems, which enormously complicates the search for optimal design points. The other main challenge that will be tackled is the development of a more complete understanding of the interplay of design decisions related to different cost metrics, such as energy, reliability, predictability and cost. This is at the basis of trade-off analysis and sensitivity analysis which are critically required when designing systems under multi-dimensional constraints.

Technical Achievements Expected

The conceptual front-ends of application design flows are programming models and abstractions, which must be efficiently supported by an application development environment that provides templates, components and libraries. KTH, DTU, Bologna and CEA will work in this area, and contribute to the definition of efficient (both in terms of productivity and of execution) programming abstractions as well as to the creation of a “specification toolbox” for linking functional specification to non-functional properties such as reliability, power, timing. The front-end development flow will also support successive refinements and incremental specification.

Application modelling and specification interface with application mapping which takes care of binding abstract functional specification and non-functional requirements onto the available hardware resources. Static (design time) mapping is essential for design space exploration and for application refinement, and will be supported in strong synergy with the analysis activity in the cluster. ETH Zurich, DTU, IMEC, TUBS and Linkoping will contribute to this topic.

While design time mapping and design space exploration are essential, they cannot provide a complete answer, especially in dealing with reliability and variability issues that are becoming increasingly important in embedded systems. For this reasons the partners in the cluster will focus also on dynamic (run-time) resource management. The construction of a dynamic resource management layer requires both the creation of a support environment that provides efficient observability and controllability mechanisms for the target system. Bologna and CEA will work in this area. ETH Zurich, DTU; IMEC, TUBS and Linkoping will focus on the policies, i.e., the control laws that drive the online adaptation performed by the resource management sub-system in response to variations in environmental conditions workloads, user requirements. KTH will focus on policies and methodology development and tools for dynamic resource management

The teams involved in this effort have been at the forefront of the research community in the exploration of both static and dynamic allocation and management techniques for multi-core platforms. Their expertise covers the critical competences required to achieve the objectives. In particular the partners have a quite unique mix of competences both in formal techniques for system analysis and optimization (ETH Zurich, TUBS, DTU, Linkoping) and in the development deployment of resource management solutions on platforms and systems (Bologna; IMEC; CEA, KTH). Hence, the integration activity performed in this cluster will provide the generality and theoretical strength provided by formal techniques, as well as the practicality and applicability of highly tuned implementations.

The main difficulties to be encountered are in the characterization of practical computing platforms and their workload. Current embedded systems platforms are very complex both in terms of their internal architecture and in their workload. A characterization of both is required to perform offline analysis and optimization, and a detailed knowledge of their development environment is essential for deployment of practical dynamic resource management solutions. These difficulties will be tackled by establishing strong links with the companies that develop the most advanced platforms in various application areas.

JPRA Activity: “Platform and MPSoC Analysis”

Core Teamleaders

Lothar Thiele (ETH Zurich - Switzerland); Luca Benini (Bologna - Italy); Rolf Ernst (TUBS - Germany); Jan Madsen (DTU - Denmark)*;* Petru Eles (Linkoping - Sweden); Stylianos Mamagkakis (IMEC - Belgium); Axel Jantsch and Hannu Tenhunen (KTH - Sweden)

Affiliated Teamleaders

Michaela Huhn (TUBS - Germany); Kai Richter (Symtavision); Henrik Lönn (Volvo Technology Corporation - Sweden); FreeScale, STM, CoWare; Infineon

Policy Objective

With growing maturity of scalable performance analysis algorithms and tools, new aspects such as the platform robustness can be included in analysis. Robustness to changes is particularly important for systems on chip since the cost of a redesign is high. At the same time robustness to faults is becoming a concern with shrinking feature sizes. In most practical cases, power consumption must be considered. There is currently no team in Europe that addresses all aspects. So integration of methods and tools will be needed to be able to (1) define meaningful robustness metrics that reflect design tradeoffs (2) assess the robustness of a design based on such metrics. This integration will extend the world leading position of Europe in the field of scalable formal performance analysis to hardware platform and MPSoC design.

Background

The activity will be based on the complementary expertise of the participating partners in terms of Hardware Platform and MPSoC Analysis. In particular, the following areas are covered: Power modelling and analysis, power robustness assessment (Bologna), platform performance modelling (TUBS), analytical methods for reliability, performance and adaptability analysis of execution platforms (DTU), reliability modelling, analysis and optimization (Linkoping), interfaces that communicate at run-time, aspects that are relevant for the efficiency of the run-time mapping components (IMEC), simulation techniques and tools for NoC performance estimation and validation, interconnect and communication centric performance estimation techniques (KTH).

In addition, there have been already joint work and publications by some of the members of this activity which will be used as a valuable starting point:

C. Moser, D. Brunelli, L. Thiele, and L. Benini, “Lazy scheduling for energy harvesting sensor nodes.”, The Fifth IFIP Working Conference on Distributed and Parallel Embedded Systems (DIPES 2006), Braga, Portugal, October 13-15, 2006.

Simon Künzli, Francesco Poletti, Luca Benini, Lothar Thiele: Combining Simulation and Formal Methods for System-Level Performance Analysis, IEEE Design Automation & Test in Europe (DATE), Munich, Germany, March 2006.

C. Moser, D. Brunelli, L. Thiele, and L. Benini, “Real-time scheduling with regenerative energy.”, 18th Euromicro Conference on Real-Time Systems (ECRTS 2006), Dresden, Germany, July 5-7, 2006.

Kai Richter, Marek Jersak, Rolf Ernst. How OEMs and suppliers can tackle the network dimensioning problem, Embedded Real Time Software Congress (ERTS06), Toulouse, France, January 25-27, 2006.

Kai Richter, Rolf Ernst. Applying Real-Time Network Research in the Automotive Industry: Lessons Learned and Perspectives, Euromicro Conference on Real-Time Systems (ECRTS), satellite workshop on Real Time Networks (RTN), Dresden, Germany, July 2006.

In more details, the above mentioned group has been working intensively on Power Modeling for SoC Platforms. In particular, they developed a virtual platform for power modelling of complex multi-core systems on chip. This platform can facilitate further integration among partners and associates, thanks to is flexibility and generality. In terms of “scheduling based energy optimization for energy-scavenging wireless sensor networks”, a novel scheduling strategy (called lazy scheduling) that is well suited to energy-harvesting systems operating under real-time constraints has been developed by ETH Zurich and Bologna. It is the first result of this kind in this quickly growing research area and received a lot of attention in the scientific community.

At ETH Zurich, an open tool set is available that allows the performance analysis of distributed embedded systems and MPSoC. It is based on the concept of Modular Performance Analysis (MPA). In addition, there are first results available that connect this system to the MPARM simulation framework from Bologna and the Symta/S analysis system from TUBS and Symtavision.

First results on the algorithm distribution and on topology determination have been published in:

S. Stein, A. Hamann, and R. Ernst. Real-time Property Verification in Organic Computing Systems. In Proceedings of the 2nd International Symposium on Leveraging Applications of Formal Methods, Verification and Validation (ISoLA 2006), Nov. 2006.

S. Stein, A. Hamann, and R. Ernst. Real-time Management in Emergent Systems. In C.Hochberger and R. Liskowsky, editors, INFORMATIK 2006 Informatik für Menschen, volume P-93 of GI-Edition. Lecture Notes in Informatics, pages 112-119, Bonn, Germany, Sept. 2006. Köllen Verlag.

S. Schliecker, S. Stein and R. Ernst. Performance Analysis of Complex Systems by Integration of Dataflow Graphs and Compositional Performance Analysis. Proc. of Design Automation and Test in Europe (DATE), Nice, 2007

Technical Description: Joint Research

The major focus of the activity on Platform Analysis is to establish a set of models and analysis methods that (a) scales to massively parallel and heterogeneous multiprocessor architectures, (b) is applicable to distributed embedded systems as well, (b) allows for the analysis of global predictability and efficiency system properties and (c) takes the available hardware resources and the corresponding sharing strategies into account. Promising approaches are based on composable frameworks and treating resources as first class citizens in the analysis. Both, simulation-based and analytic methods will be combined. In addition, methods that focus on worst-case/best-case results as well as those based on stochastic models will be combined.

As a central ingredient of any analysis model, synchronization & communication abstractions are required for successfully deploying MPSoC hardware in embedded application domains. Efficiency is inherently related to both power and performance; hence it is an energy metric. In embedded systems, abstractions are acceptable only if they do not compromise efficiency. It is also extremely important to take into account variability of both hardware fabrics and application workloads, which are deemed to rapidly increase. In particular, the above abstractions need to be embedded into a framework that allows to analyze the performance properties and memory requirements of distributed systems. In particular, we will focus on methods that satisfy composability properties and to lift the component-based methods as known from software design to interfaces that talk about resource interaction. In addition, we are interested in adding run-time adaptivity to systems while using efficient run-time estimation methods combined with distributed finite horizon control methods. Again, the focus is on predictability AND efficiency. Here, we will use the expertise that is available at ETH Zurich (Lothar Thiele) and Bologna (Luca Benini). Hannu Tenhunen (KTH), Stylianos Mamagkakis (IMEC), Rolf Ernst (TUBS) will be involved in this activity.

Another major challenge is to provide analysis tools and techniques to support the transitions between different abstraction levels in the design flow. Constraints should be communicated at design-time from one step to the next, taking into account the global effect that they will introduce in the system. Also, in order to ensure adaptivity of the system an interface should communicate at run-time the changes in the resource requests and the changes in the actual resource availability.

WP7 Description - Transversal Integration

WP number	7			**Start date or starting event:** T0 *(start of the project)*						
WP Title	**Transversal Integration (JPRA)**									
Activity type	RTD *Research and Technological Development*									
WP Leader	Alberto Sangiovanni (PARADES)									
Participant number	2	3	4	5	6	7	8	9	10	11
Participant short name	UJF/VERIMAG	Aachen	Aalborg	Aveiro	Bologna	TUBS	Cantabria	CEA	DTU	Dortmund
Person-months per participant	14,75	2,75	2,00	2,50	5,25	2,75	2,50	2,75	2,25	5,25
Participant number	12	13	14	15	16	17	18	19	20	21
Participant short name	EPFL	ESI	ETH Zurich	IMEC	INRIA	TUKL	KTH	Linkoping	ULund	MDH
Person-months per participant	2,50	9,50	5,25	5,25	2,25	2,50	4,50	2,75	2,50	2,25
Participant number	22	23	24	25	26	27	28	29	30	31
Participant short name	OFFIS	PARADES	Passau	SSSA-Pisa	Porto	Saarland	PLU-Salzburg	Uppsala	Vienna	York
Person-months per participant	1,50	4,00	1,75	2,75	2,50	2,50	1,50	2,75	2,50	5,25

Objectives

UJF/VERIMAG (France), Aachen (Germany), Aalborg (Denmark), Aveiro (Portugal), Bologna (Italy), TUBS (Germany), Cantabria (Spain), CEA (France), DTU (Denmark), Dortmund (Germany), EPFL (Switzerland), ESI (Netherlands), ETH Zurich (Switzerland), IMEC (Belgium), INRIA (France), TUKL (Germany), KTH (Sweden), Linkoping (Sweden), ULund (Sweden), MDH (Sweden), OFFIS (Germany), PARADES (Italy), Passau (Germany), SSSA-Pisa (Italy), Porto (Portugal), Saarland (Germany), PLU-Salzburg (Austria), Uppsala (Sweden), Vienna (Austria), York (United-Kingdom).

The aim of this workpackage is to seek global integration, through complementary types of activities. It has been defined as a simple workpackage rather than a cluster, mainly because its activities are transversal to all the Thematic Clusters. Transversal Integration is a key activity to the NoE's success. To varying degrees, all the ArtistDesign partners participate in it.

Activities of this workpackage include Integration of Thematic Clusters, and Integration Driven by Industrial Applications.

Description of work

- Integration of Thematic Clusters
  Integration between Thematic Clusters will combine Thematic competencies in a coherent design flow. Initially, it will target design methodologies for Adaptivity, and

Predictability & Performance.

- For *Adaptivity*, we will study frameworks for efficient use of resources, adaptive QoS management, as well as adaptive mechanisms for achieving robustness and dependability. This activity will lead to development around tools, such as the Shark RTOS, and the TrueTime simulator.
- For *Predictability and Performance*, we will study frameworks allowing for predictable behaviour, with a low performance overhead. This activity will lead to development around tools such as the WCET analysis tool from TUBS, the Symta/S (TUBS), MPA-RTC (ETH Zurich) and UPPAAL, and the aiT timing analyzer of AbsInt.

- Integration Driven by Industrial Applications
  The aim of this activity is to take into account specific industrial needs and provide inputs for the Integration of the Thematic Clusters. It will mainly consist of organisation of meetings, with selected industrial partners, to analyse the design flow for application areas such as: Automotive, Nomadic, Health Applications for Independent Living. This will result in the identification of important issues that cut across the existing Thematic Cluster topics.
  The conclusions will be published in a white paper, widely distributed through the ARTIST Web Portal, in workshops, and journals. These will also be used to drive integration activities between Thematic Clusters.

Deliverables

Each deliverable is a report on the activity's work, provided yearly.

D-7.1-Y1	Design for Adaptivity Report
D-7.2-Y1	Design for Predictability Report
D-7.3-Y1	Industrial Integration Report
D-7.1-Y2	Design for Adaptivity Report
D-7.2-Y2	Design for Predictability Report
D-7.3-Y2	Industrial Integration Report
D-7.1-Y3	Design for Adaptivity Report
D-7.2-Y3	Design for Predictability Report
D-7.3-Y3	Industrial Integration Report
D-7.1-Y4	Design for Adaptivity Report
D-7.2-Y4	Design for Predictability Report
D-7.3-Y4	Industrial Integration Report

The aim of this workpackage is to seek global integration, through complementary types of activities. It has been defined as workpackage rather than a cluster, mainly because its activities are transversal to all the Thematic Clusters. Transversal Integration is essential to the NoE's success. To varying degrees, all the ArtistDesign partners participate in it.

Activities of this workpackage include Integration of Thematic Clusters, and Integration Driven by Industrial Applications.

- Integration of Thematic Clusters
  Integration between Thematic Clusters will combine thematic competencies in a coherent design flow. In general, this will target design methodologies leading to systems that meet general requirements such as adaptivity, predictability, security, etc. This is a long-term approach – the list of such requirements can be very long. To start, the NoE will focus on *Adaptivity* and *Predictability*. The workplan for these 2 transversal activities is described below
- Integration Driven by Industrial Applications
  The aim of this activity is to take into account specific industrial needs and provide inputs for the Integration of the Thematic Clusters. It will mainly consist of organisation of meetings, with selected industrial partners, to analyse the design flow for application areas such as: Automotive, Nomadic, Health Applications for Independent Living. This will result in the identification of important issues that cut across the existing Thematic Cluster topics.

JPRA Activity: "Design for Adaptivity" (Integration of Thematic Clusters)

Core Teamleaders

Karl-Erik Årzén (ULund – Sweden); Giorgio Buttazzo (SSSA-Pisa - Italy); Alan Burns (York - United-Kingdom); Lothar Thiele (ETH Zurich - Switzerland); Luca Benini (Bologna - Italy); Stylianos Mamagkakis (IMEC - Belgium); Rolf Ernst (TUBS - Germany); Rainer Leupers (Aachen – Germany); Hannu Tenhunen (KTH – Sweden); Björn Lisper (MDH – Sweden) ;

Affiliated Teamleaders

Pau Martí (UPC – Spain); Alejandro Alonso (UPM – Spain); Lucia Lo Bello (Catania – Italy); Johan Eker (Ericsson – Sweden); Paolo Gai (EVIDENCE Srl – Italy); Zdenek Hanzalek (Czech TU – Czech Republic)

Policy Objective

An embedded hardware-software system is adaptive, if it can modify its behaviour and/or architecture to changing requirements. Adaptivity is increasingly important as the complexity and autonomy of embedded systems increases. Adaptivity is required both off-line at design-time and on-line at run-time. Off-line adaptivity is required to handle changing system specifications and to support platform-based or product-family based development. On-line adaptivity is required to be able to dynamically respond to changing conditions and contexts and through this improve performance and resource utilisation. The changes can involve different types of resource requirements, changing system objectives, and changing external conditions.

Adaptivity is a cross-cutting system characteristic that affects both hardware and software. At the software-level adaptivity is mainly concerned with flexible and adaptive resource scheduling, e.g., CPU time scheduling. At the hardware-level adaptivity includes both adaptation of operation modes, e.g., supply voltage and clock frequency, processor instruction sets, and dynamic management of hardware resources, e.g., processing elements and memory.

Background

This activity has its background in the ARTIST and ARTIST2 networks of excellence. In ARTIST2 the cluster on Adaptive Real-Time Scheduling and the cluster on Control for Embedded Systems have jointly worked on software and network-based approaches to adaptive scheduling. Within this context several tools have been developed, including the SHARK RTOS and the TrueTime real-time kernel and network simulator. In the current activity this circle is now widened to also include hardware-based approaches to embedded system adaptivity.

Technical Description: Joint Research

The scientific challenges within the cluster include:

Adaptivity in system modelling – how is adaptivity modelled

- Efficient adaptation – how can adaptation mechanisms be made resource efficient
- Frameworks for adaptivity – unified frameworks for adaptivity (negotiation, contracts, QoS)
- Predictable and dependable adaptivity – what types of formal guarantees concerning predictability and dependability can be stated for an adaptive system
- Robustness and adaptivity – the relationships between robust design techniques and adaptive design techniques
- Adaptivity from an application's point of view – how should the adaptation mechanisms be exposed to the application developers (APIs etc)

Both software and hardware related adaptivity issues will be considered within the cluster, although the majority of the teams are working on the software issues. The main focus will be run-time adaptivity, rather than off-line adaptivity.

Technical Description: Tools and Platforms

The tools-based activities will build upon the developments already available through ARTIST2. The tools that will be further developed, integrated and disseminated include:

- The SHARK RTOS

  SHARK (Soft and HArd Real-time Kernel) is a real-time operating system developed at the ReTiS Lab of SSSA-Pisa, with the collaboration of the Robotics Lab of the University of Pavia. It provides a number of internal kernel mechanisms specifically designed to facilitate the development of demonstrators and prototypes. It supports applications where computational tasks can have explicit timing constraints; it includes several advanced algorithms for task scheduling and shared resource management, which can be dynamically selected by the user through a configuration file. It includes drivers for the most common I/O peripherals; it complies with the POSIX standard, PSE51 profile.

- The TrueTime simulator
- Aachen tool chain for automated customization of embedded processor architectures (see also R. Leupers, P. Ienne: Customizable Embedded Processors, Morgan Kaufmann, 2006) in combination with ESL tool chain from CoWare.
- SWEET (SWEdish Execution Time tool). This is a WCET analysis tool which includes an advanced automatic flow analysis to reduce the need for manual annotations specifying loop iteration bounds and infeasible paths. Currently supported processors are ARM7 and NEC V850.

Main Funding

ULund:

- VR project “Modelling and Control of Server Systems”,
- VINNOVA project “Feedback Based Resource Management and Code Generation for Soft Real-Time Systems” together with Ericsson
- New proposal to VR under submission
- STREP proposal to EU FP7 under submission
- EU FP7 FET proposal under submission
- VINNOVA Embedded Systems proposal under submission

Aachen:

- UMIC Excellence Cluster (German Research Foundation)
- EU FP6 projects (SHAPES, HiPEAC)
- Industrial grants

MDH:

- SSF strategic centre PROGRESS
- CUGS Swedish National Research School in Computer Science
- KK-foundation project “Execution Time Analysis of Time-Critical Embedded Software“
- STREP proposal to EU FP7 under submission

ETH Zurich:

- EU IP SHAPES (FP 6)
- National Competence Research ‘Mobile Information and Communication Systems’
- Industry Cooperation, especially SIEMENS Building Technologies
- Swiss National Science Foundation Project on “Performance Evaluation of Distributed Embedded Systems”

IMEC

- Funds from Flemish community
- International & Flemish industry
- European community projects
- European space agency projects

JPRA Activity: "Design for Predictability and Performance"
(Integration of Thematic Clusters)

Core Teamleaders

Bengt Jonsson (Uppsala - Sweden); Luca Benini (Bologna - Italy); Michael Gonzalez-Harbour (Cantabria - Spain); Peter Marwedel (Dortmund - Germany); Tom Henzinger (EPFL - Switzerland); Lothar Thiele (ETH Zurich - Switzerland); Arnout Vandecappelle (IMEC - Belgium); Alain Girault (INRIA - France); Petru Eles (Linkoping - Sweden); Reinhard Wilhelm (Saarland - Germany); Bengt Jonsson (Uppsala - Sweden); Peter Puschner (Vienna - Austria); Alan Burns (York - United-Kingdom); Alberto Sangiovanni-Vincentelli (PARADES)

Affiliated Teamleaders

Rolf Ernst (TUBS, Germany)

Policy Objective

Embedded systems in many application domains are required to satisfy strict requirements on timing, while respecting limited supply of resources in terms of memory, processing power, power consumption, etc. All systems also have increasing demands on (average) performance, which has motivated the introduction of features such as caching, pipelining, and (now becoming very prominent) multiprocessor platforms. Almost all such efficiency-increasing features drastically increase variability and decrease analyzability of response-times, etc. and thus have a detrimental effect on predictability. Since the introduction of new architectural features is inevitable, it is important to

- develop technology and design techniques for achieving predictability of systems built on modern platforms, and
- investigate the trade-offs between performance and predictability.

This work will need to be carried out in a synergistic manner, involving all levels of abstraction in embedded systems design, spanning from high-level requirements to detailed implementation details on specific platforms, and is therefore the subject of a transversal activity involving all clusters of the NoE.

Background

During the operation of the ARTIST2 network of excellence, links have been developed between groups working on compiler techniques for achieving predictability of code. There is a close cooperation between ETH Zurich (Lothar Thiele), Saarland (Reinhard Wilhelm) and Dortmund (Peter Marwedel) on the subject of predictability and efficiency. This resulted in joint journal papers on this issue and the joint organization of an international workshop. The results are related to assessing the state of the art in combining predictability and efficiency as well as in describing new approaches, models and methods. During ARTIST2, links have also been established with groups working on general techniques for guaranteeing predictability in component-based design. For instance, EPFL (Tom Henzinger) and ETH Zurich (Lothar Thiele) are part of a large national project in the area of mobile information and communication systems. The cooperation relates to interface-based design of real-time embedded systems. EPFL, PLU-Salzburg and PARADES are collaborating on compositional languages and approach to embedded system that can be considered the extension of the Giotto approach and are reminiscent of the Metropolis and Ptolemy work carried out at Berkeley. Finally, work in the Operating Systems and Networks areas have established many

links both to other activities, e.g., by the development of technology for contract-based scheduling, which provides a nice interface to systems modelling activities.

Technical Description: Joint Research

The longer-term Challenges addressed by this activity appear at all levels of abstraction in the design process:

- **Modeling and Validation of systems and of components**: Principles and structures for system and component modelling that are conducive to achieving predictability, by allowing *a priori* predictability analysis and by allowing mappings to platform architectures that preserve predictability. Investigations of how modelling and analysis techniques extend to non-traditional system structures, including distributed and networked architectures, for which predictability is more difficult to achieve. Exploring trade-offs between predictability, resource consumption and performance.
- **Timing Analysis**: Foundations for timing predictability and system-design concepts that increase predictability. The issues stretch from the processor architecture across all layers to the application and is caused by the variability of execution times. This activity should increase the predictability of system behaviour (Dortmund, Saarland). Timing analysis for compilation, especially in the light of multiple processors and other architectural features (Saarland, Vienna).
- **OS/MW/Networks**: Exploring the trade-off between performance and predictability in scheduling (York). Investigations of software architectures for time-predictable real-time operating systems, with the goal to avoid that the execution of OS code adversely affects the time-predictability of application tasks and vice versa, thus making the computation-time needs of both operating system activities and application tasks easily predictable (Vienna).
- **System Architectures and Hardware Platforms**: Modeling of resources, and multiple-objective optimization (ETH Zurich, IMEC). Architectures for timing-predictable systems (ETH Zurich, Saarland, Vienna). Component-based design for predictable and efficient systems (ETH Zurich).

The technical achievements will contribute to a suite of techniques across the abstraction levels of embedded system design, including application modelling and analysis, scheduling support, compilers, and platform design techniques. The achievements will also entail interfacing of existing tools for design of embedded systems.

Expected technical achievements during the first 18 months include:

- **Modeling and Validation:** Techniques for analyzing timing predictability that extends traditional techniques to distributed architectures. Utilization of component resource interfaces and contracts for scheduling in component and system modelling (Cantabria, Linkoping, Uppsala) *(this links with OS/MW/Networks and Hardware platforms)*

- **Compilation Techniques and Timing Analysis:**
  Investigation of the link between intra-task level scheduling and WCET analysis. The goal is to use the methods of abstract interpretation in order to combine both areas in a cross-layer approach. In particular, we expect results that answer the question whether preemptive scheduling is still of use in modern processor architectures (ETH Zurich, Saarland), and to develop techniques for WCET analysis and system scheduling for multiprocessors with shared memory access (TUBS, Linkoping). Also developed will be compile-time techniques that address the memory wall problem and avoid the resulting huge variability of the access times (Dortmund). A reduction of execution 50% of WCET without negative impact on average performance is expected *(this links with Modeling and Validation and Hardware platforms).*

- **OS/MW/Networks:**
  Definition of an operating-system architecture that supports a modular and composable analysis of the worst-case timing of operating-system activities and application tasks (Vienna).
  A framework will be constructed that will allow the resources of modern platforms to be abstracted so that overall predictions of rates of progress and, where appropriate, energy usage can be obtained. The work on scheduling will involve all the core members from the Resource Management cluster. Definition of an operating-system architecture that supports a modular and composable analysis of the worst-case timing of operating-system activities and application tasks (Vienna). Links to model driven approaches will be explored by collaboration with the Modeling and verification cluster *(this links with Modeling and Validation and Hardware platforms).*

- **System Architectures and Hardware Platforms:**
  Combining expertise on low power design in order to determine systems that optimize the average case behaviour but still are able to meet time bounds. The intention is to use control algorithms for this purpose and combine them with resource interfaces (Bologna, ETH Zurich). Memory structures and bus architectures for predictability (Linkoping, Bologna, Dortmund) *(this links with all the other clusters).* Using flexible multi-level architectural models in a unified modelling framework to favour “horizontal” and “vertical” composition with predictable performance (PARADES).

Technical Description: Tools and Platforms

It will be investigated how tools that focus on different abstraction levels in design flow can be interfaced for predictable design.

- The WCET analysis tool from TUBS will be integrated into the system level analysis, scheduling, and optimization tool from Linkoping.
- ETH Zurich will investigate the effect of the different abstractions used in tools like Symta/S (TUBS), MPA-RTC (ETH Zurich) and UPPAAL on the accuracy of the performance analysis.
- The aiT timing analyzer of AbsInt will be more closely integrated with wcc, the worst case execution time aware compiler from the University of Dortmund. Flow facts generated by wcc will be accessible to aiT and potentially lead to tighter execution time bounds.
- The UPPAAL and TIMES tools will be compared with and interfaced to the MPA-RTC tool (ETH Zurich): it will be considered how to interface with the contracts technology developed in the FRESCOR project (Cantabria).
- Vienna will work on a definition of the architecture and components of a time-predictable operating system, as well as a prototype implementation, capitalizing on expertise also of other partners.

- PARADES will work on architectural models that encompass multiple non functional properties using the quantity manager approach introduced by Metropolis to achieve predictable refinements of design.
- A definition of the architecture and components of a time-predictable operating system shall be available by month 18 of ArtistDesign. By the end of the running period of the NoE, a prototype implementation of the OS shall be available for demonstration.

Main Funding

Linkoping: Public (national) funding from the Swedish Foundation for Strategic Research, and the Swedish Research Council.

ETH Zurich: EU IP SHAPES (FP 6), National Competence Research 'Mobile Information and Communication Systems', Industry Cooperation, especially SIEMENS Building Technologies, Swiss National Science Foundation Project on "Performance Evaluation of Distributed Embedded Systems'

Uppsala: Swedish Research Council (VR, CATS project); Swedish Strategic Research Foundation (SSF, SAVE project); FP6 project CREDO.

CEA: Generates 75% of its total budget coming from industrial partners and national and European project and received 25% of funding from the French government.

JPRA Activity: "Integration Driven by Industrial Applications"

Core Teamleaders

Alberto Sangiovanni Vincentelli (PARADES - Italy), **Ed Brinksma (ESI - Netherlands)**, UJF/VERIMAG (France), Aachen (Germany), Aalborg (Denmark), Aveiro (Portugal), Bologna (Italy), TUBS (Germany), Cantabria (Spain), CEA (France), DTU (Denmark), Dortmund (Germany), EPFL (Switzerland), ETH Zurich (Switzerland), IMEC (Belgium), INRIA (France), TUKL (Germany), KTH (Sweden), Linkoping (Sweden), ULund (Sweden), MDH (Sweden), OFFIS (Germany), Passau (Germany), SSSA-Pisa (Italy), (Portugal), Saarland (Germany), PLU-Salzburg (Austria), Uppsala (Sweden), Vienna (Austria), York (United-Kingdom)

This activity is de facto open to all core partners in the consortium, who can use the specific budget for this activity to attend its technical meetings.

Policy Objective

Each of the ArtistDesign Thematic Clusters (WP3-WP6) is important *per se* for advancing the state-of-the-art in embedded system design. However, if we wish to have a strong impact on industry and society at large, the results of the Thematic Clusters have to be harmonized in an overall design flow that can sustain the embedded design chain from conception of the product to its implementation. The chains vary in length and players according to the industrial segment addressed: for example, the design chain in automotive electronics starts with the car maker (e.g., BMW, Daimler Chrysler, Peugeot, Fiat), goes through the Tier 1 suppliers (e.g., Contiteves, Bosch, Magneti Marelli) and connects to the Tier 2 suppliers (e.g., FreeScale, ST, Infineon, Hitachi). It often includes IP providers such as programmable cores, RTOS and software development tool providers and design service companies. In the mobile communication domain, the chain starts with the application developers (e.g., gaming and video content), includes the telecommunication operators (e.g., Telecom Italia and Telefonica), the device makers (e.g., Nokia and Ericsson), the silicon makers (e.g., TI,

Qualcomm and ST) and outsourcing manufacturing companies (e.g., Flextronics). Today, there is stress in the chain as the technology advances may create opportunities to redefine the roles of the various players. In addition, the system integrators are often faced with an almost impossible task of composing their design out of parts supplied by companies whose design methods and standards are widely different and about which they have limited or no information. There is a need for an all-encompassing approach to system design that can make an entire industrial segment work as a virtual vertically integrated company.

The benefits of these flows and methods are obvious as they provide shorter time to market and better quality designs but require a will of the industrial segment to work together towards this goal. In the automotive domain, Autosar is an excellent step in that direction. Other industrial segments are less cohesive in searching for a unified approach to design.

In addition, society concerns such as energy, health and environment conservation, are offering new business opportunities for emerging technologies such as wireless sensor networks. The difficulty in these new opportunities resides in lack of standards and of experience with new communication concepts and, last but not least, in security.

We believe that all the Thematic Clusters bring something important to all industrial segments, but we need to pay attention to the way the results obtained by the clusters are formulated. Integration is a matter of modelling and providing interfaces that guarantee that the properties of the components are maintained after integration. Integration takes two forms: an horizontal one where different IPs coming from different companies or from different design groups in the same company have to be assembled; a vertical one, where the requirements are clearly and possibly formally communicated from a higher level player to a lower level one and where the information about the capabilities and limitations of the IPs are unambiguously communicated from the lower level to the higher level.

The ultimate goal of this activity is to provide the “meta rules” according to which the design transformations are carried out and interfaces are built and hence to provide strong guidance to the clusters to make their results more relevant and applicable. Understanding the roles and dynamics of an existing, well-established, vertical industrial segment is a complex task. We could only imagine the complexity of industrial segments that are coming together in these years. While we do target some industrial domain to be the driver for this activity, we understand that our research is going to be more relevant and better quality if we can distil some common traits of these domains and work with those to choose at a later date which particular chains to address.

The transversal activity hence has two prongs: one is to dive into particular vertical industrial segments and package design methods out of the Thematic Clusters results for the segments; the other is to identify some important common features among verticals and work towards developing methods to address these topics.

We note that the two concerns objects of the Transversal JPRAs (**predictability** and **adaptability**) are common to almost all industrial concerns: For this reason, they provide a framework to start the work on integration driven by industrial applications.

Predictability has been a goal since the beginning of the modern industry: predicting the capabilities of existing components allows to come to market faster with new products and prevents taking dead ends, predicting the effort needed to develop parts of the design and to integrate it correctly prevents early recalls and associated costs. The faster is the dynamics of the industry, the more important is to have predictability in design.

Adaptability is the property of a design to be adapted to changing environments and working conditions. Reconfigurability, programmability, dynamic restructuring are all facets of adaptability. Novel approaches to communication could benefit greatly from adaptability. In fact, much research is being carried out to design devices that could sense available bandwidth and adapt the communication protocol to the most convenient band at the time.

We believe that it will be eventually easier to compose the vertical design industrial flows once these two sub-flows have been examined and results obtained. In addition, being generic concerns they do not require effort from the academic partners to understand the *modus operandi* of entire industrial segments and offer a shorter time to results.

The vertical industrial segment motivated prong will begin by bringing up-to-speed the largest possible number of participants to the logic of the design chain by organizing workshops for discussion with the participants to the chain. In particular, we will target Automotive, Nomadic and Health Applications as potential vertical segments where we have a range of maturity from well-established (automotive) to emerging (health). Given the nature of this work, the main participants in the cluster are the groups that have industrial vocation such as PARADES, ESI, OFFIS, and IMEC.

Technical Description: Joint Research

The activities of the two sub-flows on adaptivity and predictability are detailed in the previous JPRAs. We believe that the work can start at the beginning of the operation of the new NoE as their requirements and approach can be abstracted from what it is known now of the needs of the embedded system community.

This activity will organize two large, open meetings each year, and according to opportunity, one or two smaller ones.

The industry-motivated part necessitates additional care as on one hand, we need to understand the concerns of companies that have been investing substantially in embedded system design such as the ones in automotive and aerospace domains; on the other hand, we need to understand the characteristics of emerging domains such as independent living and health, and nomadic. In both sectors, the links among the different players are not clear as yet when we look at the promises of these markets. Hence we will organize two sets of activities:

- ***Meeting and workshops with automotive and aerospace companies*** to verify their future directions and how our integration activities can help in moving forward. We propose to have a workshop in the first year of life of the project. The participants will be technical leaders in industry and the ArtistDesign partners. Presentations by the partners will be followed by presentations and critique of the industrial technical leaders. We expect to draft a document that will capture the discussion and provide a roadmap for the integration activities as well as guidelines for the Thematic Clusters. We also expect that the interaction with the industrial leaders will be continuous so that the relevance of our work can be continuously monitored. In the second year of operation of the NoE, we propose to revisit the issues and to receive formal feedback from industry again collected in a refinement of the report of the first year. The third year of operation will be devoted to summarizing our results and demonstrate how our activities can help industry to advance their design approaches. The document will be continuously updates as a living paper that will be shared with the Thematic Clusters.
- ***Meeting and workshops with companies interested in Health and Nomadic***. This activity will be certainly more open-ended than the previous one, but it is likely to have an important impact in building the design approach foundations. We propose to organize these meetings as brainstorming sessions where different scenarios will be analyzed with the intent of defining design flows and of providing interested parties with our multi-year experience in embedded system design. We expect that networked embedded systems with wireless technology playing a fundamental role will be the centre of the discussion here. As in the previous case, the workshops will be organized once a year to provide continuity. We expect to publish our work in this

domain in some of the leading conference in embedded systems as it is likely that new approaches will be discovered.

- ***Special sessions in conferences***. We propose to organize special sessions about industrial design flows at major conferences where we can obtain feedback above and beyond the partners of the NoE and the industrial partners we will have been able to enlist as active participants.
- ***Meetings with Thematic Clusters and the sub-flow participants***. We argued that this activity is important to keep the cluster approach cohesive. To do so, we need to check along the way whether indeed the integration activities are coming together in a relevant fashion for the industrial community. This can only be achieved if the thematic clusters participate to internal meetings with the goal of collaborating in driving their activities towards standardized interfaces and models. We believe that a six month cadence is appropriate here.

We are acutely aware of the burden that these activities can bring to the involved partner and will make sure that the minimum amount of overhead is added to the activities of the NoE. We also hope to leverage the Artemis technology platform and the corresponding industrial association, Artemisia, to help in attracting the appropriate technical leaders and in providing access to roadmaps and guidelines they will produce during the year of operation of the NoE.

The results of this analysis will be published in a white paper, widely distributed through the ARTIST Web Portal, in workshops, and journals. These results will also be used to drive integration activities between Thematic Clusters.

1.3.6. Efforts for the Full Duration of the Project

Partic. no.	Partic. Short name	WP0	WP1	WP2	WP3	WP4	WP5	WP6	WP7	Total person months
1	Floralis	**37,50**		**8,50**						**46,00**
2	UJF/VERIMAG	13,50	**14,50**	2,25	17,50				14,75	**62,50**
3	Aachen		8,25	2,50		7,50			2,75	**21,00**
4	Aalborg		9,25	2,75	**11,50**				2,00	**25,50**
5	Aveiro		6,00	3,25			7,00		2,50	**18,75**
6	Bologna		15,25	4,75				13,75	5,25	**39,00**
7	TUBS		9,50	3,00				9,25	2,75	**24,50**
8	Cantabria		10,25	3,25			10,25		2,50	**26,25**
9	CEA		9,00	2,75	6,50			4,50	2,75	**25,50**
10	DTU		7,25	2,25				**9,25**	2,25	**21,00**
11	Dortmund		17,25	5,25		**19,00**			5,25	**46,75**
12	EPFL		9,75	3,00	9,75				2,50	**25,00**
13	ESI		12,75	4,00	6,50				**9,50**	**32,75**
14	ETH Zurich		17,00	5,25				16,00	5,25	**43,50**
15	IMEC		20,25	6,25		7,50	3,50	9,25	5,25	**52,00**
16	INRIA		7,25	2,25	6,50				2,25	**18,25**
17	TUKL		8,25	2,50			10,25		2,50	**23,50**
18	KTH		14,75	4,50	6,50			9,25	4,50	**39,50**
19	Linkoping		9,25	2,75				9,25	2,75	**24,00**
20	ULund		7,25	1,50			3,00		2,50	**14,25**
21	MDH		8,25	2,50		7,50			2,25	**20,50**
22	OFFIS		1,00	1,50	3,00				1,50	**7,00**
23	PARADES		12,75	4,00	6,50				**4,00**	**27,25**
24	Passau		6,00	1,75		7,50			1,75	**17,00**
25	SSSA-Pisa		14,50	4,50			**15,25**		2,75	**37,00**
26	Porto		8,25	2,50			10,25		2,50	**23,50**
27	Saarland		14,25	4,25		15,25			2,50	**36,25**
28	PLU-Salzburg		5,25	1,50	6,50				1,50	**14,75**
29	Uppsala		9,25	2,75	6,50				2,75	**21,25**
30	Vienna		8,25	2,50		7,50			2,50	**20,75**
31	York		21,25	6,50		7,50	13,50		5,25	**54,00**
	Total	**51,00**	**322,00**	**106,75**	**87,25**	**79,25**	**73,00**	**80,50**	**109,00**	**908,75**

1.3.7. List of Milestones and Planning of Reviews

Milestone number	Milestone name	WP(s) Involved?	Expected date[1]	Means of verification
M-Integr-Y2	Integration through key projects	WP1, WP3, WP4, WP5, WP6, WP7	T0+24	See below
M-Integr-Y4	Integration though EU Centres of Excellence	WP1, WP3, WP4, WP5, WP6, WP7	T0+48	
M-Indus-Y1	Industrial Liaison: ARTEMISIA – Y1	WP1, WP3, WP4, WP5, WP6, WP7	T0+12	
M-Indus-Y3	Industrial Liaison: ARTEMISIA – Y3	WP1, WP3, WP4, WP5, WP6, WP7	T0+36	
M-Educ-Y2	Education Y2	WP2, WP3, WP4, WP5, WP6, WP7	T0+24	
M-Educ-Y4	Education Y4	WP2, WP3, WP4, WP5, WP6, WP7	T0+48	
M-Web-Y*n* *n=1,2,3,4*	Web Y1	WP2, WP3, WP4, WP5, WP6, WP7	T0+12, T0+24, T0+36, T0+48	
M-Web-Y*n* *n=1,2,3,4*	International Collaboration Y1	WP2, WP3, WP4, WP5, WP6, WP7	T0+12, T0+24, T0+36, T0+48	

Description of the milestones, and their means of verification:

Our experience gained in the ARTIST2 NoE shows that it is intrinsically difficult to plan specific milestones, given the very wide technical scope and the limited controllability in an NoE. Nonetheless, we count on the common willingness of the participants to move forward by acting in concert to integrate the area. We anticipate the following milestones:

Integration Milestones: These are the main milestones planned, that measure the degree of integration achieved through the NoE's. The vision is to achieve at T0+48 a set of European Centres of Excellence (ECE) in Embedded Systems Design. This concept of ECE can coincide with the ECE promoted by ARTEMIS/ARTEMISIA, or with a type of Center that is more specific to research. This is the milestone: *M-Integr-Y4*.

An intermediate milestone is *M-Integr-Y2*. We are working to realise this, by setting up collaborative research projects on strategic topics, such as component-based design, generic embedded system platforms. This will allow the emergence of clusters of excellence in targeted areas, and the creation of critical mass.

Industrial Liaison Milestones: The ambition for the end of year1 (*M-Indus-Y1*) is to coordinate and/or play a determining role in ARTEMISIA Working Groups on embedded systems design. We will pursue our action in ARTEMISIA, with the objective to integrate the best research teams into the ECE above (*M-Indus-Y3*).

Education and Training Milestones: The goal for the end of the NoE is to coordinate a network of international Master's Programs, managed by the NoE partners (*M-Educ-Y4*).

[1] Measured in months from the project start date (month 1).

Each year starting at the end of Year2, we will publish via the ARTIST Web Portal a Wiki-based reference curriculum, recognised as the de facto standard by the international community (*M-Educ-Y2*).

Web Portal Milestones: ArtistDesign will build on structures and infrastructure created in ARTIST2, and already enjoys international recognition. We will extend the functionalities and services of the Web Portal, as specified in the workplan. Each year, the ArtistDesign Web Portal will gain in visibility and impacts, with respect to the previous year, as measured in number of hits, Google ranking, etc. (*M-Web-Y1234*).

International Collaboration Milestones: ArtistDesign will build on collaboration and international contacts, and existing events. Each year, ArtistDesign will organise a major international event on Embedded Systems Design, such as an International Summer School with distinguished speakers, a high-level event involving world-class speakers and major funding agencies, international workshops on education for embedded systems design. (*M-IntlCollab-Yn where n=1,2,3,4*).

Planning of reviews

Reviews will be held on an annual basis, within 10 weeks of the end of each annual reporting period.

B.2. Implementation

2.1. Management Structure and procedures

2.1.1. General Definitions

The ArtistDesign network is composed of core partners and affiliated partners.

A **Core Partner** is an institution (academic or industrial) whose members are working actively on one or more research activities. The researchers involved in the research activities are accounted for in Form A3 of Part A of this proposal and thus take into account for calculating the grant from the EC. The Consortium Agreement must be signed by all Core Partners before they start working in the NoE.

An **Affiliated Partner** is an institution (academic or industrial) whose members are involved in some activity. The researchers of these institutions are not accounted for in Form A3 of Part A of this proposal and thus not taken into account for calculating the grant from the European Commission. However, they are entitled to receive part of the ArtistDesign budget funding according to the decisions of the Strategic Management Board, to participate in the NoE's activities. The Consortium Agreement must be signed by all affiliated partners before they start working in the NoE.

A **Cluster** is a set of core teams working on an essential topic of the NoE.

Cluster activities include: internal activities (called "Cluster Integration" activities), as well as cross-cutting activities, in collaboration with other clusters (called "NoE Integration" activities).

The **Cluster Leader(s)** is (are) the person(s) responsible for the overall coordination of the cluster's activities.

Cluster Members are researchers from the core partners or affiliated partners working on one or more research activities in a cluster.

A **Workpackage (WP)** is a group of related activities.

2.1.2. Management Structure

We distinguish 3 levels in the management structure, each composed of a set of bodies (see figure below):

- Strategic Management
  The General Assembly, and the Strategic Management Board.
- Operational Management
  The Operational Management Board, the ArtistDesign Office, and the Cluster Leaders (represented by asterisks in the diagram below).

The **ArtistDesign Office** assisted by the **Executive Management Board** (composed of the cluster leaders) ensures the day to day management.

The **Strategic Management Board** leads the scientific policy of the NoE, by deciding the budget allocations for the different activity types. Decisions are taken with a majority vote of 2/3 of the votes of the members

Most decisions requiring a vote will require a simple majority, in which each member will have one vote. Details are in the ArtistDesign Consortium Agreement (CA) – based on the ARTIST2 CA, and is currently being finalized.

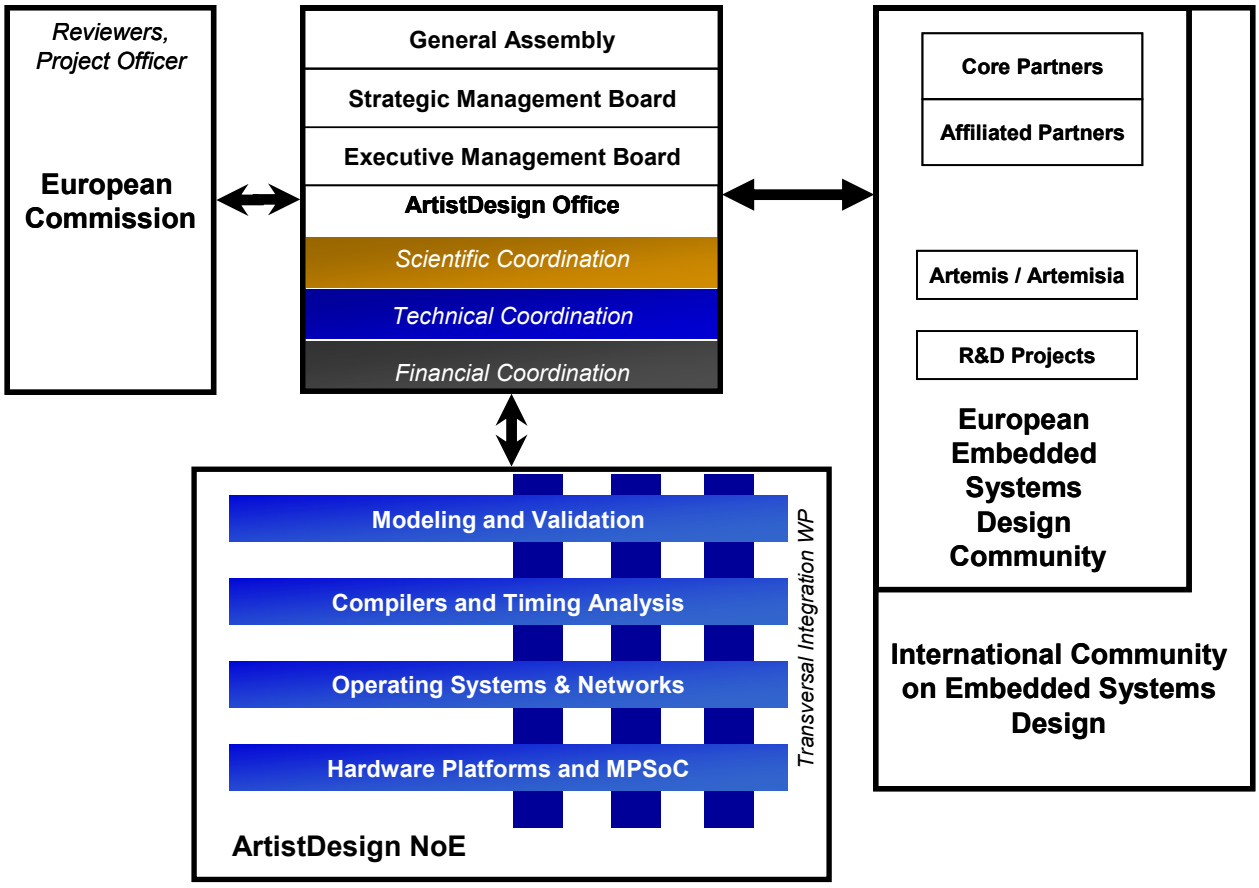
The SMB is composed of representatives from each cluster. It is chaired by the Scientific Coordinator, assisted by the Technical Coordinator. It meets at least once per year – close to the General Assembly meeting. Its members are elected by the General Assembly every two years, according to modalities to be determined in the Consortium Agreement.

In the following sections, we describe roles of each body.

Strategic Management

The **General Assembly** is composed of one representative per core partner. It is convened at the beginning of the project and meets once per year. It is chaired by the Scientific Coordinator. Its role is to:

- Review the yearly report of activities presented by the Scientific Coordinator
- Elect the members of the Strategic Management Board every two years,
- Elect a new Scientific Coordinator at year 3, if required by the Strategic Management Board, in order to ensure a stable future beyond the funding period. For this point on the agenda, it would be chaired by the oldest General Assembly member present.
- Discuss and ratify proposals from the Strategic Management Board for modifying the Consortium, the Consortium Agreement, or any other decision requiring approval and signature by all the core partners.



The Strategic Management Board is composed of representatives from each cluster. It is chaired by the Scientific Coordinator, assisted by the Technical Coordinator. It meets at least once per year – close to the General Assembly meeting. Its members are elected by the General Assembly every two years, according to modalities to be determined in the Consortium Agreement.

The **Strategic Management Board** leads the scientific policy of the NoE, by deciding the budget allocations for the different activity types. The precise procedures will be defined in the Consortium Agreement.

The Strategic Management Board's responsibilities include:

- Updating/extending/modifying the JPA (18 month perspective), such as: setting up activities for spreading excellence; adding/removing/modifying clusters. This can include major changes in the JPA, in response to new problems or situations. These will require consensus or a qualified majority.
- Selection of JPA activities and their associated budget. The selection process and budget decisions are made by the Strategic Management Board.
- Evolution of the consortium: adding or excluding partners.
- Validation of annual reports to the European Commission (except for the financial report).
- Search for funding and evolution towards self-sustainment.
- Continuous monitoring of the NoE's scientific quality, with advice from the International Scientific Council.
- Evaluation of the quality of the deliverables, assisted by the International Scientific Council.
- Transfer of knowledge and of all the activities related to knowledge management.
- Execution of arbitration policies to resolve conflicts of interest.

Certain decisions of the Strategic Management Board, such as bringing in new partners, or ending membership for one or more existing core partners, must be ratified by the General Assembly. The Consortium Agreement will define the procedure for modifying the consortium.

Operational Management

The Operational Bodies are the following:

- The **Executive Management Board** is composed of one representative from each cluster, amongst the Cluster Leaders, and a representative of the Coordinator – who attends, with no voting rights. It is chaired by the Scientific Coordinator, assisted by the Technical Coordinator. It meets on monthly basis – either in person or via phone conference. It implements the decisions of the Strategic Management Board, and supervises the day-to-day management for implementing the JPA
  The **Cluster Leaders** are responsible for the overall coordination of the activities led by their cluster. A cluster functions as a virtual team – with a degree of autonomy for defining its internal meetings and day to day management
  Each cluster has one or more cluster leaders, who meet on a monthly basis in person or via phone conference. They monitor the day-to-day JPRA activities driven by the cluster, and report to the ArtistDesign Operational Management Board as a whole. Cluster leaders are responsible for:

- Satisfactory progress in intra-cluster activities, including: integration between core partners to achieve critical mass at the cluster level; and building and spreading world-class excellence.
- Overseeing the scientific and technical work in the inter-cluster activities driven by their cluster, to ensure the progress of integration and excellence.

- The **ArtistDesign Office** brings together a set of tightly interrelated functions, which are necessary for managing the NoE on an operational basis. It performs the day-to-day management of the NoE. It consists of three strongly collaborating entities: 1) Scientific Coordinator (Joseph Sifakis). 2) Technical Coordinator (Bruno Bouyssounouse), 3) Legal, administrative and Financial Coordinators (Liliane Pereira Bahia and Olivier Guérard).
  - The **Legal, administrative and Financial Coordination** is carried out by the NoE coordinator (Floralis). Its role consists of:
    - Receiving all payments made by the European Commission for the contractors.
    - Dispatching funds, for the various workpackages to the contractors, in accordance with the Consortium Agreement, and the decisions of the Strategic Management Board.
    - Reporting to the European Commission and to the Strategic Management Board, on the consumption of funds.
    - Negotiating the contracts, agreement, and annual amendments, including the Consortium Agreement. Ensures signatures.
    - Checking the work progress against the planned schedule
    - Checking the manpower consumption pursuant to the reports submitted by the contractors
    - Checking that internal audits have been finalized, pursuant to the Contractors' contractual obligations
    - Organising meetings to prepare and finalize reports and submits deliverables and schedules to the European Commission

    Floralis has created a department specialized in the management of European research projects.

  - The **Technical Coordination** is carried out by UJF/VERIMAG (Bruno Bouyssounouse).
    The Technical Coordination ensures, under responsibility of the Scientific Coordinator, the following tasks, including:
    - Checking the work progress against the planned schedule
    - Checks that milestones are met, and deliverables are properly produced, pursuant to the reports submitted to the contractors.
    - Organises meetings to prepare and finalize technical reports and submits deliverables and schedules to the European Commission.
    - Organizes the information flow throughout the consortium (webpages, mailing lists, newsletter)

- The Scientific Coordination is carried out by UJF/VERIMAG (Joseph Sifakis)
  The Scientific Coordinator will be responsible for implementing the scientific policy as it is defined by the Cluster Coordinator's group, and their related decisions. Both the Scientific Coordinator, and the Cluster coordinators are accountable for their actions under a process to be defined
  The Scientific Coordinator reports to the Executive Management Board, and is especially in charge of informing this body of any modifications in manpower, or resource consumption and planning compared to the original contract, so that the Executive Management Board and the ArtistDesign Office take corrective actions in a timely fashion.

Relations with the R&D Community at large

The ArtistDesign Office manages day-to-day relations for the distribution of announcements, coordination of workshops ad conferences, in conjunction with the ArtistDesign Executive and Strategic Management boards.

For relations with ARTEMIS/ARTEMISIA, ArtistDesign will set up the "Artemisia Liaison" task force composed of prominent ArtistDesign members, also active in ARTEMIS/ARTEMISIA: Luca Benini, Ed Brinksma, Werner Damm, Rudy Lauwereins, and Joseph Sifakis,.

Initiatives for setting up new R&D projects and setting up collaborations with industry are initiated within the ArtistDesign Strategic Management Board. It also discusses with International Collaboration partners and elaborates action yearly plans.

The main effect of this activity is in coordinating and implementing the Jointly Executed Programme for Spreading Excellence (JPASE).

2.2. Beneficiaries

This section contains the list of ArtistDesign core partners.

The NoE also has affiliated partners (academic, industrial and SME), described in detail in WP3, who are already committed to working in the NoE.

The approach for building the consortium, including its future possible extensions, is described in Section B.2.3 as “Consortium as a whole”.

2.2.1. Partner 1: Floralis

Organisation

UJF-Filiale (Floralis) was founded in February 2004 and is a subsidiary of the University Joseph Fourier (UJF), the University of Science, Technology and Medicine of Grenoble. Floralis is a private company devoted to acting as an intermediary between academic research and industry, facilitating the steps leading towards technology transfer.

Floralis acts as an interface for companies wishing to establish collaborative relationship with research laboratories. By identifying the appropriate partners and negotiating the technical, financial and economic conditions of an R&D agreement, Floralis is able to streamline and greatly facilitate the technology transfer process.

Main Tasks Attributed

- Administrative Coordination of the NoE

Previous Experience in the Area

Floralis has direct relationships with more than 110 academic research laboratories. It also has privileged access to many networks in the field of technology and innovation and initiates many R&D partnerships with its industrial partners.

Staff Members

Liliane Pereira Bahia

Legal and administrative aspects

Olivier Guérard

Administrative and financial aspects

Viviane Chilton
Projects manager

2.2.2. Partner 2: UJF/VERIMAG

Organisation

Université Joseph Fourier Grenoble 1’s laboratory VERIMAG (UJF/VERIMAG) is one of the main European labs in embedded systems. It develops theory, methods and tools for safety critical and embedded systems. Work directions in the context of embedded systems include modelling of systems as well as verification, testing and simulation methods and tools. Research activities are complemented by development carried out in tight collaboration with industrial partners:

VERIMAG Laboratory has been established in 1993. It is a research lab associated with the CNRS, Université Joseph Fourier, and the INPG Technical University. It has a total staff of 85 persons, including 30 permanent researchers.

Main Tasks Attributed

- Scientific Coordination of the NoE
- Technical Coordination of the NoE
- Cluster “Modelling and Validation”
  Activity “Modelling”
  Our role in this activity will be to investigate different sub-classes of component-based systems in the BIP modelling framework.
  Interaction will mainly be with INRIA, PARADES, EPFL.
- Workpackage “Transversal Integration”
  Activity “Design for Adaptivity”
  Our role in this activity will be to study design techniques for quality management of multimedia applications by controlling quality parameters.

Previous Experience in the Area

UJF/VERIMAG has a long experience in modelling and validation of component-based real-time systems. Its main contributions to the area are:

- Synchronous languages for the development of embedded systems: The LUSTRE language and a dedicated tool set (compilers, program validation tools) have been developed since 1984 and taken over in the SCADE tool commercialised by Esterel-Technologies. This tool has been adopted by major actors in critical embedded systems like Airbus (flight control), Schneider Electric (nuclear plant control), CSEE-Transport (railway signalling).
- Tools and methods for timed and hybrid systems: Timed and hybrid models are extensions of discrete models in order to describe the interaction between a computer and the physical environment in which it operates. Since 1990 UJF/VERIMAG plays a leading role in this area, situated at the border between computer science and control theory.
- The results of UJF/VERIMAG have given rise to transfer and to numerous contractual relations implying Verilog, Schneider Electric (nuclear plants), EADS for the development of safety critical systems in Airbus, Prover-Technology develops a verification tool dedicated to LUSTRE. Other industrial partners of UJF/VERIMAG are Alcatel, CS-Transport, Airbus, EADS, EDF, France Telecom, IBM, Intrasoft, ISD, LETI/CEA, Prover Technology, RATP, Schneider Electric, Silicomp, ST Microelectronics, and Trusted Logic.

UJF/VERIMAG has been and is currently involved in many European projects: LTR VIRES (Verification of Real time systems, 98-00), IST Crisys (98-00), IST Interval (00-02), IST SafeAir I & II (Advanced Design Tools for Aircraft Systems and Airborne Software, 00-02) and Agedis (00-04). IST Next-TTA (01-03), IST-RISE, IST-AMETIST, ASSERT, and SPEEDS. UJF/VERIMAG coordinated the IST projects OMEGA (Correct Development of Real-Time Embedded Systems, 02–04) and CC.

UJF/VERIMAG coordinates the IST-004527 ARTIST2 NoE on Embedded Systems (http://www.artist-embedded.org/), which started September 1st 2004 and has a duration of 48 months. The NoE includes 35 partners representing the top research teams in embedded systems design.

Bruno Bouyssounouse has been the Technical Coordinator for both the ARTIST FP5 Accompanying Measure, and the ARTIST2 Network of Excellence.

Staff Members

Dr. Susanne Graf

Modelling and validation tools.

Dr Joseph Sifakis
Component-based modelling – theory and tools.

Dr. Paul Caspi

Synchronous languages – theory and implementation.

Pr. Florence Maraninchi

Synchronous languages and applications to system modelling.

Bruno Bouyssounouse (consultant in house)

Technical coordinator

2.2.3. Partner 3: Aachen

Organisation

Rheinisch-Westfaelische Technische Hochschule Aachen (Aachen) is an internationally top-ranked technical university and a member of the IDEA league. Its Institute for Integrated Signal Processing Systems (ISS), being part of the Department of Electrical and Computer Engineering, is headed by Prof. R. Leupers, Prof. G. Ascheid, and Prof. H. Meyr. ISS performs research and development in different areas of embedded system design technology, especially covering algorithms, architectures, and tools for wireless communication systems. ISS has comprehensive experience and technology in design tools for embedded processors and MPSoC, which its project contributions will be based upon. ISS also has a persistent success track in technology transfer to industry, with its spin-off company LISATek Inc (acquired by CoWare in 2003) being a most recent example.

Main Tasks Attributed

- Cluster “Software Synthesis, Code Generation and Timing Analysis”
  Activity “Software Synthesis and Code Generation for Embedded Systems”
  Our role in this activity will be to work on compiler platforms, adaptive compilation, and MPSoC compilation
  Interaction will mainly be with Dortmund, IMEC, Passau, ACE.

Previous Experience in the Area

Aachen has been involved in numerous compiler R&D projects, e.g. LANCE (www.lancecompiler.com), CoWare Compiler Designer (www.coware.com), as well as research projects funded by the German Science Foundation (DFG) and the EU (e.g. HiPEAC and SHAPES). Aachen has also carried out industry-funded compiler R&D with ACE and has been heading the compiler cluster in the ARTIST2 project.

Staff Members

Prof. Dr. Rainer Leupers	*team leader.*
Dipl.-Ing. Felix Engel	*compiler platform coordination*
M.Sc. Jianjiang Ceng	*MPSoC compilation*
M.Sc. Kingshuk Karuri	*compilation for ASIPs.*

2.2.4. Partner 4: Aalborg

CISS

Organisation

CISS (Center for Embedded Software Systems, www.ciss.dk) is a research competence centre founded in 2002 by Aalborg Universitet (Aalborg), the Region of Northern Denmark, the Danish Government and a number of companies. The mission is: 'To contribute with decisive importance to the innovation process of the collaborating companies within the area of embedded systems software through joint projects and advanced research'. Apart from a large number of industrial projects (approx. 40), knowledge dissemination is carried out through work-based learning, seminars and moderation of company networks with a special focus on subjects like development methods, testing, mobile technologies, etc. Approx. 35 researchers (15 PhD students) are associated with CISS. A key competence is algorithms and tools for automated analysis of real-time systems, and a fundamental result is the real-time model checker Uppaal – jointly developed with Uppsala.

Main Tasks Attributed

- Cluster "Modeling and Validation", Activity "Modeling"
  Our role in this activity will be to work on integrated, multi-disciplinary modelling Interaction will mainly be with ESI, OFFIS, PARADES and UJF/VERIMAG to obtain industrially applicable modelling methods.
- Cluster "Modeling and Validation", Activity "Validation"
  Our role in this activity will be to act as cluster leader and to work on model-based test methods. Interaction will mainly be with ESI, OFFIS, PARADES and UJF/VERIMAG to obtain scalable model-based test methods.
- WP on Transversal Integration, Activity "Integration Driven by Industrial Applications"
  Our role in this activity will be to identify important design issues that cut across the existing Thematic Cluster topics.

Previous Experience in the Area

CISS have built up substantial and highly relevant experience through numerous past and current national (e.g. MoDES, www.cs.aau.dk/modes and BRICS, www.brics.dk) and European research projects (e.g. AMETIST, VHS).

Staff Members

Prof. dr Kim G. Larsen (scientific director, full professor): *model-based design &verification, real-time testing, industrial application*

Prof. dr. Anders P. Ravn (full professor): *UML-based modelling, model-driven engineering, hybrid systems, industrial application*

Dr Brian Nielsen (associate professor): *real-time testing*, *industrial application, model-based design &verification*

Dr Arne Skou (associate professor): *real-time testing*, *industrial application, model-driven engineering, UML-based modelling*

2.2.5. Partner 5: Aveiro

Organisation

The participation of Universidade de Aveiro (Aveiro) in this project will be carried out through the Electronic Systems Laboratory at the IEETA research unit. The mission of the Electronic Systems Lab is to contribute to the development of more predictable, reliable and efficient embedded systems by developing appropriate input/output, computing and communication infrastructures. One of its main research lines concerns the development and analysis of communication protocols that support timeliness, dependability, flexibility and scalability in an efficient way, over different media, including wireless.

Main Tasks Attributed

- Cluster “Operating Systems and Networks”
  Activity “Embedded Real-Time Networking” (activity leader)
  Our role will be to develop protocols, analysis and tools for distributed adaptivity.
  Interaction will mainly be with SSSA-Pisa on mobile wireless sensor networks, with Cantabria on networking support for contract-based middleware, and with affiliates
- Cluster “Operating Systems and Networks”
  Activity “Scheduling and Resource Management”
  Our role will be to develop models and analysis for reconfigurable systems.
  Interaction will mainly be with SSSA-Pisa on dynamic reconfiguration in mobile wireless communication, and with several affiliates.

Previous Experience in the Area

We believe that more and more embedded systems will be distributed and, for efficiency reasons, will require higher levels of integration and flexibility. This calls for an appropriate networking infrastructure that supports on-line adaptation in a predictable and safe way. In the last few years, our research activity has consistently covered this issue leading to several achievements that were internationally recognized by peers. The Flexible Time-Triggered communication framework and its associated protocols is one such broad achievement as well as the analysis methods and tools related to that framework, covering dynamic QoS management, fault-tolerance of/in adaptive networks and holistic design.

Staff Members

Luis Almeida
Real-time network protocols, real-time scheduling, dynamic reconfiguration

Paulo Pedreiras
Real-time network protocols and operating systems and dynamic QoS management

José A. Fonseca
Embedded network protocols and wireless communication

Alexandre Mota
Non-linear control and systems identification

2.2.6. Partner 6: Bologna

Organisation

Universita di Bologna (Bologna), created in 1088, is recognized as the oldest university in the western world, and one of the largest in Italy (with more than 100,000 enrolled students). It is one of most active Italian universities in research and technology transfer. At European level, the University is partner in more than 150 European projects in FP5 and FP6.

The UNIBO research group participating in the network belong to the Department of Electronics, Computer Science and Systems (DEIS) DEIS is a research-led institute employing about 70 professors, 40 research associates, 90 doctorate students, 40 graduated research assistants, and several visiting researchers. The Department expertise spans the whole range of electronics, communications, computer science and biomedical engineering. The DEIS research groups Micrel Lab (http://www-micrel.deis.unibo.it/)

The research activity of on focuses on the design and deployment of embedded and mobile systems, with special emphasis on energy-efficient multi-core platforms. The group is also active in the hardware/software design and implementation of wireless sensor networks and their integration in vertical applications. The group has been involved in several EU-funded research projects (EU IST-SensactionAAL, AIST-ARTIST, IST-ARTIST2, ESPRIT-TTN Hipcom, National PRIN 2005, regional projects LAICA and SUMMIT) and a number of industrial cooperations (STMicroelectronics, Hewlett-Packard, FreeScale Semiconductors and others).

Main Tasks Attributed

- Cluster “Hardware Platforms and MPSoC Design”
  Activity “Platforms and MPSoC Design”
  Our role in this activity will be that of activity leader. From the technical viewpoint, the focus will be on designing a resource management layer that would facilitate run-time adaptation without compromising efficiency and scalability.
  Interaction will mainly be with all the partners participating in the activity, both for coordination and for technical interaction. The end goal is to develop a coherent view on how to design and manage complex multi-core hardware platforms in a highly dynamic application environment...

- Cluster “Hardware Platforms and MPSoC Design”
  Activity “Platforms and MPSoC Analysis”
  Our role in this activity will be to develop modelling abstractions for non functional properties, with special emphasis with power and reliability
  Interaction will mainly be with ETH Zurich on modelling power consumption of distributed platforms for wireless sensors, and with the other partners participating to the cluster on power and reliability modelling of MPSoC platforms. The main goal in this activity is to develop a holistic analysis framework that takes into account not only functional properties, but provides information also on non-functional properties and constraints.

- Transversal Integration Activity: “Design for Adaptivity”
  Our role in this activity will be to investigate techniques for run-time dynamic power management. The idea is to enhance the adaptivity of HW platforms in reaction of continuous changes in workload and environmental conditions. The goal is to enhance the energy efficiency without compromising quality of service in real-time constrained application contexts.

- Transversal Interaction Activity: “Design for Predictability”
  Our role in this activity will be to develop modelling abstractions rooted on physical mechanisms for the reliability losses in current HW platforms, and to propose techniques for enhancing the robustness of the platforms using a moderate amount of hardware and

software redundancy and protection techniques. The main challenge is to provide ensure predictable operation even with unreliable underlying fabrics at a reduced overhead in terms of cost and power consumption.

Previous Experience in the Area

Bologna has multi-year experience on modelling and designing hardware platforms for embedded applications. It has been involved in a number of projects on power optimization and reliability enhancement, and it has pioneered the concepts of dynamic power management for electronic systems and of scalable on-chip communication fabrics (NoCs). In these two areas, the group's coordinator, Professor Luca Benini, has published two well-known textbooks (Dynamic Power management – design techniques and CAD tools 1998, edited by Kluwer and Networks on chips; technology and tools 2006, edited by Morgan Kaufman) and a large number of papers in peer reviewed journals and conferences.

Staff Members

Title(s) Prof Luca Benini
Coordinator. *He will be leading the Bologna activities and will be a member of the ArtistDesign Strategic Management Board of the NoE.*

Title(s) Prof. Michela Milano
She will focus on design techniques for optimal mapping of applications on MPSoC platforms, with special emphasis of complete off-line mapping techniques.

Title(s) Prof. Eugenio Faldella
He will focus on design techniques for dynamic management of computational resources and storage on MPSoC platforms,

2.2.7. Partner 7: TUBS

Institute of Computer and Communication Network Engineering (IDA)

Organisation

The Institute of Computer and Communication Network Engineering (IDA) is a public research institute attached to the Technische Universitaet Braunschweig (TUBS). The institute employs approximately 35 researchers.

The main research focus of IDA includes embedded system design automation (in particular real-time systems), parallel systems, communication networks, and space born data processing units.

Main Tasks Attributed

- Cluster "Hardware Platforms and MPSoC Design"; Activity "Platform and MPSoC Design" - The role of TUBS in this activity is the development of online algorithms that continuously control the real-time properties and efficiency of an evolving system on chip.
- Cluster "Hardware Platforms and MPSoC Design"; Activity "Platform and MPSoC Analysis" - The role of TUBS in this activity includes platform performance modelling as well as system robustness evaluation and optimization.

Previous Experience in the Area

The research group is internationally known as one of the pioneers in embedded system design automation. Starting in 91 with work on HW-SW co-design with more than listed 500 references to a single paper, the work extended to embedded system architectures, system analysis and

optimization. It ranges from high-performance reconfigurable architectures for highest resolution electronic film applications to network processors to automotive and space applications. In the past 6 years, there was a major emphasis at IDA on timing analysis and optimization for networked systems leading to a recent spin-off, Symtavision. The research results allow to precisely analyze sophisticated timing data, such as end-to-end timing bounds, jitter, or lost packets in a realistic automotive networks using CAN, FlexRay, including gateways, and ECUs and real automotive software stacks with AUTOSAR and OSEK standards. From these and other previous projects, IDA has extended experience and in-depth knowledge of tool technology and methodologies. Some of the current projects in this domain are Morpheus (IST-4-027342, http://www.morpheus-ist.org/), FlexFilm (German BmBF, www.flexfilm.org) SuReal (German BmBF, http://www.sureal-projekt.org/), EPOC (Organic Computing http://www.organic-computing.de/spp) and numerous projects of the German DFG.

Staff Members

Dipl.-Ing. Steffen Stein: Development of online algorithms that continuously control timing properties.

Dipl.-Ing. Simon Schliecker: Semantic extensions to platform model, MPSoC (shared) memory access analysis

Dipl.-Inform. Arne Hamann: Development of design robustness metrics and optimization techniques

Prof. Dr. Rolf Ernst: Involved in all above activities

2.2.8. Partner 8: Cantabria

Organisation

Universidad de Cantabria (Cantabria) is a public Spanish university created in 1972, with 12000 students and over 1250 research and teaching staff.

Main Tasks Attributed

- Cluster “Resource-Aware Operating Systems and Networks”
  Activity “Real-Time Operating Systems”
  Our role in this activity will be to specify the services of the underlying real-time kernels required by the FRESCOR framework for flexible resource, and cooperate with the other partners in the implementation of these services on different kernels.
  Activity “Scheduling and Resource Management”
  Our role in this activity will be to provide and adapt the FRESCOR framework for flexible resource management to implement the scheduling and resource management techniques developed by other partners.
  Activity “Real-Time Networks”
  Our role in this activity will be to provide and adapt the FRESCOR framework for flexible resource management to implement the real-time protocols and distributed services developed by other partners.

- Cluster “Hardware Platforms and MPSoC”
  Activity “Platform and MPSoC Analysis”
  Our role in this activity will be the improvement of the heterogeneous system specification methodology in its design refinement capabilities (vertical heterogeneity), and the extension of the PERFidiX tool for complex MPSoC with NoC.

Previous Experience in the Area

The Group of Computers and Real-Time Systems in Cantabria is the coordinator of the FRESCOR EU project, in which a framework for flexible resource management of real-time embedded systems based on contracts is being developed. Within ArtistDesign, this framework can be adapted and used as an integrated platform that can make use of all the developments in the cluster, linking the OS, the resource management techniques, and the real-time networks. Cantabria has also participated in the FIRST EU project, where a prototype resource management framework was developed, and in the ARTIST and ARTIST2 NoE's, as well as in many other national and industrial research projects. Group's web page: http://www.ctr.unican.es

Cantabria is also active in ITEA (MERCED, Spices and MARTES projects), Medea (ToolIP and LoMoSa) and IST FPVI (Andres). The research activities in these projects have been modelling of the HW-dependent SW (HdS) in MPSoC with NoC, SystemC modelling of AADL and UML specs and specification and design of reconfigurable systems.

Staff Members

Michael González Harbour: *Flexible resource management, RTOS, real-time distr. systems*

José María Drake Moyano: *Real-time design methods, real-time components*

José Javier Gutiérrez García: *Real-time distribution middleware, real-time networks*

José Carlos Palencia Gutiérrez: *Real-time schedulability analysis techniques*

Mario Aldea Rivas: *Real-Time kernels, application-defined scheduling*

Prof. Eugenio Villar: *Heterogeneous system specification. PERFidiX tool for MPSoC w NoC.*

2.2.9. Partner 9: CEA

LIST Laboratory

Organisation

Created in 1945, Commissariat à l'Energie Atomique (CEA) is a large French public research institution with around 15,000 employees. CEA has a long experience in driving large technological research projects in multidisciplinary fields such as nuclear power, alternative energy technology, new materials for industry, information technology, biotechnology and healthcare, microelectronics, micro and nanotechnologies and systems. CEA manages also fundamental research in physics and chemistry in an international context to support technological developments.

The DRT division of CEA (Technological Research Directory) helps companies to increase their competitiveness by fostering technological innovation and transfer to industry, in sectors including nuclear power & energy, defence, information technology (HW & SW), automotive, telecommunications, aerospace, computer peripherals. "**CEA LIST**", located south of Paris, is the software and systems division of CEA/DRT.

Contributions of CEA to ArtistDesign will involve experts from two different temps: the LLSP group and the embedded computing group.

Within CEA LIST, the LLSP ("Software for process safety group") conducts studies on Design method, Architecture, Safety and Performance of Digital Systems. It gained a solid expertise on complementary and essential facets: (i) safety oriented design method, modular architectures and implementation technologies for the development of distributed, real time and embedded systems; (ii) formal analysis and verification of models and specification and automatic generation of test sequences; (iii) model driven engineering of distributed systems. Expertise of the LLSP in these domains has lead to its active participation to several projects and industrial collaborations

Within CEA LIST, the “embedded computing group” is about thirty full-time researchers and has been doing research on architecture for embedded systems for about 15 years, focusing on high performance parallel computing platforms, with vision systems as primary "historical" target. Since two years, MPSOC has become the driver of CEA LIST architecture research in the objective of studying generic / multi-application computing platforms with a system-wide approach. Areas of expertise in that domain cover intercommunion issues, reconfigurable IPs for optimized implementation of classes of algorithms, on-line testing and diagnosis, and reliability & fault tolerance at the architecture level. The embedded computing group in CEA LIST contributes to several multi-processor projects in the System@tic Paris “competitivity cluster” and is the coordinator of the FP6 IST FET AETHER project on future technologies for pervasive embedded computing platforms.

Main Tasks Attributed

- **Cluster “Modeling and Validation”**
  Activity “Modeling”
  Our role in this activity will be to contribute research and experience on model-based development of embedded systems, control systems and distributed systems, as well as expertise in model-based systems engineering.
  Interaction will mainly be with KTH, Volvo technologies and Turku Centre for Computer Science.
- **Cluster “ Hardware Platforms and MPSoC”**
  Activity “Platform and MPSoC Design”
  Our role in this activity will be to provide a formal framework to specify heterogeneous system by defining structuring mechanisms of MoCCs. Concerning compositional validation, CEA will define a framework for symbolic execution of models of heterogeneous systems as a basis for testing or model checking activities. The definition of a compositional methodology for testing will also be addressed.
  Interaction with Bologna, DTU and KTH

Previous Experience in the Area

The LLSP laboratory (“Logiciels pour la sureté des procédés”) within CEA LIST was already core member of the Artsist2 NoE and is also involved in a lot of national and European projects related to the topics related to the cluster “Modeling and Validation”: www.atesst.org, http://www.ara-reve.org, http://www.carroll-research.org, http://www.memvatex.org, http://niven.disam.etsii.upm.es/public/projects/COMPARE/, etc.

LLSP is also strongly involved in normalization organisms (specially the OMG). In this context, Sébastien Gérard is the chairman of the Promarte consortium (www.promarte.org) which has defined the new OMG standard for modelling and validation of real-time and embedded systems, the UML profile for MARTE.

The Embedded Computing group of CEA LIST is strongly involved in design of embedded reliable embedded solutions based on reconfigurable and multicore architectures. This group leads the AETHER project (Future Emerging Technologies project of the FP6), participates to MOPHEUS project (FP6), and is a key actor of the Ter@ops project (National project in the “pole de compétitivité” system@tic).

Staff Members

PhD Sébastien Gérard - LLSP
He will bring his experience and expertise on MDD and component-based development for real-time system design and validation.

Pr. Francois Terrier - LLSP
He will bring his experience and expertise on MDD for real-time system design and validation

PhD Christophe Gaston
He will bring his experience related to formal methods for testing, simulation and heterogeneity treatment.

Raphael DAVID, CEA LIST
He will bring his experience and expertise on reconfigurable multicore architecture development

Nicolas VENTROUX, CEA LIST
He will bring his experience and expertise on development of embedded scheduler for MPSoC architectures

Thierry Collette, CEA LIST
He will bring his experience and expertise on multicore and reconfigurable architecture.

2.2.10.Partner 10: DTU

Embedded Systems Engineering Lab (ESELAB)

Organisation

The Embedded Systems Engineering Lab (ESELAB) is a research laboratory at the Informatics and Mathematical Modelling (IMM) department, Danmarks Tekniske Universitet (DTU). ESELAB is covering a broad class of topics in the area of embedded systems, such as real-time systems, fault-tolerant systems, hardware/software co-design, architecture and execution platforms, and a variety of models, techniques and tools used in connection with such systems.

The Department of Informatics and Mathematical Modelling (IMM) at the Danmarks Tekniske Universitet (DTU) has a unique environment with two divisions comprising both computer science and applied mathematics. IMM research projects range from basic to applied research; most projects have industrial partners, or are carried out in collaboration with other research institutions and organizations. IMM has a very active graduate student environment with more than 50 PhD-students. The newly established ITMAN graduate school offers research training involving all groups at IMM.

The division Computer Science and Engineering (CSE) covers hardware as well as software. In particular, the division covers research in the areas: System-on-Chip comprising Platform Architectures (including low-power IP cores, Network-on-Chip and reconfigurability), and System-Level modelling, analysis and design (including application, operating system and co-design); Safe and Secure IT-Systems comprising Network Technology (including privacy and intrusion detection), and Language-Based Technology (including static program analysis, operational semantics, process calculi and software validation); Software Engineering comprising object-oriented design (including development tools), and formal specification languages (including functional, algebraic and logical descriptions).

Main Tasks Attributed

- Cluster “Hardware Platforms and MPSoC Design”
  Activity “Platform and MPSoC Design”
  Our role in this activity will be to develop program models which allow the application developer to work with adaptability and reliability and refinement from application model to platform implementation, including application mapping, optimizing for reliability, in addition to energy, cost and timing.
  Interaction will mainly be with Linkoping on reliability optimization for efficient safety-critical systems, Linkoping and TUBS on design time mapping for design space exploration and IMEC on dynamic resource management for increased adaptability.
- Cluster “Hardware Platforms and MPSoC Design”
  Activity “Platform and MPSoC Analysis”

Our role in this activity will be to develop analytical methods for reliability, performance and adaptability analysis of execution platforms.
Interaction will mainly be with TUBS on abstract models that cover complex realistic hardware and software architectures aiming at derive guidelines and examples for predictable platforms, Bologna and Linkoping on simulation-based and analytic analysis methods related to system timing, reliability and energy.

Previous Experience in the Area

The faculty members of ESE have been involved in many research projects in the recent years, sponsored by The Danish Research Agency as well as the EU. Most relevant for the proposed project are: MoDES (Model Driven Development of Intelligent Embedded Systems, eselab.imm.dtu.dk/MoDES) funded by The Danish Agency for Science, Technology and Innovation (The Danish Council for Strategic Research); DaNES (Danish Network for Intelligent Embedded Systems, eselab.imm.dtu.dk/DaNES) funded by The Danish National Advanced Technology Foundation; HOGTHROB (hogthrob.dk), a wireless sensor network for sow monitoring, funded by The Danish Council for Strategic Research ; ARTIST2, a Network of Excellence for Embedded Systems Design funded by EU IST.

Through these projects, ESELAB provides a broad forum covering industrial cases, formal models, models of execution platforms, development methods and advanced verification tools for embedded, real-time systems.

Staff Members

Professor Jan Madsen *Modeling and simulation of MPSoC-based platforms; system-level design space exploration for performance and energy optimization for embedded systems.*

Associate Professor Michael Reichardt Hansen *Formal modelling and model checking for embedded systems.*

Associate Professor Paul Pop *Timing analysis and design optimization of distributed real-time embedded systems; reliability analysis and optimization of safety-critical embedded systems.*

2.2.11.Partner 11: Dortmund

Organisation

The computer science department of Universitaet Dortmund (Dortmund) is one of the largest CS departments in Germany, with an enrolment of around 2,800 students. The embedded systems group within the computer science department was established in 1989, when its current chair moved to Dortmund.

Main Tasks Attributed

- Cluster “Software Synthesis, Code Generation and Timing Analysis”
  Activity “Software Synthesis, Code and Generation”
  Our role in this activity will be to lead this activity and to provide results on compilation for MPSoCs stimulated by the interaction with the other 3 core teams of this activity.
- Cluster “Transversal Integration”
  Activity “Design for Predictability, Design for Adaptivity”
  In this activity we will cover compilation aspects of predictability.
  Interaction will mainly be with other partners working on predictability. Our emphasis will be on compilation issues resulting from the processor/memory speed gap.

Previous Experience in the Area

The goal of the group is to propose new design methodologies and tools for the design of microelectronic systems. Initially, the focus was on architectural synthesis (an area partially created by the team members). The focus later shifted toward design automation of embedded systems with a focus on compilers for embedded processors. The group worked on resource-aware, energy-aware and worst-case execution time aware compilation for embedded processors (see http://ls12-www.cs.uni-dortmund.de/publications/_global_index. html). Transfer of results to industry is facilitated through ICD e.V. (see www.icd.de), a technology transfer centre headed by Peter Marwedel.

The group led the CHIPS project funded by the EC. The CHIPS project was one of the first projects demonstrating the need for specialized compilers for embedded systems. The creation of the now well-known company Target Compiler B.V. (see www.retarget.com) and the SCOPES series of workshops (see www.scopesconf.org) can be attributed to the project. In addition to nationally funded projects, the group is working on the MORE and ARTIST2 projects funded by the EC.

Staff Members

Prof. Dr. Peter Marwedel
Co-Chair of the cluster on Software Synthesis, Code Generation and Timing Analysis; Chair of the Embedded Systems Group at Dortmund. Responsible leader for all ArtistDesign activities at Dortmund.

Dr. Heiko Falk
Leading research on transversal integration.

Prof. Dr. Olaf Spinczyk
Provides local expertise on embedded operating systems.

2.2.12.Partner 12: EPFL

Organization

Ecole Polytechnique Fédérale de Lausanne (EPFL) is one of the two Federal Technical Universities in Switzerland, located in Lausanne.

Main Tasks Attributed

- Cluster "Modeling and validation"
  Activity "Modeling"
  Our role in this activity will be to provide and understand theories for component, resource, and quantitative modelling. Interaction will mainly be with UJF/VERIMAG and PARADES on component modelling, with INRIA on reliability analysis, and with PLU-Salzburg on time-triggered languages.
- Cluster "Modeling and validation"
  Activity "Verification"
  Our role in this activity will be to provide and analyze algorithms for component, resource, and quantitative verification. Interaction will mainly be with CFV and Oxford on quantitative verification.

Previous Experience in the Area

Tom Henzinger has developed several formalisms for component modelling and corresponding verification algorithms, including Hybrid Automata and the verification tool HyTech for hybrid systems; Reactive Modules and the verification tool Mocha for component-based systems;

Interface Automata and the verification tool Chic for component interfaces; and the coordination language Giotto for hard real-time systems.

Laurent Doyen has developed novel methods for the verification and implementation of timed and hybrid systems, and for controller synthesis.

Staff Members

Tom Henzinger (Professor)
Leader of the Modeling Activity in the cluster on Modeling and Verification.

Laurent Doyen (Postdoctoral Researcher)
Research on component modelling, reliability analysis, and quantitative verification.

2.2.13.Partner 12: ESI

Organisation

The Embedded Systems Institute (ESI) is a research organisation founded in 2002 by the three Dutch technological universities and a number of companies: Delft University of Technology, Eindhoven University of Technology, University of Twente, TNO, ASML, Océ and Philips. Its mission is: 'To advance industrial innovation and academic excellence in embedded systems engineering'. It carries out a broad research programme (2007: appr. 125 fte), mostly based on cases from industrial practice. The research is carried out in collaboration with many academic and industrial partners, as well as other research institutes. ESI also maintains an extensive knowledge dissemination programme. Being network institute, ESI also acts as an interface to its industrial and academic partners, who carry out almost all of the embedded systems research in the Netherlands.

Main Tasks Attributed

- Cluster "Modeling and Validation", Activity "Modeling"
  Our role in this activity will be to work on integrated, multi-disciplinary modelling
  Interaction will mainly be with Aalborg, OFFIS, PARADES and UJF/VERIMAG to obtain industrially applicable modelling methods.
- Cluster "Modeling and Validation", Activity "Validation"
  Our role in this activity will be to work on model-based test methods
  Interaction will mainly be with Aalborg, OFFIS, PARADES and UJF/VERIMAG to obtain scalable model-based test methods.
- WP on Transversal Integration, Activity "Integration Driven by Industrial Applications"
  Our role in this activity will be to identify important design issues that cut across the existing Thematic Cluster topics.

Previous Experience in the Area

ESI and its constituent partners have built up substantial and highly relevant experience through numerous past and current national (e.g. Boderc, Tangram, Trader, Ideals, Stress, see www.esi.nl under projects) and European research projects (e.g. AMETIST , OMEGA).

Staff Members

Prof. dr Ed Brinksma (ESI, scientific director, full professor):
model-based design &verification, real-time testing, hybrid systems, industrial application

Dr Jozef Hooman (ESI, senior research fellow)
theorem proving, model checking, UML-based modelling, industrial application

Dr ir Jan Tretmans (ESI, senior research fellow)
model-based testing, software verification, industrial application

Dr ir Jeroen Voeten (ESI, senior research fellow)
model-driven engineering and performance modelling, industrial application

2.2.14.Partner 14: ETH Zurich

Organisation

Eidgenoessische Technische Hochschule Zuerich (ETH Zurich) is an institution of the Swiss Confederation dedicated to higher learning and research. Together with the ETH Lausanne and four research institutes, it forms the federally directed, and to a major degree financed, ETH domain. The institutions of the ETH domain uphold their autonomy and identity on the basis of the ETH Federal Law and in the full awareness of their social, economic and cultural responsibility to the nation and its citizens.

Main Tasks Attributed

- Cluster “Transversal Integration” - Activity “Design for Predictability and Performance”
  Our role in this activity will be analytic methods to analyze the performance properties and memory requirements of distributed systems. Adding run-time adaptivity to systems while using efficient run-time estimation methods combined with distributed finite horizon control methods. Interaction will mainly be based on the following activities: Modeling of resources, and multiple-objective optimization (ETH Zurich, IMEC), Architectures for timing-predictable systems (ETH Zurich, Saarlandes, Vienna), Component-based design for predictable and efficient systems (ETH Zurich).
- Cluster “Transversal Integration” - Activity “Design for Adaptivity”
  Our role in this activity will be on using control techniques, e.g., MPC, to adapt schedules and task allocation to changes in requirements, system state, and estimations. Application domains are power and energy management, and timing properties. Extension to hierarchical and distributed systems Interaction will mainly be with Bologna (Luca Benini) to link power and energy estimations with new adaptive control techniques.
- Cluster “Execution Platform and MPSoC” - Activity “Analysis”
  Our role in this activity will be on component-based analytic methods to analyze the performance properties and memory requirements of distributed embedded systems.
  Interaction will mainly be with Bologna (Luca Benini) and IMEC in terms of integrating methods for performance analysis and to develop on-line estimation methods.
- Cluster “Execution Platform and MPSoC” - Activity “Design”
  Our role in this activity will be on adding run-time adaptivity to systems while using efficient run-time estimation methods combined with distributed finite horizon control methods.
  Interaction will mainly be with Bologna and KTH on programming models and dynamic resource management and adaptation based on predictive control resource optimization and predictability.

Previous Experience in the Area

The Computer Engineering and Networks Laboratory at Swiss Federal Institute of Technology has about 60 PhD students and is lead by Prof. Lothar Thiele. Other faculty members are Prof. Eckart Zitzler, Prof. Bernhard Plattner and Prof. Roger Wattenhofer. The involved researchers in the ARTIST project have experience in the following areas:

Multi-objective Optimization: The research group is a centre of excellence in multi-objective optimization. Results as well relate to the underlying theory as to providing algorithms and software which is currently used by many research groups worldwide.

Performance Estimation: The group has been developing analytic methods based on max-+ algebra to analyze combined computation and communication systems. The method leads to a modular approach to performance analysis of distributed hardware-software systems.

Stream-based Processing: The research group has outstanding expertise in modelling and analyzing flows of packets in communication and computation systems. Currently, the research group is involved in the European network of Excellence ARTIST2 (leading the activities in the area of execution platforms for real-time applications) and the European IP project SHAPES (leading the software related activities of mapping parallel applications to a tiled processor array).

Staff Members

Prof. Lothar Thiele
Performance Analysis, Embedded System Design, Sensor Networks

Dr. Iuliana Bacivarov
Simulation Methods, MPSoC Analysis and Design

2.2.15.Partner 15: IMEC

Organisation

Interuniversitair Micro-Electronica Centrum VZW (IMEC) was founded in 1984 by the Flemish Government and is headquartered in Leuven, Belgium. Currently, it is Europe's leading independent research centre for the development and licensing of microelectronics and Information and Communication Technologies (ICT).

Main Tasks Attributed

- Cluster "Hardware Platforms and MPSoC'" - Activity "MPSoC design"
  Our role in this activity will be to introduce novel run-time resource management for MPSoC, which exploit metadata from the Software and Hardware. Interaction will mainly be with Uni. Bologna and ETH Zurich, on run-time resource management and APIs, to obtain energy and performance optimizations.
- Cluster "Software Synthesis, Code Generation and Timing Analysis" - Activity "Compiler"
  Our role in this activity will be to introduce novel source code parallelization and memory source-to-source optimizations for MPSoC platforms
  Interaction will mainly be with Uni. Dortmund, on MPSoC parallelization and memory mapping, to obtain efficient and predictable memory mappings.

Previous Experience in the Area

IMEC is internationally recognized as a centre of excellence, which is illustrated by the large number of scientific papers that are yearly published, the numerous patent applications that have been submitted and the several spin-off companies that have been set up. It has an annual budget of more than 100 million Euros and employs more than 1000 people. IMEC performs scientific research that runs 3 to 10 years ahead of industrial needs. The research activities concentrate on design of integrated information and communication systems; silicon process technology; silicon technology and device integration; micro-systems, components and packaging; and advanced training in microelectronics.

Staff Members

Prof. Rudy Lauwereins *will act as an Artemisia Liaison and will lead the overall contribution of IMEC.*

Dr. Stylianos Mamagkakis *will be responsible for the contribution to the 'Hardware Platforms and MPSoC', the 'Resource-aware Operating Systems and Networks' and the 'Design for Adaptivity' clusters*

Dr. Arnout Vandecappelle *will be responsible for the contribution to the 'Software Synthesis, Code Generation and Timing Analysis' cluster and the 'Design for Predictability and Performance' activity within the Transversal Integration cluster.*

2.2.16.Partner 16: INRIA

Organisation

Institut National de Recherche en Informatique et Automatique (INRIA) is a public research institute devoted to fundamental and applied research on computer science and control. It is organised as a set of 8 research units, located respectively in Rocquencourt, Rennes, Sophia-Antipolis, Nancy, Grenoble, Saclay, Lille, and Bordeaux. Each research unit hosts several project-teams (typically between 20 and 30), which are groups of permanent researchers with PhD students and engineers, working together towards a well identified scientific challenge. INRIA focuses on several strategic research axes, one of them being embedded systems and software. Finally, INRIA has always shown a very strong commitment to industrial transfer, through the creation of numerous start-up companies (among them PolySpace Technologies, Kelkoo, …) and through its involvement in contractual collaborations with industrial partners (including Thales, EADS, Schneider Electric, STMicroelectronics, Dassault Systèmes, Dassault Aviation, Philips, just to name a few that are related to embedded systems and software).

Main Tasks Attributed

- Cluster "Modelling and validation"
  Activity "Component modelling"
  Our role in this activity will be to collaborate on programming languages for real-time systems, model-based development methods, semantic issues in distributed systems, compositional design and verification of embedded systems, and languages for component-based design.
  Interaction will mainly be with PARADES, on semantic issues, to obtain new results on models of computation and communication, and with UJF/VERIMAG, on component-based design methods (the BIP framework).
- Cluster "Modelling and validation"
  Activity "Resource modelling"
  Our role in this activity will be to investigate new methods for optimized distributed deployment for heterogeneous architectures.
- Cluster "Modelling and validation"
  Activity "Quantitative modelling"
  Our role in this activity will be to study inter-procedural abstract interpretation methods, discrete controller synthesis methods, and probabilistic models and verification methods for dependable embedded systems.
  Interaction will mainly be with EPFL, Aalborg, and DTU, on verification and dependability, to obtain new design methods for embedded systems.
- Cluster "Modelling and validation"
  Activity "Validation"
  Our role in this activity will be to improve symbolic model-based test selection techniques using approximate analysis.

Previous Experience in the Area

In the previous years, INRIA has been involved in a number of European projects related to embedded systems and software, hence acquiring a vast experience in this domain, in particular, EAST EEA, ARTIST, ARTIST2, SafeAir, and Speeds, to name a few. INRIA is also involved in several French Competitivity Poles: Minalogic, System@tic, Aerospace Valley, and SCS, all closely related to embedded systems and software.

Staff Members

Dr. Alain Girault
Research fellow. Responsible for all INRIA activities within ArtistDesign. Involved in all aspects related to dependable embedded systems.

Dr. Gregor Goessler
Research fellow. Involved in component-based design and adapter synthesis.

Dr. Bertrand Jeannet
Research fellow. Involved in inter-procedural abstract interpretation.

Dr. Albert Benveniste
Research director. Involved in semantic issues of distributed systems.

Dr. Benoît Caillaud
Research fellow. Involved in semantic issues of distributed systems.

Dr. Jean-Pierre Talpin
Research director. Involved in model-based development methods.

Dr. Yves Sorel
Research director. Involved in optimized distributed deployment for heterogeneous architectures.

Dr. Robert de Simone
Research director. Involved in latency insensitive designs and GALS systems.

Dr. Thierry Jéron
Research director. Involved in model-based test selection.

2.2.17.Partner 17: TUKL

Organisation

Technische Universitaet Kaiserslautern (TUKL), founded 1970, is a technical oriented University comprising nine departments with about 150 professors. Approximately 8000 students are currently registered. The University has a high reputation: 2 Frauenhofer Institutes, the German Research Centre for Artificial Intelligence, a Max-Planck Institute for Softwaresystems and several other institutes are embedded in the University.

The department of Electrical and Information Technology consists of 14 research groups with strong emphasis on communications, digital systems and microelectronics. The department is active in numerous collaborative national and international research projects

Main Tasks Attributed

- Cluster “Operating Systems and Networks”
  Activity “Resource-Aware Operating Systems”

Our role in this activity will be to work on Real-time resource management and media processing. Interaction will mainly be with NXP, SSSA-Pisa and ULund, on flexible resource management to obtain resource management and control for media processing results.

- Cluster “Operating Systems and Networks”
  Activity “Real-Time Networks”
  Our role in this activity will be to work on bandwidth management for media processing. Interaction will mainly be with CSEM, SSSA-Pisa and ULund on bandwidth management, to obtain media processing results.

Previous Experience in the Area

The group for real-time systems has expertise in particular adaptive resource allocation methods for Quality-of-Service in real-time embedded systems, real-time communication middleware on off-the-shelf components, and component based scheduling architectures. The group has applied real-time technology to determine and plan adaptive resource demands and their matching in wireless networks.

The group is involved in several national and international research project and networks, including EU IST projects, FABRIC, FIRST – Flexible Integrated Real-Time Systems Technologies, which it coordinated, its successor FRESCOR, BETSY, IP WASP, and the EU IST Networks of Excellence on Embedded Systems, ARTIST and ARTIST2, the ESF Network of Excellence on middleware, MINEMA.

Staff Members

Prof Gerhard Fohler will lead the activities of the group in the NoE.

Dr Peter Kosack will work on wireless sensor networks.

Dipl. Ing. Ramon Serna Oliver will work on bandwidth management methods for real-time networks and wireless sensor networks.

Dipl. Ing. Raphael Guerra will work adaptive resource management.

Prof. Jean-Dominique Decotignie (CSEM) will work on wireless sensor networks and real-time communication issues.

Liesbeth Steffens (NXP) will work on real-time resource management for consumer electronics.

Clara Otero Perez (NXP) will work on multi resource management for consumer electronics.

Prof Hermann Härtig (TU Dresden) will work on real-time operating system services.

Prof Norbert Wehn will provide support for embedded system design and synthesis.

2.2.18.Partner 18: KTH

Organisation

Kungliga Teknika Hogskolan (KTH) is the largest technical university in Sweden corresponding roughly 50 % of academic technical research in Sweden. ArtistDesign NoE activities focuses to two departments at KTH: Department of Electronic and Computer Systems (NoC and MPSOC) and department of Machine Design (real-time and mechatronic systems).

Main Tasks Attributed

- Cluster “Execution Platform and MPSoC” - Activity “Analysis”
  Our role in the activity is to design agent based architectural and software support to handle dynamic reconfigurability and task reallocations in NoC platform. The target is autonomous NoC supporting power and hardware resource efficient performance and dependability enhancements. Interaction will mainly be with other cluster partners and

through the Activities of the Transversal Integration workpackage on Adaptivity and Predictability

- Cluster “Execution Platform and MPSoC” - Activity “Design”
  Our role is to develop further framework for simulation and performance analysis of complex network-on-chip platforms and to support validation and verification for these. On hardware execution platforms interconnect and communication centric performance analysis methods and techniques are addressed. Interaction will mainly be with other cluster partners and through the Activities of the Transversal Integration workpackage on Adaptivity and Predictability
- Cluster “Modeling and Validation” - Activity “Modeling”
  Our role in this activity will be to integrate domain languages (e.g. Simulink and the AADL) with analysis techniques and in extending the ForSyDe framework to model also continuous time systems (Component modelling - A), to compare different approaches to multi-objective optimization and to design networked control protocols using cross-layer optimization techniques (Resource modelling - B), and through definition of design metrics (Quantitative systems modelling - C).
  Interaction will mainly be with other cluster partners and through the Activities of the Transversal Integration workpackage on Adaptivity and Predictability to obtain modelling techniques that support systematic model based development of embedded systems.
- Cluster “Modeling and Validation” - Activity “Validation”
  Our role in this activity will be to develop a framework and methodology for systematic validation of embedded systems. This framework will take into account the multiple behaviours and aspects that are typically dealt with at different levels of abstraction and using different modelling and analysis approaches. The research relates to that of modelling since the underlying models are neither unified nor managed in a consistent way. Interaction will mainly be with the cluster partners and through the Activities of the Transversal Integration workpackage.
- Cluster “Transversal Integration” – Activity “Design for Adaptivity”
  Our role in this activity is to provide autonomous NoC platform based on hierarchical distributed agent architecture to augment the communication and processing elements in NoC platform.

Previous Experience in the Area

KTH is a leading research institution in the area of embedded systems, manifested through its participation in the EU-projects ANDRES, ARTIST2, ATESST, DYSCAS, EU-MechaPro, HIPEAC, HYCON, RUNES, SOCRADES.

KTH provides expertise in the areas of MPSOC and NoC execution platforms, design and analysis techniques for embedded systems, model based development of embedded systems, networked control systems, systems engineering and mechatronics.

Staff Members

Prof. Hannu Tenhunen
Will lead the KTH participation in cluster “Hardware Platforms and MPSOC Design” with focus on various design aspects, architectures, and agent based run-time reconfigurability and adaptivity.

Prof. Axel Jantsch
Will contribute to KTH participation and Hardware Platforms and MPSOC Design with focus on run-time environments and analysis techniques. Furthermore he will contribute experience in formal models of computation and communication, the ForSyDe framework.

Prof. Li-Rong Zheng
Will contribute to KTH participation in cluster “Hardware Platforms and MPSOC Design” with focus on interconnect centric architectures and NoC applications.

Professor Martin Törngren
Will lead the KTH participation in the cluster Modeling and Validation. Contributes experience in model based development and verification of embedded systems.

Ass. Prof. Karl-Henrik Johansson
Will contribute experience in modelling and validation of hybrid systems with applications to control systems and networks..

Prof. Jan Wikander
Will contribute experience in modelling and validation of mechatronic systems.

2.2.19.Partner 19: Linkoping

Organisation

Public University.

The Embedded Systems Laboratory at Linköpings Universitet (Linkoping) is conducting research in the areas of real-time embedded systems, system analysis, design methodologies and optimization, system verification, testing, and low power SoC systems.

Main Tasks Attributed

- Cluster “Hardware Platforms and MPSoC Design” - Activity “Platform and MPSoC design”
  Our role in this activity will be: Energy efficient implementation of real-time applications; optimisation of fault tolerant systems. Interaction will mainly be with Bologna, DTU, TUBS, on system modelling and design methodologies, tool integration.
- Cluster “Hardware Platforms and MPSoC Design”
  Activity “Execution Platforms and MPSoC Analysis”
  Our role in this activity will be: Timing analysis, distributed systems, reliability analysis. Interaction will mainly be with Bologna, TUBS, DTU, IMEC, on timing analysis of distributed systems and tool integration.
- Transversal Activity “Predictable Systems”
  Our role in this activity will be: predictable multiprocessor systems; predictable fault tolerant systems. Interaction will be with Dortmund, Saarland, ETH Zurich, Bologna, TUBS, on reliability modelling, fault tolerance, execution time analysis, architectures.

Previous Experience in the Area

The group has a strong experience in the area of embedded systems and an active presence at international level. Projects: COTEST (EC), VERTIGO (EC), SYDIC (EC), STRINGENT (Swedish Excellence Centre for Microelectronic Research).

Staff Members

Professor Petru Eles	*Embedded systems analysis, design, and optimisation*
Professor Zebo Peng	*Design tools, system testing*
MSc Soheil Samii	*System analysis*

2.2.20.Partner 20: ULund

Organisation

The Faculty of Engineering LTH is one of the most important faculties of Lunds Universitet, one of Scandinavia's largest establishments for higher education and research. LTH is also one of Sweden's largest higher educational institutes for the technical and engineering sciences. The Department for Automatic Control is recognized world-wide for contributions to modelling, control and embedded real-time systems. The expertise within the group includes real-time kernel implementation, domain-specific programming languages, real-time control, computer-control theory, networked control loops, hybrid control, and general control theory. During recent years the work has been focused on integrated control and real-time scheduling, temporal robustness, and feedback-based scheduling, where the group has done pioneering work.

Main Tasks Attributed

- Cluster: Operating Systems and Networks
  Activity: Scheduling and Resource Management
  Our role in this activity will be to work on control-theoretic approaches to resource scheduling. Interaction will mainly be with SSSA-Pisa, York, TUKL, UPC, and Ericsson on adaptive and flexible scheduling.
- Transversal Integration workpackage - Activity: Design for Adaptivity
  Our role in this activity will be to lead the activity. Interaction will be with all the partners involved in the activity,

Previous Experience in the Area

The group is and has been a member of several EU projects in the field, including the FP6 projects ARTIST2, HYCON, RUNES, CEMACS, and SMErobot. The group has participated and/or been the leader of several national projects within the area.

Staff Members

Professor Karl-Erik Årzén
Responsible person from ULund. Leader for the Design for Adaptivity activity. Member of the SMB.

Assistant Professor Anton Cervin
Will be working on control and scheduling.

Associate Professor Anders Robertsson
Will work on applying control to computer systems.

2.2.21.Partner 21: MDH

Organisation

Maelardalens Hoegskola (MDH, http://www.mdh.se/) is a Swedish public university with campuses in Eskilstuna and Västerås. The most prominent research is in real-time systems at MDH Real-Time Research Centre (http://www.mrtc.mdh.se/), located at the Department of Computer Science and Electronics (http://www.mdh.se/ide/). The programming languages group, which will carry out the work of the partner in the NoE, belongs to this department.

Main Tasks Attributed

- Cluster “Software Synthesis, Code Generation and Timing Analysis” - Activity Timing Analysis
  Our role in this activity will be to work on the different approaches to WCET flow analysis for MPSoC/Multicore systems, as detailed in the cluster description, and to arrange the bi-annual WCET Tool Challenge. Interaction will mainly be with Saarland University, AbsInt, and Vienna, on WCET flow analysis for MPSoC systems.
- Transversal activity on adaptivity, where we will work on applications of parametric WCET analysis to adaptive scheduling.

Previous Experience in the Area

A major activity of the programming languages group is WCET analysis research. We have ten years experience in the area. Current research focuses on the *flow analysis*, which produces constraints describing the possible program flows. Another strong activity is evaluation of WCET analysis tools and methods on real industrial real-time codes. We are members of the current ARTIST2 NoE. The team leader also has previous experience in parallel algorithms and parallel programming models.

See also http://www.mrtc.mdh.se/index.php?choice=projects&id=0017.

Staff Members

Prof. Björn Lisper	*WCET analysis, parallel programming models*
Docent Jan Gustafsson	*WET analysis*
Dr. Andreas Ermedahl	*WCET analysis*
Mr. Stefan Bygde	*Parametric WCET analysis*

2.2.22. Partner 22: OFFIS

Organisation

The non-profit research institute OFFIS E.V. (Offis, http://www.offis.de/), founded in 1991 by the State of Lower Saxony, the University of Oldenburg, and professors from the Department of Computer Science, has successfully implemented its mission of establishing close industrial cooperation on the international, national and regional level. The R&D division of Safety Critical Systems (SC) is internationally renowned for its applied research in embedded and safety critical systems. The division is cooperating with many international companies in the transportation domain (automotive, avionics and railway systems) in research projects funded by public authorities and by direct industrial cooperations.

Main Tasks Attributed

- Cluster “Modeling and Validation”
  Activity “Modeling”
  Our role in this activity will be to bring in our expertise in component based design and semantic foundation, in particular non functional aspects as real-time and safety. Collaboration with industry.
  Interaction will mainly be with the other core members on component and resource modelling, to obtain a component based theory for heterogeneity.
- Cluster “Modeling and Validation”
  Activity “Validation”
  Our role in this activity will be to provide our expertise in formal analysis techniques.

Interaction will mainly be with the other core members on compositional analysis techniques regarding safety and real-time as well on deployment synthesis to obtain new methods and tools in that area.

Previous Experience in the Area

OFFIS is a partner of the NoE ARTIST 2. OFFIS is participating in the IP SPEEDS; related past EU funded projects are OMEGA, SafeAir and SafeAir II, EASIS, ISAAC and others. Experience is also based on national projects like VeriSoft, Oprail, IMOST and AVACS.

Staff Members

Prof. Dr. Werner Damm: design of embedded systems, modelling and analysing techniques, semantic foundations, industrial liaison.

Prof. Dr. Martin Fränzle: real-time and hybrid systems, robust semantic models and related decision procedures for correctness certificates.

Prof. Dr. Bernhard Josko: embedded systems designs, modelling and verification techniques.

PD Dr. Hardi Hungar: validation of embedded systems, certification.

PD Dr. Henning Dierks: real-time embedded systems.

2.2.23.Partner 23: PARADES

Organisation

The Project on Advanced Research of Architecture and Design of Electronic Systems European - Gruppo Europeo Di Interesse Economico (PARADES) was founded in 1996 by Cadence, Magneti Marelli and ST Microelectronics and since then directed by Prof. Alberto Sangiovanni Vincentelli. PARADES focuses on applications of new technologies to the industrial world. In collaboration with the founding companies, the Laboratory has applied innovative methodologies to the design of embedded systems to improve time-to-market for automotive electronics products. PARADES has a history of deep collaboration with companies (among which the founding companies) and several other international research institutes and Universities and participates on projects in EU funded programs. By taking advantage of its particular position between the industrial and academic worlds, PARADES experience covers several design aspects necessary for effectively and efficiently exploring the design solution space for the realization of distributed control on networks of embedded systems, from system conceptualization to HW/SW architecture definition, while meeting constraints and requirements on costs, performance and dependability.

Main Tasks Attributed

- Member of the Strategic Management Board
- Leader of the Integration Driven by Industrial Applications activity (in the Transversal Integration workpackage).

- Cluster: “Modeling and Validation” : JPRA Activity: “Modeling”
  PARADES will participate in all three sub-activities: it will contribute to A (component modelling) by developing meta-model theories based on trace algebras to integrate heterogeneous components and by addressing contract-based design; it will contribute to B (Resource Modeling) by developing models for resources based on architectural services following the Platform-Based Design paradigm of considering architectures as services to functionality of the design; it will contribute to C (Quantitative Modeling) by developing quantity managers that will be able to estimate non functional characteristics of the design. In particular, PARADES will work with its industrial partners to apply these methods to relevant industrial problems.
- JPRA Activity: “Validation”
  PARADES will participate to all three sub-activities: it will contribute to A (*Compositional validation)* by working on interface and refinement validation in the Metropolis framework; it will contribute to B (Quantitative Validation) by working on multiple levels of abstraction for reliability and performance assessment in the Metropolis framework; it will participate to C (Cross layer validation) by working on the automatic mapping of functional requirements to heterogeneous platforms.

- Workpackage Transversal Integration: JPRA “Design for Predictability”
  PARADES will work on architectural models that encompass multiple non functional properties using the quantity manager approach introduced by Metropolis to achieve predictable refinements of design.

Previous Experience in the Area

PARADES has experience in several industrial projects ranging from hybrid control design and verification, to synthesis of embedded software for real-time systems, multi-processor and fault-tolerant architectures for embedded controllers and system level modelling for early design space exploration.

PARADES has taken part in several European and National Projects in the past and is currently taking part in the ARTIST2 Network of Excellence in Embedded Systems (http://www.artist-embedded.org/artist/) and HyCon Network of Excellence on Hybrid Control (http://www.ist-hycon.org), in the SPEEDS IP for speculative design process control in systems engineering (http://www.speeds.eu.com) and in the RI-MACS STREP for radically innovative manufacturing control systems (http://www.rimacs.eu)

Staff Members

Prof. Alberto Sangiovanni-Vincentelli: *Embedded Systems, Design Methodologies, EDA, Analogue and Digital Design, Wireless Sensor Networks*

Dr. Alberto Ferrari *Embedded Systems, Design methods, Architectures, Software Architecture, IC design, Fault tolerant architectures*

Dr. Leonardo Mangeruca: Embedded Systems, Formal Methods, Models of computation, VLSI design

Dr. Massimo Baleani: Embedded Systems, Fault tolerant Architectures, VLSI design

Dr. Christos Sofronis: Embedded Systems, Software Design and Architecture

2.2.24. Partner 24: Passau

Organisation

Universitaet Passau (Passau, http://www.uni-passau.de) was founded in 1978. Its four departments are Informatics and Mathematics, Philosophy, Law, and Economics and Business Administration. A department of Catholic Theology has been suspended in 2006. The university has around 100 professors and between 8000 and 9000 students.

The Department of Informatics and Mathematics (http://www.fim.uni-passau.de) with nine professors in informatics and six professors in mathematics has been conducting research at an internationally high standard since its inception. Its graduates have created more than 600 jobs in information technology in the Passau area. (Passau has 50000 inhabitants.)

In recent years, the University of Passau has been embracing information technology more forcefully in an interdisciplinary manner. An interdisciplinary graduate school on the topic of self-organization in machine and human interaction has just been created. Embedded systems play an important role in this topic area.

Main Tasks Attributed

Cluster “WP4: Software Synthesis, Code Generation and Timing Analysis”
Activity “Software Synthesis and Code Generation”
We will investigate the synthesis of software for heterogeneous multiprocessor systems, in particular for MPSoCs, and contribute knowledge from high-performance computing and working on its adaptation for embedded systems and multicores.

Previous Experience in the Area

We have extensive experience in methods of program parallelization and parallel programming for high-performance computing. Our main activities have been in automatic loop parallelization (parallelizer LooPo, http://www.fim.uni-passau.de/loopo) and in parallel programming with skeletons, particularly, divide-and-conquer skeletons. We are a member of the NoE CoreGRID (http://www.coregrid.net) and a founding member of the IFIP WG 2.11 (http://www.smart-generators.org). Our research projects have been funded by a good number of DFG and DAAD grants.

Staff Members

Prof. Christian Lengauer, Ph.D. *Holding the Chair for Programming in Passau. Leader of the Passau group. Leading the technical activities on approaches other than loop parallelization.*

Dr. Martin Griebl *Leader of the LooPo team. : loop parallelization.*

Dipl.-Inf. Armin Größlinger *Technical activities on compilation for multicore architectures and MPSoCs.*

2.2.25.Partner 25: SSSA-Pisa

Scuola Superiore di Studi Universitari e di Perfezionamento Sant'Anna (SSSA-Pisa) is a public Italian university specializing in applied sciences, including Industrial and Computer Engineering. SSSA has adopted three principles that constitute the foundation of its mission: *excellence in education and research*, ensured by rigorous selection criteria for entering students, attracting teachers and researchers of high scientific stature; *interdisciplinarity*, as a cultural and methodological premise for addressing the complex problems of today's scientific and social realities; *Internazionalization*, understood as a propensity to cultivate relationships with other institutions at the international level. It has 1652 students and 72 researcher and teaching staff.

Main Tasks Attributed

- Cluster leader for "Resource-Aware Operating Systems and Networks"
- Activity leader for "Real-Time Operating Systems"
  Our role in this activity will be to provide novel real-time kernels that enable adaptive resource management and predictable behaviour, and cooperate with the other partners in the implementation of these services on different platforms.
- Activity "Scheduling and Resource Management"
  Our role in this activity will be to provide feedback-based scheduling and energy-aware algorithms for achieving adaptivity in battery-operated systems.
- Activity "Real-Time Networks"
  Our role in this activity will be to provide real-time communication protocols for guaranteeing end-to-end timing constraints for sensor-networks applications.
- Activity "Design for adaptivity"
  Our role in this activity will be to provide design methodologies that allow optimizing system performance as a function of task timing constraints.

Previous Experience in the Area

The Real-Time Systems (RETIS http://retis.sssup.it/) Group at the SSSA-Pisa is one of the world's leading research teams in the area of embedded real-time systems, time critical scheduling algorithms, advanced operating systems and adaptive resource management. The group was established by Giorgio Buttazzo in 1993 and it is currently composed of 22 people. The RETIS group has been involved in many European research projects related to several aspects of real-time systems, including scheduling (FIRST – "Flexible Integrated Real-time Systems Technology", IST-2001-32467), operating systems support for embedded systems (OCERA – "Open Components for Embedded Real-time Applications", IST-2001-35102), and quality of service in home entertainment networks (FABRIC – "Federated Applications Based on Real-time Interacting Components", IST-2001-37167). Another relevant activity of the RETIS group is the development and maintenance of a novel real-time kernel, called SHARK (http://shark.sssup.it/) for integrating tasks with hard and soft real-time constraints. The kernel has been designed to be modular and provide predictable and efficient support to critical control applications, as well as multimedia systems. SHARK is currently used in more than 30 institutions all over the world.

Staff Members

Giorgio Buttazzo (Full Professor) – Real-time scheduling and resource management

Paolo Ancilotti (Full Professor) – Fault-tolerant computing and concurrent languages

Giuseppe Lipari (Associate Professor) – Multiprocessor scheduling and operating systems

Marco Di Natale (Associate Professor) – Embedded Systems Design Methodologies

Enrico Bini (Assistant Professor) – Schedulability analysis of real-time systems

Tommaso Cucinotta (Assistant Professor) – Security and QoS management

2.2.26.Partner 26: Porto

Instituto Superior de Engenharia do Porto (Porto)

Organisation

Instituto Superior de Engenharia do Porto (ISEP) of the Polytechnic Institute of Porto (IPP) is a public institution dedicated to higher education, research and development activities, and one of the largest and oldest engineering schools in Portugal. ISEP-IPP will participate in the ArtistDesign NoE through its CISTER/IPP-HURRAY research group (http://www.hurray.isep.ipp.pt). The CISTER/IPP-HURRAY research group essentially focuses its activity in the areas of real-time embedded and distributed systems in dynamic environments; supporting timing and reliability requirements in distributed applications. In the recent international evaluation of research centres in Portugal, the CISTER research unit was the only one (out of 28 nationwide in the area of Electrical and Computer Engineering) to be top-rated as excellent.

Main Tasks Attributed

- Cluster “Operating Systems and Networks”
  Activity “Resource-Aware Operating Systems”
  Our role in this activity will be to contribute research and knowledge on middleware, tiny operating systems and exploitation of multicores.
  Interaction will mainly be with SSSA-Pisa and Aveiro, on multicores and tiny OSs, to aiming at obtaining results on embedded OS support for multicores/multiprocessors and data aggregation distributed approaches using CAN-based devices.
- Cluster “Operating Systems and Networks”
  Activity “Scheduling and Resource Management”
  Our role in this activity will be to contribute research and knowledge on multiprocessor scheduling, QoS-aware distributed and collaborative computing, and resource management in sensor networks.
  Interaction will mainly be with York and SSSA-Pisa, on run-time adaptability and multicores, aiming at obtaining results related to mode changes on multicore systems and run-time adaptability with anytime approaches, respectively.
- Cluster “Operating Systems and Networks”
  Activity “Real-Time Networks”
  Our role in this activity will be to contribute research and knowledge on wireless sensor networks, dynamic MACs, information processing in sensor networks and holistic analysis tools.
  Interaction will mainly be with ULund and York, on wireless networks, aiming at obtaining results on adaptable distributed algorithms for cyber-physical systems supported by dynamic medium access control protocols suitable for WSN, and on architectures and protocols for innovative processing approaches for large-scale densely populated networks of small embedded devices.

Previous Experience in the Area

The CISTER/IPP-HURRAY research group is, and has been involved, in several research projects at the European Level, of which the relevant are: NNE5-2001-00825 REMPLI Project (Real-time Energy Management via Power-lines and Internet); IST-1999-11316 R-FIELDBUS Project (High Performance Wireless Fieldbus in Industrial Multimedia-Related Environment); IST-2000-25088 Cabernet Project (Network of Excellence in Distributed Computing Systems Architectures). Several members of the research group have already served as PC Chairs / General Chairs in reputed scientific forums such as ECRTS or Ada Europe.

Staff Members

Prof. Eduardo Manuel Médicis Tovar
Scheduling and schedulability analysis, distributed systems, wireless sensor networks.

Prof. Mário Jorge Andrade Ferreira Alves
Wireless sensor networks, heterogeneous communication systems, architectures.

Prof. Luis Miguel Rosário Silva Pinho
QoS-aware computing, middleware, real-time languages and operating systems.

Dr. Björn Arne Andersson
Multiprocessor systems, wireless sensor networks protocols and applications, scheduling and schedulability analysis.

Dr. Anis Koubaa
Network calculus, wireless sensor networks, modelling and simulation, energy-aware computing

Prof. Luis Miguel Lino Ferreira
Mobile and ad-hoc networks, operating systems.

Eng. Nuno Alexandre Magalhães Pereira
Wireless sensor networks, stochastic scheduling, resource-aware operating systems.

Eng. Luis Miguel Pinho Nogueira
QoS-aware computing, genetic algorithms, dynamic coalitions of entities, anytime approaches.

2.2.27.Partner 27: Saarland

Organisation: Universitaet des Saarlandes (Saarland), University, public.

Main Tasks Attributed

- Cluster “Software Synthesis, Code Generation and Timing Analysis”
  Activity “Timing Analysis”
  Interaction will be with MDH on parametric timing analysis, with Dortmund on Code Generation and Timing Analysis, to obtain higher precision, with AbsInt on improving timing-analysis technology, with ETH Zurich and Bologna on improving predictability and on extending timing analysis to multi-core and MPSoC architectures, with Tidorum and MDH on running and improving the ACET Tool Challenge.

Previous Experience in the Area

The group of Reinhard Wilhelm together with its spin-off company AbsInt is world-wide leading in the area of timing analysis of hard real-time systems. The development of aiT, the timing-analysis tool of AbsInt, is based on many years of research on static analysis at Reinhard Wilhelm’s chair at Saarland University. Static analysis of an embedded program is used to derive invariants about execution states for all inputs to the program. These invariants allow the derivation of reliable upper and lower bounds on the execution times of programs on a given hardware architecture.

This technology has been developed in a series of national and EU-funded projects. The most important of those was the IST project Daedalus, IST-1999-20527, concerned with the derivation of guarantees for safety-critical avionics software. Daedalus was considered a highly successful project. The aiT technology developed in the project has been instantiated for roughly 10 different processors ranging from simple microprocessors up to most complex processors of the PowerPC family. The tool is used in the European aeronautics and automotive industry. By working on this wide range of architectures Reinhard Wilhelm's group and AbsInt have gained deep insights into the predictability properties of hardware architectures. Reinhard Wilhelm directs the timing analysis activity in the European Network of Excellence ARTIST2 combining all European groups working in this area.

A new approach to static analysis based on 3-valued logic has been developed together with Mooly Sagiv (Tel Aviv University) and Tom Reps (University of Wisconsin at Madison). It has been successfully applied to systems with dynamically growing and shrinking sets of objects/threads/actors. This technology is extended to systems with dynamically changing communication topologies in the nationally funded project AVACS (Automatic Verification and Analysis of Complex Systems).

Staff Members

Prof. Dr. Reinhard Wilhelm, *Leader timing-analysis activity*.
Oleg Parshin (PhD student), *integration with code generation,*
Jan Reineke (PhD student), *improving predictability*,
Daniel Grund (PhD student), *improving predictability,*
Marc Schlickling (PhD student), *timing-analysis for multi-core and MPSoC architectures,*
Markus Pister (PhD student), *timing-analysis for multi-core and MPSoC architectures.*

2.2.28.Partner 28: PLU-Salzburg

Organisation

The Computational Systems Group at the Department of Computer Sciences at Universitaet Salzburg (PLU-Salzburg), lead by Prof. Dr. Christoph Kirsch is a research group devoted to studying and teaching the principled design and implementation of systems software. The current research focus is on queuing, http://tap.cs.uni-salzburg.at, and virtualization, http://tiptoe.cs.uni-salzburg.at, as well as on real time, http://htl.cs.uni-salzburg.at, and control, http://jarol.cs.uni-salzburg.at, of model helicopters, http://javiator.cs.uni-salzburg.at. The curriculum includes graduate classes and seminars on operating systems, compiler construction, embedded software engineering, and the theory of computation.

Main Tasks Attributed

- Cluster "Modeling and Validation" - Activity "Modeling"
  Our role in this activity will be to study operational and transformational modelling in the exotask system, and reliability modelling in HTL and the exotask system. Interaction will mainly be with Prof. Dr. Thomas Henzinger, EPFL, on reliability modelling, to obtain a hierarchical coordination language for interacting real-time tasks with reliability constraints.

- Cluster “Modeling and Validation” - Activity “Validation”
  Our role in this activity will be to study compositional scheduling of real-time software tasks in the exotask system, reliability validation in HTL and the exotask system, and time-portable execution of real-time software tasks in the exotask system. Interaction will mainly be with Prof. Dr. Thomas Henzinger, EPFL, on reliability validation, to obtain a tool supporting a hierarchical coordination language for interacting real-time tasks with reliability constraints.

Previous Experience in the Area

We have experience in designing and implementing integrated modelling and programming environments for real-time systems, including language, compiler, and runtime system design. Previous projects are the Giotto project started in 2000, http://embedded.eecs.berkeley.edu/giotto, and the ongoing HTL project started in 2006, http://htl.cs.uni-salzburg.at. Giotto and HTL are real-time programming languages for distributed embedded control systems.

Staff Members

Prof. Dr. Christoph Kirsch
Faculty researcher working on combining operational and transformational modelling in the exotask system, and reliability modelling in HTL and the exotask system.

Dr. Ana Sokolova
Postdoctoral researcher working on combining operational and transformational modelling in the exotask system, and reliability modelling in HTL and the exotask system.

Arkadeb Ghosal *PhD student working on reliability modelling in HTL and the exotask system.*

2.2.29.Partner 29: Uppsala

Organisation

Uppsala Universitet (Uppsala), founded in 1477, is the oldest university in Scandinavia, with over 30,000 students. The Research group participating in the NoE is situated in the Department of Information Technology, which has around 80 faculty members and 90 Ph.D. students. Annually, 3,600 undergraduate students take courses at the department.

Main Tasks Attributed

- Cluster “Modeling and Validation”
  Activity “Modeling”

Our role in this activity will be to develop modelling formalisms to express dependencies between timing and resource properties, and transformations between them.Interaction will mainly be with EPFL, on Component Modeling.

Cluster “Modeling and Validation”Activity “Validation”
Interaction will mainly be with Aalborg, on the UPPAAL tool, to obtain new analysis algorithms.

- Cluster “Transversal Integration”
  Activity “Design for Predictability”
  Our role in this activity will be as activity leader. From the technical point, we will study modelling idioms and mappings that support predictability in design
  Interaction will be, among others, with ETH Zurich, Linkoping, and Cantabria, on the TIMES/CATS tool, to obtain new techniques for combining functional models and platform descriptions.

Previous Experience in the Area

Research contributions of Uppsala University have been in the area of modelling and validation of real-time and distributed systems. Development of the UPPAAL and TIMES tools for analysis of timed systems, and for analysis of scheduling algorithms. Uppsala has been coordinating the ARTES national Swedish network on real-time systems (www.artes.uu.se) and the ASTEC Competence Center for Advanced Software Technology (www.astec.uu.se). It has participated to several relevant European Projects, including ARTIST, ARTIST2, WOODDES, ADVANCE, and CREDO.

Staff Members

Professor Bengt Jonsson *Coordinating the Activity "Design for Predictability". Participation in the "Modeling" activity by research on transformations between different representations.*

Professor Wang Yi R*esearch on modelling and validation algorithms concerning timing and resource properties. Coordinating tools development activity.*

Professor Parosh Abdulla *Research on validation algorithms concerning timing and resource properties.*

2.2.30.Partner 30: Vienna

Organisation

Technische Universitaet Wien (Vienna) has about 20.000 students and a heavy emphasis on research in the engineering sciences. The Faculty of Informatics of the Vienna has about 3.000 students. The Institute of Computer Engineering is one of its seven computer science institutes. There are 5 professors, 15 university assistants and at present 16 project assistants at the Institute of Computer Engineering.

The Institute of Computer Engineering's research and teaching activities focus on the area of Embedded Systems. Research is primarily dedicated to all aspects of time-triggered real-time systems as well as fault-tolerant distributed algorithms. The actual research topics range from modelling and analysis over SW/HW architectures and touch even the area of chip design. With respect to teaching, the Institute of Computer Engineering is mainly involved in the master and bachelor program in "Computer Engineering", which offers a profound scientific-technological education in the field of Embedded Systems.

Main Tasks Attributed

- Cluster "Software Synthesis, Code Generation, and Timing Analysis"
  Activity "Timing Analysis"
  Our role in this activity will be to focus on the possibility of extending the timing analysis platform to synchronous MPSoC architectures and to investigate coding strategies for improving the precision of timing analysis.
  Interaction will mainly be with Mälardalen University and Saarland University, on timing analysis for MPSoC architectures, to obtain design guidelines for building predictable synchronous MPSoC systems as well as with AbsInt on improving the timing-analysis precision to obtain high quality WCET bounds.
- Cluster "Transversal Integration"
  Activity "Design for Predictability and Performance"
  Our role in this activity will be to investigate into software architectures for time-predictable real-time operating systems.

Interaction will mainly be with York and the other partners of the activities on “resource-aware operating systems” and “scheduling and resource management”, on scheduling methods and resource management strategies, to obtain an operating system with a time-predictable scheduler and resource management.

Previous Experience in the Area

The Institute of Computer Engineering is partner in the FP6 Integrated Project DECOS, the Network of Excellence ARTIST2 and the FIT-IT funded projects TT-SoC, and Te-DES. In FP5 the Institute of Computer Engineering participated in a number of research projects, such as SETTA, Pamela, FIT, HRTC and DSoS, and successfully coordinated the FP5 project NEXT TTA.

Staff Members

Prof. Dr. Peter Puschner is a professor in computer science at Vienna University of Technology. He received his PhD from Vienna University of Technology in 1994 and then worked as a research associate at Vienna. In 1999 Puschner became a professor. In 2000/2001 Puschner held a Marie-Curie Category 30 fellowship (contract HPMF CT 1999-00184) and was a Marie-Curie research fellow at the University of York, England.

P. Puschner’s main research interest is on hard real-time systems for safety-critical applications, with a focus on the worst-case execution time (WCET) analysis of real-time programs and software/hardware architectures for time-predictable computing. He has strongly influenced the state of the art in these fields, published more than 80 refereed conference and journal papers, and was a guest editor for the special issue on WCET analysis of the Kluwer International Journal on Real-Time Systems in 2000. P. Puschner has been member of numerous program committees on embedded real-time systems (program-committee chair of the ISORC 2003 and ECRST 2004; general chair of the Euromicro Conference on Real-Time Systems 2002 and of ISORC 2004).

P. Puschner has been coordinator and researcher in a number of research projects. At the European level, he has been involved in the EC-funded projects PDCS, DeVa, SETTA, NextTTA, and DECOS, was an executive-board member in the EC-funded Network of Excellence on distributed and dependable systems (CaberNet), and is a member of the ARTIST2 Network of Excellence on embedded systems. Nationally, he has participated as partner or coordinator in a number of projects funded by the Austrian Science Fund (FWF) and projects funded within the FIT-IT embedded-systems initiative of the Austrian ministry of Transport, Innovation and Technology (Rapid Prototyping Kit, MoDECS, TeDES). P. Puschner is a member of the IEEE Computer Society, IFIP working group 10.2 on Embedded Systems, Euromicro, the OCG (Austrian Computer Society), and the Marie-Curie Fellowship Association.

Within ArtistDesign, Peter Puschner will work on strategies for improving computed WCET bounds and architectures that support the time-predictable execution of applications and operating system code.

Dr. Raimund Kirner
Mr. Kirner will work on strategies for code translation that support the time-predictable execution of code on target platforms.

Dr. Roman Obermaisser
Mr. Obermaisser will work on the design of synchronous time-triggered MPSoC architectures for predictable hard-real time systems.

2.2.31.Partner 31: York

Organisation

The University of York (York) is a public funded research-oriented university with the usual range of departments. It has over 10,000 students involved in undergraduate and postgraduate courses. The department of Computer Science is one of the top rated departments in the country undertaking research is a number of areas including real-time systems, embedded systems, high-integrity systems, HCI, graphics, AI, non-stand computation including quantum computing and advanced architectures.

Main Tasks Attributed

- Activity leader for “Scheduling and Resource Management”
  Our role in this activity will be to provide a comprehensive framework for managing a range of resource and scheduling methods, and to cooperate with the other partners in the integration of these methods.
- Activity “Real-Time Operating Systems”
  Our role in this activity will be to provide server-based scheduling for achieving adaptation and protection in embedded system multi-processor operated systems.
- Activity “Real-Time Networks”
  Our role in this activity will be to provide a knowledge-based means of assessing sensor-networks protocols, and an assessment of NoE protocols aimed at supporting flexible QoS.
- Activity “Design for adaptivity”
  Our role in this activity will be to provide integrating resource management techniques that can be subject to adaptability.
  Activity “Design for Predictability, Design for Adaptivity”
  Our role in this activity will be to provide scheduling analysis for use in predictability.
- Activity “Timing Analysis”
  Our role in this activity will be to provide measurement-based approaches to timing analysis.

Previous Experience in the Area

The Real-Time Systems group at the University of York was founded in 1990 by Professors Burns and Wellings and currently has over 30 researchers (including post-docs and PhD students). It is one of the leading research groups in the world looking at real-time systems and embedded systems. The group has been involved in many European projects related to several aspects of real-time systems, including scheduling (recent projects are: FIRST – “Flexible Integrated Real-time Systems Technology”, the follow-on project FRESCOR, HIJA – “High Integrity Java Applications”). The branch of analysis known as RTA (response time analysis) was primarily developed at York and is now used as the basis for many research approaches world-wide and has extensive industrial application. Current work on FPGAs is also being taken up industrially.

Staff Members

Alan Burns (Professor) – Real-time scheduling and resource management

Andy Wellings (Professor) – Real-Time and concurrent languages

Neil Audsley (SL) – Multiprocessor and FPGA scheduling and synthesis

Iain Bate (Lecturer) – WCET analysis and system synthesis

Guiem Bernat (Lecturer) – System scheduling and measurement-based WCET analysis

2.3. Consortium as a whole

- **No subcontracting is planned for the ArtistDesign NoE.**
- **None of the partners are from a country outside EU Member states and Associated Countries.**

The ArtistDesign NoE is the visible result of the ongoing integration of a community, that emerged through the ARTIST FP5 Accompanying Measure and that was organised through the ARTIST2 FP6 NoE.

The ARTIST FP5 Accompanying Measure (http://www.artist-embedded.org/artist/ARTIST-FP5.html) on Advanced Real-Time Systems allowed a first analysis of the research landscape in Europe, and the identification of the main research teams in the area. The common vision achieved by these teams has been published and disseminated via the ARTIST Roadmap for Research.

The FP6 ARTIST2 NoE has achieved the first main steps towards integration of the embedded systems community in Europe. Initially composed of 7 Thematic Clusters, and. it gathers together 40 partners, implementing a 4-year JPA with a budget of 6.5 Million Euros, ARTIST2 is a significant success:

- It has achieved a strong level of integration within and between the clusters, around an ambitious and realistic research programme. This integration extends to the wider community of academic and affiliated partners, who effectively participate in the workprogramme. This ARTIST2 community enjoys world-wide recognition and plays a leading role in structuring the area.
- ARTIST2 is a main focal point for dissemination, through an appropriate technical infrastructure, coordination team, and networking with the community.
- ARTIST teams have a strong involvement in industrial R&D projects – both through direct contracts and EC-funded projects. The strength of this relationship was visible in setting up ARTEMIS/ARTEMISIA, and particularly for writing its Strategic Research Agenda (SRA).

The ArtistDesign NoE will shift gears and accelerate to the next level. The main structuring principles from ARTIST2 have been preserved (Clusters, Thematic and Transversal activities, core and affiliated partners), and updated to reflect the progress on integration.

Here are the main differences brought:

- There is a reduction in the size of the consortium, from 40 to 31 core partners. Many partners have been removed, and new ones have been added for better thematic coverage. The ARTIST2 core partners not taken up in ArtistDesign remain present as Affiliated Partners.
  We believe that this tighter consortium presents the right balance between critical mass, and focus.
- We have implemented a drastic shift in priorities, bringing a strong focus on essential Design activities. We have significantly reworked the cluster landscape. There are new clusters on “Operating Systems and Networks”, and “Modelling and Validation”. The Execution Platforms cluster has been extended to cover MPSoC design. In parallel, the large number of transversal activities in ARTIST2 has been replaced by a few activities focused on Design. Thus, ArtistDesign has 4 Thematic Clusters and a Transversal Integration workpackage.

- ArtistDesign will fulfil its institutional role, and interact with other entities such as ARTEMISIA, to ensure a strong connection between the research community and the overall research community in Europe.
- ArtistDesign will complete the integration of the Embedded Systems Design community, initiated in ARTIST2. ARTIST2 has invested considerable efforts to set up a communication infrastructure and recognized web portal – as attested by the Special Mention received in the IST website contest in November 2006 The ARTIST2 web portal received an 'honourable mention' from the jury in last November's «Best IST Website» contest where 256 websites were entered and 22,000 votes were cast on the internet (http://ec.europa.eu/information_society/istevent/2006/competitions/websites/index_en.htm). Within ArtistDesign, our ambition is to make the web portal a worldwide reference in the area.

ArtistDesign is a natural continuation/extension of ARTIST2. It is addresses a wider scope; including System-on-Chip and integration of results in design flows. In defining the consortium, we have sought to minimize the overall number of core partners. This has been achieved to a certain degree, but it was impossible to reduce it further without introducing significant gaps and incoherencies.

Embedded systems design is a large knowledge domain that includes hardware, software, architecture, control, communication, and computation issues that must be considered in a holistic fashion. European research is still relatively fragmented, despite recent progress. We still lack large centres of excellence comparable to those found in the US. The restriction to a smaller number of core partners (e.g.: 10) would lead to insufficient coverage, and worse – to problems arising from the exclusion of significant players in the area.

The ArtistDesign NoE is a strong further step for the integration of the embedded systems design community. It is the logical continuation of a process started with ARTIST FP5, and expanded and continued within the ARTIST2 NoE.

The ArtistDesign NoE will anchor the embedded systems design research community to ARTEMIS / ARTEMISIA, and open the way for sustainability.

2.4. Resources to be Committed

The requested funding corresponds well to the work to be performed, and to the expected results. The resources planned are adequate for meeting the overall and detailed objectives. The nature of the objectives justifies the composition of the consortium and in particular the number of partners. This is necessary to ensure success of the project, as well as the take-up and exploitation of the results, after its completion.

The project duration is 48 months, which is the adequate duration for achieving long-term benefits. A shorter span of time would be insufficient.

- The overall ArtistDesign budget amounts to 5.766.237 €
- The funding requested is 4.500.000 €.
- WP0 Management amounts to 7% of the overall funding.

The implementation of the JPA mobilizes considerable resources, at least 10 times the actual funding amount. Each cluster has identified the sources of additional funding, as given below:

Thematic Cluster: Modeling and Validation

Teams involved in this activity are funded by the following agencies and participate in the following projects.

IST-FP6 projects ASSERT, DECOS, and SPEEDS.

EPFL: Swiss National Science Foundation.

KTH: FP6 projects ANDRES, ATESST, DYSCAS, RUNES, SOCRADES.

PLU-Salzburg: Austrian Science Fund, IBM.

Uppsala: Swedish Research Council (VR, the CATS project); Swedish Strategic Research Foundation (SSF, via the SAVE project); European Commission (EU, the CREDO project).

OFFIS: FP6 project SPEEDS (SPEculative and Exploratory Design in Systems Engineering); German national projects IMOST (Integrated Modeling for Safe Transportation) and AVACS (Automatic Verification and Analysis of Complex Systems, German Transregional Collaborative Research Center).

Aalborg: CISS is a national competence centre for embedded software systems funded by the Ministry of Science, Technology and Innovation, the Region of North Jutland, the City of Aalborg, Aalborg University as well as a large collection of industrial partners. A new major national initiative coordinated by CISS is the DaNES project (Danish Network of Embedded Systems) involving IMM/DTU and CSI/SDU as well as 7 companies. DaNES is sponsored by the Danish National Advanced Technology Foundation. Other sources of funding includes ARTIST2 (NoE within EU), the national high-tech networks (sponsored by Ministry of Science, Technology and Innovation) Mobile Systems and Pervasive Communication, as well as the national project MoDES.

UJF/VERIMAG: The main sources of funding are the Integrated Project SPEEDS and the ITEA project SPICES. Other sources of funding are national projects (French RNTL/Galogic project) as well the SCEPTRE project of the Minalogic competitivity Pole.

ESI: The main source of funding is the Dutch Bsik programme on Embedded Systems. Additional funding is provided by the Dutch Ministry of Economic Affairs and ESI industrial partners.

CEA: The main source of funding are the FP6 project ATESST, the ITEA project Spices. Other sources of funding are national projects (Both French RNTL Memvatex and OpenEmbeDD projects) and the “Usine Logiciel” project of the System@tic competitively pole.

PARADES: The main source of funding is the Shareholders (Cadence and ST) contributions and contracts from United Technologies and Pirelli. In addition, PARADES participated to the FP6 projects SPEEDS and Ri-macs, and to the ARTIST and HYCON Networks of Excellence.

It is expected that in the framework of the Technology Platform ARTEMIS, in particular if it will be installed as a JTI, related projects with the involvement of cluster members will be launched, contributing to the topics of this cluster.

Thematic Cluster: Software Synthesis, Code Generation and Timing Analysis

In addition to funding through ArtistDesign, the partners will use funds provided by their own institution and by funding agencies.

The group at Dortmund receives funds from the CEC (e.g. through the IST project MORE). Furthermore, it receives funds from the national government, through the EXIST-SEED program of the national ministry of research (BMBF).

Passau receives funds from the Deutsche Forschungsgemeinsschaft (DFG). In particular, the group is supported for its work in the CompSpread project. Furthermore, our partners at the University of Passau are members of the CoreGRID network of excellence.

The ISS institute at Aachen also receives funds from the Deutsche Forschungsgemeinsschaft (DFG), e.g. via the new Excellence Cluster UMIC (Ultra High Speed Mobile Information and Communication), a large scale next-generation mobile internet research program. Further funding is received from EU FP6 projects like SHAPES, HiPEAC, and NEWCOM, as well as from industry partners like Siemens, Nokia, Infineon, CoWare, and Tokyo Electron.

The group at Saarland receives funding from the Transregional Research Centre AVACS of the Deutsche Forschungsgemeinschaft.

Vienna receives funds from the Austrian Science Foundation (FWF) for the projects COSTA and FORTAS. Further, Vienna is involved in two STREP proposals under EU FP7.

MDH: PROGRESS strategic research centre (SSF foundation, national), KKS-foundation (national), FP7 STREP proposal in preparation, planned VR application (national).

Thematic Cluster: Operating Systems and Networks

FRESCOR is a consortium research project funded in part by the European Union's Sixth Framework Programme (FP6/2005/IST/5-034026). The main objective of the project is to develop the enabling technology and infrastructure required to effectively use the most advanced techniques developed for real-time applications with flexible scheduling requirements, in embedded systems design methodologies and tools, providing the necessary elements to target reconfigurable processing modules and reconfigurable distributed architectures. The following academic partners are involved: Cantabria, York, SSSA-Pisa, TUKL, Technical University of Valencia and the Czech Technical University in Prague, together with the following industrial partners: Thales Communications France, ENEA EPACT, Visual Tools, Rapita Systems, EVIDENCE.

ARTDECO (Adaptive Infrastructures for Decentralised Organisations) is an Italian project managed by the SSSA, aimed at identifying the basic determinants affecting the establishment of reliable and effective network, which maximizes the level of confidence of each player and its willingness to cooperate, by distinguishing between knowledge that can be shared and protected knowledge that pertains to an individual player.

THREAD Spanish project, in which the following academic partners are involved: Technical University of Madrid, Universidad de Cantabria, and Technical University of Valencia.

GO-PLURATLITY is a Portuguese project involving Porto, which aims at the advancement of the state-of-the-art in Wireless Sensor Networks, QoS-Aware Computing and multiprocessor scheduling computing.

REFLECT is a Portuguese project involving Porto, aiming at investigating generic frameworks for dynamic application monitoring and control. Porto also has a new proposal under evaluation for an adaptable framework for embedded systems to allow constrained devices to cooperate with more powerful (or less congested) neighbours.

CMU-PT is a five-year research program between Portuguese universities (Porto and Aveiro among them) and the Carnegie Mellon University. Porto is a core partner within the cluster on cyber-physical systems, aiming at advancing the state-of-the-art in the use of information and communication technologies for monitoring and providing risk assessment to physical critical infrastructures. Research will focus on aspects such as large-scale multi sensory systems.

SSSA-Pisa and Porto are involved in a FP7 IST STREP project proposal aiming at synthesizing real-time applications for multicores based on software models of configurable software.

Porto, ULund and UPC are involved in a FP7 IST FET project proposal aiming at the development of scalable distributed algorithms for Cyber-Physical Computer Systems by exploiting specifics of the medium access control protocol.

ULund: VR project “Modelling and Control of Server Systems”; VINNOVA “Feedback Based Resource Management and Code Generation for Soft Real-Time Systems” together with Ericsson; New proposal to VR under submission ; STREP proposal to EU FP7 under submission; EU FP7 FET proposal under submission; VINNOVA Embedded Systems proposal under submission.

e-MAGERIT Emerging Applications for Next Generation Internet) - Region of Madrid S-0505/TIC/0251; 2006-2009.

WASP IST project, in which the following academic partners are involved: TUKL, Aachen, University of Paderborn, Imperial College London, Technical University of Eindhoven, University of Lille, EPFL together with the following research and industrial partners: IMEC, CSEM, Philips, Fiat, CEFRIEL, Microsoft Aachen, Fraunhofer IIS, IGD & Fokus, SAP.

MICS Swiss project, in which the following academic partners are involved: EPFL, CSEM, ETH Zurich.

Thematic Cluster: Hardware Platforms and MPSoC Design

Bologna: industrial grants for FreeScale and STMicroelectronics

TUBS: Public (national) funding from German Research Foundation and Federal Ministry of Education and Research

Linkoping: Public (national) funding from Swedish Foundation for Strategic Research, and Swedish Research Council

DTU: Public (national) funding from Danish National Advanced Technology foundation and Danish agency for science, technology and innovation

KTH: Public (national) funding from VINNOVA, National Research Funding

IMEC: Generates 82% of its total budget (197 million Euro), the remaining 18% being funded by the Flemish community. Self-generated income (162 million Euro): 68 % : International industry; 22 % : Flemish industry; 8 % : European Community; 2 % : European Space Agency

ETH Zurich: EU IP SHAPES (FP 6), National Competence Research ‘Mobile Information and Communication Systems’, Industry Cooperation, especially SIEMENS Building Technologies, Swiss National Science Foundation Project on “Performance Evaluation of Distributed Embedded Systems’

B.3. Impact

3.1. Expected impacts listed in the work programme

3.1.1. Workprogramme

The « ICT-2007.3.3: Embedded Systems Design Objective » target outcomes for NoEs are:

> ***Theory and methods for system design***
> *Methods that can increase system development productivity while achieving predictable system properties, including dependability and security. This will require a formal framework for systems design in addition to holistic and adaptive component-based design and verification methods. Key issues encompass heterogeneity (building embedded systems from components with different characteristics); composability; predictability of extra-functional properties such as performance and robustness (e.g. safety, security, timing and resources); concepts and tools for specifying and evaluating security properties; adaptivity for coping with uncertainty; and unification of approaches from computer science, electronic engineering and control. International cooperation should address foundational research challenges and provide mutual benefits; cooperation activities with the US National Science Foundation (NSF) will continue and extend to other countries.*

We believe that the ArtistDesign NoE matches these objectives perfectly.

3.1.2. Durability and Long-Term Impact

ArtistDesign will achieve a durable structuring effect on European research in a variety of respects:

- There will be a direct impact on the integration of academic research. It will allow for new, coherent theoretical frameworks to emerge, particularly those that can contribute to the unification of the area. For this, the NoE will take measures to overcome the inherent contextual, cultural, and disciplinary diversity. Through the various JPA and backbone activities, ArtistDesign will encourage the construction of new research frameworks, theoretical approaches, and meaningful validation through implementation.
- ArtistDesign will impact R&D activity from an organizational perspective. Until now, a researcher or a research group had little opportunity to appreciate or – at best – incorporate alternative approaches and contexts. Even when there was genuine effort to negotiate new types of research plans and objectives, it was extremely difficult to do so in the context of proposal preparation or even during the preparation of R&D deliverables. Some groups simply avoided joining such large consortia, preferring isolated work and funding from national agencies. ArtistDesign will explicitly aim to create a context, an infrastructure and a culture for the design of joint, multi-organisational, multi-disciplinary R&D work in embedded systems design. This will be achieved by the JPA activities, and also by the growing community spirit generated.
- ArtistDesign will have structural impact on European education in Embedded Systems Design, by:
    1) Integrating state of the art knowledge into the curricula, and accelerating the convergence towards unified multi-disciplinary approaches.
    2) Promoting approaches, techniques, which are well-adapted to meeting current and future industrial needs.

A more refined analysis of the expected relevance and impact, for each of the topics covered in the ArtistDesign NoE is provide here:

Modeling and Validation

Modeling and validation are key activities in the design of any complex system. Proper modelling is necessary to predict design properties before an implementation is built, and to reuse components across different platforms and multiple generations of a design. Model and implementation validation are necessary to ensure the desired degree of confidence in the design properties in a wide variety of possible deployment situations. While modelling and validation practices are well established in traditional engineering disciplines, many embedded systems are still designed in an ad-hoc manner, using situation-specific craftsmanship, without a generally accepted scientific foundation. This cluster attempts to bring together and advance several promising but isolated attempts at building such a foundation.

Software Synthesis, Code Generation and Timing Analysis

The approach of increasing the performance of embedded systems by using multiple processors is dictated by technological constraints. It is well known that the lack of tools is a very crucial issue of this approach. It is bound to fail if the required tools are missing. The result of such a failure would dramatically limit the potential to implement new, performance-hungry applications. Performance-hungry applications are on the horizon in various industrial sectors, including consumer electronics and the automotive industry. The overall objective of this activity is to avoid such a situation by making the required tools available.

Operating Systems and Networks

The major application domains that can benefit from the results of this cluster include Consumer Electronics, Multimedia Systems, Automotive Applications, Medical Systems, Industrial Automation, Advanced Robotic Systems, Assisted Living, and Cyber-Physical Systems.

In such domains, the characteristics of the workload, or even the overall system, cannot be easily predicted in advance and a static design approach cannot be pursued due to cost, power, space and memory constraints. As a consequence, system adaptation is highly desired to adjust the level of performance in a controlled fashion.

Hardware Platforms and MPSoC

Embedded systems are computer systems embedded into a technical environment. Therefore, they consist of hardware and software components. As the boundaries between the two domains are getting more blurred (adaptable embedded systems, breakthrough in power consumption and performance) and challenging questions are at the border (trade-offs in mapping applications to hardware and software components, WCET analysis, performance of distributed computer and communication systems), it is necessary to have both aspects represented in a NoE on embedded systems. Embedded systems are growing more software and communication centric. As a consequence, new models and new analysis and design space exploration tools are needed in order to support optimal implementation of applications on distributed embedded architectures such as MPSoC.

There has been a lot of work in the area of real-time systems which traditionally have concentrated on issues like schedulability analysis, software engineering of real-time systems, modelling and verification. Such a limited view of the problem is insufficient in the context of the above mentioned developments in embedded real-time applications. They are characterized by a continuously increasing complexity and strong constraints on safety, performance, power consumption, and costs. To be able to design such systems, it is needed to (1) consider the hardware platform and software components of MPSoC systems in their interaction, in order to produce a system which satisfies the requirements at low cost, (2) support the designer with tools for accurate estimation of certain design parameters (power, performance) based on appropriate models for hardware and software components and (3) provide the designer with adequate support for design space exploration and optimisation.

Embedded architectures and heterogeneous distributed embedded systems have grown to extremely complex computation and communication patterns. New performance models and a corresponding theory are urgently needed Europe needs to develop skills to safely design such systems.

3.2. Spreading Excellence, Exploiting Results, Disseminating Knowledge

3.2.1. Strengthening Excellence through Integration of Multidisciplinary Communities

ArtistDesign will have a strategic impact on the integration of academic research which is necessary to establish the new area of embedded systems design. The NoE will contribute to the construction of a framework for integration, which reflects the complexity of the topics involved and the different communities.

As stated earlier, there is an urgent need for Europe to establish an R&D potential in embedded systems design which supports innovation in key industrial sectors. This potential must be created by bringing together competencies from teams on the essential topics identified.

This need for bringing together competencies to create critical mass must overcome two main difficulties: 1) traditional fragmentation of European research; 2) the tendency for each scientific community working on a particular topic to follow its own path.

ArtistDesign will continue the work initiated in the ARTIST2 NoE by impacting European research in Embedded Systems Design, and providing new impetus to achieving further integration.

Spreading Excellence operates at two levels: within the ArtistDesign community, including the core and affiliated teams. This is done essentially within the JPIA and JPRA (WP1, WP3-WP7). The second level is explicitly addressed through the JPASE (WP2) activities.

3.2.2. Spreading Excellence Beyond the Network of Excellence

This integrated culture of research and development will be made visible and operationally integrated with a wider community of national networks and programmes, the establishment of institutes on embedded systems, including the Embedded Systems Institute in Eindhoven, and CISS - Centre for Indlejrede Software Systemer in Denmark).

ArtistDesign will operationally work with a set of existing academic networks at the national level, and provide momentum and motivation for the creation of new ones. ArtistDesign has, by construction, the necessary representation and weight to deeply influence all the institutions (universities, scientific associations, other bodies) and instruments (journals, conferences, summer schools) having the mission to disseminate knowledge in the area.

The JPASE (WP2) is designed to spread excellence from the Network of Excellence to the research and industrial communities in the large, through the adoption of the appropriate measures. As was done at the start of ARTIST2, ArtistDesign will hold a press conference to announce the start of the NoE. These measures are described in detail in WP2.

3.2.3. Transfer of Results through Collaboration with Industry

ArtistDesign has numerous activities with promoting the transfer of results and collaboration with industry. The Industrial Liaison activities gather many of these, and are described in the JPASE detailed description – WP2. These include the organisation of technical meetings open to industry, the Artemisia Liaison Task Force, as well as interactions with selected industrial affiliated partners. A detailed list of industrial affiliated partners is provided in WP3.

The NoE will leverage on its members and teams, who are strongly implicated in collaboration with industry, to organize and structure industrial relations, and develop mutually beneficial interactions. Furthermore, through Industrial Liaison, ArtistDesign will receive useful feedback about the relevance of work directions and priorities.

A list of collaborations with industry involving ArtistDesign partners is provided below by Thematic Clusters and Activities.

Modeling and Validation

Modeling

Many industrial sectors are expected to be impacted by our results, including safety-critical embedded systems for avionics, automotive, and space. These sectors are currently moving to a different OEM/supplier organization. In particular, aeronautics used to perform a large part of system development in house (typically about 70% for Airbus). Being under pressure of globalization and international competition, major aircraft manufacturers are now moving to an organization where a larger part of the system will be provided by suppliers. This will not be in the form of packaged final sub-systems, however, but rather through middleware and generic devices, which requires a novel development process. Integrated Modular Avionics is such a new process in aeronautics. It requires integrating components and sub-systems from suppliers according to an open architecture referred to as IMA. A similar move is under way in the automotive industry through the AUTOSAR standard. All this calls for fundamental research to support sophisticated component and sub-system integration techniques, such as interface theories that expose functional and quantitative requirements, including resource consumption and system reliability.

Validation

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We provide below an indicative list of industrial collaborations for the teams involved in the Modeling and Validation cluster:

- IAI (Israel Aerospace Industries Ltd) (Contact: Michael Winokur) is interested to have an active input and influence in the NoE in the areas of a) Systems Modeling and analysis methodology, b) Design Process, c) Industrial trialling of the methodology and supporting tools, and d) Efficient chains of integrated tool sets for systems design.

- ASML (Jan Stoeten): Collaboration (via ESI) on model-driven design for embedded software systems in semiconductor production equipment. Multi-disciplinary modelling and performance and dependability system requirements are important concerns.
- Philips Research (Eelco Dijkstra) Collaboration (via ESI) on modelling and analysis of reliability of application of wireless sensor network technology in consumer applications.
- NXP (Jan Raven) Collaboration (via ESI) on methods and tools to optimize reliability of high-volume products (TV software) with a user-centric approach to failure minimization.
- Cadence (Ted Vucurevich, Moshe Gavrielov, Andreas Kuehlman, Yoshi Watanabe, Yaron Kashai) (via PARADES) Collaboration on design methodology and tools for embedded system design.
- United Technologies Company (UTC) (Clas Jacobson, Scott Bortoff, Michael McQuade, Murilo Bonilha) (via PARADES) on applications of Platform-based design to air conditioning systems and intelligent building management
- General Motors (GM) (Marco di Natale, Paolo Giusto, Byron Shaw, Patrick Popp) (via PARADES) Collaboration of design methods and tools for automotive applications.
- Intel (Ken Tallo, Pat Gelsinger, Sean Maloney, Gadi Singer) (via PARADES) Collaboration on design methodology and tools (Metropolis) for multi-processor platforms.
- Sonics (Drew Wingard) (via PARADES) Collaboration on communication based design and architectures.
- FreeScale (Paul Grimme) (via PARADES) Collaboration on fault-tolerant multi-processor embedded controllers.
- ST (Marco Monti, Fabio Marchio', Maurizio Peri) (via PARADES) Collaboration on chip architectures for automotive applications; tools and methodologies.
- Pirelli (Giorgio Audisio) (via PARADES) Collaboration on WSN applied to stability control using tire data.
- Volvo: Collaboration with KTH on the EAST-ADL embedded systems modelling language and related analysis techniques.
- dSPACE (Joachim Stroop): provides expertise in embedded control systems tools and standards, and is interested in a dialogue with the NoE on future technologies and trends.

Software Synthesis, Code Generation and Timing Analysis

Software Synthesis, and Code Generation

The partners have numerous links to industry.

The group at Dortmund runs a separate technology transfer centre called ICD in order to provide adequate legal conditions for industrial partners. ICD is completely financed through industrial contracts. Current customers of the embedded system group include major silicon providers like ELMOS and Infineon. Other customers include T-Online International AG, the Federal Agency for Cartography and Geodesy, Grundig AG and Thomson Broadcast & Media Solutions GmbH. Additional industrial contacts exist directly between the group at the University of Dortmund and industry.

The group at IMEC had successful collaborations with design companies like NXP and ST, and also with EDA companies like Coware and Target. Successful spin-offs have originated from IMEC, notably Target compiler technologies. Many R&D projects have been carried out with industrial collaborations.

The ISS institute at Aachen maintains tight cooperations with semiconductor vendors, system houses, and EDA companies, and frequently provides industrial consulting services. Many R&D projects at ISS have contributed to the development of industrial products. Moreover, several successful EDA spin-off originated from the ISS, e.g. Cadis (acquired by Synopsys), Axys (acquired by ARM), and LISATek (acquired by CoWare).

Timing Analysis

Large parts of the embedded systems industry such as avionics and automotive start to understand that they need to verify the real-time constraints by sound methods for Timing Analysis. Several tool providers and technology customers will be partners in this activity

We provide below an indicative list of industrial collaborations for the teams involved in the Software Synthesis, Code Generation and Timing Analysis cluster:

- Joseph van Vlijmen (Ace – Amsterdam / Netherlands)
- *ACE will to provide CoSy as a compiler development platform and also continue to attend meetings and workshops in order to transfer knowledge from the partners to ACE and vice versa.*
- CoWare (Bart Vanthournout)
  Partners at Aachen are actively cooperating with CoWare through many projects. This contact will also be used to transfer results from the current project.
- AbsInt (C. Ferdinand)
  AbsInt provides partners with tools for worst case execution time analysis. In turn, research results are made available to AbsInt.
- IAR Systems AB (J-E Dahlin)
  provider of compilers and design tools for embedded systems. and collaborates with MDH around industrial case studies, and the interfacing of tools for the "Software Synthesis, Code Generation and Timing Analysis" cluster.
- Christian Ferdinand (AbsInt - Germany)
  AbsInt will enable and perform worst-case execution time analyses of embedded code. In particular, AbsInt will contribute to the design of architecture timing models by abstraction and transformation from a formal specification of the architecture, and the extension of timing analysis to full controller boards, multi-core architectures, and MPSoCs.
- Niklas Holsti (Tidorum - Finland)
  This company will make the commercial WCET analysis tool Bound-T, available and will participate in the WCET Tool Challenge.

Operating Systems and Networks

Resource-Aware Operating Systems

Industrial domains that will directly benefit of the results of this research include consumer electronics and telecommunications, for improving the functionality and the utilization of multimedia applications, automotive industry, to handle overload conditions that frequently occur in the microcontrollers embedded in the car, and industrial automation, where often robotics applications consists of several tasks with different criticality and timing constraints.

Real-Time Networks

The research conducted within this activity has a large potential for practical industrial applications. On one hand, the work on WSNs and MANETs can impact domains such as industrial automation (e.g. discrete-part, process control), domotics (home and building automation), surveillance systems, environment and critical infrastructures monitoring, assisted living, disaster recovery operations and military operations. On the other hand, the research on NES, wired and wireless, will address application domains related to distributed control, including safety-critical systems, which can impact on the industrial automation, automotive and aerospace industries, but also on the consumer electronics industry, particularly the one related to distributed multimedia systems like streaming servers and remote games, and also on integrated telecommunication services at the access networks level, to support adequate QoS management.

We provide below an indicative list of industrial collaborations for the teams involved in Operating Systems and Networks cluster:

- Ericsson (Affiliated to ULund)
  Team leader: Johan Eker
  Topic: Telecommunication systems
- NXP (Affiliated to TUKL)
  Team leader: Liesbeth Steffens
  Topic: Multimedia processing and QoS management
- Evidence srl (Affiliated to SSSA-Pisa)
  Team leader: Paolo Gai
  Topic: Operating systems and Tools
- Microchip Technology (Affiliated to SSSA-Pisa)
  Team leader: Antonio Bersani
  Topic: Platforms for embedded systems
- WindRiver (Affiliated to SSSA-Pisa)
  Team leader: Salvatore Scafidi
  Topic: Real-time operating systems
- PARADES (Affiliated to SSSA-Pisa)
  Team leader: Alberto Ferrari
  Topic: Real-time operating systems
- Johan Eker (Ericsson - Sweden, Affiliated to ULund) - Models of computation and adaptive scheduling for mobile cellular phone applications
- Liesbeth Steffens (NXP – Netherlands, Affiliated to TUKL)- Multimedia processing and QoS management
- John Goodacre (ARM, Affiliated to York) - Platform-level resource management

- Ian Broster (Rapita, Affiliated to York) - Simulation tools
- Antonio Bersani (Microchip Technology, Affiliated to SSSA-Pisa) – Platforms for embedded systems
- Salvatore Scafidi (Windriver, Affiliated to SSSA-Pisa) – Real-time operating systems
- Alexandre Mota (Micro-I/O - Affiliated to Aveiro)
  Distributed embedded systems, building automation, access control, systems integration
- Critical Software
  Team leader: Gonçalo Quadros
  Topic: Distributed systems and networks / high integrity systems
- PT-Inovação
  Team leader: Jorge Pinto
  Topic: Telecommunication systems
- Bosch Motorsport
  Team leader: Pedro Kulzer
  Topic: Automotive systems
- Jose Alberto Fonseca (Micro-I/O - Affiliated to Aveiro)
  Distributed embedded systems, building automation, access control, systems integration
- Nuno Cunha (Critical Software – Affiliated to Aveiro)
  Distributed systems and networks / high integrity systems

Hardware Platforms and MPSoC

Platform and MPSoC Design

All the key industrial sectors in Europe (and worldwide) are now struggling with multi-core programming, application mapping and management issues. In the area of nomadic multimedia, the evolution toward heterogeneous multicore has been tumultuous. The leading platforms on the market are now featuring around ten programmable cores (e.g., CPU, GPU, multimedia compression and decompression engines, video management unit, etc.), and their orchestration through device drivers under control of a traditional single-processor operating system is increasingly unwieldy. Automotive platforms are following the same trajectory in terms of increased parallelism, even though the design emphasis shifts from energy efficiency in nomadic towards predictability. Furthermore, design robustness has always been a concern for automotive. Future automotive control units will include multi-core devices. The new integration work will close a missing link between single core and distributed systems. The same holds for aerospace.

Domains such as wireless and wired data network infrastructure are even more aggressively pursuing architectural parallelism, given the highly parallel nature of their workload (e.g. IP packet processing). Home multimedia for high quality video, audio appliances has also embraced multicore solutions. Similar to the networking area, the focus here is on high performance within a power envelope (to reduce manufacturing and operational cost of the systems). The work, however, will have industrial application far beyond automotive and aerospace. Continuous system evolution and software updates have found their way into consumer electronics, mobile communication, medical devices, and industrial electronics. More than in classical distributed automotive and aerospace systems, however, power consumption is a primary design objective in these applications. This makes robustness a more complicated task requiring integration of power, reliability, and performance methods and tools.

All these sectors strategically need innovation on how to effectively program and manage applications for these highly parallel platforms. Thus, the integration activity in the cluster will be extremely helpful in accelerating the adoption of advanced programming models and resource management framework that will accelerate application deployment.

Platform and MPSoC Analysis

State-of-the art analysis techniques are a necessary for meeting design constraints and targets while keeping cost under control. In addition, design robustness has always been a concern of automotive manufacturers. There are already several automotive companies that use a tool, SymTA/S, for formal robustness analysis and optimization. Future automotive control units will include multi-core devices. The new integration work will close a missing link between single core and distributed systems. The same holds for aerospace

The work, however, will have industrial applications far beyond automotive and aerospace. Continuous system evolution and software updates have found their way into consumer electronics, nomadic embedded systems, communication systems, medical devices, and industrial electronics. More than in classical distributed automotive and aerospace systems, however, power consumption is a primary design objective in these applications. This makes robustness a more complicated task requiring integration of power, reliability, and performance methods and tools.

We provide below an indicative list of industrial collaborations for the teams involved in the Hardware Platforms and MPSoC cluster:

- Roberto Zafalon (STMicroelectronics – Italy)
  Providing industrial input on energy-efficient platforms for nomadic and multimedia computing. Power optimization techniques, low power design. Hosting interns and giving feedback on industrial relevance of integration results.
  ST has been working for over a decade in cooperation with Bologna on power-aware and energy efficient execution platforms. Many research results have been transferred to STM as a result of this cooperation. Several PhD and graduate students have been hired by STMicroelectronics. STMicroelectronics has hosted interns and given feedback on industrial relevance of integration results in the past. This interaction will continue.
- Henrik Lönn (Volvo Technology Corporation - Sweden)
  Electronic automotive systems; industrial input, evaluation of results, hosting interns.
- Nigel Drew (FreeScale Semiconductors – United-Kingdom)
  Providing input on industrially relevant problems in the area of operating-system based power management, including variable voltage and variable frequency techniques. Hosting interns and providing feedback on industrial relevance of integration results.
  FreeScale been working for more than three years in cooperation with bologna on power minimization based on middleware and operating systems for state-of-the art execution platforms for nomadic multimedia. Several technologies developed in bologna have been transferred to FreeScale as a result of the cooperation. PhDs have been funded. Several interns have been hosted. Feedback on industrial relevance of integration results will be provided.
- Rune Domsteen (Prevas – Denmark)
  Providing input on platforms for embedded systems. System level modelling and exploration. Feedback on industrial relevance of integration and evaluation of results.
- Karsten Nielsen (ICEpower Bang & Olufson – Denmark)
  Providing input on intelligent audio systems. Power optimization. Evaluating design methods for platform based design.

- (PAJ Systemteknik - Denmark)
  Input on embedded system platforms. Feedback on industrial relevance of integration results.
- Turku Centre for Computer Science (TUCS) at University of Turku and Åbo Akademi University
  The key persons there are Ass.Prof. Tiberiu Seceleanu (MPSOC) and prof. Johan Lilius (embedded software systems)
- Kai Richter, Symtavision, will investigate the applicability in automotive electronics.

Transversal Integration

Design for Adaptivity

The industrial sectors that are expected to be impacted by the work within this cluster include both the sectors that develop embedded hardware and software components, e.g., operating systems and embedded hardware, and the sectors that use embedded system technology in order to develop products and services. The latter include automotive, aerospace, automation, consumer electronics, and mobile telecommunications. Further collaborations are envisioned with EDA and compiler vendors that provide tooling for adaptive HW architectures such as ASIPs and reconfigurable architectures.

Design for Predictability and Performance

The industrial sectors that will be impacted by this work include sectors that manufacture components for embedded systems for which guarantees on timing and resource requirements is part of the product, as well as sectors performing systems integration where it must be understood how to relate system predictability to requirements on components. An example of an integrated project, which develops bridges between the component and systems view on predictability is IP-SPEEDS: the industrial partners from IP-SPEEDS project (Airbus, Saab, IAI, Carmeq, Bosch, Esterel-Technologies, TNI-Software, Telelogic, Extessy) represent sectors that will benefit from the results of this activity.